

POWER MANAGEMENT

Features

- Dual N-Channel MOSFET Driver with Programmable Dead Time Control
- Wide Power Stage Input Voltage: Up to 36V
- Integrated 5.25V LDO
- Smart Gate Drive to Reduce EMI
- Integrated Bootstrap Switch
- Diode Emulation for High Light Load Efficiency
- Tri-State PWM Input for Drive Stage Shutdown
- UVLO, Over Temperature Shutdown
- 10 Lead MLPD-UT 2.3mm x 2.3mm Package
- Full Industrial Temperature Range
- Fully WEEE and RoHS Compliant

Applications

- DC Motor Drive (with SC32300B)
- Synchronous DC-DC Converters
 - Single Phase
 - Multiphase

Description

The SC32300A is a high-side and low-side N-channel MOSFET driver with integrated bootstrap switch. This driver can be used as a synchronous buck converter MOSFET driver. It can also be used together with the SC32300B in applications driving a DC motor or similar load. An external capacitor to program the dead-time offers the flexibility to design the switch clamp circuitry and produce more reliable system operation for the DC motor driving application. The SmartDrive™ function at the turn-on of the high-side MOSFET is a standout feature of this part to reduce the EMI. The diode emulation mode operation offers the opportunity to achieve high efficiency at light load. The integrated LDO reduces the cost and the footprint of the system.

An Under-Voltage-Lock-Out (UVLO) function is included to ensure the driver outputs are off when the input voltage falls below 4.75V. An over temperature shutdown feature is also included to prevent the driver from overheating.

The SC32300A is available in a space-saving 10 lead 2.3mm x 2.3mm MLPD-UT package and operates over the industrial temperature range.

Typical Application Circuit

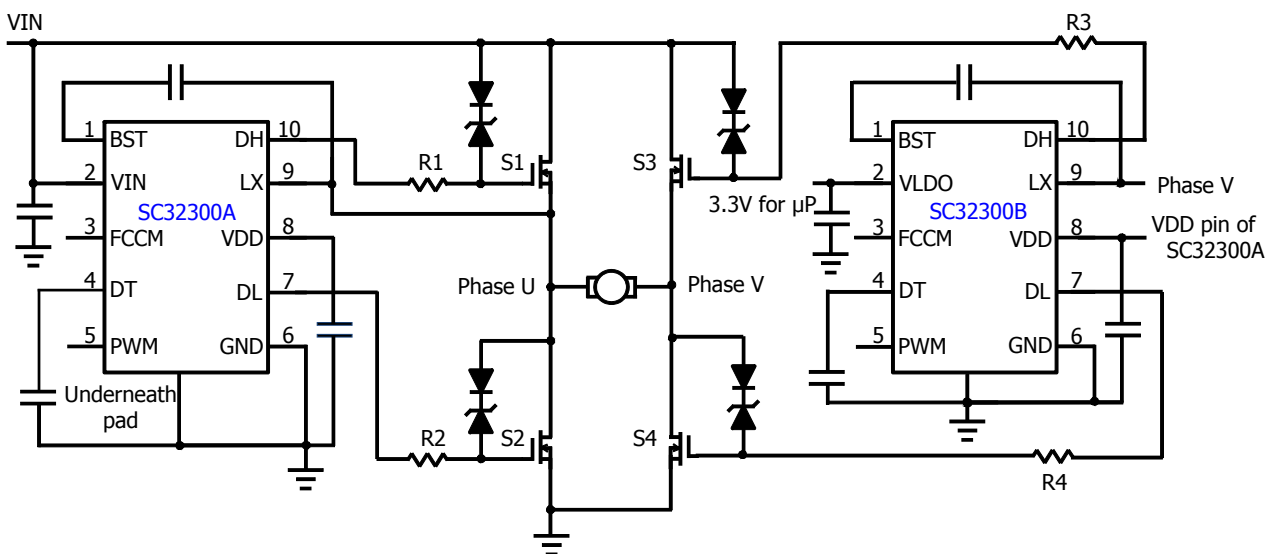
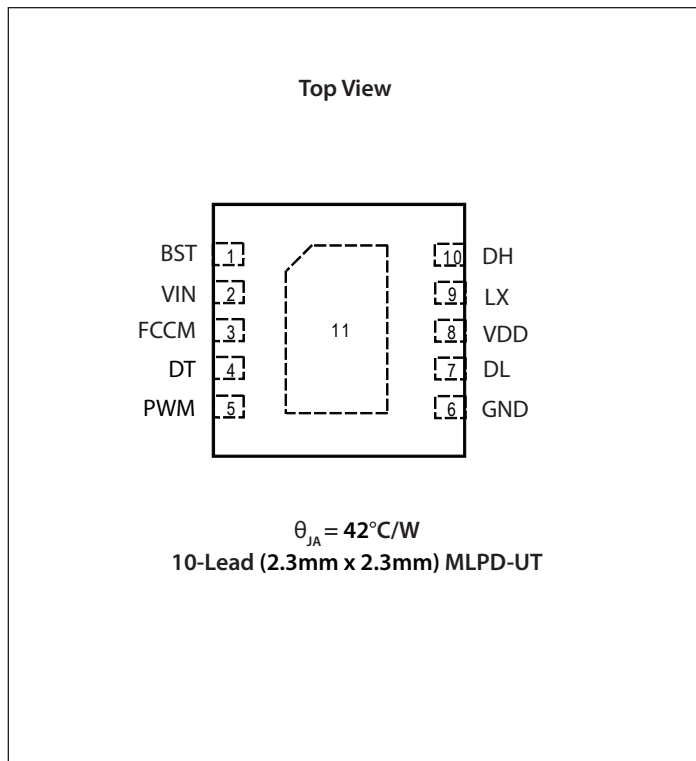


Figure 1. Typical Application for DC Motor Driving

Pin Configuration



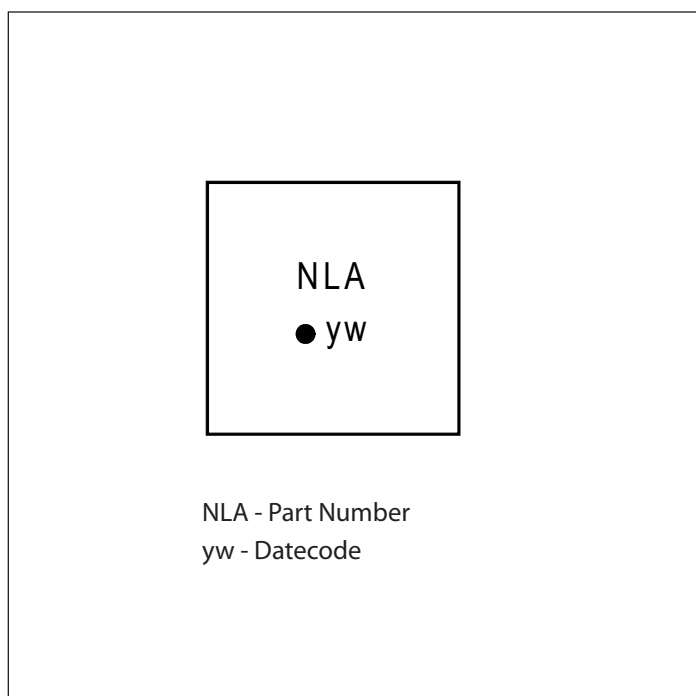
Ordering Information

Device	Package
SC32300AULTRC ^{(1)/(2)}	MLPD-UT-10 (2.3mm x 2.3mm)
SC32300A/B.EVB	Motor Drive Evaluation Board

Notes:

- (1) Available in tape and reel only. A reel contains 3,000 devices.
- (2) Available in lead-free package only. Device is WEEE and RoHS compliant and halogen free.

Marking Information



Absolute Maximum Ratings

VIN to GND (V)	-0.3 to +38
LX ⁽¹⁾ to GND (V)	-2.0 to +38
DH, BST to LX (V)	-0.3 to +6.0
DH, BST to GND (V)	-0.3 to +44
VDD to GND (V)	-0.3 to +6.0
PWM, FCCM, DT, DL to GND (V)	-0.3 to VDD+0.3
ESD Protection Level ⁽²⁾ (kV)	3

Recommended Operating Conditions

VIN (V)	$6.0 \leq V_{IN} \leq 36.0$
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Thermal Information

Thermal Resistance, Junction to Ambient ⁽³⁾ (°C/W)	42
Maximum Junction Temperature (°C)	+150
Storage Temperature Range (°C)	-65 to +150
Peak IR Reflow Temperature (10s to 30s) (°C)	+260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:

- (1) The transient negative voltage specification for the LX pin is -6V for 100ns.
- (2) Tested according to JEDEC standard JS-001-2012. BST-VDD passed 1.5kV.
- (3) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless noted otherwise $T_J = 25^\circ\text{C}$ for typical, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ for min and max, VIN = 22V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VIN						
Operating range	Vin		6.0		36	V
UVLO threshold		rising edge	4.78	4.94	5.10	V
		falling edge	4.59	4.75	4.89	
Input bias current	lin	PWM = High	213	267	413	μA
		PWM = Low	340	430	626	μA
		Shutdown mode, PWM pin floating	376	456	657	μA
Internal LDO						
LDO output accuracy	VDD	LDO load = 10mA		5.25		V
Line regulation		Vin = 6.0V to 36V, LDO load = 10mA		0.1		%/V
Load regulation		LDO load = 5mA to 150mA, VIN = 6V		0.7		%
Current limit		VIN = 6V	200			mA
Over Temperature Shutdown						
Over temperature shutdown		temperature rising threshold		150		°C

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Hysteresis				20		°C
High-Side Driver						
Peak source current		BST-LX=5.25V		2		A
Source resistance		BST-LX=5.25V		1.2	1.7	Ω
Rise time ⁽¹⁾	t_{DH_R}	$C_L = 3.3nF$, BST-LX = 5.25V, LX = 5V		12		ns
Peak sink current		BST-LX=5.25V		2		A
Sink resistance		BST-LX=5.25V		0.8	1.4	Ω
Fall time ⁽¹⁾	t_{DH_F}	$C_L = 3.3nF$, BST-LX = 5.25V		8		ns
Propagation delay time ⁽¹⁾	t_{DH_PD}	From PWM input falling to DH output falling		16		ns
Low-Side Driver						
Peak source current		VDD = 5.25V		2		A
Source resistance		VDD = 5.25V		1.1	1.7	Ω
Rise time ⁽¹⁾	t_{DL_R}	$C_L = 3.3nF$, VDD = 5.25V		12		ns
Peak sink current		VDD = 5.25V		4		A
Sink resistance		VDD = 5.25V		0.4	0.8	Ω
Fall time ⁽¹⁾	t_{DL_F}	$C_L = 3.3nF$, VDD = 5.25V		6		ns
Propagation delay time ⁽¹⁾	t_{DL_PD}	From PWM input rising to DL output falling		16		ns
PWM Input						
Tri-state rising threshold		$V_{PWM_PEAK} = 3.3V$ and 5V, VDD = 5.25V	0.75	1.0	1.3	V
Tri-state falling threshold		$V_{PWM_PEAK} = 3.3V$ and 5V, VDD = 5.25V	1.7	2.1	2.5	V
Tri-state voltage		PWM float		1.45		V
Tri-state shutdown entry delay ⁽¹⁾	t_{TR_END}	VDD = 5.25V		303		ns
Tri-state shutdown exit delay ⁽¹⁾	t_{TR_EXD}	VDD = 5.25V		62		ns
PWM sink impedance			7.5	10	14	kΩ
PWM source impedance			19	26	34	kΩ
Operating frequency range			4		1000	kHz
Minimum pulse width at high				30		ns

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
FCCM						
Input logic high		Rising threshold	2.0			V
Input logic low		Falling threshold			0.8	V
Zero cross detector threshold		VDD = 5.25V	-1		+1	mV
Zero cross blanking time		FCCM enabled, VDD = 5.25V		325		ns
FCCM pin leakage current		FCCM = VDD		3.5	5.6	μA
		FCCM = GND	-1.5		1.5	μA
Intenal Bootstrap Switch						
On resistance				10		Ω
Leakage current				5	15	μA
Dead Time						
Minimum dead time		DT pin is floated		20		ns
Dead Time ⁽²⁾	t_{DT}	A capacitor $C_{DT} = 100\text{pF}$ connected from DT pin to GND		100		ns
Internal series resistor			15	24.5	38	kΩ

NOTES:

- (1) Refer to Figure 2 and Figure 3 for the timing definition.
- (2) The dead time is $C_{DT} \times 1\text{ns/pF}$, where C_{DT} is in pF.

Timing Diagram

Figure 2. Timing Diagram 1

Figure 3. Timing Diagram 2

Pin Descriptions

Pin #	Pin Name	Pin Function
1	BST	Bootstrap pin, supply for the high-side driver.
2	VIN	Power supply pin for the device.
3	FCCM	If FCCM pin is low, the low-side MOSFET is turned off when the inductor current reaches zero (diode emulation mode); if FCCM pin is pulled high or floated, the device operates in forced continuous conduction mode (FCCM).
4	DT	Dead time programming pin. Connect a ceramic capacitor from this pin to GND to set the dead time (1ns/pF) between DH and DL.
5	PWM	PWM input pin.
6	GND	Ground pin.
7	DL	Low-side drive output pin.
8	VDD	5.25V LDO output pin.
9	LX	Phase node.
10	DH	High-side drive output pin.
	THERMAL PAD	The exposed pad enhances thermal performance and is not electrically connected inside the package. It is recommended to connect the exposed pad to the ground plane.

Block Diagram

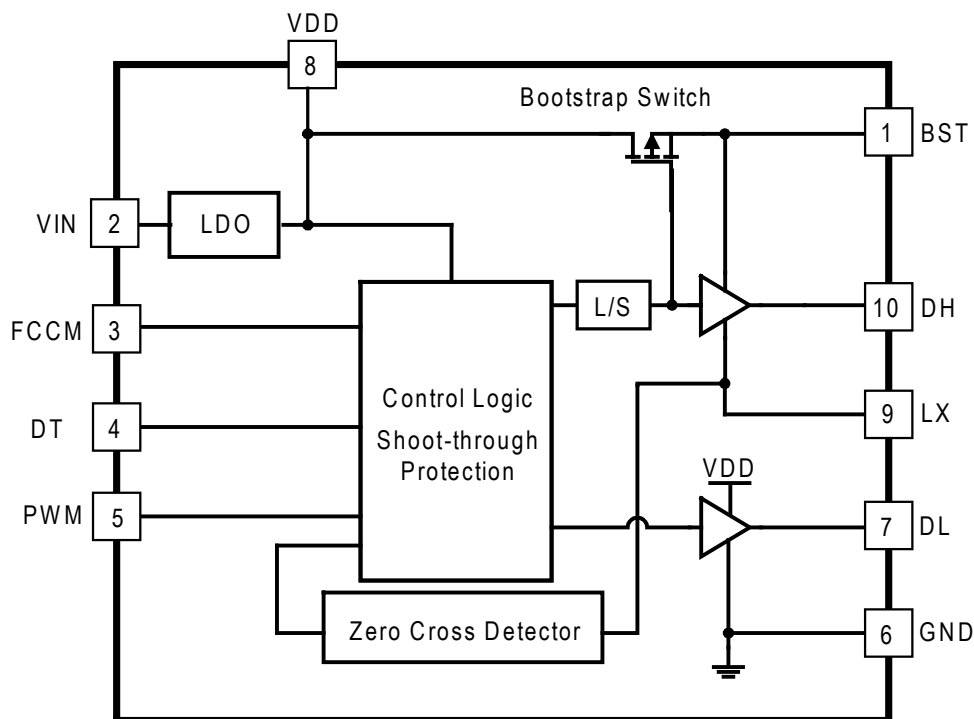
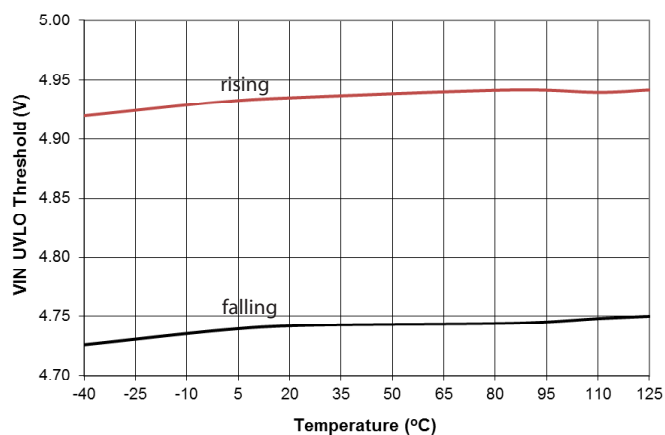


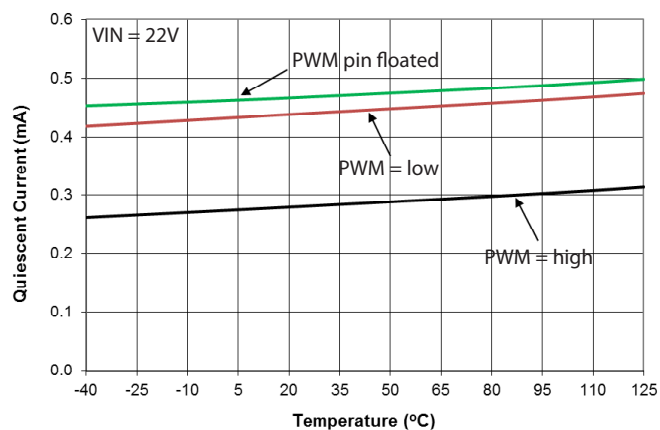
Figure 4. SC32300A Block Diagram

Typical Characteristics

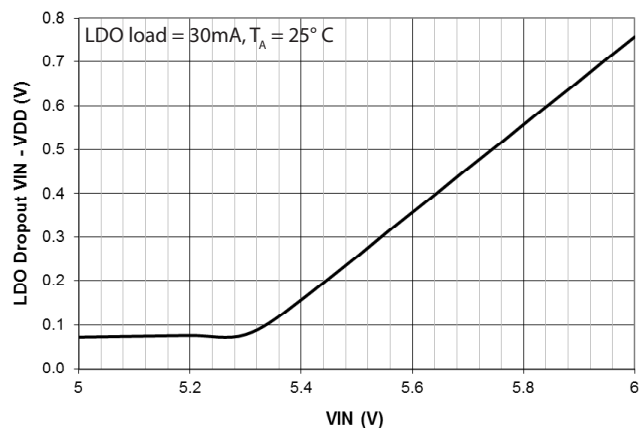
Under Voltage Lockout Threshold



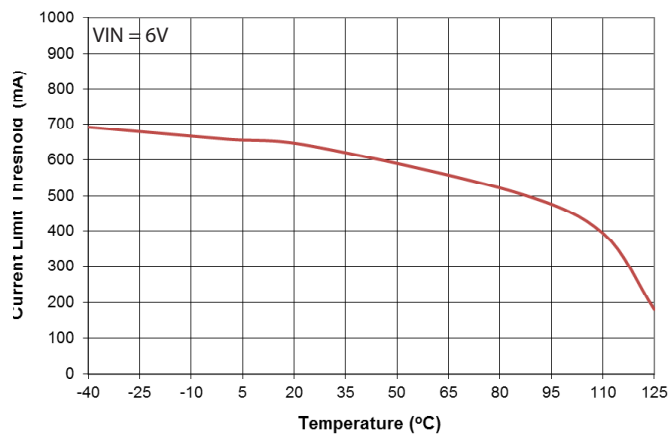
Input Bias Current



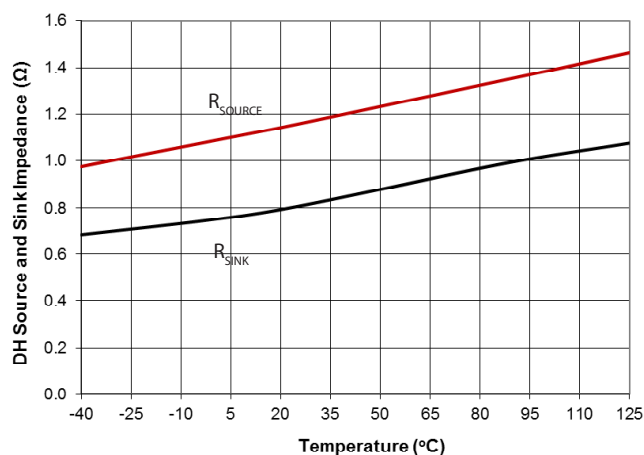
5.25V LDO Dropout Voltage



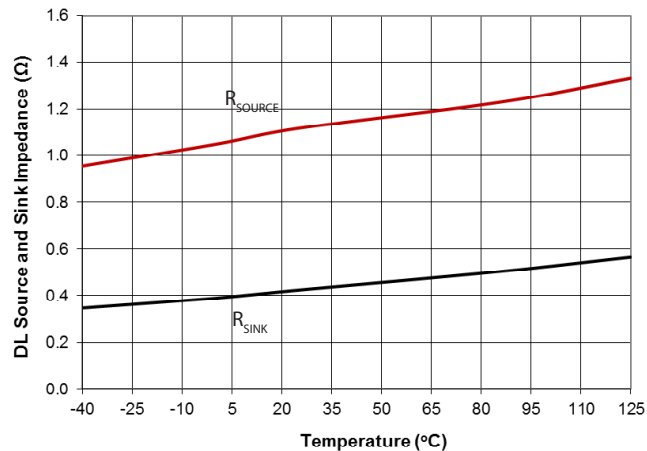
5.25V LDO Current Limit



High-Side Driver Source and Sink Impedance

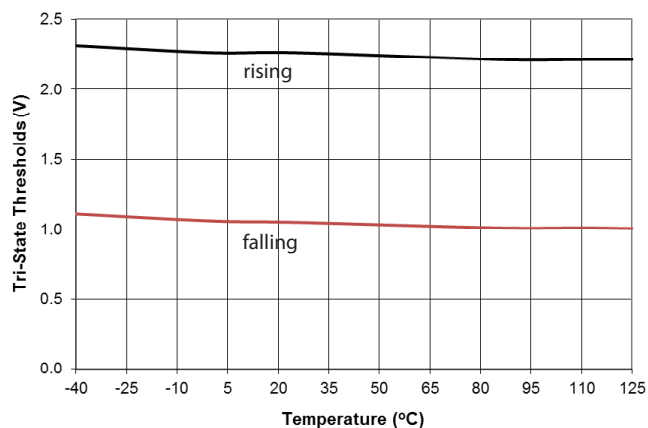


Low-Side Driver Source and Sink Impedance

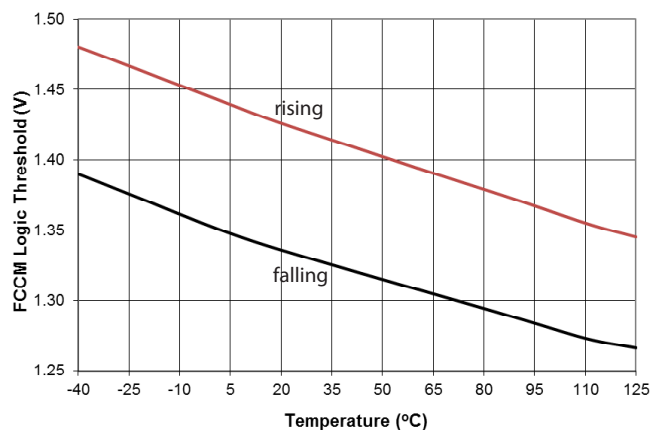


Typical Characteristics (Continued)

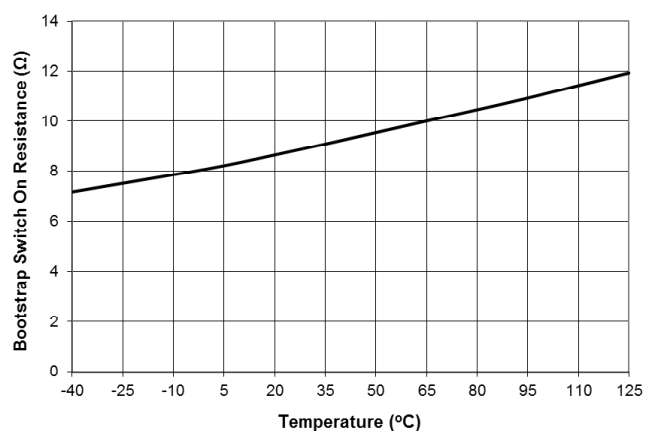
PWM Tri-State Thresholds



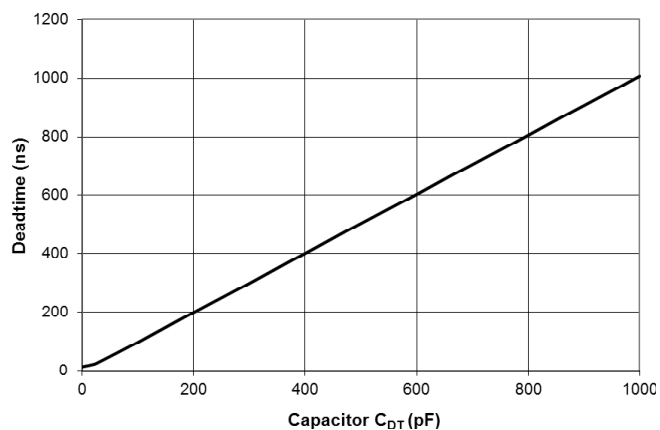
FCCM Logic Thresholds



Bootstrap Switch On Resistance



Dead Time vs C_{DT}



Application Information

Overview

The SC32300A is a high-side and low-side N-channel MOSFET driver. The driver receives a ground-referenced PWM signal with fast slew rate to drive two N-channel MOSFETs in a synchronous buck converter or any other application with two MOSFETs in a half-bridge configuration. The SmartDrive™ function at the turn-on of the high-side MOSFET reduces the voltage ringing on the low-side switch and also reduces the EMI. Tying the FCCM pin to ground offers diode emulation mode operation to achieve high efficiency at light load. The Under-Voltage-Lock-Out (UVLO) threshold ensures a reliable drive voltage for the external MOSFETs. The over temperature shutdown feature is also included to prevent the driver from overheating.

For a synchronous buck converter application, the SC32300A takes the PWM signal from the buck controller as the input, and outputs drive signals on the DH pin and the DL pin to drive the external MOSFETs. The buck controller senses and regulates the output voltage of the converter as shown in Figure 5 on page 13.

The SC32300A can also be used together with the SC32300B to drive a DC motor or similar load. Figure 7 on page 15 shows one typical application for driving the DC motor in an electronic tool. The SC32300A and SC32300B are controlled by PWM signals from the microcontroller. The SC32300A takes its input from the battery and regulates a 5.25V output on its VDD pin. This 5.25V is used to bias the internal control circuitry and the low-side driver. The 5.25V LDO output is also connected to the VDD pin of the SC32300B to bias its internal circuitry and low-side driver, and functions as the input for a 3.3V LDO in the SC32300B. The 3.3V LDO can then be used to power the microcontroller. The feature of programming the dead-time offers the flexibility to design the switch clamp circuitry for more reliable system operation.

Under Voltage Lockout

The SC32300A has an under voltage lockout (UVLO) circuit which keeps the driver off when the input voltage is not high enough to drive the external MOSFETs reliably. During power on, the driver outputs (DH and DL) are low until the input voltage reaches the UVLO rising threshold. Once the UVLO threshold is reached, the driver outputs

are determined by the signals on the PWM pin and FCCM pin. The UVLO falling threshold is about 0.2V lower which prevents the driver from turning on and off due to a slow input slew rate.

Tri-State PWM Input

The SC32300A features a tri-state PWM input pin. When the PWM signal is less than 1V (typical), it is considered as a logic low while the signal is taken as a logic high when it is higher than 2.1V (typical). 1V to 2.1V is the tri-state window for the PWM signal. These thresholds make it work well for both 3.3V logic and 5V logic PWM signals. If the PWM pin is left floating, the internal resistor divider sets the voltage on the PWM pin to 1.45V which is within the tri-state window. For a synchronous buck converter application, pre-biased output startup is supported if the buck controller features a tri-state PWM output pin.

Programmable Dead Time Control

The dead time control is to prevent shoot-through of the high-side MOSFET and the low-side MOSFET. Shoot-through can cause poor efficiency and even cause the MOSFET to blow up. The dead time control circuitry of a MOSFET driver is thus very important in real applications. An adaptive dead time control function is implemented in the SC32300A by sensing the DH and DL signals. The SC32300A has a DT pin which offers an option to program the dead time with a ceramic capacitor from this pin to the GND pin. A ceramic capacitor with tight tolerance such as Murata C0G material capacitor should be used for this purpose. The dead time is 20ns typical with the DT pin floated.

For DC motor drive in electronic tool applications, the system designer generally will add clamp circuitry for each external MOSFET as shown in Figure 7. In order to make the clamp circuitry work, an external gate resistor with value up to 20Ω is needed. The MOSFET drivers with traditional adaptive dead time control will not work with such a big external gate resistor added. The ability of programming the dead time from SC32300A is a good fit for this kind of application to provide the freedom to adjust the dead time based upon the added gate resistor to ensure reliable operation.

Application Information (Continued)

FCCM/Diode Emulation Mode Operation

There are two operating modes which can be configured with the FCCM pin of the SC32300A. When the FCCM pin is floated or tied to a logic high signal (e.g. VDD), the drive signal DL is always complementary to DH. This is called forced continuous conduction mode (FCCM) operation. If the FCCM pin is grounded, a zero-crossing circuit is activated in the SC32300A. The DL output is turned to low when the current in the external low-side MOSFET reaches zero. In other words, the external low-side MOSFET acts like a diode. This operation mode is thus called diode emulation mode. The benefit of this diode emulation mode is to reduce conduction losses at light load for high efficiency.

Smartdrive™

For each DH drive pulse, the SC32300A initially turns on the high-side MOSFET with a weak driver, allowing a softer, smooth turnoff of the low-side MOSFET. Once the low-side MOSFET is turned off and the LX pin voltage has risen about 2.5V above ground, the SC32300A switches to a much stronger driver to complete the turn-on of the high-side MOSFET at a more rapid rate. This technique reduces the voltage ringing for the switching node, which relieves the need for a snubber or a gate resistor.

Bootstrap Capacitor

The SC32300A integrates the bootstrap switch. Only an external bootstrap capacitor connected between the BST pin and the LX pin is needed for a complete bootstrap circuit. The bootstrap capacitor, which is charged from VDD during the on time of the low-side MOSFET, provides the energy to turn on the high-side MOSFET. The capacitance for the bootstrap capacitor is mainly determined by the gate charge Q_g of the high-side MOSFET. The equation below gives a first order estimate:

$$C_b = Q_g / \Delta V_b$$

Where ΔV_b is the allowable voltage drop of the drive voltage for the high-side MOSFET. In a real application, considering the capacitance tolerance, Q_g variation, leakage current of the BST pin etc., a capacitor with two

times the calculated value is a good starting point. A ceramic capacitor of X5R or X7R, or equivalent material, should be used.

VDD Decoupling Capacitor

The VDD pin is the 5.25V LDO output which provides the bias for the low-side driver and the internal control circuitry. A high frequency decoupling capacitor with low ESR and low ESL should be put from the VDD pin to the GND pin with minimum trace length. A typical value of 2.2μF, 10V rating, X5R or X7R ceramic capacitor is recommended.

VIN Decoupling Capacitor

The VIN pin is the input of the internal 5.25V LDO. This pin is also used for the input UVLO check. As for the VDD pin, a high frequency decoupling capacitor with low ESR and low ESL should be put from the VIN pin to the GND pin with minimum trace length. A typical value of 1μF, X5R or X7R ceramic capacitor is recommended. The voltage rating of the decoupling capacitor is determined by the input voltage. Please note that this decoupling capacitor is not the input bulk capacitor for the power stage. It is also recommended that the input for the driver should be connected to some point ahead of the input bulk capacitor instead of close to the external high-side MOSFET.

Power Dissipation

The power dissipation in this driver consists of two main components: the power loss for turning on and off the external MOSFETs, and the power loss in the internal LDO. The below equation can be used to estimate the total power dissipation in the driver:

$$P_d = 5.25 f_s (Q_{gh} + Q_{gl}) + (VIN - 5.25) (f_s (Q_{gh} + Q_{gl}) + I_L)$$

Where:

f_s is the switching frequency

Q_{gh} is the total gate charge of the high-side MOSFET

Q_{gl} is the total gate charge of the low-side MOSFET

I_L is the external load connected to the VDD pin

To ensure proper operation and long-term reliability, the power dissipation should be examined in the real

Application Information (Continued)

application to make sure the junction temperature will not go beyond 125°C. Multiple vias should be used to connect the thermal pad underneath the driver package to the ground plane on the system board for good thermal management.

$$T_j = T_A + P_d \theta_{JA}$$

Where:

T_j is the junction temperature

T_A is the ambient temperature

θ_{JA} is the thermal resistance, 42°C/W

There is a temperature monitor in the driver which will shut down the driver outputs and the LDO when the junction temperature reaches 150°C. The driver will automatically recover when the junction temperature cools to less than 132°C.

Layout Recommendations

The SC32300A is designed to provide strong source and sink capability for MOSFET drive at high frequency. In order to achieve this objective, the PCB layout is critical. Some guidelines are highlighted below to achieve good performance with SC32300A.

A. Locate the driver as close as possible to the MOSFETs. For a high conversion ratio buck converter (e.g. 12V input to 1V output), locate the driver as close as possible to the low-side MOSFET.

B. Mount the decoupling capacitors as close as possible between the VIN pin and the GND pin, the VDD pin and the GND pin, the BST pin and the LX pin.

C. Minimize the PCB trace length between the DL pin to the low-side MOSFET gate, the GND pin and the source of the low-side MOSFET. Avoid mixing the ground trace of the drive loop with the power stage current path.

D. Apply a similar rule for the high-side drive loop.

E. Use wide PCB trace > 20 mils for the drive loops.

F. Use two or more vias if the PCB trace for the drive loops needs to be routed from one layer to another.

G. The ground of the input signals (PWM, FCCM and DT) should be separated from the power ground plane and directly connected to the GND pin of the driver.

H. Use multiple vias to connect the thermal pad to the ground plane.

Typical Application Circuits

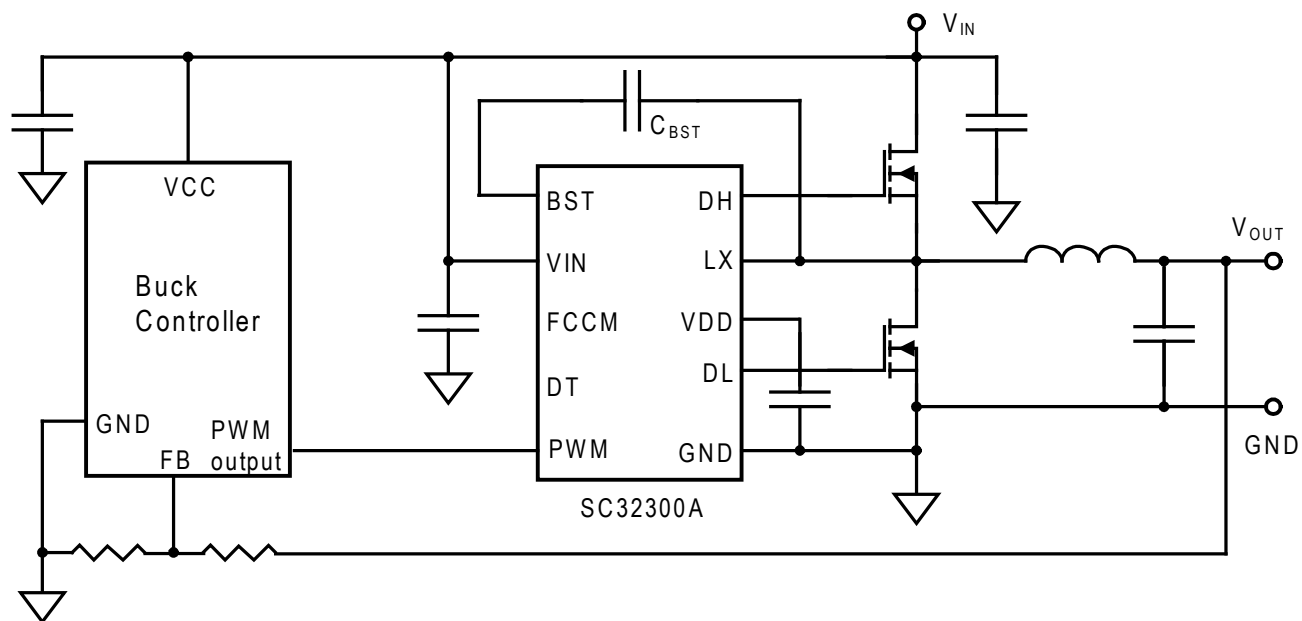
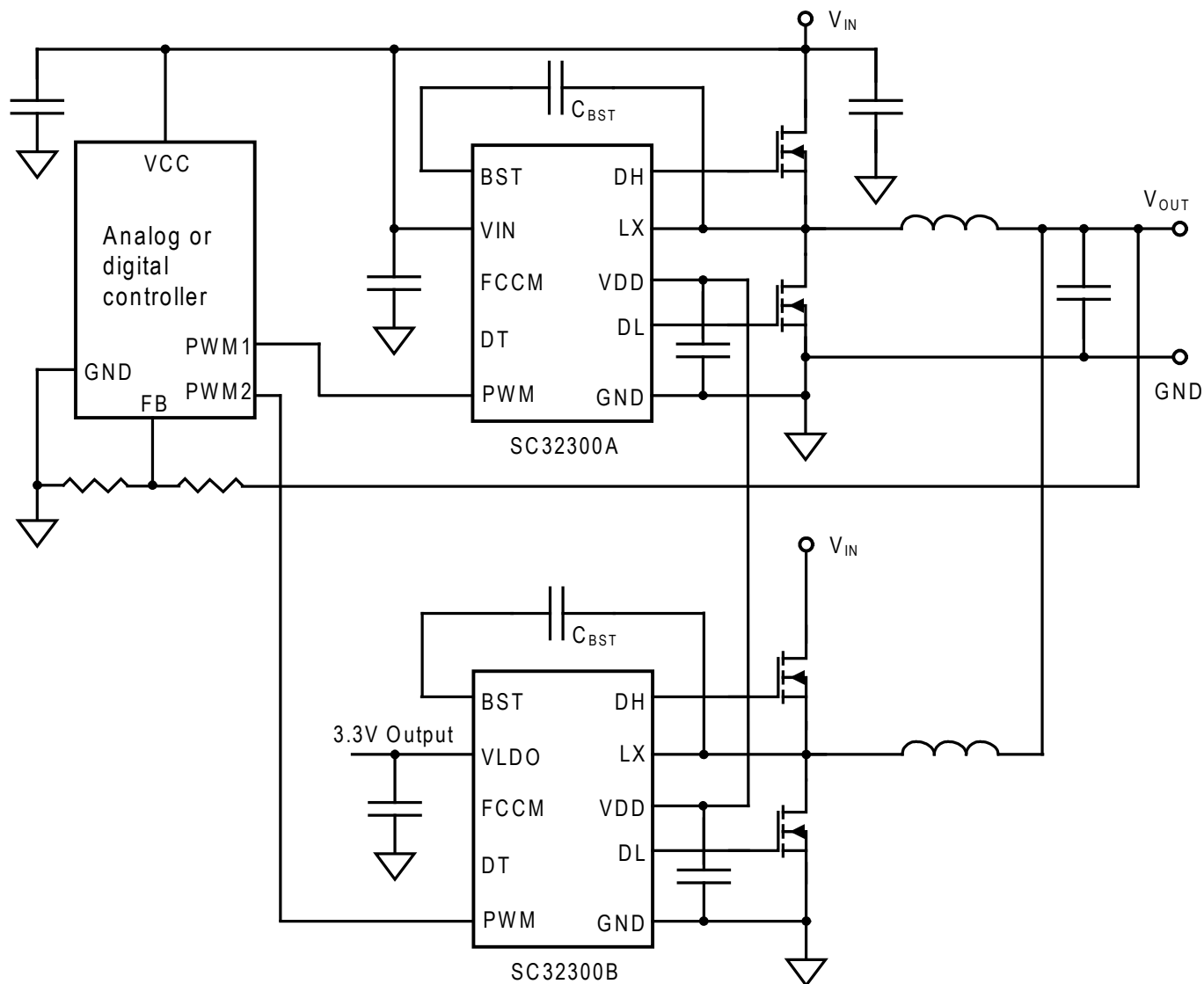


Figure 5. Single-Phase Synchronous Buck Converter

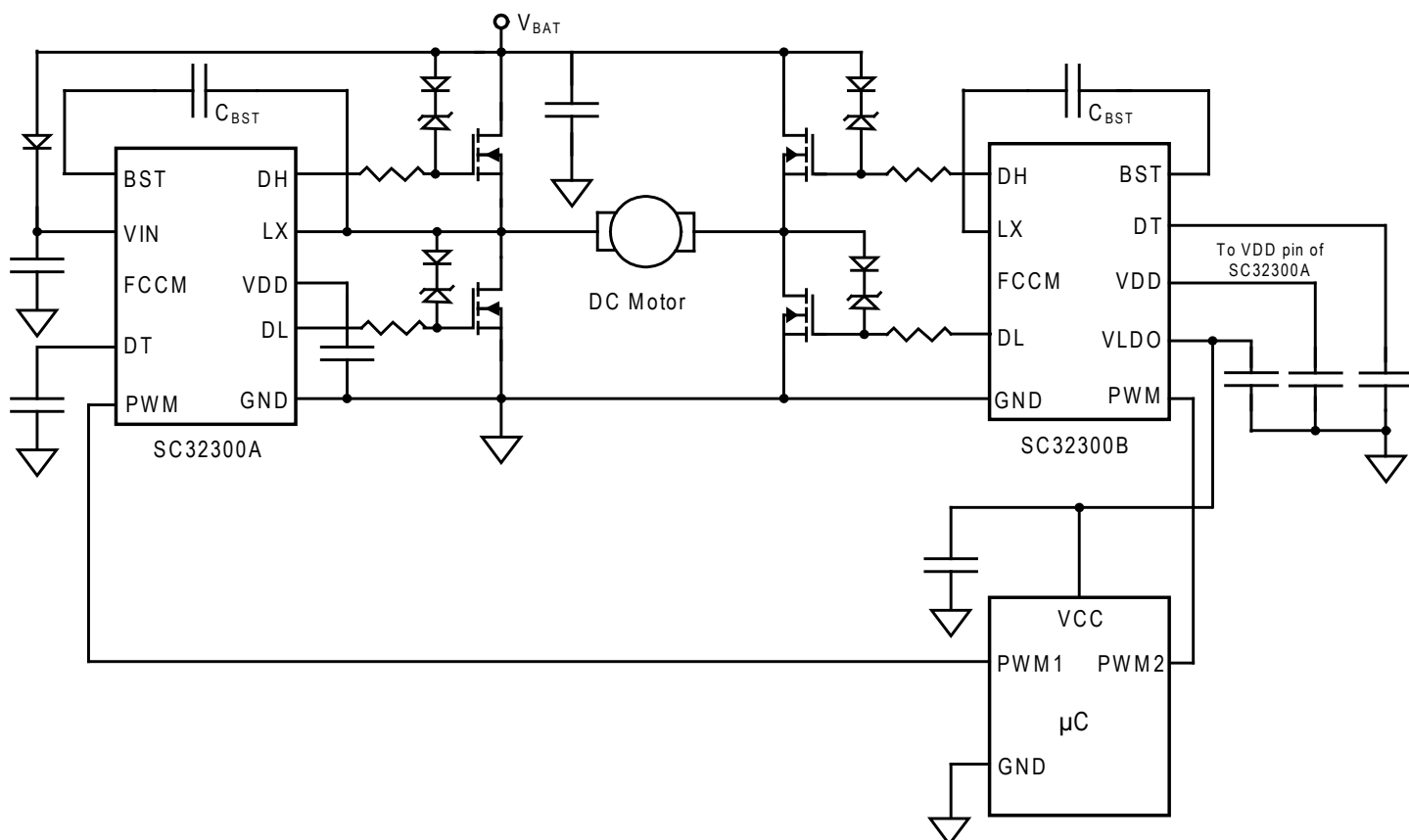
Typical Application Circuits (Continued)



Note: Referencing SC32300B datasheet

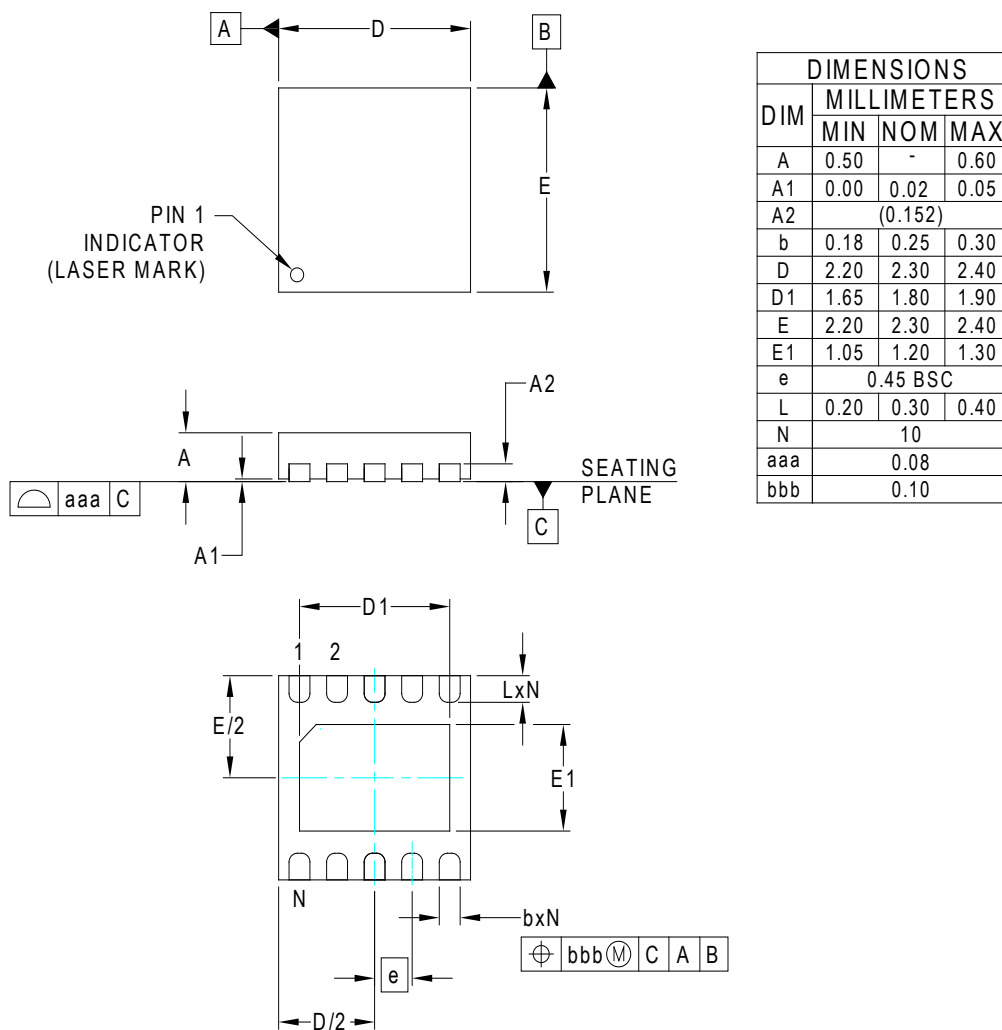
Figure 6. Dual-Phase Synchronous Buck Converter

Typical Application Circuits (Continued)

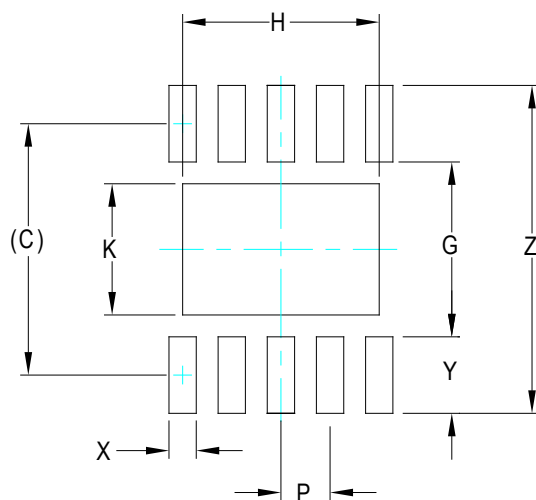


Note: Referencing SC32300B datasheet

Figure 7. DC Motor Drive

Outline Drawing — 2.3mm x 2.3mm MLPD-UT-10

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS TERMINALS.

Land Pattern — 2.3mm x 2.3mm MLPD-UT-10


DIMENSIONS	
DIM	MILLIMETERS
C	(2.30)
G	1.60
H	1.80
K	1.20
P	0.45
X	0.25
Y	0.70
Z	3.00

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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