74LV241

Octal buffer/line driver; 3-state

Rev. 03 — 10 October 2005 Product data sheet

1. General description

The 74LV241 is a low-voltage, Si-gate CMOS device and is pin and function compatible with 74HC241 and 74HCT241.

The 74LV241 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs (pins $1\overline{OE}$ and 2OE).

2. Features

- Optimized for low-voltage applications from 1.0 V to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- ESD protection:
  - HBM EIA/JESD22-A114-C exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay 1An to 1Yn, 2An to 2Yn	C_L = 15 pF; V_{CC} = 3.3 V		-	8.0	-	ns
C_i	input capacitance			-	3.5	-	pF
C_{PD}	power dissipation capacitance	V_{CC} = 3.3 V; V_I = GND to V_{CC}	[1]	-	30	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

PHILIPS

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV241N	–40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74LV241D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LV241DB	–40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LV241PW	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

5. Functional diagram

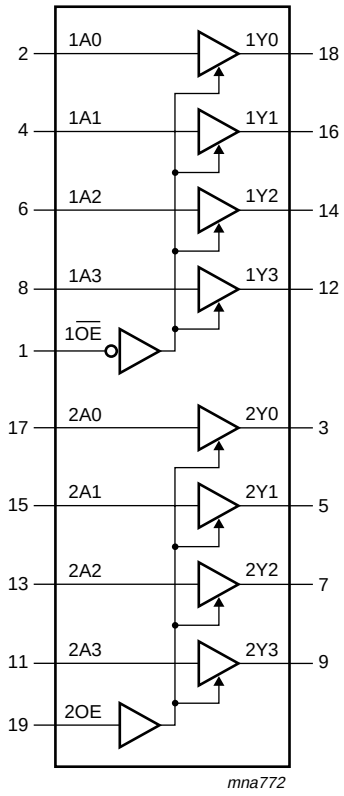


Fig 1. Functional diagram

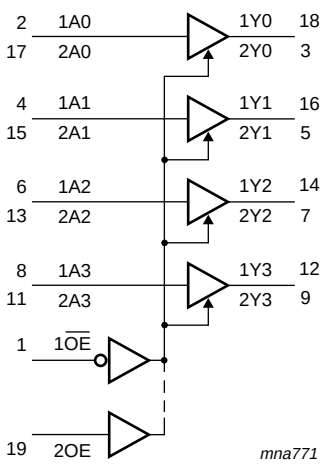


Fig 2. Logic symbol

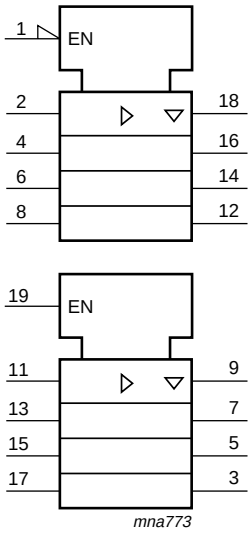


Fig 3. IEC logic symbol

6. Pinning information

6.1 Pinning

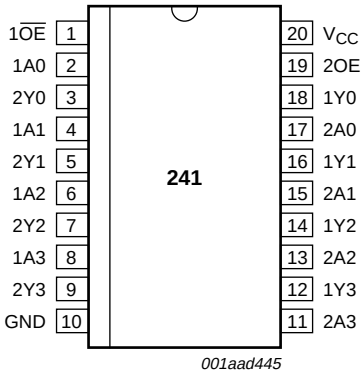


Fig 4. Pin configuration

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
1$\overline{OE}$	1	1 output enable input (active LOW)
1A0	2	1 data input 0
2Y0	3	2 bus output 0
1A1	4	1 data input 1
2Y1	5	2 bus output 1

Table 3: Pin description *...continued*

Symbol	Pin	Description
1A2	6	1 data input 2
2Y2	7	2 bus output 2
1A3	8	1 data input 3
2Y3	9	2 bus output 3
GND	10	ground (0 V)
2A3	11	2 data input 3
1Y3	12	1 bus output 3
2A2	13	2 data input 2
1Y2	14	1 bus output 2
2A1	15	2 data input 1
1Y1	16	1 bus output 1
2A0	17	2 data input 0
1Y0	18	1 bus output 0
2OE	19	2 output enable input (active HIGH)
V_{CC}	20	supply voltage

7. Functional description

7.1 Function table

Table 4: Function table [1]

Input		Output	Input		Output
$1\overline{OE}$	1An	1Yn	2OE	2An	2Yn
L	L	L	H	L	L
L	H	H	H	H	H
H	X	Z	L	X	Z

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+4.6	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±50	mA
I_O	output current	$V_O = 0.5$ V to $V_{CC} + 0.5$ V	-	±35	mA

Table 5: Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
I_{CC}	supply current		-	±70	mA
I_{GND}	ground current		-	±70	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C [1]			
	DIL20 package		-	750	mW
	SO20 package		-	500	mW
	(T)SSOP20 package		-	400	mW

[1] For DIL20 packages: above 70 °C the value of P_{tot} derates linearly with 12 mW/K.
For SO20 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For (T)SSOP20 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage		[1]	1.0	3.3	3.6	V
V_I	input voltage			0	-	V_{CC}	V
V_O	output voltage			0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air		–40	-	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.0 V to 2.0 V		-	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V		-	-	200	ns/V
		V_{CC} = 2.7 V to 3.6 V		-	-	100	ns/V

[1] The 74LV241 is guaranteed to function down to 1.0 V (input levels GND or V_{CC}); static characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 3.6 V.

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.9	-	-	V
		V_{CC} = 2.0 V	1.4	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.3	V
		V_{CC} = 2.0 V	-	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V

Table 7: Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		V_{CC} = 1.2 V; I_O = –100 µA	-	1.2	-	V
		V_{CC} = 2.0 V; I_O = –100 µA	1.8	2.0	-	V
		V_{CC} = 2.7 V; I_O = –100 µA	2.5	2.7	-	V
		V_{CC} = 3.0 V; I_O = –100 µA	2.8	3.0	-	V
		V_{CC} = 3.0 V; I_O = –8 mA	2.40	2.82	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		V_{CC} = 1.2 V; I_O = 100 µA	-	0	-	V
		V_{CC} = 2.0 V; I_O = 100 µA	-	0	0.2	V
		V_{CC} = 2.7 V; I_O = 100 µA	-	0	0.2	V
		V_{CC} = 3.0 V; I_O = 100 µA	-	0	0.2	V
		V_{CC} = 3.0 V; I_O = 8 mA	-	0.20	0.40	V
I_{LI}	input leakage current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND	-	-	1.0	µA
I_{OZ}	3-state output OFF-state current	V_{CC} = 3.6 V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND	-	-	5	µA
I_{CC}	quiescent supply current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0 A	-	-	20	µA
ΔI_{CC}	additional quiescent supply current per input pin	V_{CC} = 2.7 V to 3.6 V; $V_I = V_{CC}$ – 0.6 V	-	-	500	µA
C_i	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.9	-	-	V
		V_{CC} = 2.0 V	1.4	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.3	V
		V_{CC} = 2.0 V	-	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		V_{CC} = 1.2 V; I_O = –100 µA	-	-	-	V
		V_{CC} = 2.0 V; I_O = –100 µA	1.8	-	-	V
		V_{CC} = 2.7 V; I_O = –100 µA	2.5	-	-	V
		V_{CC} = 3.0 V; I_O = –100 µA	2.8	-	-	V
		V_{CC} = 3.0 V; I_O = –8 mA	2.20	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		V_{CC} = 1.2 V; I_O = 100 µA	-	-	-	V
		V_{CC} = 2.0 V; I_O = 100 µA	-	-	0.2	V
		V_{CC} = 2.7 V; I_O = 100 µA	-	-	0.2	V
		V_{CC} = 3.0 V; I_O = 100 µA	-	-	0.2	V
		V_{CC} = 3.0 V; I_O = 8 mA	-	-	0.50	V
I_{LI}	input leakage current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND	-	-	1.0	µA

Table 7: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OZ}	3-state output OFF-state current	V_{CC} = 3.6 V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	-	-	10	µA
I_{CC}	quiescent supply current	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 A	-	-	160	µA
ΔI_{CC}	additional quiescent supply current per input pin	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} – 0.6 V	-	-	850	µA

[1] All typical values are measured at T_{amb} = 25 °C

11. Dynamic characteristics

Table 8: Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF; unless otherwise stated; for test circuit see Figure 8

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]							
t_{PHL}, t_{PLH}	propagation delay 1An to 1Yn, 2An to 2Yn	see Figure 5					
		V_{CC} = 1.2 V		-	45	-	ns
		V_{CC} = 2.0 V		-	15	31	ns
		V_{CC} = 2.7 V		-	11	23	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	-	9	18	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	8	-	ns
t_{PZH}, t_{PZL}	3-state output enable time 1$\overline{OE}$ to 1Yn, 2OE to 2Yn	see Figure 6 and Figure 7					
		V_{CC} = 1.2 V		-	55	-	ns
		V_{CC} = 2.0 V		-	19	36	ns
		V_{CC} = 2.7 V		-	14	26	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	-	10	21	ns
t_{PHZ}, t_{PLZ}	3-state output disable time 1$\overline{OE}$ to 1Yn, 2OE to 2Yn	see Figure 6 and Figure 7					
		V_{CC} = 1.2 V		-	60	-	ns
		V_{CC} = 2.0 V		-	22	39	ns
		V_{CC} = 2.7 V		-	17	29	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	-	13	24	ns
C_{PD}	power dissipation capacitance	V_{CC} = 3.3 V; V_I = GND to V_{CC}	[3]	-	30	-	pF
T_{amb} = –40 °C to +125 °C							
t_{PHL}, t_{PLH}	propagation delay 1An to 1Yn, 2An to 2Yn	see Figure 5					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.0 V		-	-	36	ns
		V_{CC} = 2.7 V		-	-	26	ns
		V_{CC} = 3.0 V to 3.6 V		-	-	21	ns

Table 8: Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF; unless otherwise stated; for test circuit see Figure 8

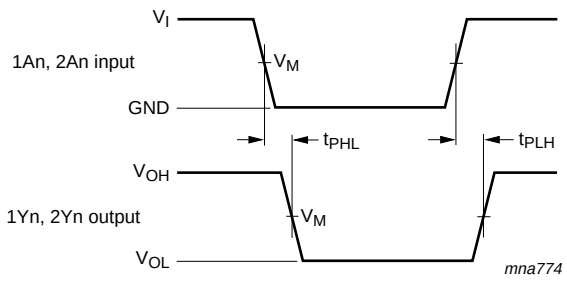
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PZH}, t_{PZL}	3-state output enable time $1\overline{OE}$ to 1Yn, 2OE to 2Yn	see Figure 6 and Figure 7				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.0 V	-	-	44	ns
		V_{CC} = 2.7 V	-	-	33	ns
		V_{CC} = 3.0 V to 3.6 V	-	-	26	ns
t_{PHZ}, t_{PLZ}	3-state output disable time $1\overline{OE}$ to 1Yn, 2OE to 2Yn	see Figure 6 and Figure 7				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.0 V	-	-	48	ns
		V_{CC} = 2.7 V	-	-	36	ns
		V_{CC} = 3.0 V to 3.6 V	-	-	29	ns

[1] All typical values are measured at T_{amb} = 25 °C

[2] These typical values are measured at V_{CC} = 3.3 V

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

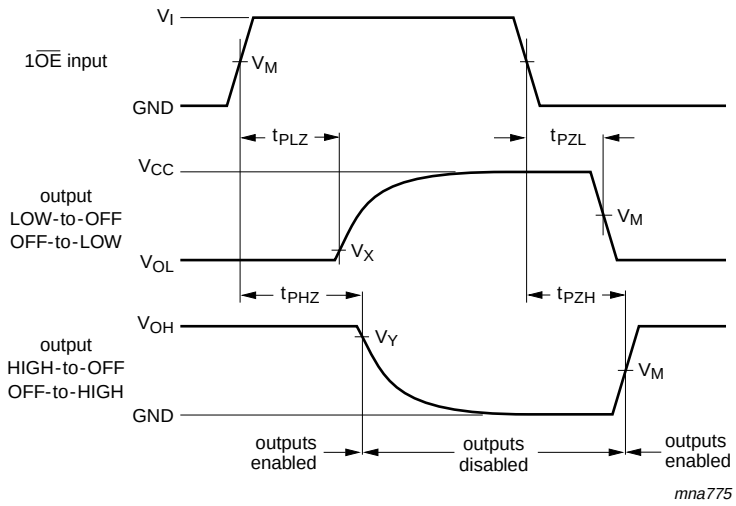
12. Waveforms



For measurement points see Table 9

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

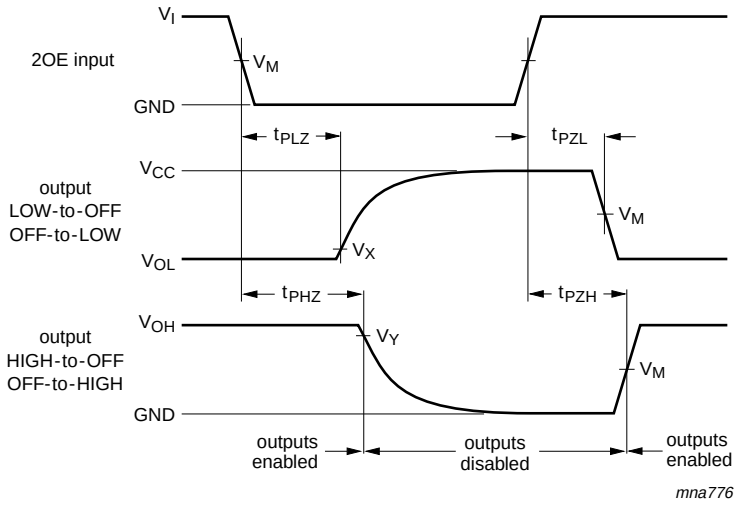
Fig 5. Input (1An, 2An) to output (1Yn, 2Yn) propagation delay



For measurement points see Table 9

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

Fig 6. 3-state enable and disable times for input $1\overline{OE}$



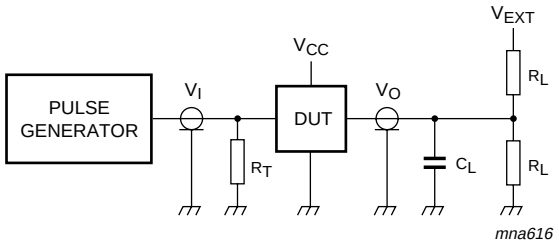
For measurement points see Table 9

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

Fig 7. 3-state enable and disable times for input 2OE

Table 9: Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_X	V_Y	V_M
< 2.7 V	$0.5 \times V_{CC}$	$V_{OL} + 0.1 \times V_{CC}$	$V_{OH} - 0.1 \times V_{CC}$	$0.5 \times V_{CC}$
≥ 2.7 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V	1.5 V



Test data is given in Table 10.

Definitions test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External test voltage

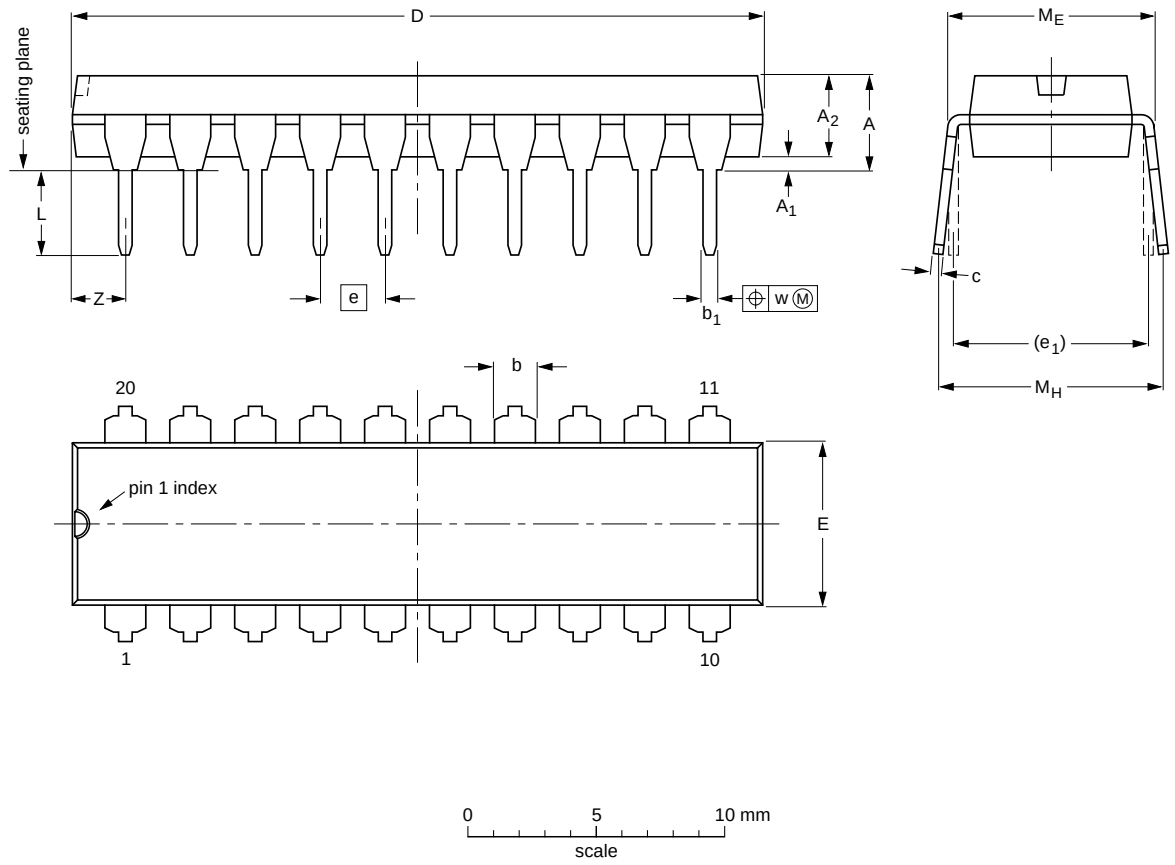
Fig 8. Load circuitry for switching times

Table 10: Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
< 2.7 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	open	GND	$2 \times V_{CC}$
≥ 2.7 V	2.7 V	≤ 2.5 ns	50 pF	1 kΩ	open	GND	$2 \times V_{CC}$

13. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

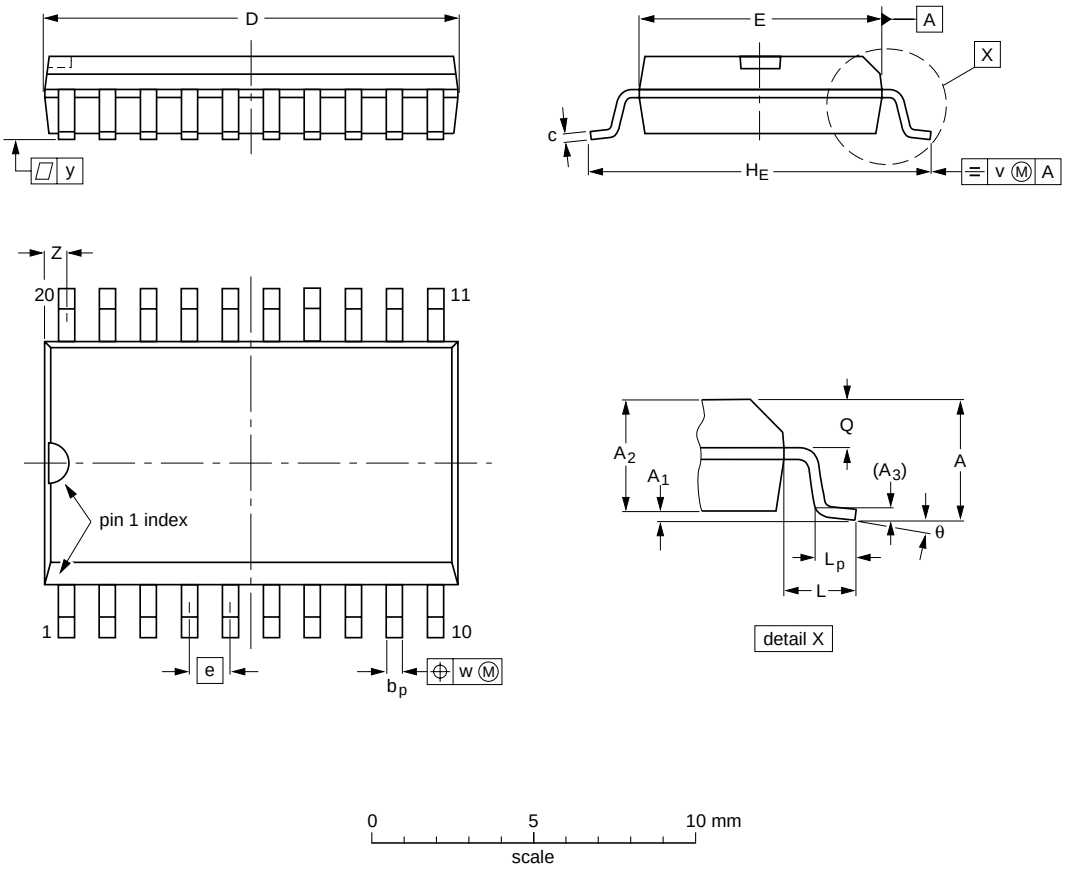
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT146-1		MS-001	SC-603			~~99-12-27~~ 03-02-13

Fig 9. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

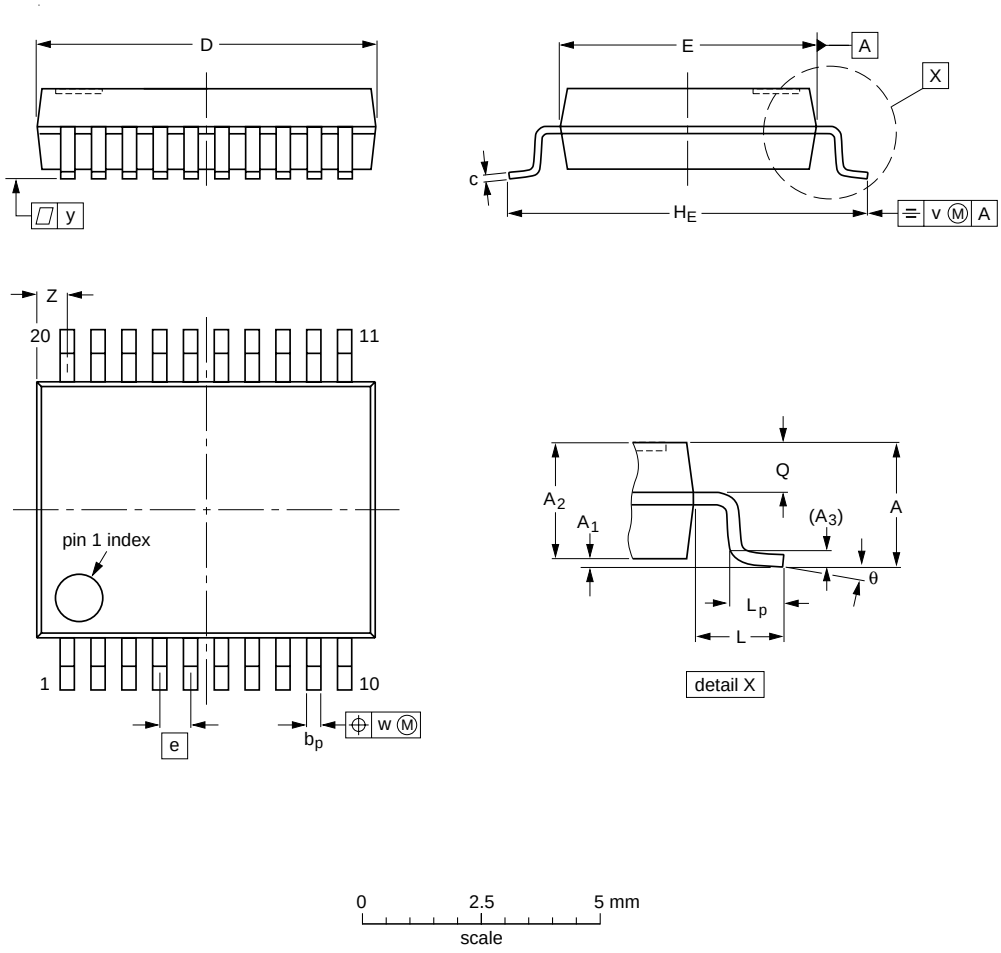
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8^o 0^o

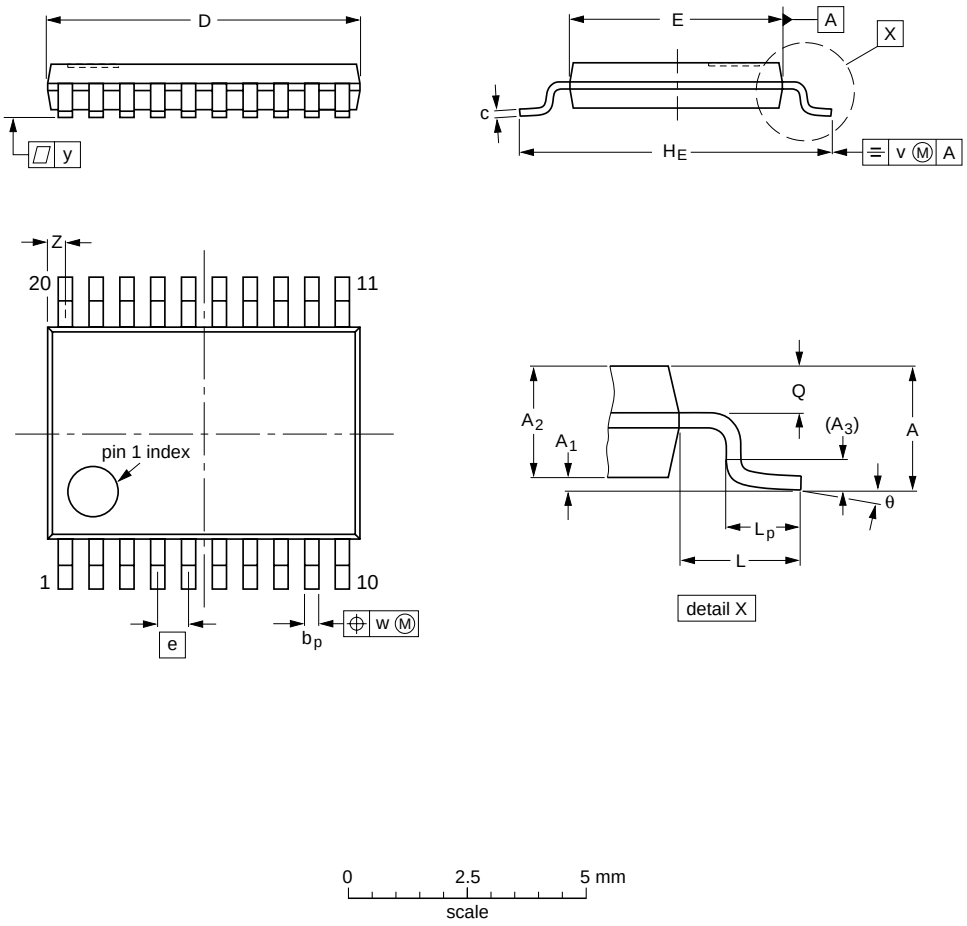
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT360-1 (TSSOP20)

14. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74LV241_3	20051010	Product data sheet	-	-	74LV241_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Section 7.1 “Function table”: Corrected 1Yn values				
74LV241_2	19980520	Product specification	-	9397 750 04436	74LV241_1
74LV241_1	19970219	Product specification	-	-	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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20. Contents

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