# 20-W MONO DIGITAL INPUT AUDIO AMPLIFIER

## FEATURES

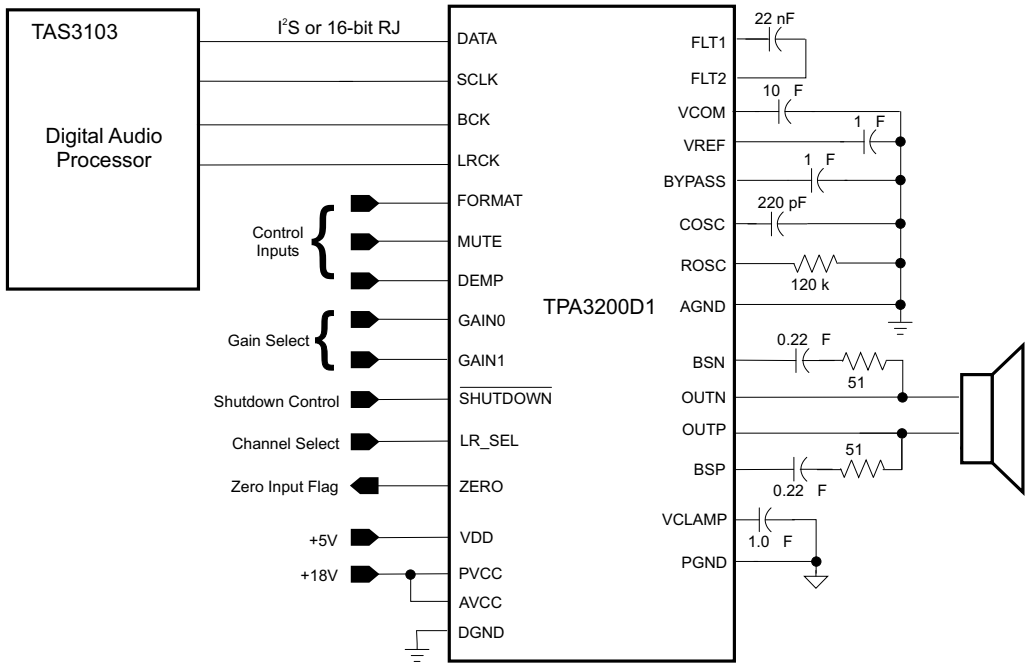
- **Digital Interface**
  - **– 24-bit Resolution**
  - **– Supports I²S and 16-Bit Word Right-Justified Digital Input Formats**
  - **– Multiple Sampling Frequencies: 5 kHz – 200 kHz**
  - **– 8x Oversampling Digital Filter**
  - **– Soft Mute**
- **Power Amplifier**
  - **– 20-W into an 8-Ω Load from an 18-V Supply**
  - **– Efficient Operation Eliminates Need for Heat Sinks**
  - **– Three Selectable, Fixed Gain Settings**
  - **– Thermal and Short-Circuit Protection**

## DESCRIPTION

The TPA3200D1 is a 20-W (per channel) efficient, digital audio power amplifier for driving a bridged-tied speaker. The TPA3200D1 can drive a speaker with an impedance as low as 4 Ω. The high efficiency of the TPA3200D1 (85%) eliminates the need for an external heat sink.

The digital input accepts 16-24 bit data in I²S format or 16-bit word right-justified. A digital filter performs an 8x interpolation function. Other features include soft mute, a zero input detect output flag for power conscious designs, and power saving shutdown mode.

**Simplified Application Circuit**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## AVAILABLE OPTIONS

| $T_A$ | PACKAGED DEVICE 44-PIN (DCP)(1) |
|---|---|
| –40°C to 85°C | TPA3200D1DCP |

(1) The DCP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA3200D1DCPR).

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

| | | TPA3200D1 | UNIT |
|---|---|---|---|
| $V_{SS}$ | Supply voltage, VCC, PVCC | –0.3 to 21 | V |
| | Supply voltage, VDD | –0.3 to 6.5 | V |
| $R_L$ | Load Impedance | ≥3.6 | Ω |
| Vi | $\overline{\text{SHUTDOWN}}$ | – 0.3 to $V_{CC}$ + 0.3 | V |
| | GAIN0, GAIN1, BCK, SCLK, DATA, LRCK, LR_SEL | –0.3 to $V_{DD}$ + 0.3 | V |
| | FORMAT, MUTE, DEMP | | |
| | Continuous total power dissipation | See Dissipation Rating Table | |
| $T_A$ | Operating free-air temperature range | –25 to 85 | °C |
| $T_J$ | Operating junction temperature range | –25 to 150 | °C |
| $T_{stg}$ | Storage temperature range | –65 to 150 | °C |
| | Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds | 260 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## DISSIPATION RATINGS

| PACKAGE | $T_A \le 25°C$ | DERATING FACTOR ($1/\theta_{JA}$) | $T_A = 70°C$ | $T_A = 85°C$ |
|---|---|---|---|---|
| 44-pin DCP | 4.89 W | 39.1 mW/°C(1) | 3.13 W | 2.54 W |

(1) Based on a JEDEC high-K PCB with the PowerPAD™ soldered to a thermal land on the printed-circuit board. See the *PowerPAD Thermally Enhanced Package* technical brief, literature number SLMA0002. The PowerPAD must be soldered to the PCB.

## RECOMMENDED OPERATING CONDITIONS

| | PARAMETER | PIN NAME | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{SS}$ | Supply voltage | PVCC, VCC | 8 | 18 | V |
| | | VDD | 4.5 | 5.5 | |
| $V_{IH}$ | High-level input voltage | $\overline{SHUTDOWN}$, GAIN0, GAIN1, BCK, SCLK, DATA, LRCK, FORMAT, MUTE, DEMP | 2 | | |
| $V_{IL}$ | Low-level input voltage | $\overline{SHUTDOWN}$, GAIN0, GAIN1, BCK, SCLK, DATA, LRCK, FORMAT, MUTE, DEMP | | 0.8 | |
| $V_{IH}$ | High-level input voltage | LR_SEL | VDD x 0.7 | | |
| $V_{IL}$ | Low-level input voltage | LR_SEL | | VDD x 0.3 | |
| $I_{IH}$ | High-level input current | $\overline{SHUTDOWN}$: $V_I$ = VCC, VCC = 12 V | | 1 | µA |
| | | GAIN0, GAIN1, LR_SEL: $V_I$ = VDD, VDD = 5 V | | 1 | |
| | | SCLK, BCK, DATA, LRCK: $V_I$ = VDD, VDD = 5 V | | 10 | |
| | | FORMAT, MUTE, DEMP: $V_I$ = VDD, VDD = 5 V | | 100 | |
| $I_{IL}$ | Low-level input current | $\overline{SHUTDOWN}$: $V_I$ = 0 V, VCC = 12 V | | 1 | |
| | | GAIN0, GAIN1, LR_SEL: $V_I$ = 0 V, VDD = 5 V | | 1 | |
| | | BCK, SCLK, DATA, LRCK, FORMAT, MUTE, DEMP: $V_I$ = 0 V, VDD = 5 V | | 10 | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –1 mA, ZERO | 2.4 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 1 mA, ZERO | | 0.4 | |
| $f_{OSC}$ | Oscillator frequency | | 200 | 300 | kHz |

## ELECTRICAL CHARACTERISTICS

All specifications at $T_A$ = 25°C, $V_{DD}$ = 5 V, $f_S$ = 44.1 kHz, system clock = 384 $f_S$ and 24-bit data, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY REQUIREMENTS(1)** | | | | | | |
| $I_{DD}$ | Supply current | $f_S$ = 44.1 kHz | | 26 | 31 | mA |
| | | $f_S$ = 96 kHz | | 25 | | |
| | | $f_S$ = 192 kHz | | 30 | | |
| **DIGITAL FILTER PERFORMANCE** | | | | | | |
| **FILTER CHARACTERISTICS** | | | | | | |
| | Pass band | ±0.04 dB | | | 0.454 $f_s$ | |
| | Stop band | | 0.546 $f_s$ | | | |
| | Pass-band ripple | | | | ±0.04 | dB |
| | Stop-band attenuation | Stop band = 0.546 $f_S$ | –50 | | | dB |
| **ANALOG FILTER PERFORMANCE** | | | | | | |
| | Frequency response | At 20 kHz | | –0.03 | | dB |
| | | At 44 kHz | | –0.20 | | |
| **SAMPLING FREQUENCY** | | | | | | |
| fs | Sampling frequency | | 5 | | 200 | KHz |
| **DYNAMIC PERFORMANCE** | | | | | | |
| | Channel separation | $f_S$ = 44.1 KHz, 96 KHz, 192 KHz | | 100 | | dB |

(1) Conditions in 192-kHz operation are system clock = 128 $f_S$ and oversampling rate = 64 $f_S$ of register 18.

## FORMAT CHARACTERISTICS

All specifications at $T_A$ = 25°C, $V_{DD}$ = 5 V, $f_S$ = 44.1 kHz, system clock = 384 $f_S$ and 24-bit data, unless otherwise noted

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Resolution | | | 24 | | Bits |
| **Data** | | | | | |
| Audio-data interface format Audio | $I^2S$, standard | | | | |
| Audio-data bit length Audio | 16–24-bit ($I^2S$), 16-bit (Right-justified) | | | | |
| Audio data format | MSB first, 2s complement | | | | |
| System clock frequency | 128 $f_S$, 192 $f_S$, 256 $f_S$, 384 $f_S$, 512 $f_S$, 768 $f_S$, 1152 $f_S$ | | | | |

## ELECTRICAL CHARACTERISTICS

at $T_A$ = 25°C, $PV_{CC}$ = $V_{CC}$ = 12 V (unless otherwise noted)

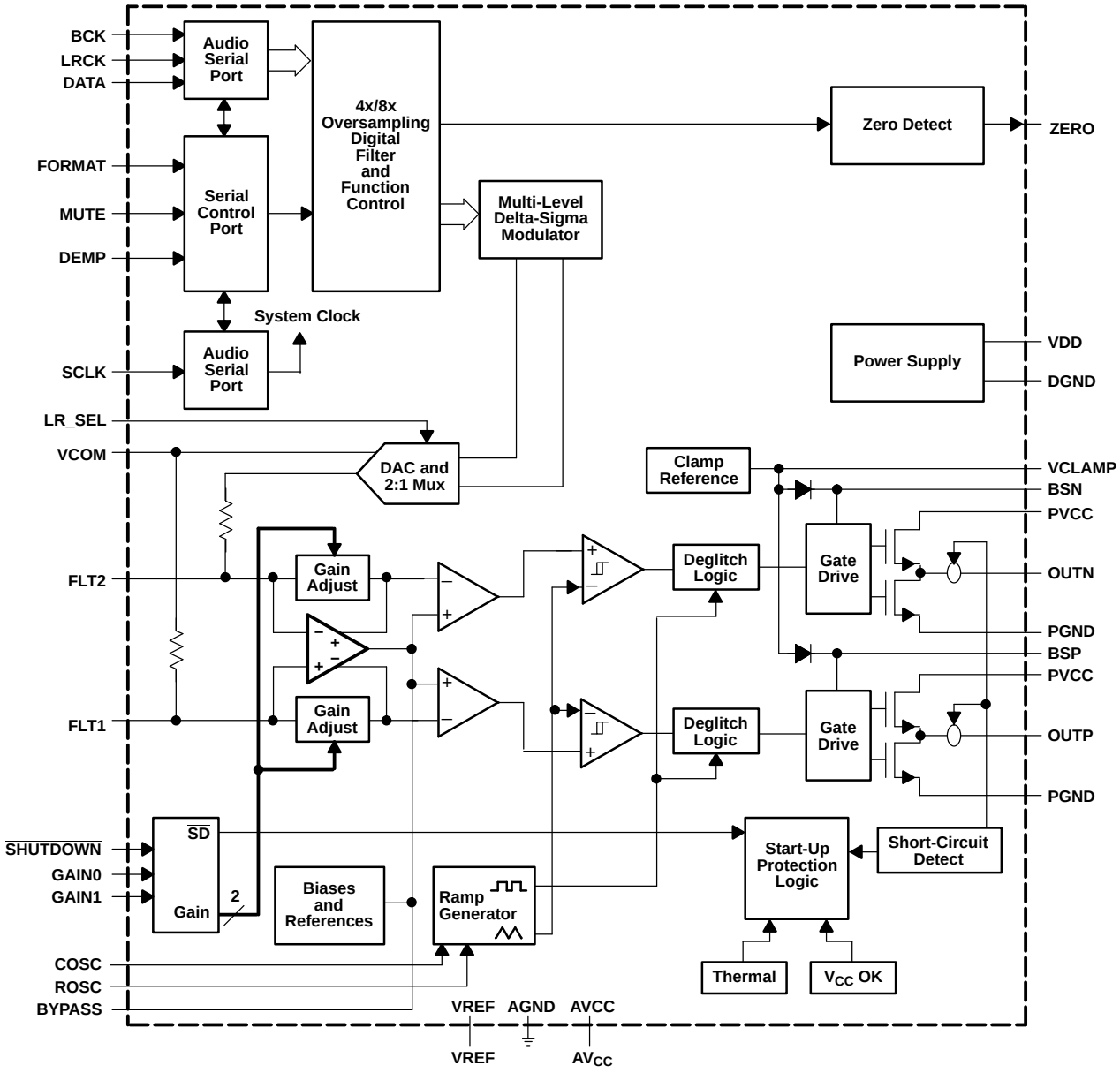
| | PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $\|V_{OS}\|$ | Output offset voltage (measured differentially) | MUTE = 2 V | $A_V$ = 12 dB | | | 100 | mV |
| PSRR | Power supply rejection ratio | $PV_{CC}$ = 11.5 V to 12.5 V | | | –73 | | dB |
| $V_{REF}$ | 5 V regulator voltage | $I_L$ = 10 mA, $V_{CC}$ = 8 V – 18 V | | 4.55 | 4.9 | 5.45 | V |
| $I_{CC}$ | Supply current | $\overline{SHUTDOWN}$ = 2.0 V, No load | | | 8 | 15 | mA |
| | | $\overline{SHUTDOWN}$ = $V_{CC}$, $V_{CC}$ = 18 V, PO = 20 W, $R_L$ = 8 Ω | | | 1.3 | | A |
| $I_{CC(SD)}$ | Supply current shutdown mode | $\overline{SHUTDOWN}$ = 0.8 V | | | 1 | 2 | µA |
| $r_{DS(on)}$ | Output transistor on resistance (high side and low side) | $I_O$ = 0.5 A, $T_J$ = 25°C | | 0.5 | 0.6 | 0.7 | Ω |
| G | Gain | GAIN1 = 0.8 V, GAIN0 = 0.8 V | | 10.9 | 12 | 13.1 | dB |
| | | GAIN1 = 0.8 V, GAIN0 = 2 V | | 17.1 | 18 | 18.6 | |
| | | GAIN1 = 2 V, GAIN0 = 0.8 V | | 22.9 | 23.6 | 24.4 | |

## OPERATING CHARACTERISTICS

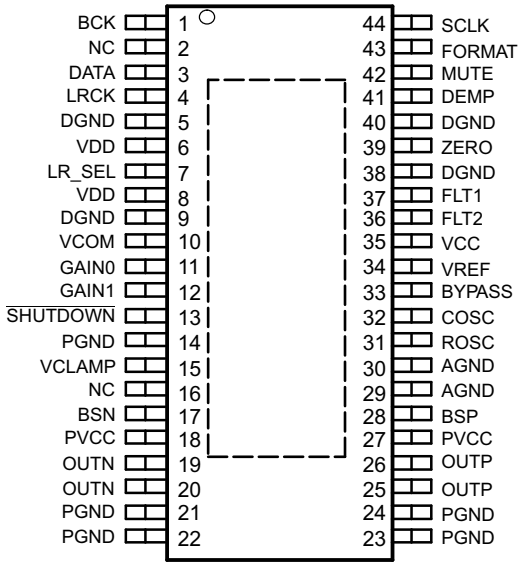
$PV_{CC}$ = $V_{CC}$ = 12 V, $T_A$ = 25° C unless otherwise noted

| | PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $P_O$ | Continuous output power at 10% THD+N | f = 1 kHz, | $R_L$ = 4 Ω | | 12.8 | | W |
| | | f = 1 kHz, | $R_L$ = 8 Ω | | 9 | | |
| | Continuous output power at 1% THD+N | f = 1 kHz, | $R_L$ = 4 Ω | | 10.3 | | |
| | | f = 1 kHz, | $R_L$ = 8 Ω | | 7.5 | | |
| THD+N | Total harmonic distortion plus noise | $P_O$ = 10 W, $R_L$ = 4 Ω | f = 20 Hz to 20 kHz | | 0.2% | | |
| $B_{OM}$ | Maximum output power bandwidth | THD = 1% | | | 20 | | kHz |
| $k_{SVR}$ | Supply ripple rejection ratio | f = 1 kHz, | $C_{(BYPASS)}$ = 1 µF | | –60 | | dB |
| SNR | Signal-to-noise ratio | $P_O$ = 10 W, $R_L$ = 4 Ω | | | 95 | | |
| $V_n$ | Noise output voltage | $C_{(BYPASS)}$ = 1 µF, A-weighted filter | f = 20 Hz to 22 kHz, Gain = 12 dB | | 150 | | µV(rms) |
| | | | | | –76.5 | | dBV |

## Functional Block Diagram



**DCP**
**(TOP VIEW)**


BCK 1
NC 2
DATA 3
LRCK 4
DGND 5
VDD 6
LR_SEL 7
VDD 8
DGND 9
VCOM 10
GAIN0 11
GAIN1 12
SHUTDOWN 13
PGND 14
VCLAMP 15
NC 16
BSN 17
PVCC 18
OUTN 19
OUTN 20
PGND 21
PGND 22
44 SCLK
43 FORMAT
42 MUTE
41 DEMP
40 DGND
39 ZERO
38 DGND
37 FLT1
36 FLT2
35 VCC
34 VREF
33 BYPASS
32 COSC
31 ROSC
30 AGND
29 AGND
28 BSP
27 PVCC
26 OUTP
25 OUTP
24 PGND
23 PGND

## Terminal Functions

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | BCK | I | Bit clock input for audio data |
| 3 | DATA | I | Audio data input |
| 4 | LRCK | I | Left and right channel audio data latch enable input |
| 7 | LR_SEL | I | Select left-channel or right-channel data<br>HIGH: Left channel active<br>LOW: Right channel active |
| 11 | GAIN0 | I | Gain select least significant bit. TTL logic levels with compliance to 5 V. |
| 12 | GAIN1 | I | Gain select most significant bit. TTL logic levels with compliance to 5 V. |
| 13 | $\overline{\text{SHUTDOWN}}$ | I | Shutdown signal for IC (low = shutdown, high = operational).<br>TTL logic levels with compliance to 18 V. |
| 5, 9, 38, 40 | DGND | - | Digital ground |
| 6, 8 | VDD | - | Digital power supply (4.5 V – 5.5 V) |
| 15 | VCLAMP | - | Internally generated voltage supply for bootstrap capacitor |
| 17 | BSN | I/O | Bootstrap I/O, negative high-side FET |
| 28 | BSP | I/O | Bootstrap I/O, positive high-side FET |
| 2, 16 | NC | - | No internal connection |
| 31 | ROSC | I/O | I/O for current setting resistor for ramp generator |
| 32 | COSC | I/O | I/O for charge/discharging currents onto capacitor for ramp generator creation |
| 33 | BYPASS | O | Midrail analog reference voltage |
| 34 | VREF | O | Analog 5-V regulated output. Not to be used for powering external circuitry. |
| 35 | VCC | - | High-voltage analog power supply (8 V to 18 V). |
| 19, 20 | OUTN | O | Class-D 1/2-H-bridge negative output |
| 39 | ZERO | O | Zero flag output<br>HIGH: No input present<br>LOW: Data present at input<br>This can be used to shutdown the device when no data is present at input. |
| 41 | DEMP | I | De-emphasis control.<br>HIGH: 44.1 kHz De-emphasis ON<br>LOW: 44.1 kHz De-emphasis OFF |
| 42 | MUTE | I | Soft mute control<br>HIGH: Mute ON<br>LOW: Mute OFF |
| 43 | FORMAT | I | Audio data format select<br>HIGH: 16-bit right justified<br>LOW: 16- to 24-bit, $I^2S$ format |
| 44 | SCLK | I | System clock input |
| 18, 27 | PVCC | - | Power supply for H-bridge (8 V to 18 V) |
| 25, 26 | OUTP | O | Class-D 1/2-H-bridge positive output |
| 29, 30 | AGND | - | Analog ground |
| 14, 21, 22, 23, 24 | PGND | - | Power ground for H-bridge |
| 10 | VCOM | - | Midrail digital reference voltage |
| 36 | FLT2 | I/O | Noise-filter terminals. Connect capacitor across pins 36 and 37 |
| 37 | FLT1 | I/O | |
| | Thermal Pad | | Connect to AGND and PGND - should be the center point for both grounds.<br>Internal esistive connection to AGND. |

## TYPICAL CHARACTERISTICS

**Total Harmonic Distortion Plus Noise vs Output Power**

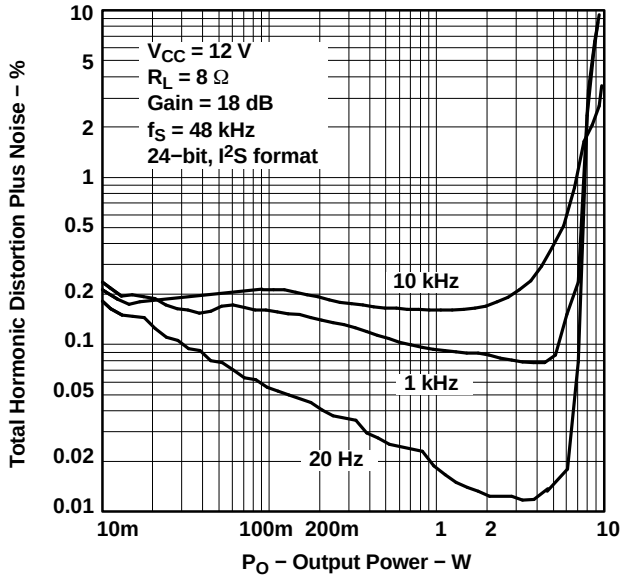



Figure 1.

**Total Harmonic Distortion Plus Noise vs Output Power**

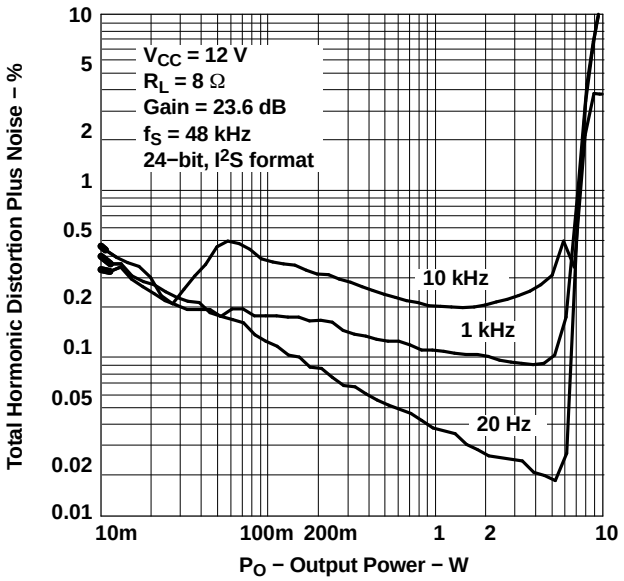



Figure 2.

**Harmonic Distortion Plus Noise vs Output Power**

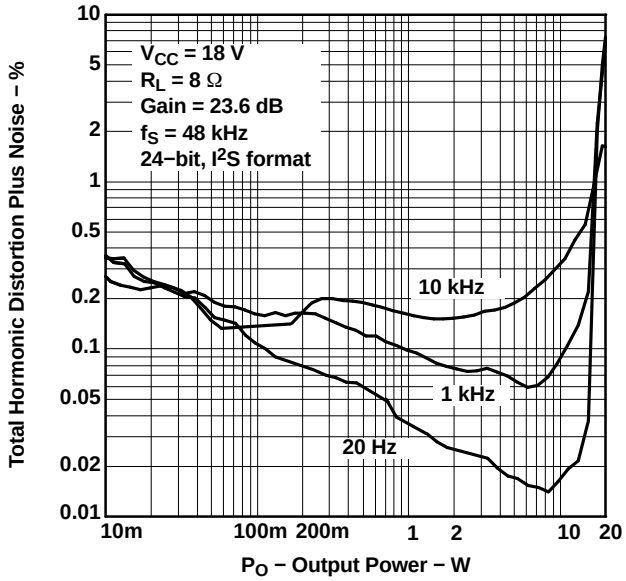



Figure 3.

**Total Harmonic Distortion vs Power**

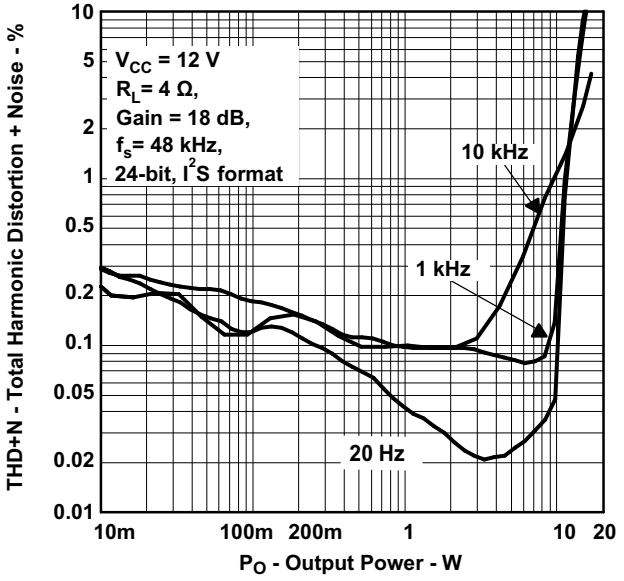



Figure 4.

## TYPICAL CHARACTERISTICS (continued)

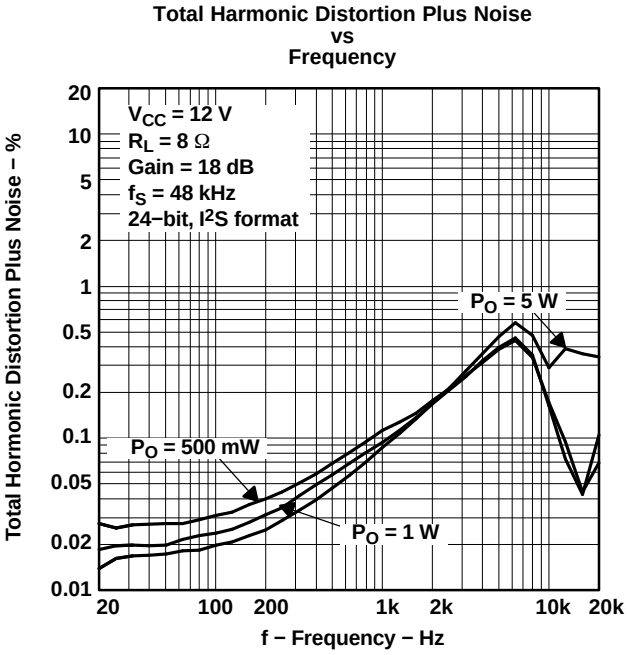



Figure 5.

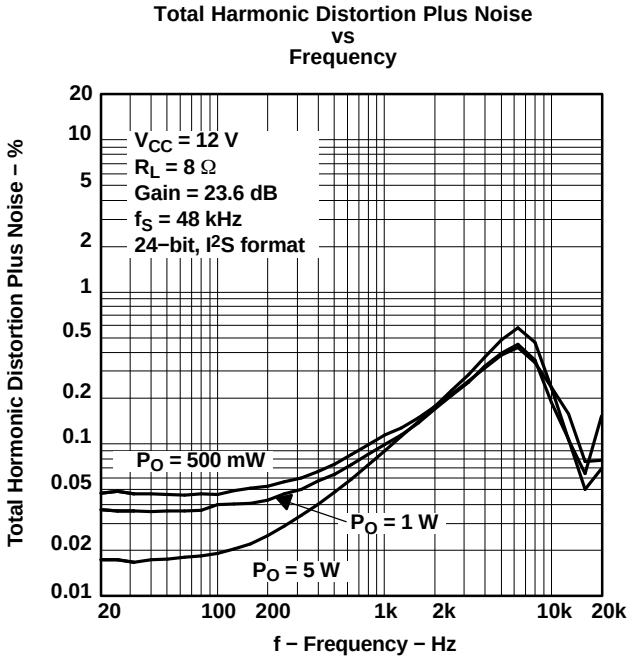



Figure 6.

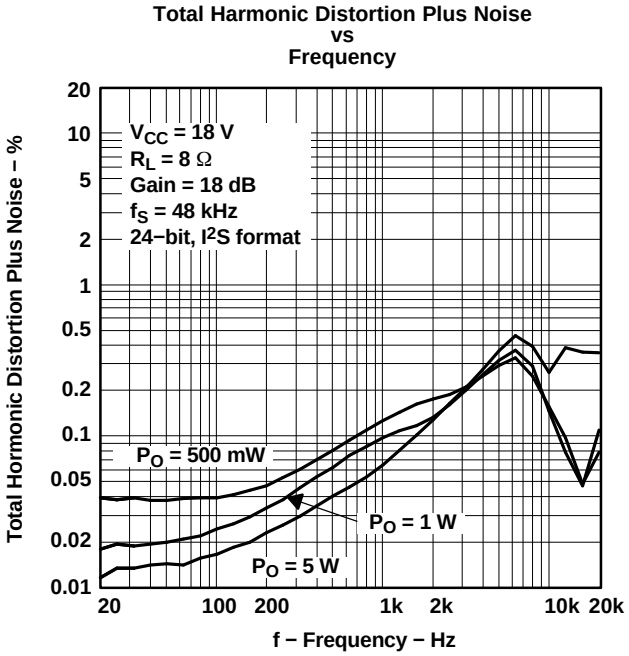



Figure 7.

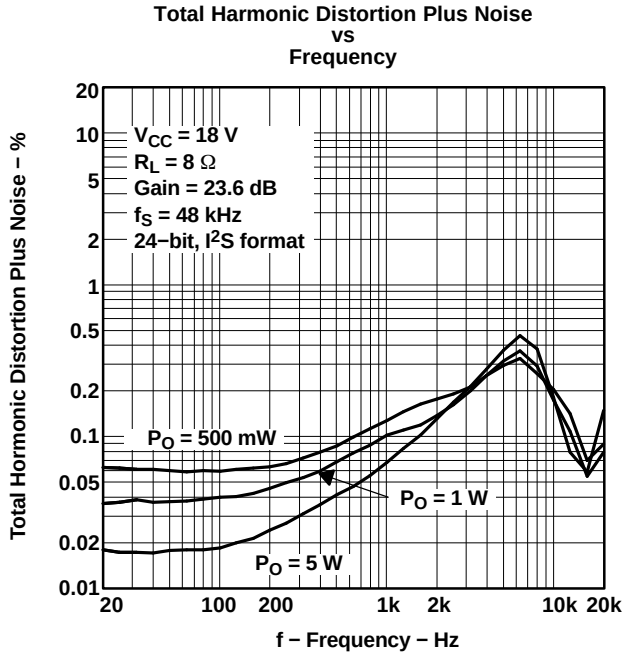



Figure 8.

## TYPICAL CHARACTERISTICS (continued)

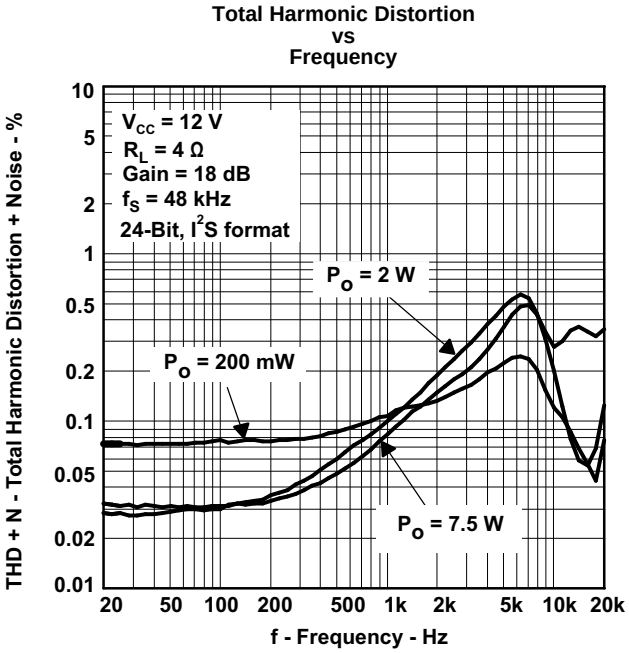



Figure 9.

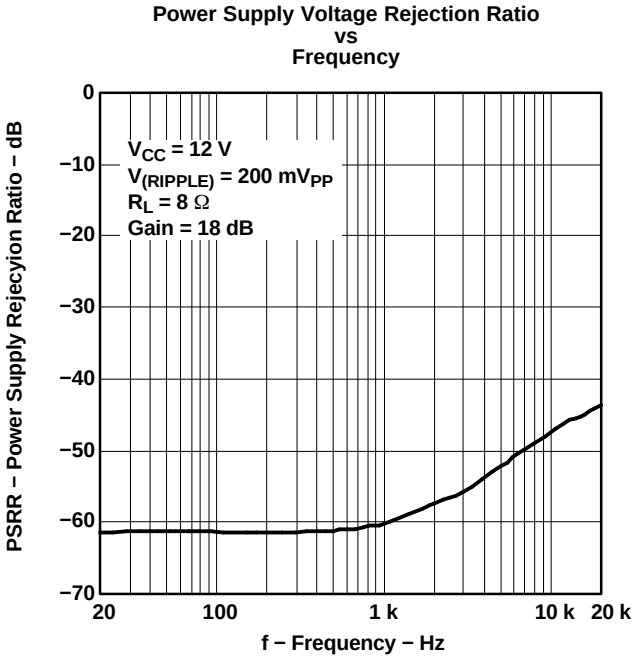



Figure 10.

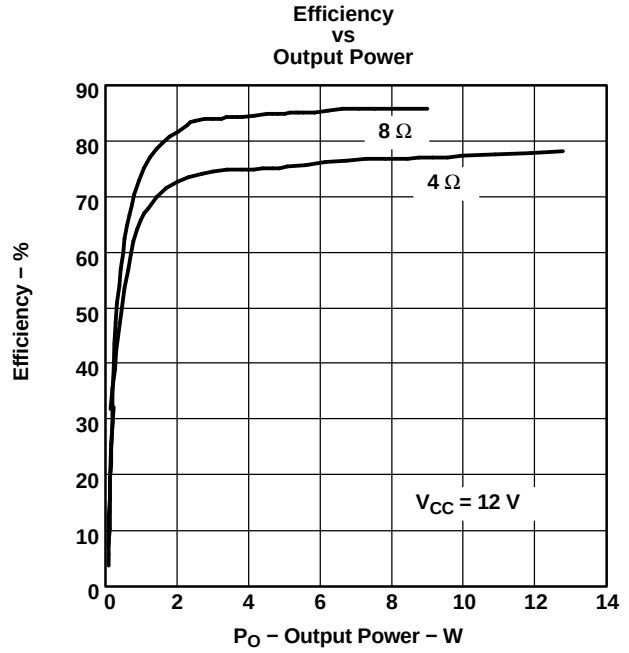



Figure 11.

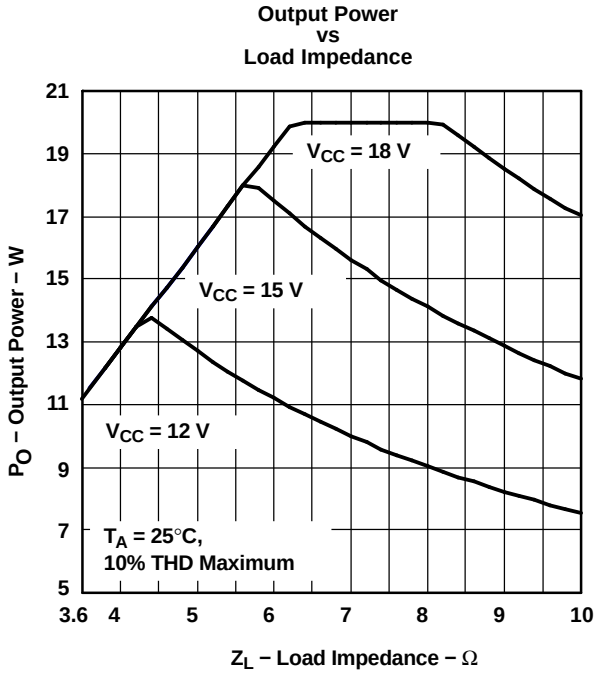



Figure 12.

## TYPICAL CHARACTERISTICS (continued)

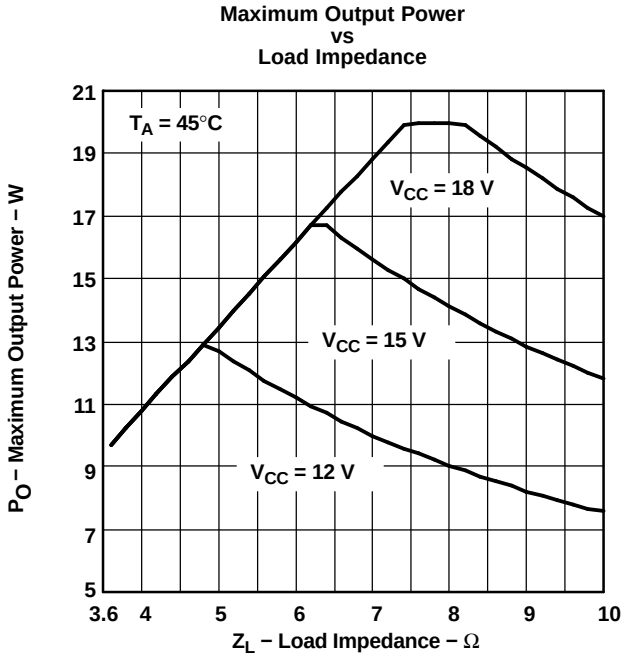



Figure 13.

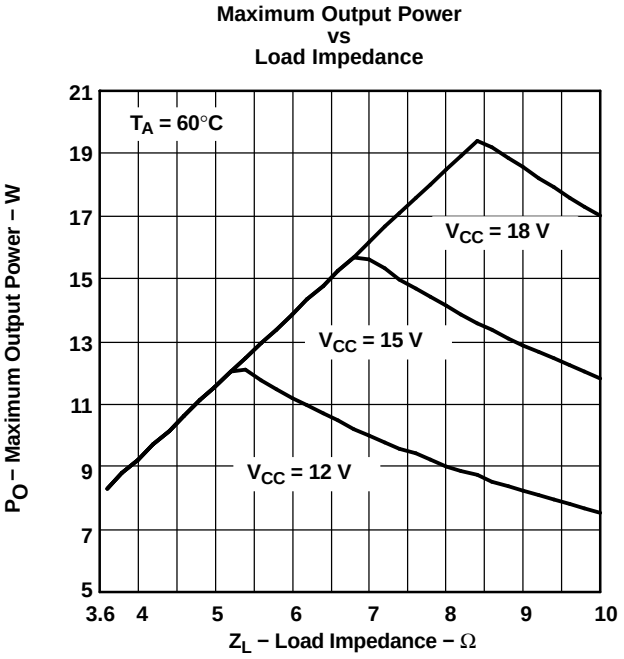



Figure 14.

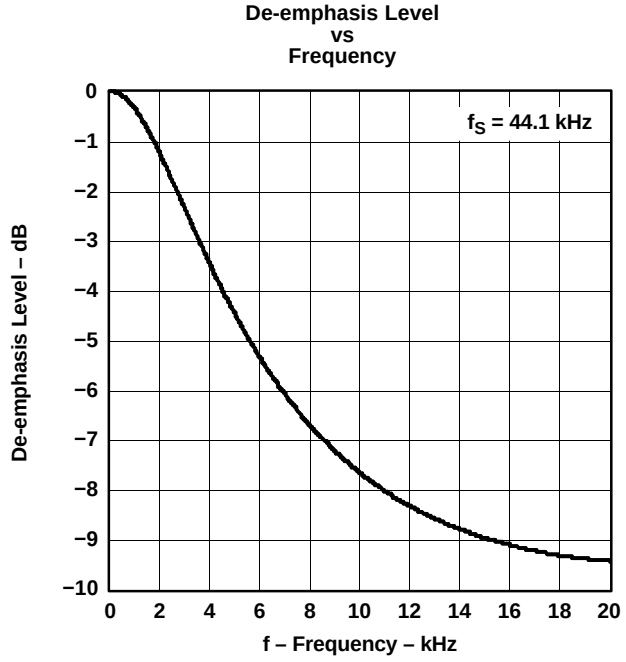



Figure 15.

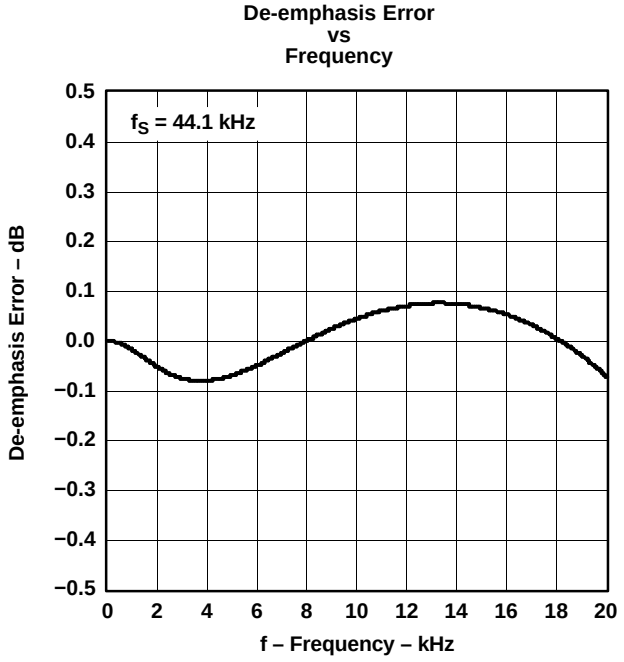



Figure 16.

## APPLICATION INFORMATION

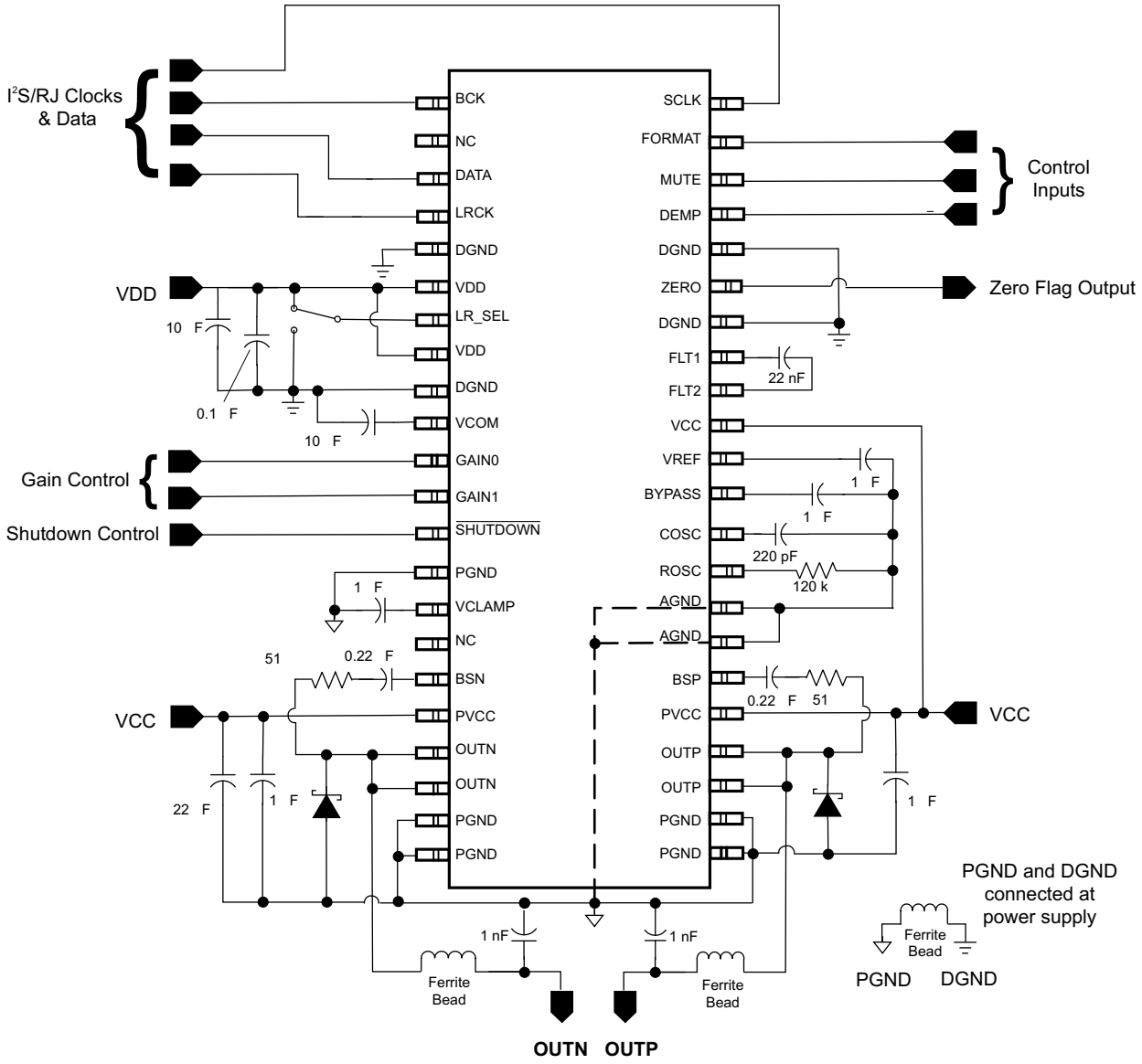



**Figure 17. Typical Application Circuit**

## APPLICATION INFORMATION (continued)

### SYSTEM CLOCK INPUT

The TPA3200D1 requires a system clock for operating the digital interpolation filters and multilevel delta-sigma modulators. The system clock is applied at the SCLK input (pin 44). Table 1 shows examples of system clock frequencies for common audio sampling rates.

Figure 18 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase-jitter and noise. TI's PLL170x family of multiclock generators is an excellent choice for providing the TPA3200D1 system clock.

**Table 1. System Clock Rates for Common Audio Sampling Frequencies**

| SAMPLE FREQUENCY | SYSTEM CLOCK FREQUENCY ($f_{SCLK}$) (MHz) | | | | | | |
|---|---|---|---|---|---|---|---|
| | 128 $f_S$ | 192 $f_S$ | 256 $f_S$ | 384 $f_S$ | 512 $f_S$ | 768 $f_S$ | 1152$f_S$ |
| 8 kHz | 1.0240 | 1.5360 | 2.0480 | 3.0720 | 4.0960 | 6.1440 | 9.2160 |
| 16 kHz | 2.0480 | 3.0720 | 4.0960 | 6.1440 | 8.1920 | 12.2880 | 18.4320 |
| 32 kHz | 4.0960 | 6.1440 | 8.1920 | 12.2880 | 16.3840 | 24.5760 | 36.8640 |
| 44.1 kHz | 5.6448 | 8.4672 | 11.2896 | 16.9344 | 22.5792 | 33.8688 | (1) |
| 48 kHz | 6.1440 | 9.2160 | 12.2880 | 18.4320 | 24.5760 | 36.8640 | (1) |
| 88.2 kHz | 11.2896 | 16.9344 | 22.5792 | 33.8688 | 45.1584 | (1) | (1) |
| 96 kHz | 12.2880 | 18.4320 | 24.5760 | 36.8640 | 49.1520 | (1) | (1) |
| 192 kHz | 24.5760 | 36.8640 | 49.1520 | See (1) | (1) | (1) | (1) |

(1) This system clock rate is not supported for the given sampling frequency.

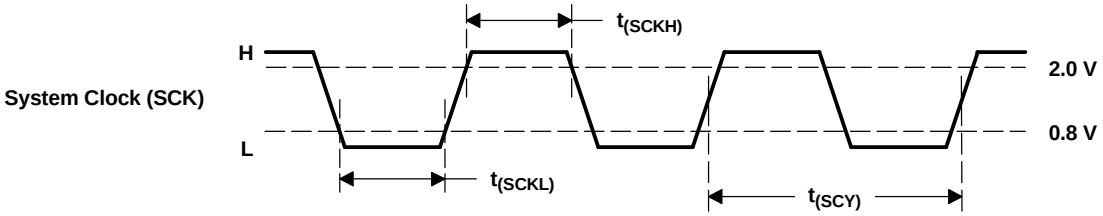



**Figure 18. System Clock Input Timing**

| PARAMETERS | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| System clock pulse duration, high | $t_{(SCKH)}$ | 7 | | | ns |
| System clock pulse duration, low | $t_{(SCKL)}$ | | | | |
| System clock pulse cycle time | $t_{(SCY)}$ | 7 | See (1) | | |

(1) 1/128 $f_S$, 1/256 $f_S$, 1/384 $f_S$, 1/512 $f_S$, 1/768 $f_S$, or 1/1152 $f_S$

### AUDIO SERIAL INTERFACE

The audio serial interface for the TPA3200D1 consists of a 3-wire synchronous serial port. It includes LRCK (pin 4), BCK (pin 1), and DATA (pin 3). BCK is the serial audio bit clock, and it is used to clock the serial data present on DATA into the serial shift register of the audio interface. Serial data is clocked into the TPA3200D1 on the rising edge of BCK. LRCK is the serial audio left/right word clock. It is used to latch serial data into the internal registers of the serial audio interface.

Both LRCK and BCK should be synchronous to the system clock. Ideally, it is recommended that LRCK and BCK be derived from the system clock input, SCK. LRCK is operated at the sampling frequency, $f_S$. BCK can be operated at 32, 48, or 64 times the sampling frequency for standard and left-justified formats. BCK can be operated at 48 or 64 times the sampling frequency for the $I^2S$ format.

Internal operation of the TPA3200D1 is synchronized with LRCK. Accordingly, internal operation is held when the sampling rate clock of LRCK is changed or when SCK and/or BCK is interrupted for a 3-bit clock cycle or longer. If SCK, BCK, and LRCK are provided continuously after this held condition, the internal operation is re-synchronized automatically in a period of less than $3/f_S$. External resetting is not required.

## AUDIO DATA FORMATS AND TIMING

The TPA3200D1 supports $I^2S$ and 16-bit-word right-justified. The data formats are shown in Figure 20. Data formats are selected using the FORMAT pin on the TPA3200D1. All formats require binary 2s-complement, MSB-first audio data. Figure 19 shows a detailed timing diagram for the serial audio interface.

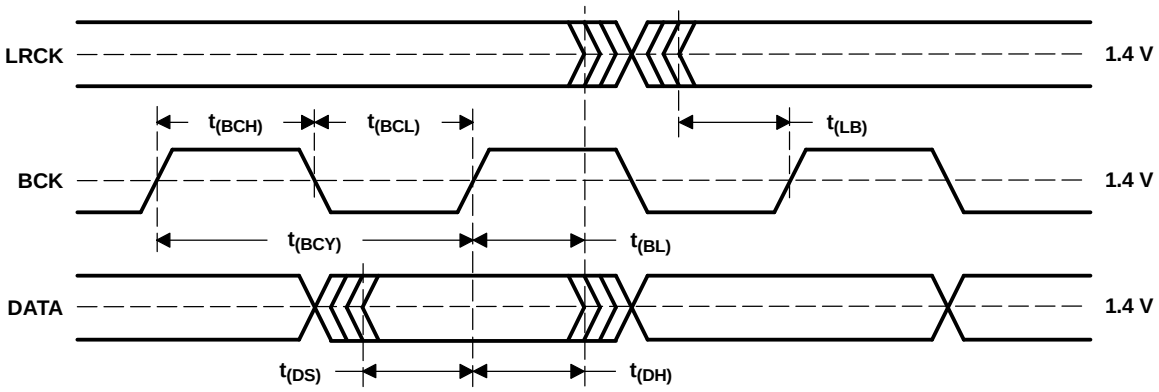
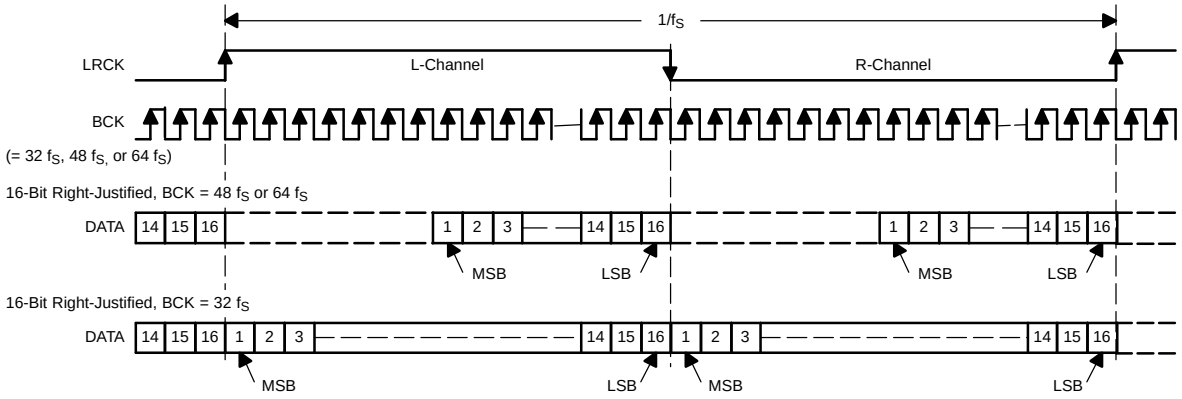



**Figure 19. Audio Interface Timing**

| PARAMETERS | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| BCK pulse cycle time | $t_{(BCY)}$ | $1/(32\ f_S)$, $1/(48\ f_S)$, $1/(64\ f_S)$ (1) | | | ns |
| BCK high-level time | $t_{(BCH)}$ | 35 | | | |
| BCK low-level time | $t_{(BCL)}$ | 35 | | | |
| BCK rising edge to LRCK edge | $t_{(BL)}$ | 10 | | | |
| LRCK falling edge to BCK rising edge | $t_{(LB)}$ | 10 | | | |
| DATA setup time | $t_{(DS)}$ | 10 | | | |
| DATA hold time | $t_{(DH)}$ | 10 | | | |

(1) $f_S$ is the sampling frequency (e.g., 44.1 kHz, 48 kHz, 96 kHz, etc.).

**(1) 16-Bit-Word Right Justified**




**(2) I²S Data Format; L-Channel = LOW, R-Channel = HIGH**

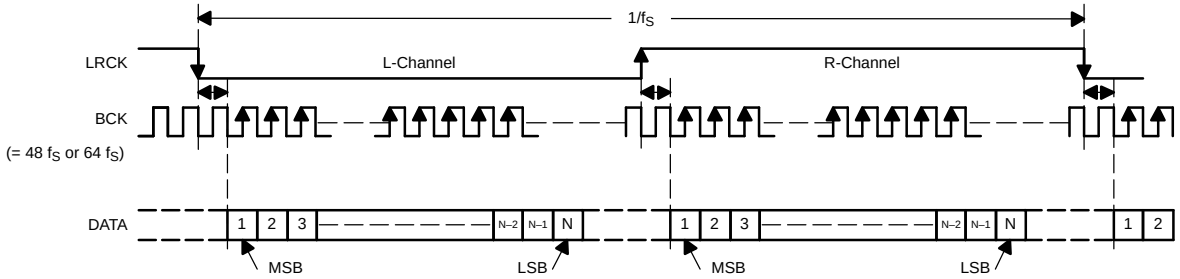



**Figure 20. Audio Data Input Formats**

## ZERO FLAG

ZERO (pin 39) is the L-channel and R-channel common zero flag pin. If the data for L-channel and R-channel remains at a 0 level for 1024 sampling periods (or LRCK clock periods), the ZERO flag output is set to a logic 1 state.

The ZERO-pin output can be inverted using a standard logic gate or transistor, and connected to the $\overline{\text{SHUTDOWN}}$ terminal (pin 13). This places the TPA3200D1 into a low-current state, conserving power, and disables the switching outputs.

## REGISTER CONTROL

The digital functions of the TPA3200D1 are controlled by 4 terminals. Table 2 shows selectable data formats, Table 3 shows de-emphasis control, Table 4 shows mute control, and Table 5 shows channel-output select.

**Table 2. Data Format Select**

| FMT (PIN 43) | DATA FORMAT |
|---|---|
| LOW | 16- to 24-bit, $I^2S$ format |
| HIGH | 16-bit right-justified |

**Table 3. De-Emphasis Control**

| DEMP (PIN 41 ) | DE-EMPHASIS FUNCTION |
|---|---|
| LOW | 44.1 kHz de-emphasis OFF |
| HIGH | 44.1 kHz de-emphasis ON |

**Table 4. Mute Control**

| MUTE (PIN 42 ) | MUTE |
|---|---|
| LOW | Mute OFF |
| HIGH | Mute ON |

**Table 5. Channel Output Select**

| LR_SEL (PIN 7 ) | ACTIVE CHANNEL (1) |
|---|---|
| LOW | Right |
| HIGH | Left |

(1) A digital data stream consists of two channels of data. In an $I^2S$ or right-justified data stream, the left-channel data precedes the right-channel data (See Figure 20). The LR_SEL input selects the channel to send to the mono output.

## OVERSAMPLING RATE CONTROL

The TPA3200D1 automatically controls the oversampling rate of the delta-sigma D/A converters with the system clock rate. The oversampling rate is set to 64× oversampling with every system clock and sampling frequency.

## VCOM OUTPUT

One unbuffered common-mode voltage output pin, VCOM (pin 10) is brought out for decoupling purposes. This pin is nominally biased to a dc voltage level equal to $0.5 \times V_{DD}$. This pin cannot be used to bias external circuits.

## CLASS-D OPERATION

This section focuses on the class-D operation of the TPA3200D1.

### Traditional Class-D Modulation Scheme

The traditional class-D modulation scheme, which is used in the TPA032D0x family, has a differential output where each output is 180 degrees out of phase and changes from ground to the supply voltage, VCC. Therefore, the differential pre-filtered output varies between positive and negative $V_{CC}$, where filtered 50% duty cycle yields 0 V across the load. The traditional class-D modulation scheme with voltage and current waveforms is shown in Figure 31. Note that even at an average of 0 V across the load (50% duty cycle), the current to the load is high, causing high loss, thus causing a high supply current.

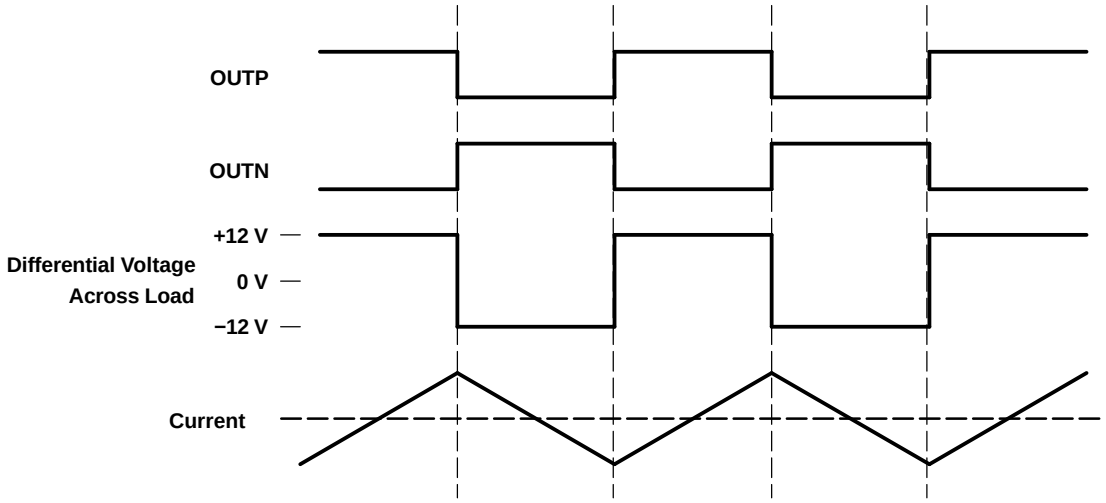



**Figure 21. Traditional Class-D Modulation Scheme's Output Voltage and Current Waveforms Into an Inductive Load With No Input**

### TPA3200D1 Modulation Scheme

The TPA3200D1 uses a modulation scheme that still has each output switching from ground to $V_{CC}$. However, OUTP and OUTN are now in phase with each other with no input. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load is 0 V throughout most of the switching period, greatly reducing the switching current, which reduces any $I^2R$ losses in the load. (See Figure 22.)

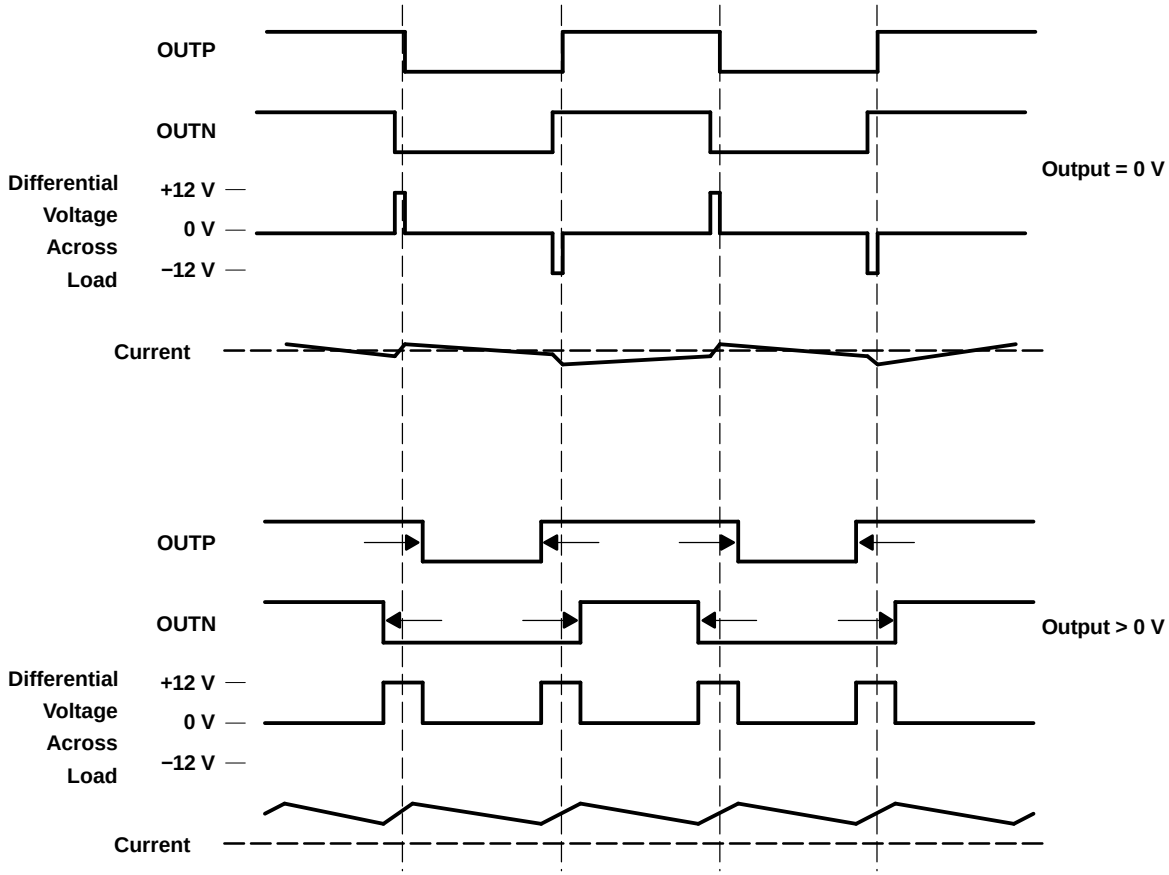



**Figure 22. The TPA3200D1 Output Voltage and Current Waveforms Into an Inductive Load**

### Maximum Allowable Output Power (Safe Operating Area)

The TPA3200D1 can drive load impedances as low as 3.6 Ω from power supply voltages ranging from 8 V to 18 V. To prevent device failure, however, the output power of the TPA3200D1 must be limited. Figure 23 shows the maximum allowable output power versus load impedance for three power supply voltages at an ambient temperature of 25°C.

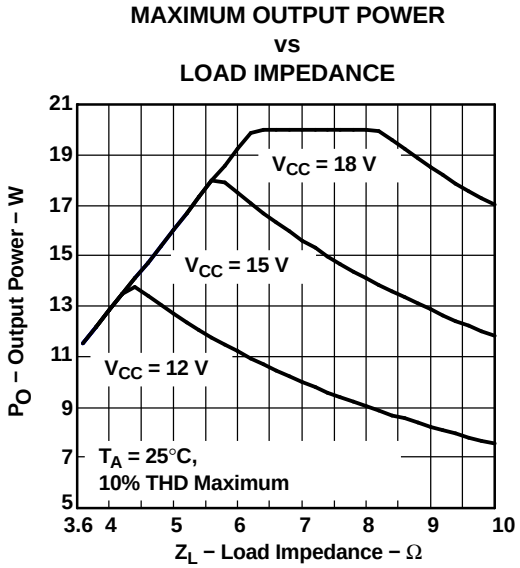



**Figure 23. Output Power**

### Driving The Output Into Clipping

The output of the TPA3200D1 may be driven into clipping to attain a higher output power than is possible with no distortion. Clipping is typically quantified by a THD measurement of 10%. The amount of additional power into the load may be calculated with Equation 1.

$$P_{O(10\%\ THD)} = P_{O(1\%\ THD)} \times 1.25 \quad (1)$$

For example, consider an application in which the TPA3200D1 drives an 8-Ω speaker from an 18-V power supply. The maximum output power with no distortion (less than 1% THD) is 16 W, which corresponds to a maximum peak output voltage of 16 V. For the same output voltage level driven into clipping (10% THD), the output power is increased to 20 W.

### Output Filter Considerations

A ferrite bead filter (shown in Figure 24) should be used in order to pass FCC and/or CE radiated emissions specifications and if a frequency sensitive circuit operating higher than 1 MHz is nearby. The ferrite filter reduces EMI around 1 MHz and higher (FCC and CE only test radiated emissions greater than 30 MHz). When selecting a ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies.

Use an additional LC output filter if there are low frequency (<1 MHz) EMI sensitive circuits and/or there are long wires (greater than 11 inches) from the amplifier to the speaker, as shown in Figure 25 and Figure 26.

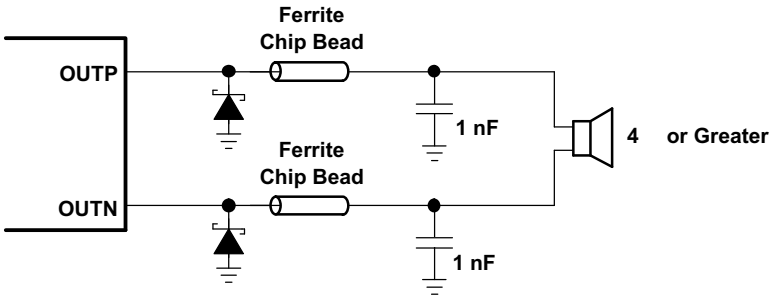



**Figure 24. Typical Ferrite Chip Bead Filter (Chip bead example: Fair-Rite 2512067007Y3)**

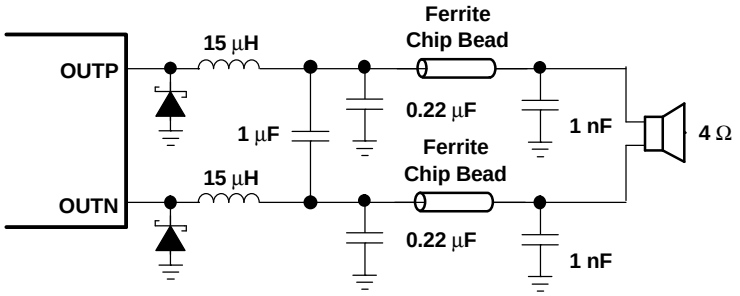



**Figure 25. Typical LC Output Filter for 4-Ω Speaker, Cutoff Frequency of 41 kHz**

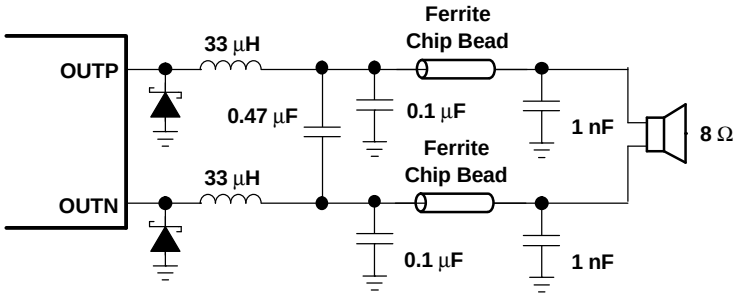



**Figure 26. Typical LC Output Filter for 8-Ω Speaker, Cutoff Frequency of 41 kHz**

## SHORT-CIRCUIT PROTECTION

The TPA3200D1 has short circuit protection circuitry on the outputs that prevents damage to the device during output-to-output shorts, output-to-GND shorts, and output-to-$V_{CC}$ shorts. When a short-circuit is detected on the outputs, the part immediately disables the output drive and enters into shutdown mode. This is a latched fault and must be reset by cycling the voltage on the $\overline{\text{SHUTDOWN}}$ pin to a logic low and back to the logic high state for normal operation. This will clear the short-circuit flag and allow for normal operation if the short was removed. If the short was not removed, the protection circuitry will again activate.

Two Schottky diodes are required to provide short-circuit protection. The diodes should be placed as close to the TPA3200D1 as possible, with the anodes connected to PGND and the cathodes connected to OUTP and OUTN as shown in the application circuit schematic. The diodes should have a forward voltage rating of 0.5 V at a minimum of 1 A output current and a dc blocking voltage rating of at least 30 V. The diodes must also be rated to operate at a junction temperature of 150°C.

If short-circuit protection is not required, the Schottky diodes may be omitted.

## THERMAL PROTECTION

Thermal protection on the TPA3200D1 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 15°C. The device begins normal operation at this point with no external system interaction.

## THERMAL CONSIDERATIONS: OUTPUT POWER AND MAXIMUM AMBIENT TEMPERATURE

To calculate the maximum ambient temperature, Equation 2 is used:

$$T_{Amax} = T_{Jmax} - \theta_{JA} P_{Dissipated}$$

$$\text{where : } T_{Jmax} = 150^{\circ}C$$

$$\theta_{JA} = \frac{1}{\text{derating factor}} = \frac{1}{0.0391} = 25.6^{\circ}C \quad (2)$$

The derating factor for the 44-pin DCP package is given in the dissipation rating table.

To estimate the power dissipation, Equation 3 is used:

$$P_{Dissipated} = P_{O(average)} \times \left(\frac{1}{\text{Efficiency}} - 1\right)$$

$$\text{Efficiency} = \sim 75\% \text{ for an } 4\text{-}\Omega \text{ load}$$

$$\text{Efficiency} = \sim 85\% \text{ for an } 8\text{-}\Omega \text{ load} \quad (3)$$

Example. What is the maximum ambient temperature for an application that requires the TPA3200D1 to drive 20 W into an 8-Ω speaker?

$$P_{Dissipated} = 20 \text{ W} \times \left(\frac{1}{0.85} - 1\right) = 3.53 \text{ W}$$

$$T_{Amax} = 150^{\circ}C - (25.6^{\circ}C/W \times 1.76 \text{ W}) = 59.6^{\circ}C \quad (4)$$

This calculation shows that the TPA3200D1 can drive 20 W of RMS power into an 8-Ω speaker up to a maximum ambient temperature rating of 60°C.

## GAIN SETTING VIA GAIN0 AND GAIN1 INPUTS

The gain of the TPA3200D1 is set by two input terminals, GAIN0 and GAIN1. See Table 6.

**Table 6. Gain Settings**

| GAIN1 | GAIN0 | AMPLIFIER GAIN (dB) | Output Voltage with Full Scale Input and $V_{DD}$=5 V ($V_{RMS}$) |
|---|---|---|---|
| | | TYP | TYP |
| 0 | 0 | 12 | 5.63 |
| 0 | 1 | 18 | 11.23 |
| 1 | 0 | 23.6 | 21.4 (1) |
| 1 | 1 | Reserved | Reserved |

(1) Output clipping with $V_{CC}$ = 18 V

The typical output voltage, measured across the load, is also given in Table 6 at each of the gain steps. This is the expected voltage with a full scale input signal applied at the digital inputs and $V_{DD}$ = 5 V. This voltage scales proportionally with a lower or higher $V_{DD}$. For example, if $V_{DD}$ = 4.5 V, scale the results in Table 6 by 4.5/5, or 0.9.

The differential offset voltage, measured across the speaker outputs, increases as the gain is increased. For the lowest offset voltage, specified in the electrical characteristics table, set the gain at the lowest step, 12 dB.

## POWER SUPPLY DECOUPLING

The TPA3200D1 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 µF placed as close as possible to the device $V_{CC}$ lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

## BSN AND BSP CAPACITORS

The full H-bridge output stage uses only NMOS transistors. It therefore requires bootstrap capacitors for the high side of each output to turn on correctly. A 0.22-µF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 0.22-µF capacitor must be connected from OUTP to BSP, and one 0.22-µF capacitor must be connected from OUTN to BSN.

## BSN AND BSP RESISTORS

To limit the current when charging the bootstrap capacitors, a resistor with a value of approximately 50 Ω (+/–10% maximum) must be placed in series with each bootstrap capacitor. The current will be limited to less than 500 µA.

## VCLAMP CAPACITOR

To ensure that the maximum gate-to-source voltage for the NMOS output transistors is not exceeded, an internal regulator clamps the gate voltage. A 1-µF capacitor must be connected from VCLAMP (pin 15) to ground. This capacitor must have a rating of $V_{CC}$ or more. The voltage at VCLAMP (pin 15) varies with $V_{CC}$ and may not be used for powering any other circuitry.

## MIDRAIL BYPASS CAPACITOR

The midrail bypass capacitor is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, $C_{(BYPASS)}$ determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

## VREF DECOUPLING CAPACITOR

The VREF terminal (pin 34) is the output of an internally-generated 5-V supply, used for the oscillator and gain setting logic. It requires a 0.1-µF to 1-µF capacitor to ground to keep the regulator stable. The regulator may not be used to power any additional circuitry.

## SWITCHING FREQUENCY

The switching frequency is determined using the values of the components connected to ROSC (pin 31) and COSC (pin 32) and may be calculated using Equation 5:

$$f_S = \frac{6.6}{R_{OSC} C_{OSC}} \quad (5)$$

The frequency may be varied from 225 kHz to 275 kHz by adjusting the values chosen for ROSC and COSC.

## $\overline{\text{SHUTDOWN}}$ OPERATION

The TPA3200D1 employs a shutdown mode of operation designed to reduce supply current ($I_{CC}$) to the absolute minimum level during periods of non-use for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, $I_{CC(SD)}$ = 1 µA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected, because amplifier operation would be unpredictable.

Ideally, the device should be held in shutdown when the system powers up and brought out of shutdown once any digital circuitry has settled. However, if $\overline{\text{SHUTDOWN}}$ is to be left unused, the terminal may be connected directly to $V_{CC}$.

## USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

A metalized polyester capacitor is recommended for the capacitor placed in parallel across the FLT1 and FLT2 inputs. This ensures the best noise performance.

## PRINTED-CIRCUIT BOARD (PCB) LAYOUT

Because the TPA3200D1 is a class-D amplifier that switches at a high frequency, the layout of the printed-circuit board (PCB) should be optimized according to the following guidelines for the best possible performance.

- Decoupling capacitors — The high-frequency 1-µF decoupling capacitors should be placed as close to the PVCC (pin 18 and pin 27) and VCC (pin 35) terminals as possible. The BYPASS (pin 33) capacitor, VREF (pin 34) capacitor, and VCLAMP (pin 15) capacitor should also be placed as close to the device as possible. The large (10 µF or greater) bulk power supply decoupling capacitor should be placed near the TPA3200D1 at the PVCC terminals.
- Grounding — The VCC (pin 35) decoupling capacitor, VREF (pin 34) capacitor, BYPASS (pin 33) capacitor, COSC (pin 32) capacitor, and ROSC (pin 31) resistor should each be grounded to analog ground (AGND, pin 29 and pin 30). The PVCC (pin 18 and pin 27) decoupling capacitors should each be grounded to power ground (PGND pins 14, 21, 22, 23, and 24). Analog ground and power ground may be connected at the PowerPAD, which should be used as a central ground connection, or star ground, for the TPA3200D1. DGND (pins 5, 9, 38, and 40) should be connected to PGND, and AGND at the power supply through a ferrite bead. Connect the VDD (pins 6 and 8) decoupling capacitor to DGND. This pattern separates the digital power-switching currents and digital input currents, and prevents interference between them.
- Digital input signal routing — The SCLK, BCK, LRCK, and DATA input are sensitive, high-frequency signals that should be shielded by a clean GND layer to avoid interference. For a 2-layer PCB, shield the signals on the bottom layer with a plane connected to DGND. On the top layer, route DGND closely around these signals.
- Output filter — The ferrite filter (Figure 24) should be placed as close to the output terminals (pins 19, 20, 25, and 26) as possible for the best EMI performance. The LC filter (Figure 25 and Figure 26) should be placed closest to the output and followed by a ferrite-bead filter. The capacitors used in both the ferrite and LC filters should be grounded to power ground.
- PowerPAD — The PowerPAD must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the PowerPAD thermal land on the PCB should be 3.5 mm by 9.5 mm. Three rows of solid vias (six vias per row, 0.3302 mm or 13 mils diameter) should be equally spaced underneath the thermal land. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB. The vias must be solid vias, not thermal relief or webbed vias. For additional information, see the *PowerPAD Thermally Enhanced Package* technical brief, TI literature number SLMA002.

For an example layout, see the *TPA3200D1 Evaluation Module (TPA3200D1EVM) User Manual*, TI literature number SLOU173. Both the EVM user manual and the PowerPAD application note are available on the TI web site at http://www.ti.com.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPA3200D1DCP | NRND | HTSSOP | DCP | 44 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TPA3200D1 | |
| TPA3200D1DCPG4 | NRND | HTSSOP | DCP | 44 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TPA3200D1 | |
| TPA3200D1DCPR | NRND | HTSSOP | DCP | 44 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TPA3200D1 | |
| TPA3200D1DCPRG4 | NRND | HTSSOP | DCP | 44 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TPA3200D1 | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

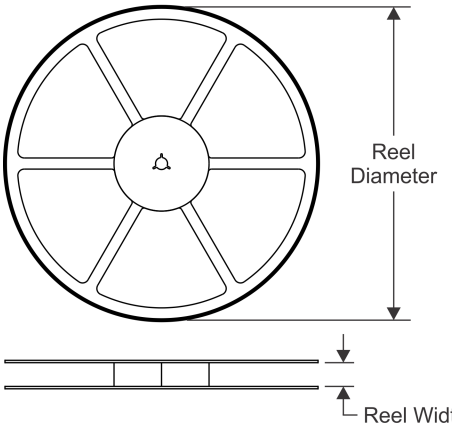
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

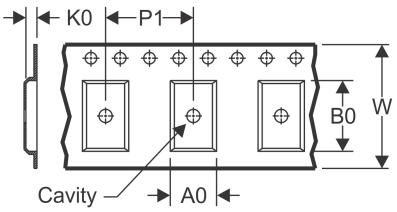
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

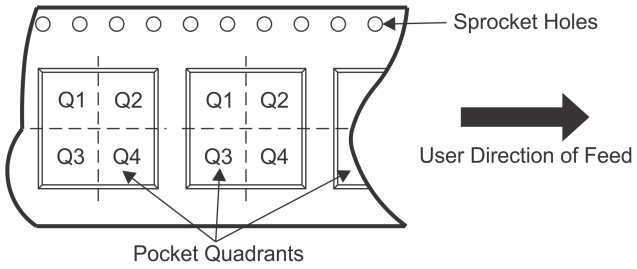



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

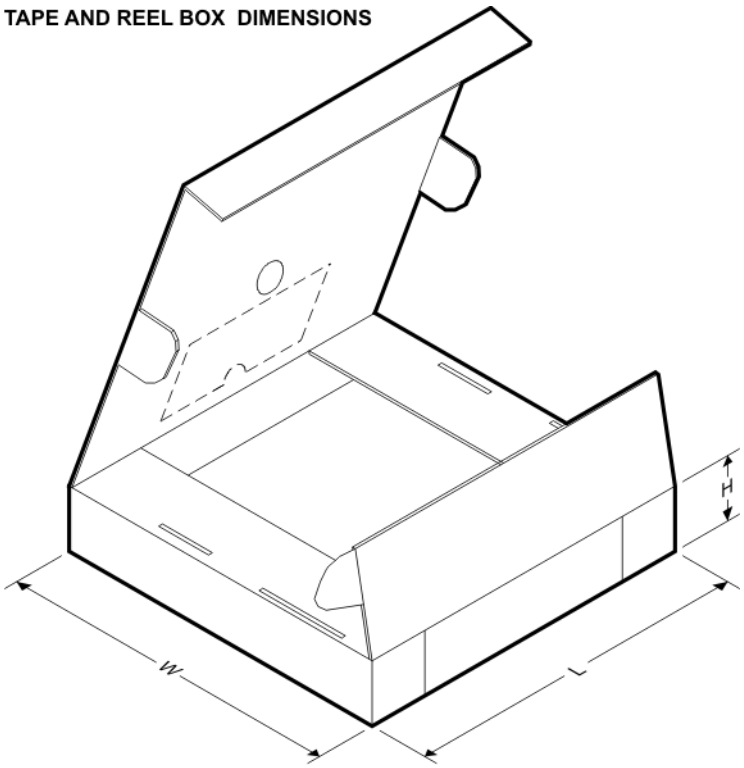
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPA3200D1DCPR | HTSSOP | DCP | 44 | 2000 | 330.0 | 24.4 | 6.8 | 11.7 | 1.6 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

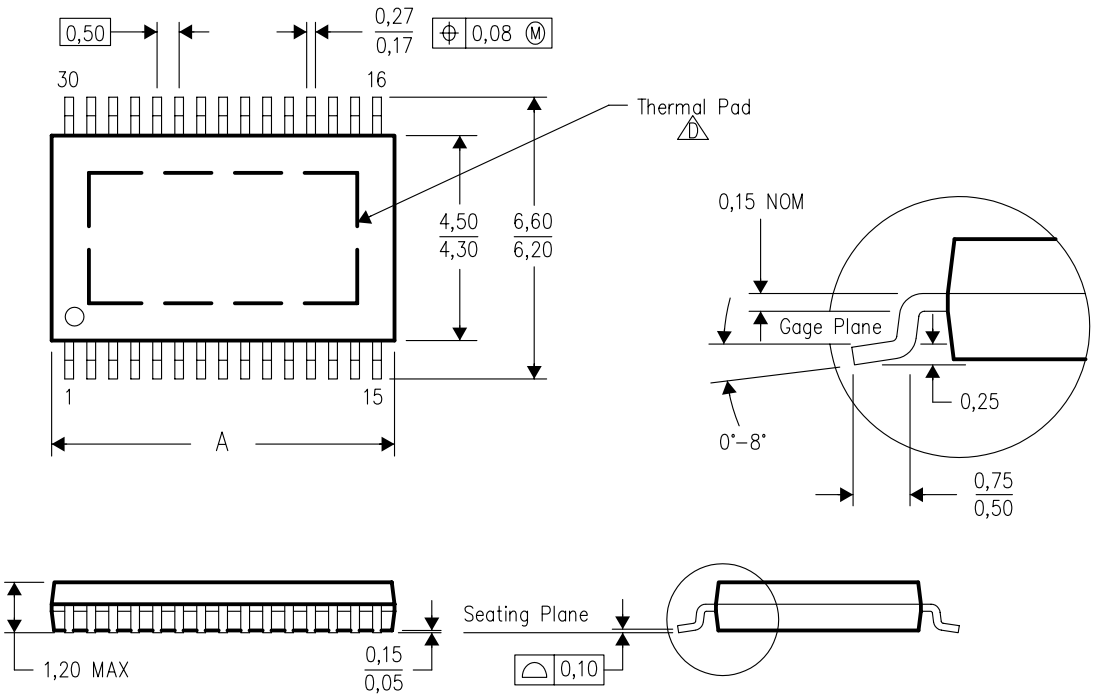



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPA3200D1DCPR | HTSSOP | DCP | 44 | 2000 | 367.0 | 367.0 | 45.0 |

## DCP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

30 PIN SHOWN




| DIM \ PINS ** | 28 | 30 | 38 | 44 | 50 |
|---|---|---|---|---|---|
| A MAX | 7,90 | 7,90 | 9,80 | 11,40 | 12,60 |
| A MIN | 7,70 | 7,70 | 9,60 | 11,20 | 12,40 |

4073267/C 03/05

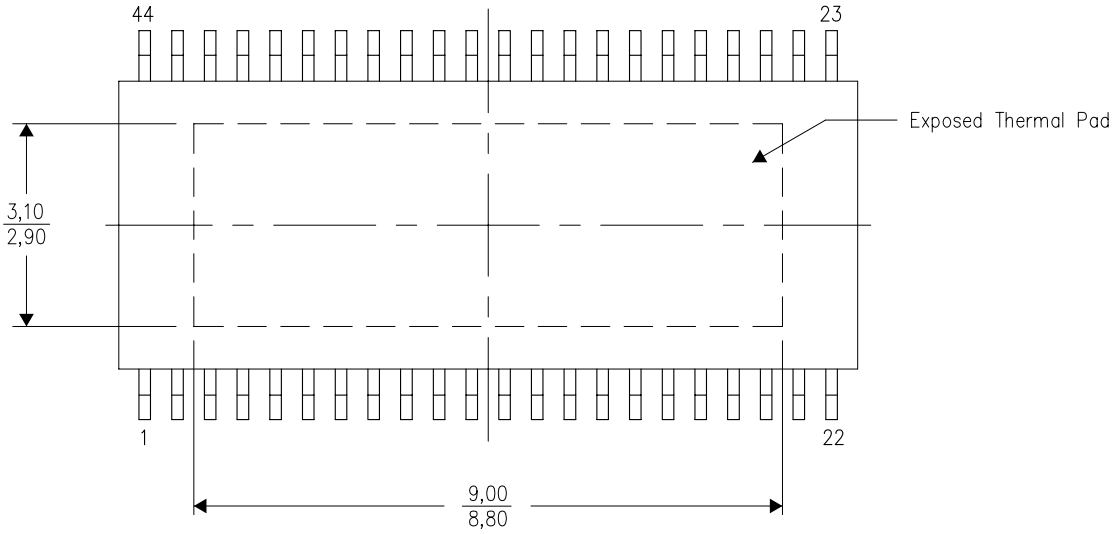
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protusions, mold flash not to exceed 0.15mm.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com. See the product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–153

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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