



1M (64K x 16) Static RAM

Features

- Very high speed: 55 ns
- Voltage range: 1.65V to 1.95V
- Ultra-low active power
 - Typical active current: 0.5 mA @ $f = 1 \text{ MHz}$
 - Typical active current: 2.5 mA @ $f = f_{\text{MAX}}$
- Ultra-low standby power
- Easy memory expansion with $\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$ and $\overline{\text{OE}}$ features
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Packages offered in a 48-ball FBGA and a 44-pin TSOP Type II

Functional Description^[1]

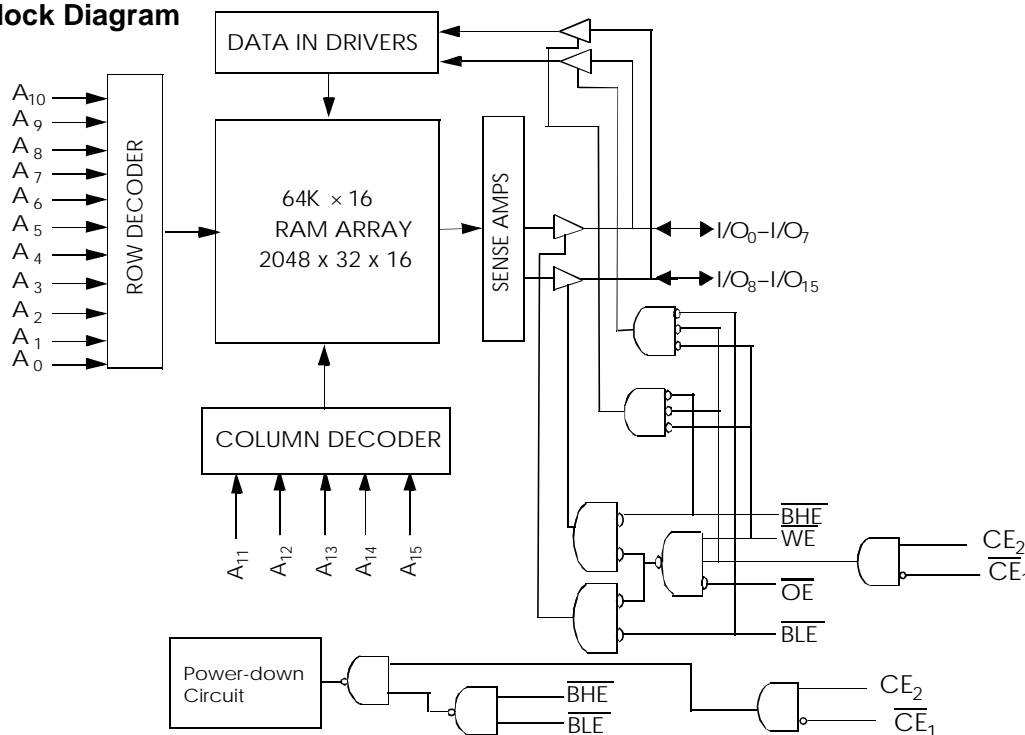
The CY62127DV18 is a high-performance CMOS static RAM organized as 64K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected Chip Enable 1 ($\overline{\text{CE}}_1$) HIGH or Chip Enable 2 ($\overline{\text{CE}}_2$) LOW or both $\overline{\text{BHE}}$ and

$\overline{\text{BLE}}$ are HIGH. The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected Chip Enable 1 ($\overline{\text{CE}}_1$) HIGH or Chip Enable 2 ($\overline{\text{CE}}_2$) LOW, outputs are disabled ($\overline{\text{OE}}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{\text{BHE}}$, $\overline{\text{BLE}}$ HIGH) or during a write operation (Chip Enable 1 ($\overline{\text{CE}}_1$) LOW and Chip Enable 2 ($\overline{\text{CE}}_2$) HIGH and $\overline{\text{WE}}$ LOW).

Writing to the device is accomplished by taking Chip Enable 1 ($\overline{\text{CE}}_1$) LOW and Chip Enable 2 ($\overline{\text{CE}}_2$) HIGH and Write Enable ($\overline{\text{WE}}$) input LOW. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{15}).

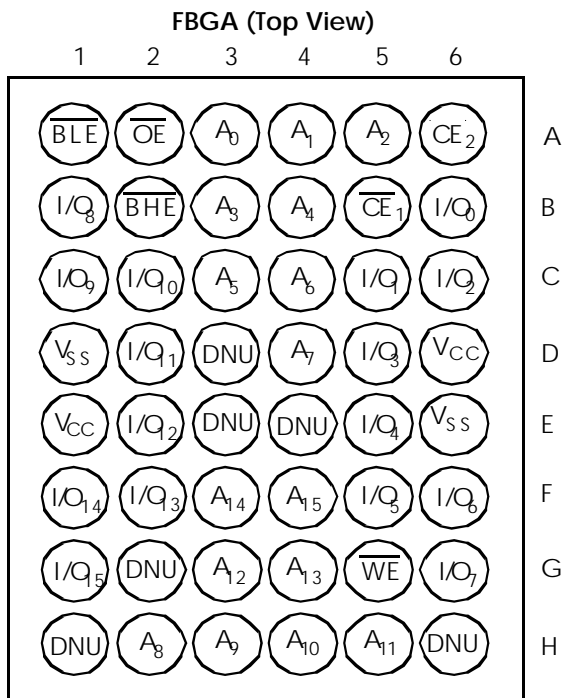
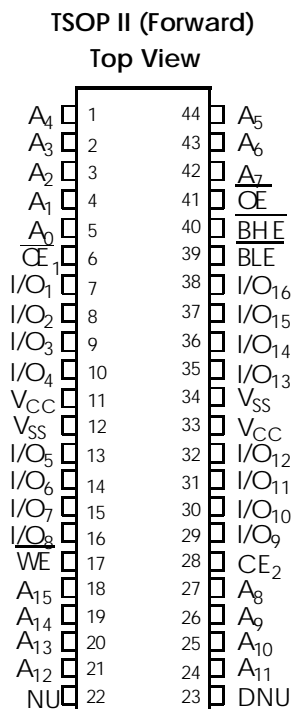
Reading from the device is accomplished by taking Chip Enable 1 ($\overline{\text{CE}}_1$) LOW and Chip Enable 2 ($\overline{\text{CE}}_2$) HIGH and Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable ($\overline{\text{WE}}$) HIGH. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the truth table at the back of this data sheet for a complete description of read and write modes.

Logic Block Diagram



Note:

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Pin Configuration^[2]

Note:

2. DNU pins are to be connected to V_{SS} or left open.



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied..... -55°C to +125°C

Supply Voltage to Ground Potential

..... -0.2V to $V_{CCMAX} + 0.2V$

DC Voltage Applied to Outputs

in High-Z State^[3] -0.2V to $V_{CC} + 0.2V$

DC Input Voltage^[3] -0.2V to $V_{CC} + 0.2V$

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Industrial	-40°C to +85°C	1.65V to 1.95V

Product Portfolio

Product	V _{CC} Range(V)			Speed (ns)	Power Dissipation					
					Operating, I _{CC} (mA)				Standby, I _{SB2} (μA)	
	f = 1 MHz		f = f _{MAX}							
	Min.	Typ. ^[4]	Max.		Typ. ^[4]	Max.	Typ. ^[4]	Max.	Typ. ^[4]	Max.
CY62127DV18L	1.65	1.8	1.95	55	0.5	1	2.5	5	0.5	3
CY62127DV18LL				55			2.5	5	0.5	2

Notes:

3. $V_{IL}(\min.) = -2.0V$ for pulse durations less than 20 ns.

4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC}(\text{typ})$, $T_A = 25^\circ C$.

DC Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions		CY62127DV18-55			Unit
				Min.	Typ. ^[4]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA	V _{CC} = 1.65V	1.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA	V _{CC} = 1.65V			0.2	V
V _{IH}	Input HIGH Voltage			1.4		V _{CC} + 0.2	V
V _{IL}	Input LOW Voltage			-0.2		0.4	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}		-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC}	V _{CC} = 1.95V, I _{OUT} = 0mA, CMOS level		2.5	5	mA
		f = 1 MHz			0.5	1	
I _{SB1}	Automatic CE Power-down Current – CMOS Inputs	CE ₁ ≥ V _{CC} - 0.2V, CE ₂ ≤ 0.2V, V _{IN} ≥ V _{CC} - 0.2V, V _{IN} ≤ 0.2V, f = f _{MAX} (Address and Data Only), f = 0 (OE, WE, BHE and BLE)	L		0.5	3	μA
			LL		0.5	2	
I _{SB2}	Automatic CE Power-down Current – CMOS Inputs	CE ₁ ≥ V _{CC} - 0.2V, CE ₂ ≤ 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0, V _{CC} = 1.95V	L		0.5	3	μA
			LL		0.5	2	

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	TA = 25°C, f = 1 MHz V _{CC} = V _{CC(typ)}	6	pF
C _{OUT}	Output Capacitance		8	pF

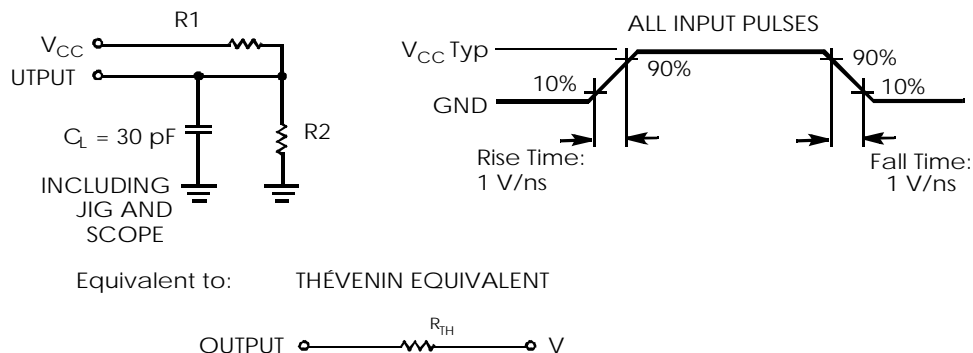
Thermal Resistance

Parameter	Description	Test Conditions	BGA	Unit
θ _{JA}	Thermal Resistance (Junction to Ambient) ^[5]	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	55	C/W
θ _{JC}	Thermal Resistance (Junction to Case) ^[5]		16	C/W

Note:

5. Tested initially and after any design or proces changes that may affect these parameters.

AC Test Loads and Waveforms

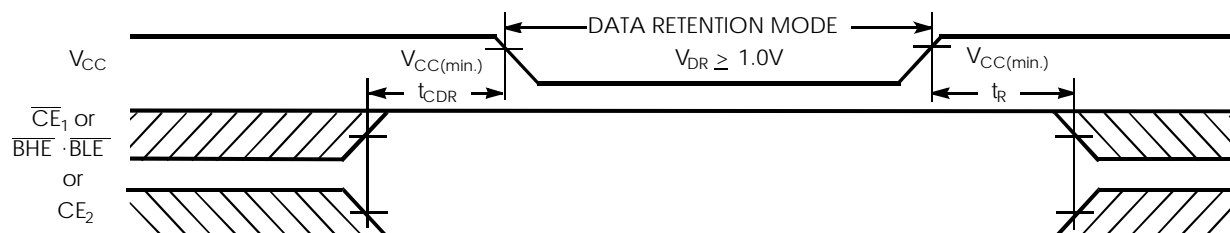


Parameters	1.8V	UNIT
R 1	13500	Ω
R 2	10800	Ω
R_{TH}	6000	Ω
V_{TH}	0.80	V

Data Retention Characteristics

Parameter	Description	Conditions	Min.	Typ. ^[4]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1		1.95	V
I_{CCDR}	Data Retention Current	$V_{CC} = 1V, CE_1 \geq V_{CC} - 0.2V, CE_2 \leq 0.2V, V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	L		1	μA
			LL		TBD	
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[6]}$	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform^[7]



Notes:

6. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} > 100 \mu s$ or stable at $V_{CC(min.)} > 100 \mu s$.

7. $\overline{BHE} \cdot \overline{BLE}$ is the AND of both \overline{BHE} and \overline{BLE} . Chip can be deselected by either disabling the chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .

Switching Characteristics (Over the Operating Range)^[8]

Parameter	Description	CY62127DV18-55		Unit
		Min.	Max.	
Read Cycle				
t _{RC}	Read Cycle Time	55		ns
t _{AA}	Address to Data Valid		55	ns
t _{OHA}	Data Hold from Address Change	10		ns
t _{ACE}	CE ₁ LOW or CE ₂ HIGH to Data Valid		55	ns
t _{DOE}	OE LOW to Data Valid		25	ns
t _{LZOE}	OE LOW to Low-Z ^[9]	5		ns
t _{HZOE}	OE HIGH to High-Z ^[9,11]		20	ns
t _{LZCE}	CE ₁ LOW or CE ₂ HIGH to Low-Z ^[9]	10		ns
t _{HZCE}	CE ₁ HIGH or CE ₂ LOW to High-Z ^[9,11]		20	ns
t _{PU}	CE ₁ LOW or CE ₂ HIGH to Power-up	0		ns
t _{PD}	CE ₁ HIGH or CE ₂ LOW to Power-down		55	ns
t _{DBE}	BLE/BHE LOW to Data Valid		55	ns
t _{LZBE} ^[10]	BLE/BHE LOW to Low-Z ^[9]	5		ns
t _{HZBE}	BLE/BHE HIGH to High-Z ^[9,11]		20	ns
Write Cycle ^[12]				
t _{WC}	Write Cycle Time	55		ns
t _{SCE}	CE ₁ LOW or CE ₂ HIGH to Write End	45		ns
t _{AW}	Address Set-up to Write End	45		ns
t _{HA}	Address Hold from Write End	0		ns
t _{SA}	Address Set-up to Write Start	0		ns
t _{PWE}	WE Pulse Width	40		ns
t _{BW}	BLE/BHE LOW to Write End	45		ns
t _{SD}	Data Set-up to Write End	25		ns
t _{HD}	Data Hold from Write End	0		ns
t _{HZWE}	WE LOW to High-Z ^[9,11]		20	ns
t _{LZWE}	WE HIGH to Low-Z ^[9]	10		ns

Notes:

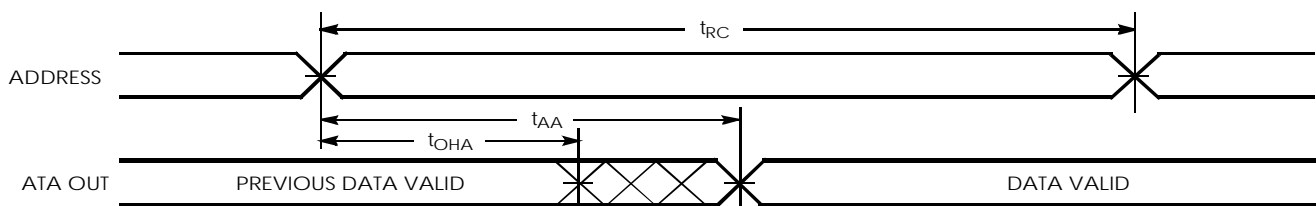
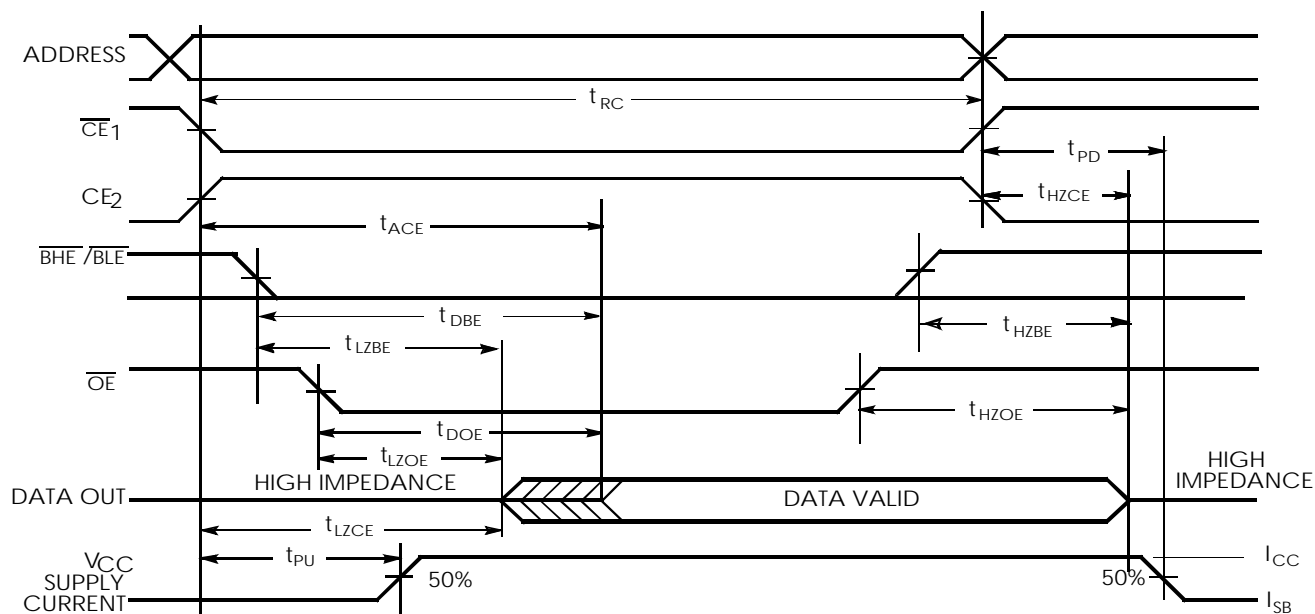
8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.

9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.

10. If both byte enables are toggled together, this value is 10 ns.

11. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.

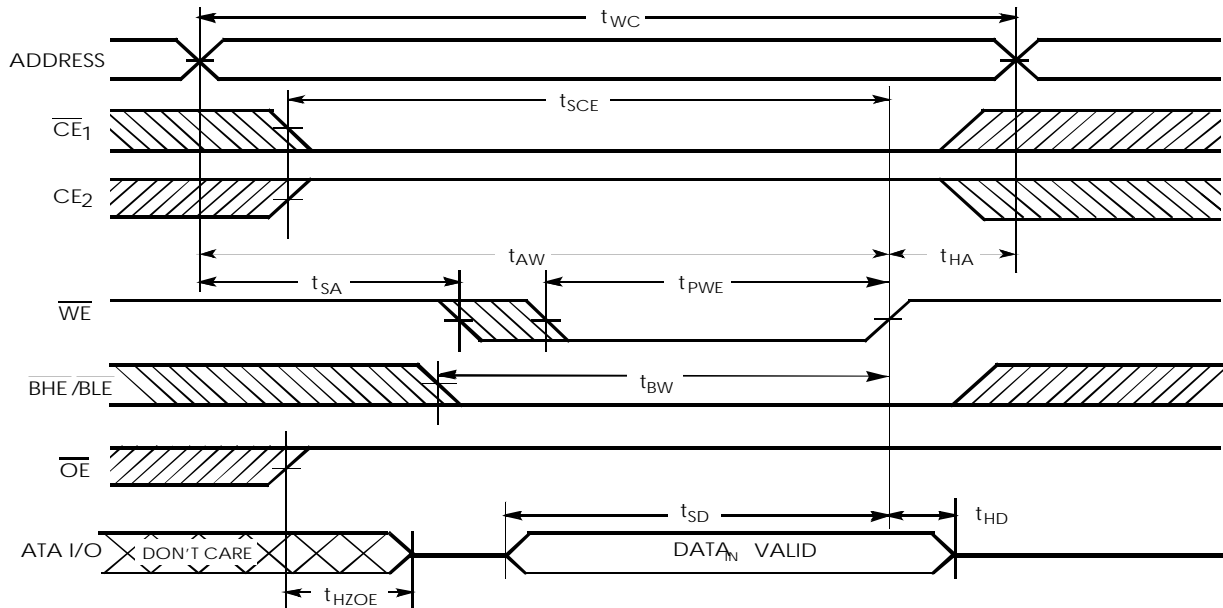
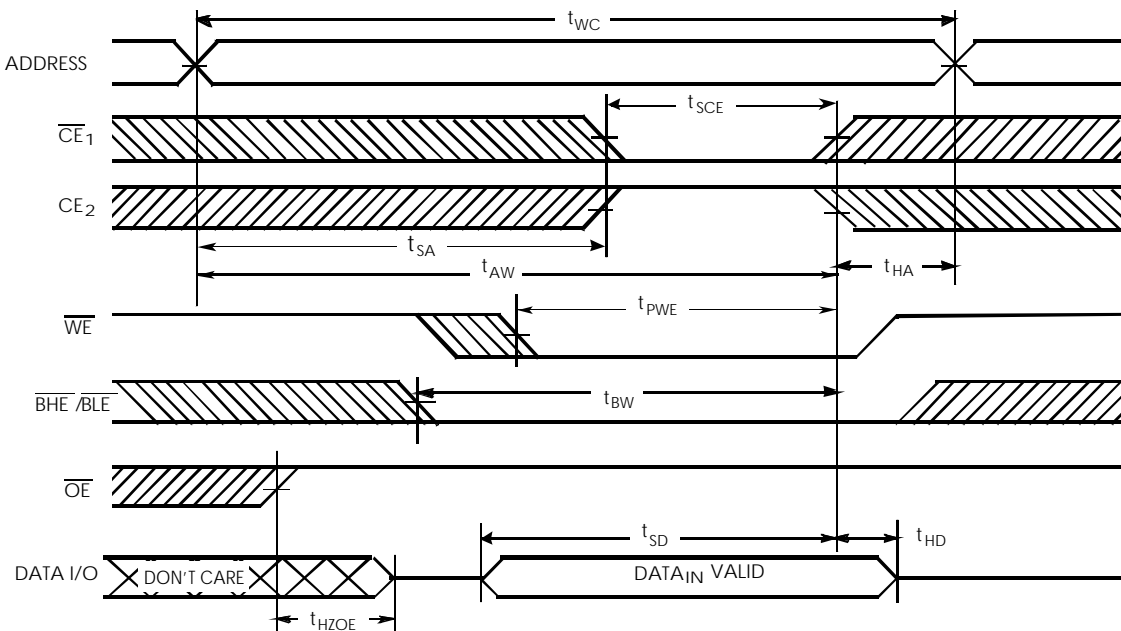
12. The internal Write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$, $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a Write and any of these signals can terminate a Write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the Write.

Switching Waveforms
Read Cycle No. 1 (Address Transition Controlled)^[13, 14]

Read Cycle No. 2 (\overline{OE} Controlled)^[14, 15]

Notes:

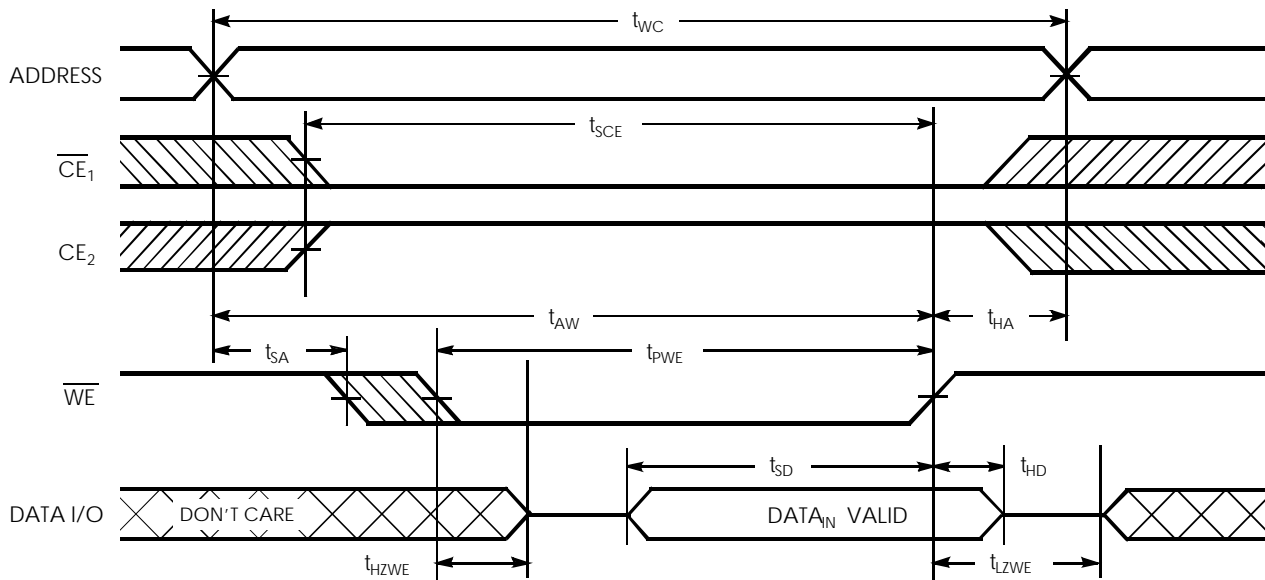
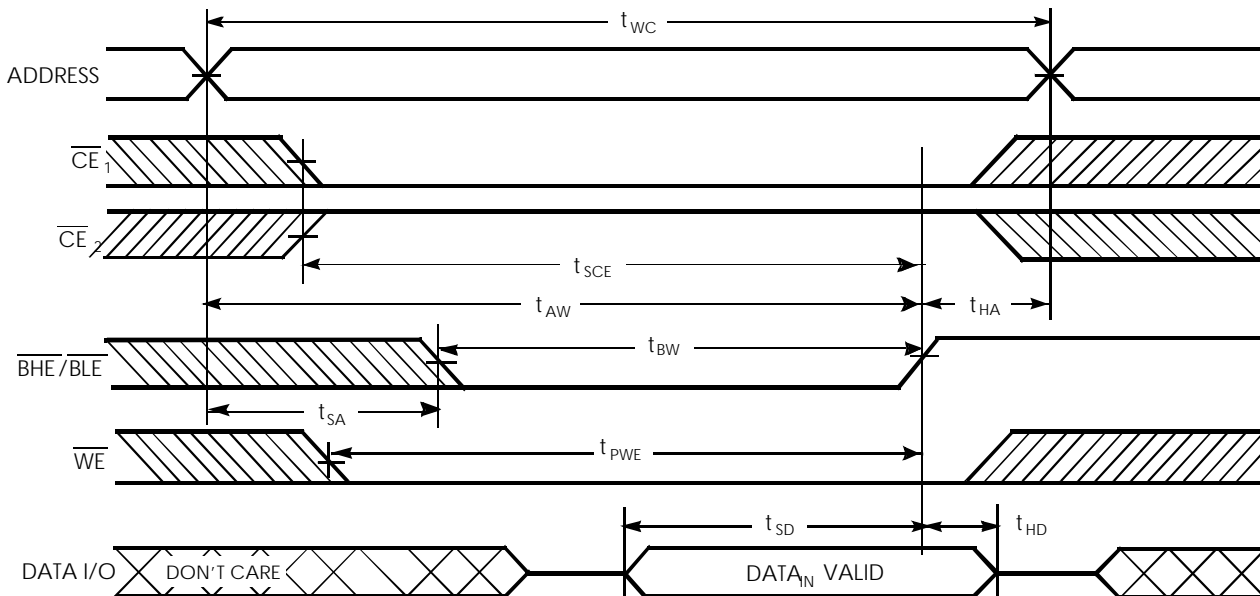
13. Device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$, $CE_2 = V_{IH}$.

14. \overline{WE} is HIGH for Read cycle.

15. Address valid prior to or coincident with \overline{CE}_1 , \overline{BHE} , \overline{BLE} transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)
Write Cycle No. 1 (\overline{WE} Controlled) [12, 16, 17, 18]

Write Cycle No. 2 (\overline{CE}_1 or \overline{CE}_2 Controlled) [12, 16, 17, 18]

Notes:

16. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
17. If \overline{CE}_1 goes HIGH or \overline{CE}_2 goes LOW simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
18. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

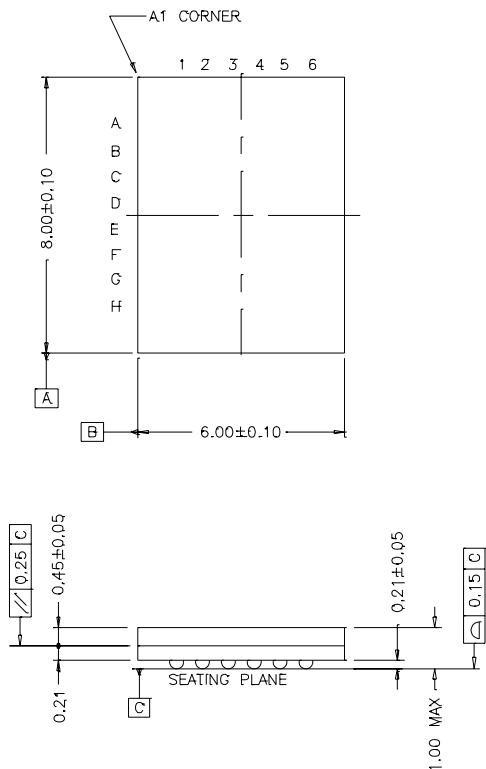
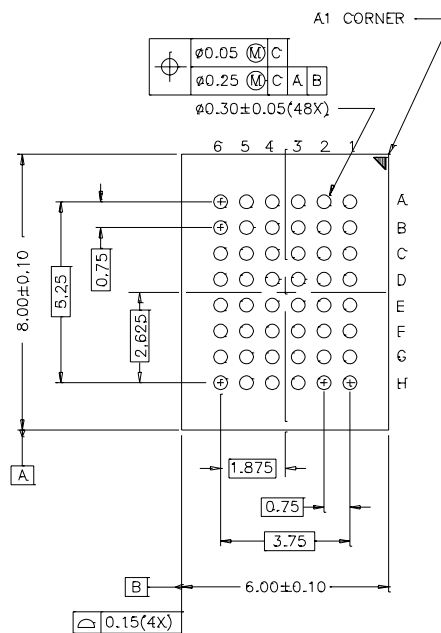
Switching Waveforms (continued)
Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[17, 18]

Write Cycle No. 4 ($\overline{\text{BHE}}/\overline{\text{BLE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[17]


Truth Table

CE ₁	CE ₂	WE	OE	BHE	BLE	Input / Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-down	Standby(I _{SB})
X	L	X	X	X	X	High Z	Deselect/Power-down	Standby(I _{SB})
X	X	X	X	H	H	High Z	Deselect/Power-down	Standby(I _{SB})
L	H	H	L	L	L	Data Out(I/O0- I/O15)	Read	Active(I _{CD})
L	H	H	L	H	L	Data Out(I/O0- I/O7); High Z (I/O8- I/O15)	Read	Active(I _{CD})
L	H	H	L	L	H	High Z (I/O0- I/O7); Data Out(I/O8- I/O15)	Read	Active(I _{CD})
L	H	H	H	L	H	High Z	Output Disabled	Active(I _{CD})
L	H	H	H	H	L	High Z	Output Disabled	Active(I _{CD})
L	H	H	H	L	L	High Z	Output Disabled	Active(I _{CD})
L	H	L	X	L	L	Data In (I/O0- I/O15)	Write	Active(I _{CD})
L	H	L	X	H	L	Data In (I/O0- I/O7); High Z (I/O8- I/O15)	Write	Active(I _{CD})
L	H	L	X	L	H	High Z (I/O0- I/O7); Data In (I/O8- I/O15)	Write	Active(I _{CD})

Ordering Information

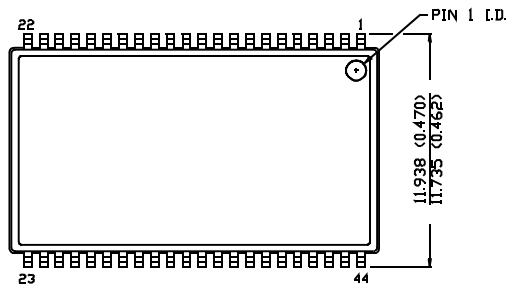
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62127DV18L-55BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	Industrial
	CY62127DV18LL-55BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62127DV18L-55ZI	Z44	44-lead TSOP Type II	
	CY62127DV18LL-55ZI	Z44	44-lead TSOP Type II	

Package Diagrams
48-ball VFBGA (6 x 8 x 1 mm) BV48A
TOP VIEW

BOTTOM VIEW


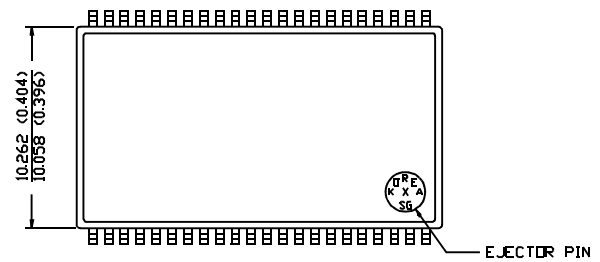
51-85150-*A

44-pin TSOP II Z44

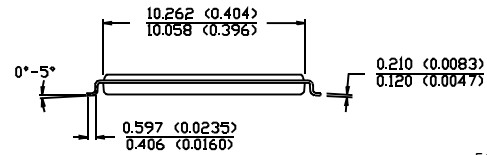
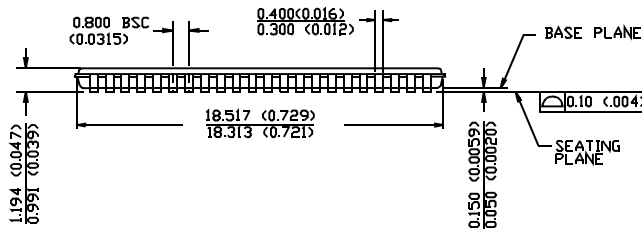
DIMENSION IN MM (INCH)
MAX
MIN.



TOP VIEW



BOTTOM VIEW



51-85087-A

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Document History Page

Document Title: CY62127DV18 MoBL2® 1M (64K x 16) Static RAM Document Number: 38-05226				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	118006	10/01/02	CDY	New Data Sheet