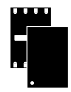
LRI64

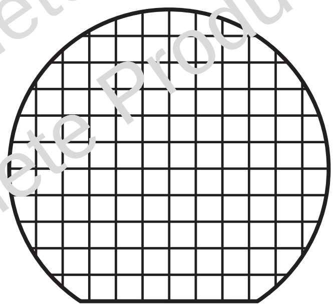
Memory tag IC at 13.56 MHz, with 64-bit unique ID and WORM user area, ISO 15693 and ISO 18000-3 Mode 1 compliant

Features

- ISO 15693 compliant
- ISO 18000-3 Mode 1 compliant
- 13.56 MHz ±7 kHz carrier frequency
- Supported data transfer to the LRI64: 10% ASK modulation using "1-out-of-4" pulse position coding (26 Kbit/s)
- Supported data transfer from the LRI64: Load modulation using Manchester coding with 423 kHz single subcarrier in fast data rate (26 Kbit/s)
- Internal tuning capacitor (21 pF, 28.5 pF, 97 pF)
- 7 × 8 bits WORM user area
- 64-bit unique identifier (UID)
- Read Block and Write Block commands (8-bit blocks)
- 7 ms programming time (typical)
- More than 40-year data retention
- Electrical article surveillance (EAS) capable (software controlled)
- Packages
  - ECOPACK® (RoHS compliant)



UFDFPN8 (MB)
2 × 3 mm² (MLP)



- Unsawn wafer
- Bumped and sawn wafer

Contents

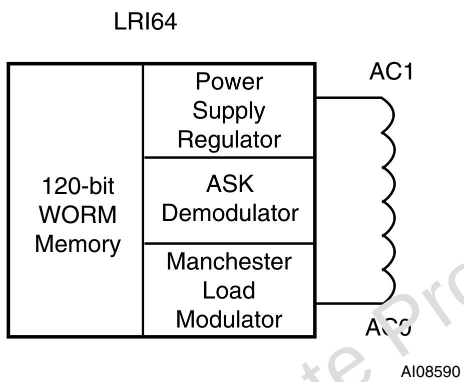
List of tables

List of figures

1 Description

The LRI64 is a contactless memory, powered by an externally transmitted radio wave. It contains a 120-bit non-volatile memory. The memory is organized as 15 blocks of 8 bits, of which 7 blocks are accessible as write-once read-many (WORM) memory.

Figure 1. Logic diagram



The LRI64 is accessed using a 13.56 MHz carrier wave. Incoming data are demodulated from the received amplitude shift keying (ASK) signal, 10% modulated. The data are transferred from the reader to the LRI64 at 26 Kbit/s, using the “1-out-of-4” pulse encoding mode.

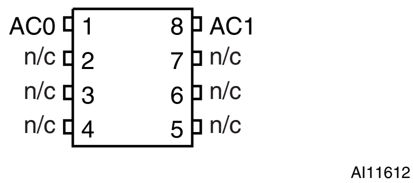
Outgoing data are sent by the LRI64, generated by load variation on the carrier wave, using Manchester coding with a single subcarrier frequency of 423 kHz. The data are transferred from the LRI64 to the reader at 26 Kbit/s, in the high data rate mode.

The LRI64 supports the high data rate communication protocols of ISO 15693 and ISO 18000 3 Mode 1 recommendations. All other data rates and modulations are not supported by the LRI64.

Table 1. Signal names

Signal name	Description
AC1	Antenna coil
AC0	Antenna coil

Figure 2. UFDFPN8 connections

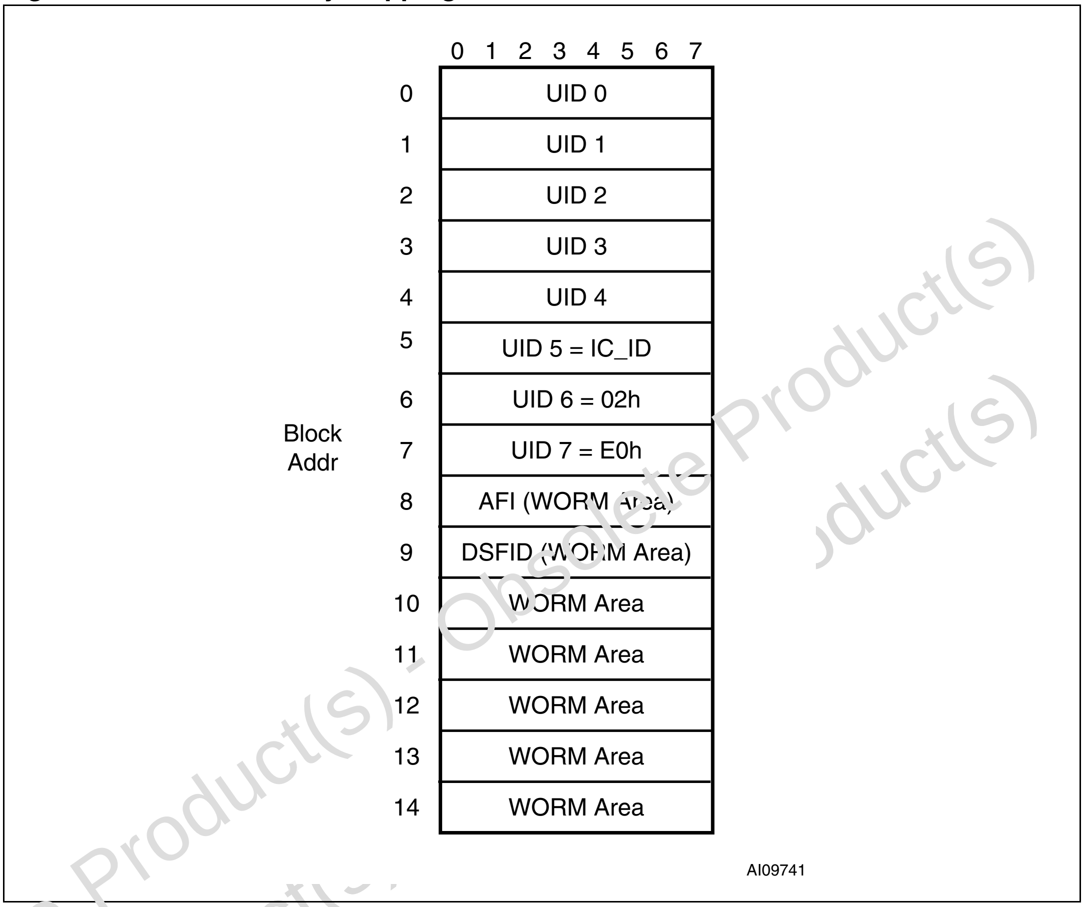


1. n/c means not connected internally.

1.1 Memory mapping

The LRI64 is organized as 15 blocks of 8 bits as shown in *Figure 3*. Each block is automatically write-protected after the first valid write access.

Figure 3. LRI64 memory mapping



The LRI64 uses the first 8 blocks (blocks 0 to 7) to store the 64-bit unique identifier (UID). The UID is used during the anticollision sequence (Inventory). It is written, by ST, at time of manufacture, but part of it can be customer-accessible and customer-writable, on special request.

The LRI64 has an AFI register, in which to store the application family identifier value, which is also used during the anticollision sequence.

The LRI64 has a DSFID register, in which to store the data storage format identifier value, which is used for the LRI64 Inventory answer.

The five following blocks (blocks 10 to 14) are write-once read-many (WORM) memory. It is possible to write to each of them once. After the first valid write access, the block is automatically locked, and only read commands are possible.

2 Signal description

AC1, AC0

The pads for the antenna coil. AC1 and AC0 must be directly bonded to the antenna.

3 Commands

The LRI64 supports the following commands:

3.1 Inventory

Used to perform the anticollision sequence. The LRI64 answers to the Inventory command when all of the 64 bits of the UID have been correctly written.

3.2 Stay Quiet

Used to put the LRI64 in Quiet mode. In this mode, the LRI64 only responds to commands in Addressed mode.

3.3 Read Block

Used to output the 8 bits of the selected block.

3.4 Write Block

Used to write a new 8-bit value in the selected block, provided that the block is not locked. This command can be issued only once to each block.

3.5 Get_System_Info

Used to allow the application system to identify the product. It gives the LRI64 memory size, and IC reference (IC_ID).

3.6 Initial Dialogue for Vicinity Cards

The dialogue between the vicinity coupling device (VCD) and the LRI64 is conducted according to a technique called reader talk first (RTF). This involves the following sequence of operations:

1. activation of the LRI64 by the RF operating field of the VCD
2. transmission of a command by the VCD
3. transmission of a response by the LRI64

4 Power transfer

Power transfer to the LRI64 is accomplished by inductive coupling of the 13.56 MHz radio signal between the antennas of the LRI64 and VCD. The RF field transmitted by the VCD induces an AC voltage on the LRI64 antenna, which is then rectified, smoothed and voltage-regulated. Any amplitude modulation present on the signal is demodulated by the amplitude shift keying (ASK) demodulator.

4.1 Frequency

ISO 15693 and ISO 18000-3 Mode 1 standards define the carrier frequency (f_C) of the operating field to be 13.56 MHz±7kHz.

4.2 Operating field

The LRI64 operates continuously between H_{min} and H_{max}.

- The minimum operating field is H_{min} and has a value of 150mA/m (rms).
- The maximum operating field is H_{max} and has a value of 5A/m (rms).

A VCD generates a field of at least H_{min} and not exceeding H_{max} in the operating volume.

5 Communication signal from VCD to LRI64

Communications between the VCD and the LRI64 involves a type of amplitude modulation called amplitude shift keying (ASK).

The LRI64 only supports the 10% modulation mode specified in ISO 15693 and ISO 18000-3 Mode 1 standards. Any request that the VCD might send using the 100% modulation mode, is ignored, and the LRI64 remains in its current state. However, the LRI64 is, in fact, operational for any degree of modulation index from between 10% and 30%.

The modulation index is defined as (a-b)/(a+b) where a and b are the peak and minimum signal amplitude, respectively, of the carrier frequency, as shown in *Figure 4*.

Table 2. 10% modulation parameters

Parameter	Min	Max
hr	–	0.1 x (a-b)
hf	–	0.1 x (a-b)

Figure 4. 10% modulation waveform

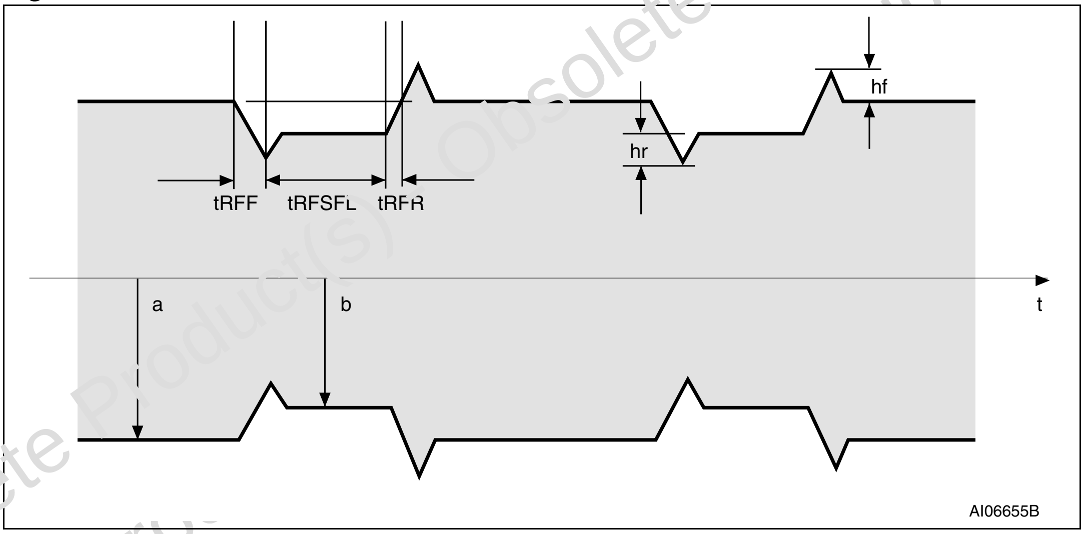
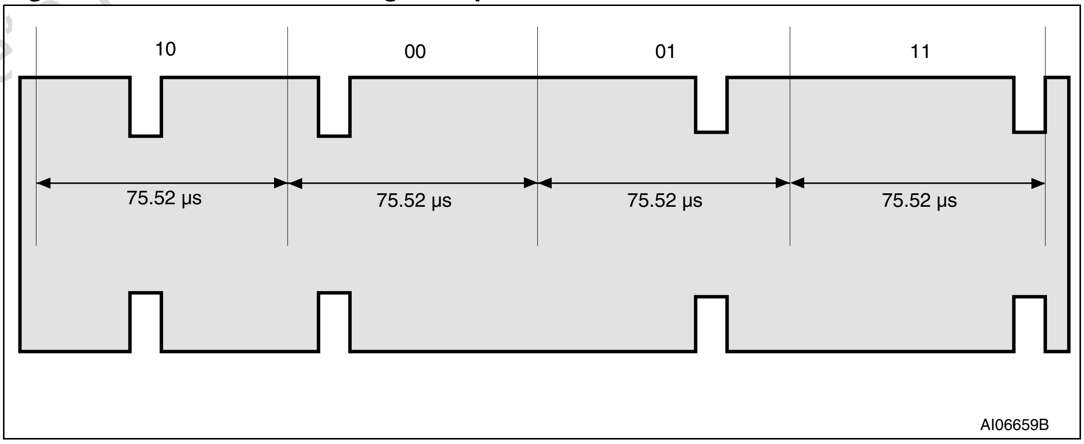


Figure 5. “1-out-of-4” coding example



6 Data rate and data coding

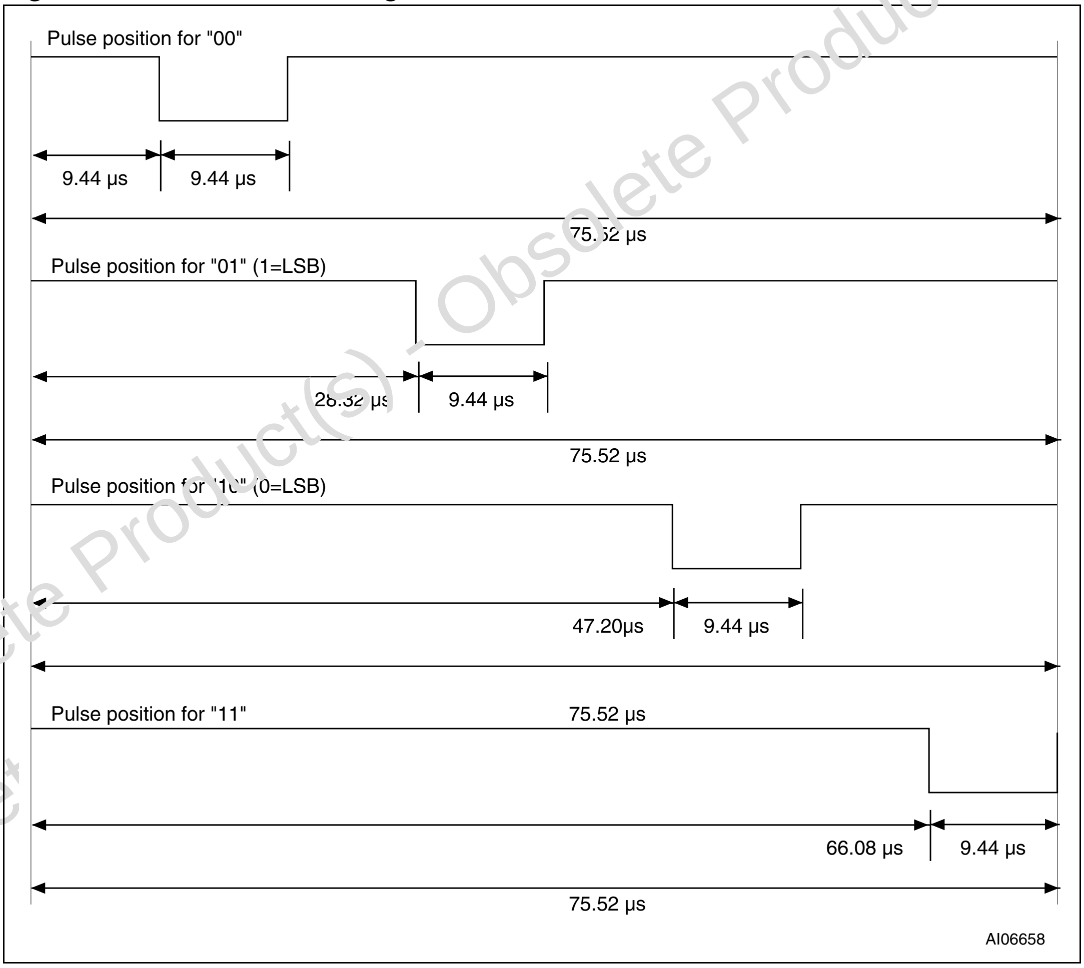
The data coding method involves pulse position modulation. The LRI64 supports the “1-out-of-4” pulse coding mode. Any request that the VCD might send in the “1-out-of-256” pulse coded mode, is ignored, and the LRI64 remains in its current state.

Two bit values are encoded at a time, by the positioning of a pause of the carrier frequency in one of four possible 18.88 µs ($256/f_C$) time slots, as shown in *Figure 6*.

Four successive pairs of bits form a byte. The transmission of one byte takes 302.08 µs and, consequently, the data rate is 26.48 Kbit/s ($f_C/512$).

The encoding for the least significant pair of bits is transmitted first. For example *Figure 5* shows the transmission of E1h (225d, 1110 0001b) by the VCD.

Figure 6. “1-out-of-4” coding mode



7 VCD to LRI64 frames

Request frames are delimited by a start of frame (SOF) and an end of frame (EOF) and are implemented using a code violation mechanism. Unused options are reserved for future use.

The LRI64 is ready to receive a new command frame from the VCD after a delay of t_2 (see *Table 14*) after having sent a response frame to the VCD.

The LRI64 generates a power-on delay of t_{POR} (see *Table 14*) after being activated by the powering field. After this delay, the LRI64 is ready to receive a command frame from the VCD.

In ISO 15693 and ISO 18000-3 Mode 1 standards, the SOF is used to define the data coding mode that the VCD is going to use in the following command frame.

The SOF that is shown in *Figure 7* selects the “1-out-of-4” data coding mode. (The LRI64 does not support the SOF for the “1-out-of-256” data coding mode.)

The corresponding EOF sequence is shown in *Figure 8*.

Figure 7. Request SOF, using the “1-out-of-4” data coding mode

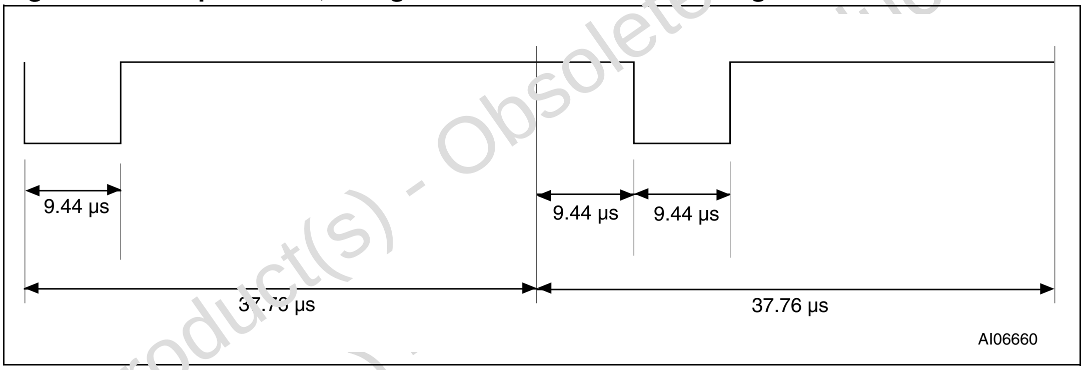
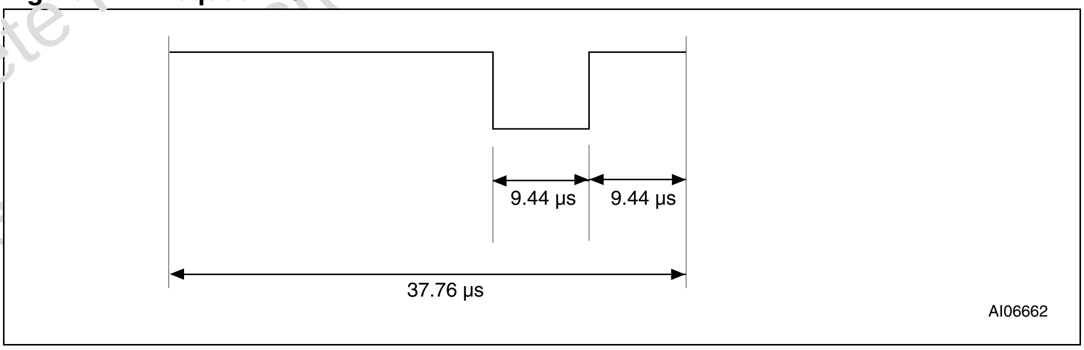


Figure 8. Request EOF



8 Communications signal from LRI64 to VCD

ISO 15693 and ISO 18000-3 Mode 1 standards define several modes, for some parameters, to cater for use in different application requirements and noise environments. The LRI64 does not support all of these modes, but supports the single subcarrier mode at the fast data rate.

8.1 Load modulation

The LRI64 is capable of communication to the VCD via the inductive coupling between the two antennas. The carrier is loaded, with a subcarrier with frequency f_S, generated by switching a load in the LRI64.

The amplitude of the variation to the signal, as received on the VCD antenna, is at least 10 mV, when measured as described in the test methods defined in International Standard ISO 10373-7.

8.2 Subcarrier

The LRI64 supports the one subcarrier modulation response format. This format is selected by the VCD using the first bit in the protocol header.

The frequency, f_S, of the subcarrier load modulation is 423.75 kHz (=f_C/32).

8.3 Data rate

The LRI64 response uses the high data rate format (26.48 Kbit/s). The selection of the data rate is made by the VCD using the second bit in the protocol header.

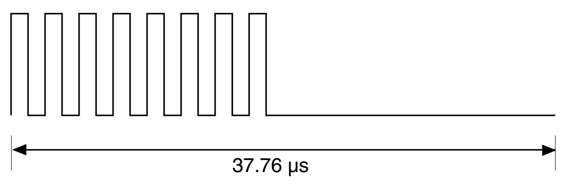
8.4 Bit representation and coding using one subcarrier, at the high data rate

Data bits are encoded using Manchester coding, as described in *Figure 9* and *Figure 10*.

8.4.1 Logic 0

A logic 0 starts with 8 pulses of 423.75 kHz (f_C/32) followed by an unmodulated period of 18.88 µs as shown in *Figure 9*.

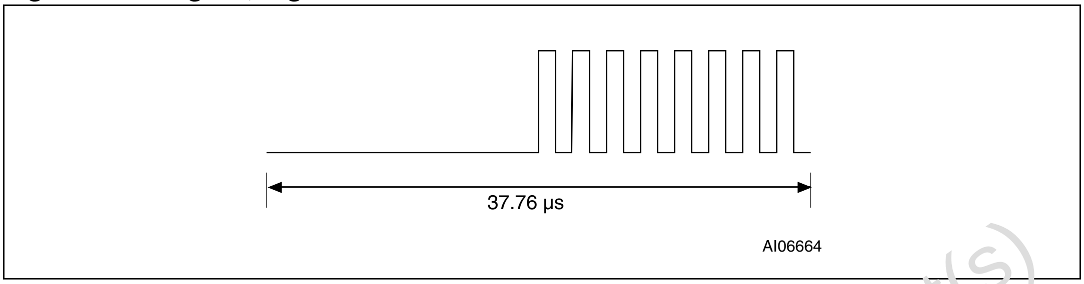
Figure 9. Logic 0, high data rate



8.4.2 Logic 1

A logic 1 starts with an unmodulated period of 18.88 µs followed by 8 pulses of 423.75 kHz (f_C/32) as shown in *Figure 10*.

Figure 10. Logic 1, high data rate



9 LRI64 to VCD frames

Response frames are delimited by a start of frame (SOF) and an end of frame (EOF) and are implemented using a code violation mechanism. The LRI64 supports these in the one subcarrier mode, at the fast data rate, only.

The VCD is ready to receive a response frame from the LRI64 before 320.9µs (t_1) after having sent a command frame.

9.1 LRI64 SOF

SOF comprises three parts: (see *Figure 11*)

- an unmodulated period of 56.64 µs,
- 24 pulses of 423.75 kHz (f_C/32),
- a logic 1 which starts with an unmodulated period of 18.88 µs followed by 8 pulses of 423.75 kHz.

9.2 LRI64 EOF

EOF comprises three parts: (see *Figure 12*)

- a logic 0 which starts with 8 pulses of 423.75 kHz followed by an unmodulated period of 18.88 µs.
- 24 pulses of 423.75 kHz (f_C/32),
- an unmodulated time of 56.64 µs.

Figure 11. Response SOF, using high data rate and one subcarrier

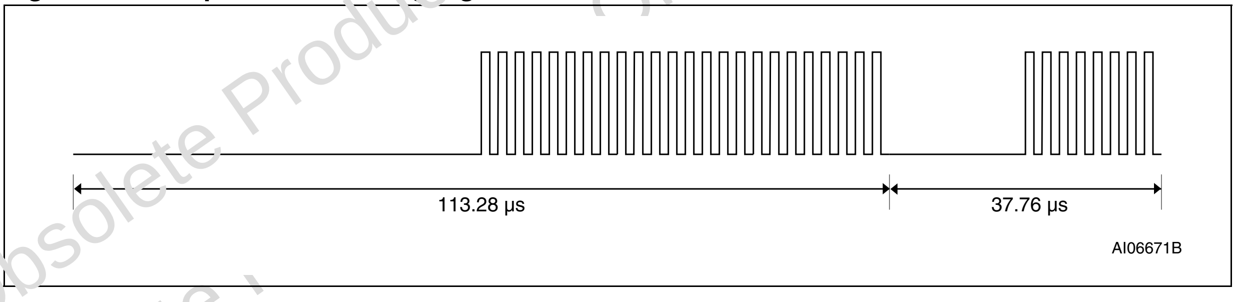
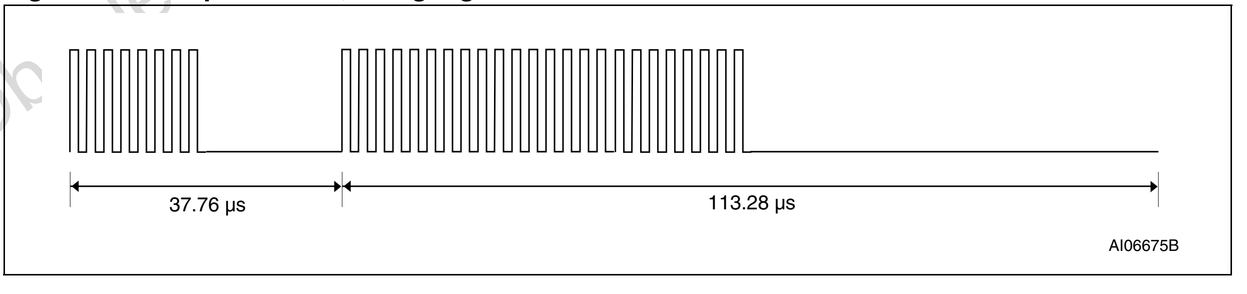


Figure 12. Response EOF, using high data rate and one subcarrier



10 Special fields

10.1 Unique identifier (UID)

Members of the LRI64 family are uniquely identified by a 64-bit unique identifier (UID). This is used for addressing each LRI64 device uniquely and individually, during the anticollision loop and for one-to-one exchange between a VCD and an LRI64.

The UID complies with ISO/IEC 15963 and ISO/IEC 7816-6. It is a read-only code, and comprises (as summarized in *Figure 13*):

- 8-bit prefix, the most significant bits, set at E0h
- 8-bit IC manufacturer code (ISO/IEC 7816-6/AM1), set at 02h (for STMicroelectronics)
- 48-bit unique serial number

Figure 13. UID format

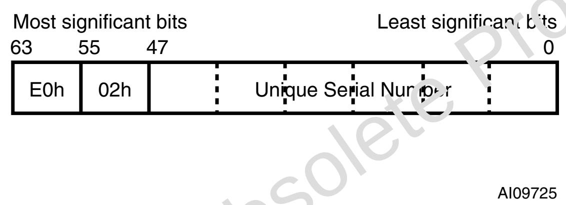
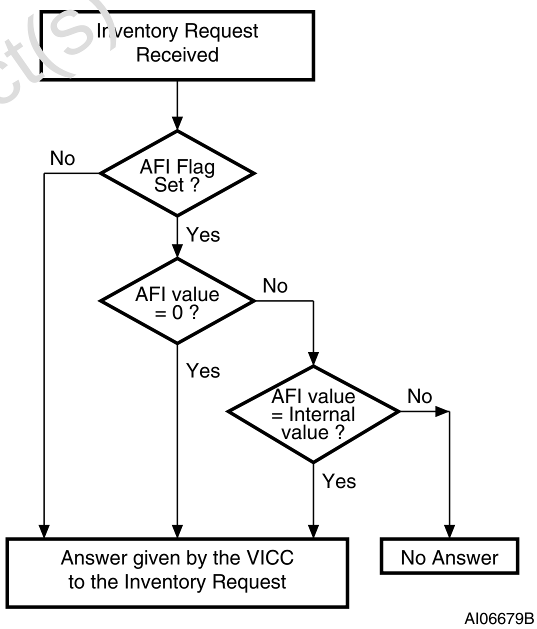


Figure 14. Decision tree for AFI



10.2 Application family identifier (AFI)

The application family identifier (AFI) indicates the type of application targeted by the VCD, and is used to select only those LRI64 devices meeting the required application criteria (as summarized in *Figure 14*). The value is programmed by the LRI64 issuer in the AFI register. Once programmed, it cannot be modified.

The most significant nibble of the AFI is used to indicate one specific application, or all families. The least significant nibble of the AFI is used to code one specific subfamilies, or all subfamilies. Subfamily codes, other than 0, are proprietary (as described in ISO 15693 and ISO 18000-3 Mode 1 documentation).

10.3 Data storage format identifier (DSFID)

The data storage format identifier (DSFID) indicates how the data is structured in the LRI64 memory. It is coded on one byte. It allows for quick and brief knowledge on the logical organization of the data. It is programmed by the LRI64 issuer in the DSFID register. Once programmed, it cannot be modified.

10.4 Cyclic redundancy code (CRC)

The cyclic redundancy code (CRC) is calculated as defined in ISO/IEC 13239, starting from an initial register content of all ones: FFFFh.

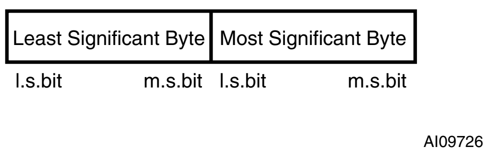
The 2-byte CRC is appended to each request and each response, within each frame, before the EOF. The CRC is calculated on all the bytes after the SOF, up to the CRC field.

Upon reception of a request from the VCD, the LRI64 verifies that the CRC value is valid. If it is invalid, it discards the frame, and does not answer the VCD.

Upon reception of a response from the LRI64, it is recommended that the VCD verify that the CRC value is valid. If it is invalid, the actions that need to be performed are up to the VCD designer.

The CRC is transmitted least significant byte first. Each byte is transmitted Least Significant Bit first, as shown in *Figure 15*).

Figure 15. CRC format



11 LRI64 protocol description

The Transmission protocol defines the mechanism to exchange instructions and data between the VCD and the LRI64, in each direction. Based on “VCD talks first”, the LRI64 does not start transmitting unless it has received and properly decoded an instruction sent by the VCD.

The protocol is based on an exchange of:

- a request from the VCD to the LRI64
- a response from the LRI64 to the VCD

Each request and each response are contained in a frame. The frame delimiters (SOF, EOF) are described in the previous paragraphs.

Each request (*Figure 16*) consists of:

- Request SOF (*Figure 7*)
- Request flags (*Table 3* to *Table 5*)
- Command code
- Parameters (depending on the command)
- Application data
- 2-byte CRC (*Figure 15*)
- Request EOF (*Figure 8*)

Each response (*Figure 17*) consists of:

- Response SOF (*Figure 11*)
- Response flags (*Table 6*)
- Parameters (depending on the command)
- Application data
- 2-byte CRC (*Figure 15*)
- Response EOF (*Figure 12*)

The number of bits transmitted in a frame is a multiple of eight, and thus always an integer number of bytes.

Single-byte fields are transmitted least significant bit first.

Multiple-byte fields are transmitted least significant byte first, with each byte transmitted least significant bit first.

The setting of the flags indicates the presence of any optional fields. When the flag is set, 1, the field is present. When the flag is reset, 0, the field is absent.

Figure 16. VCD request frame format

Request SOF	Request Flags	Command Code	Parameters	Data	2-Byte CRC	Request EOF

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Figure 17. LRI64 response frame format

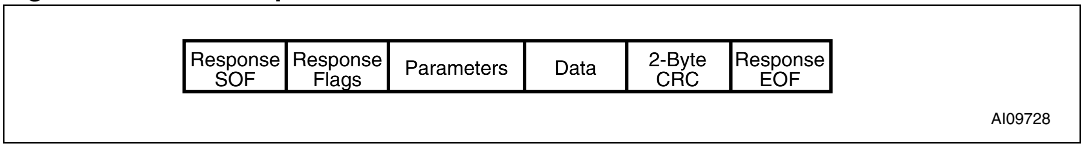
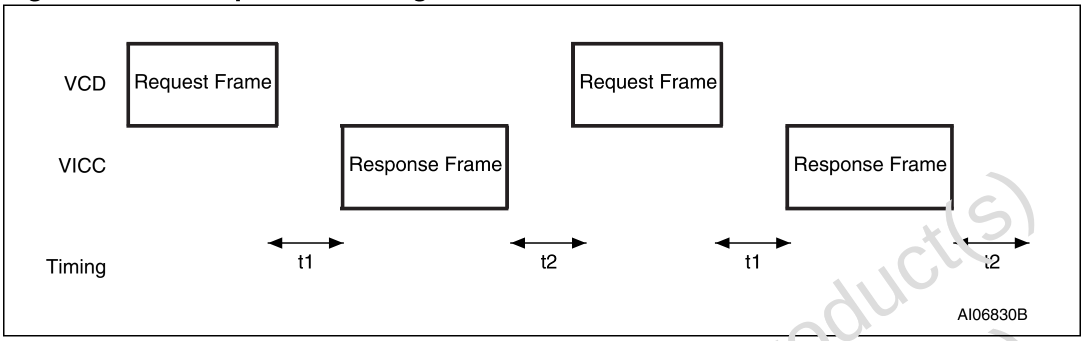


Figure 18. LRI64 protocol timing



12 LRI64 states

A LRI64 can be in any one of three states:

- Power-off
- Ready
- Quiet

Transitions between these states are as specified in *Figure 19*.

12.1 Power-off state

The LRI64 is in the Power-off state when it receives insufficient energy from the VCD.

12.2 Ready state

The LRI64 is in the Ready state when it receives enough energy from the VCD. It answers to any request in Addressed and Non-addressed modes.

12.3 Quiet state

When in the Quiet state, the LRI64 answers to any request in Addressed mode.

13 Modes

The term mode refers to the mechanism for specifying, in a request, the set of LRI64 devices that shall answer to the request.

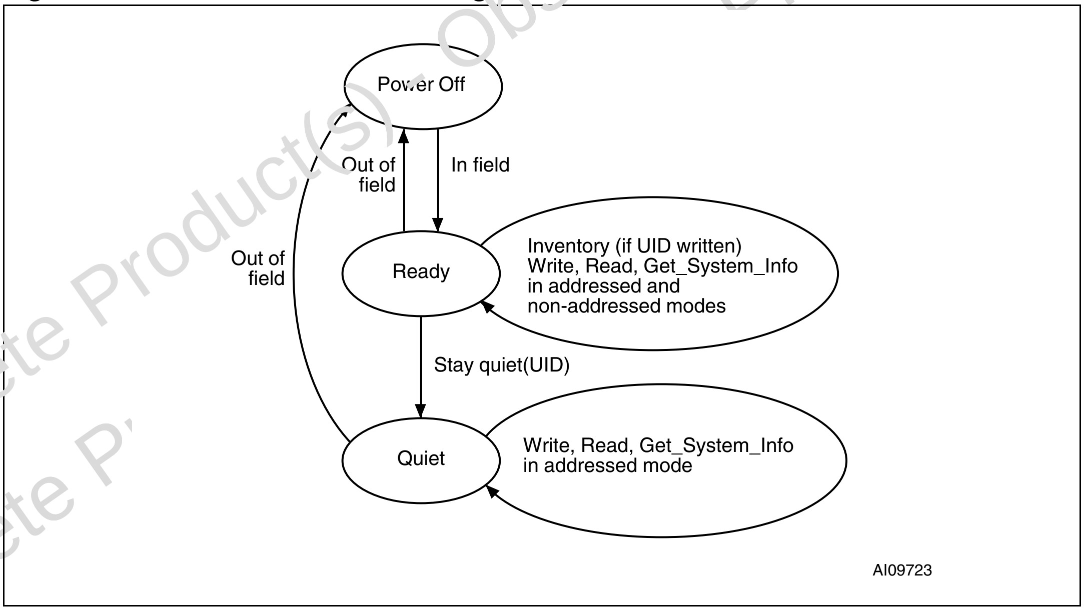
13.1 Addressed mode

When the Address_flag is set to 1 (Addressed mode), the request contains the unique ID (UID) of the addressed LRI64 device (such as an LRI64 device). Any LRI64 receiving a request in which the Address_flag is set to 1, compares the received Unique ID to its own UID. If it matches, it execute the request (if possible) and returns a response to the VCD, as specified by the command description. If it does not match, the LRI64 device remains silent.

13.2 Non-addressed mode (general request)

When the Address_flag is set to 0 (Non-addressed mode), the request does not contain a Unique ID field. Any LRI64 device receiving a request in which the Address_flag is set to 0, executes the request and returns a response to the VCD as specified by the command description.

Figure 19. LRI64 state transition diagram



14 Flags and error codes

14.1 Request flags

In a request, the 8-bit flags field specifies the actions to be performed by the LRI64, and whether corresponding fields are present or not.

Flag bit 3 (the Inventory_flag) defines the way the four most significant flag bits (5 to 8) are used. When bit 3 is reset (0), bits 5 to 8 define the LRI64 selection criteria. When bit 3 is set (1), bits 5 to 8 define the LRI64 Inventory parameters.

Table 3. Request flags 1 to 4

Bit	Name	Value (1)	Description
1	Subcarrier flag	0	Single subcarrier frequency mode. (Option 1 is not supported)
2	Data_rate flag	1	High data rate mode. (Option 0 is not supported)
3	Inventory flag	0	Flags 5 to 8 meaning are according to *Table 4*
		1	Flags 5 to 8 meaning are according to *Table 5*
4	Protocol extension flag	0	No Protocol format extension. Must be set to 0. (Option 1 is not supported)

1. If the value of the request flag is a non authorized value, the LRI64 does not execute the command, and does not respond to the request.

Table 4. Request flags 5 to 8 (when bit 3 = 0)

Bit	Name	Value (1)	Description
5	Select flag	0	No selection mode. Must be set to 0. (Option 1 is not supported)
6	Address flag	0	Non addressed mode. The UID field is not present in the request. All LRI64 shall answer to the request.
		1	Addressed mode. The UID field is present in the request. Only the LRI64 that matches the UID answers the request.
7	Option flag (1)	0	No option. Must be set to 0. (Option 1 is not supported)
8	RFU (1)	0	No option. Must be set to 0. (Option 1 is not supported)

1. Only bit 6 (Address flag) can be configured for the LRI64. All others bits (5, 7 and 8) must be reset to 0.

Table 5. Request flags 5 to 8 (when bit 3 = 1)

Bit	Name	Value[(1)]	Description
5	AFI flag	0	AFI field is not present
		1	AFI field is present
6	Nb_slots flag	0	16 slots
		1	1 slot
7	Option flag	0	No option. Must be set to 0. (Option 1 is not supported)
8	RFU	0	No option. Must be set to 0. (Option 1 is not supported)

1. Bits 7 and 8 must be reset to 0.

14.2 Response flags

In a response, the 8-bit flags field indicates how actions have been performed by the LRI64, and whether corresponding fields are present or not.

Table 6. Response flags 1 to 8

Bit	Name	Value	Description
1	Error flag	0	No error
		1	Error detected. Error code is in the "Error" field.
2	RFU	0	
3	RFU	0	
4	RFU	0	
5	RFU	0	
6	RFU	0	
7	RFU	0	
8	RFU	0	

14.3 Response error code

If the Error flag is set by the LRI64 in the response, the error code field is present and provides information about the error that occurred. *Table 7* shows the one error code that is supported by the LRI64.

Table 7. Response error code

Error code	Meaning
0Fh	Error with no specific information given

15 Anticollision

The purpose of the anticollision sequence is to allow the VCD to compile a list of the LRI64 devices that are present in the VCD field, each one identified by its unique ID (UID).

The VCD is the master of the communication with one or multiple LRI64 devices. It initiates the communication by issuing the Inventory request (*Figure 22*).

15.1 Request flags

The Nb_slots_flag needs to be set appropriately. The AFI flag needs to be set, if the Optional AFI Field is to be present.

15.2 Mask length and mask value

The mask length defines the number of significant bits in the mask value.

The mask value is contained in an integer number of bytes.

The least significant bit of each is transmitted first.

If the mask length is not a multiple of 8 (bits), the most significant end of the mask value is padded with the required number of null bits (set to 0) so that the mask value is contained in an integer number of bytes, so that the next field (the 2-byte CRC) starts at the next byte boundary.

In the example of *Figure 20*, the mask length is 11 bits. The mask value, 10011001111, is padded out at the most significant end with five bits set to 0. The 11-bit mask plus the current slot number is compared to the UID.

15.3 Inventory responses

Each LRI64 sends its response in a given time slot, or else remains silent.

The first slot starts immediately after the reception of the request EOF.

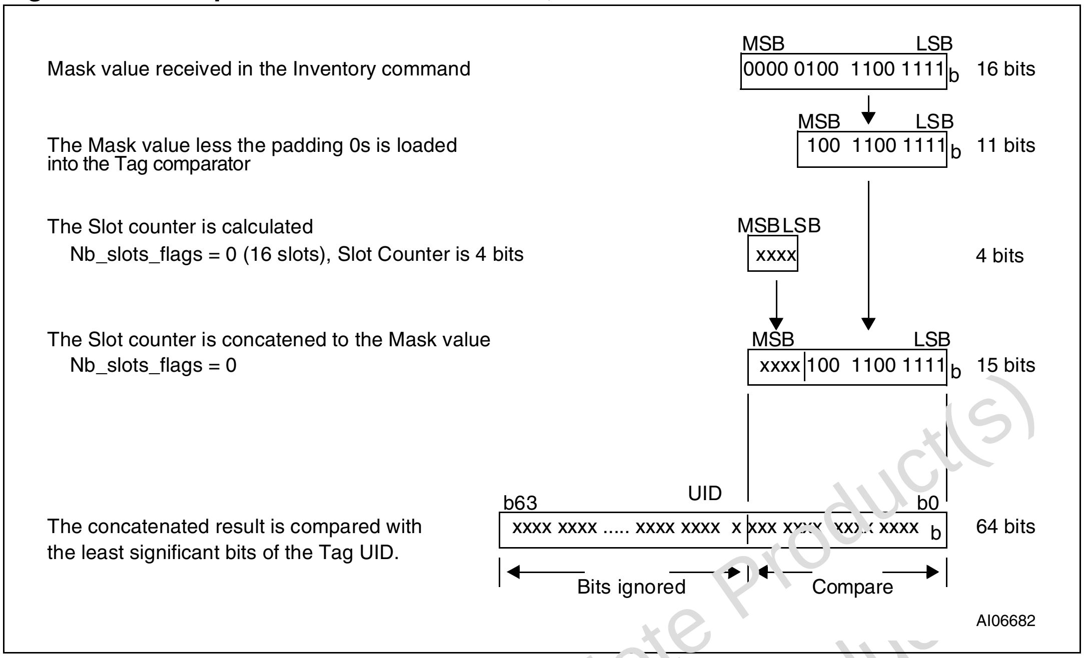
To switch to the next slot, the VCD sends another EOF.

The following rules and restrictions apply:

- if no LRI64 answer is detected, the VCD may switch to the next slot by sending an EOF
- if one or more LRI64 answers are detected, the VCD waits until the complete frame has been received before sending an EOF, to switch to the next slot.

The pulse shall be generated according to the definition of the EOF in ISO 15693 and ISO 18000-3 Mode 1 standards.

Figure 20. Comparison between the mask, slot number and UID



16 Request processing by the LRI64

Upon reception of a valid request, the LRI64 performs the following algorithm, where:

- *NbS* is the total number of slots (1 or 16)
- *SN* is the current slot number (0 to 15)
- The *LSB(value,n)* function returns the *n* least significant bits of *value*
- The *MSB(value,n)* function returns the *n* most significant bits of *value*
- “&” is the concatenation operator
- *Slot_Frame* is either a SOF or an EOF

```
SN = 0
if (Nb_slots_flag)
   then NbS = 1
         SN_length = 0
         endif
   else NbS = 16
         SN_length = 4
         endif

label1:
if LSB(UID, SN_length + Mask_length) =
  LSB(SN,SN_length)&LSB(Mask,Mask_length)
   then answer to inventory request
         endif

wait (Slot_Frame)

if Slot_Frame = SOF
   then Stop Anticollision
         decode/process request
         exit
         endif

if Slot_Frame = EOF
   if SN < NbS-1
      then SN = SN + 1
            goto label1
            exit
            endif
   endif
```

16.1 Explanation of the possible cases

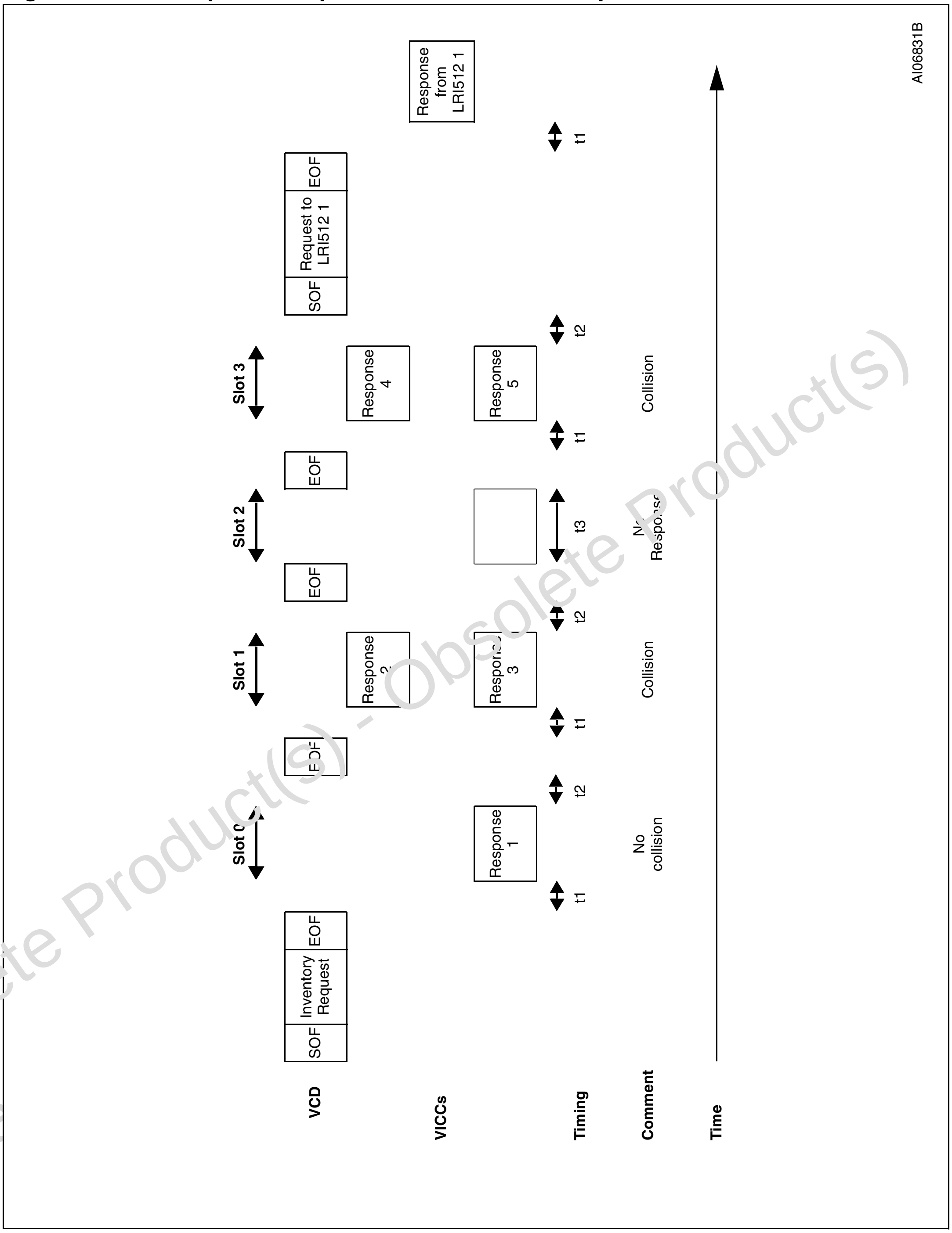
Figure 21 summarizes the main possible cases that can occur during an anticollision sequence when the number of slots is 16.

The different steps are:

- The VCD sends an Inventory request, in a frame, terminated by a EOF. The number of slots is 16.
- LRI64 #1 transmits its response in slot 0. It is the only one to do so, therefore no collision occurs and its UID is received and registered by the VCD;
- The VCD sends an EOF, to switch to the next slot.
- In slot 1, two LRI64 devices, #2 and #3, transmit their responses. This generates a collision. The VCD records it, and remembers that a collision was detected in slot 1.
- The VCD sends an EOF, to switch to the next slot.
- In slot 2, no LRI64 transmits a response. Therefore the VCD does not detect a LRI64 SOF, and decides to switch to the next slot by sending an EOF.
- In slot 3, there is another collision caused by responses from LRI64 #4 and #5
- The VCD then decides to send a request (for instance a Read Block) to LRI64 #1, whose UID was already correctly received.
- All LRI64 devices detect a SOF and exit the anticollision sequence. They process this request and since the request is addressed to LRI64 #1, only LRI64 #1 transmits its response.
- All LRI64 devices are ready to receive another request. If it is an Inventory command, the slot numbering sequence restarts from 0.

Note: The decision to interrupt the anticollision sequence is up to the VCD. It could have continued to send EOFs until slot 15 and then send the request to LRI64 #1.

Figure 21. Description of a possible anticollision sequence between LRI64 devices



17 Timing definitions

Figure 21 shows three specific delay times: t_1, t_2 and t_3. All of them have a minimum value, specified in *Table 14*. The t_1 parameter also has a maximum and a typical value specified in *Table 14*, as summarized in *Table 8*.

Table 8. Timing values[1]

	Min.	Typ.	Max.
t_1	t_1(min)	t_1(typ) = 4352 / f_C	t_1(max)
t_2	t_2(min) = 4192 / f_C	—	—
t_3	t_1(max) + t_{SOF} (see notes[2],[3])	—	—

1. The tolerance of specific timings is ± 32/f_C.
2. t_{SOF} is the duration for the LRI64 to transmit an SOF to the VCD.
3. t_1(max) does not apply for write alike requests. Timing conditions for write alike requests are defined in the command description.

17.1 LRI64 response delay, t_1

Upon detection of the rising edge of the EOF received from the VCD, the LRI64 waits for a time equal to

t_1(typ) = 4352 / f_C

before starting to transmit its response to a VCD request, or switching to the next slot when in an inventory process.

17.2 VCD new request delay, t_2

t_2 is the time after which the VCD may send an EOF to switch to the next slot when one or more LRI64 responses have been received during an inventory command. It starts from the reception of the EOF received from the LRI64 devices.

The EOF sent by the VCD is 10% modulated, independent of the modulation index used for transmitting the VCD request to the LRI64.

t_2 is also the time after which the VCD may send a new request to the LRI64 as described in *Figure 18*.

t_2(min) = 4192 / f_C

17.3 VCD new request delay when there is no LRI64 response, t_3

t_3 is the time after which the VCD may send an EOF to switch to the next slot when no LRI64 response has been received.

The EOF sent by the VCD is 10% modulated, independent of the modulation index used for transmitting the VCD request to the LRI64.

From the time the VCD has generated the rising edge of an EOF:

- The VCD waits for a time at least equal to the sum of t_3(min) and the typical response time of an LRI64, which depends on the data rate and subcarrier modulation mode, before sending a subsequent EOF.

18 Command codes

The LRI64 supports the command codes listed in *Table 9*.

Table 9. Command codes

Command code	Function
01h	Inventory
02h	Stay Quiet
20h	Read Single Block
21h	Write Single Block
2Bh	Get System Info

18.1 Inventory

When receiving the Inventory request, the LRI64 performs the anticollision sequence. The Inventory_flag is set to 1. The meanings of flags 5 to 8 is as described in *Table 5*.

The Request frame (*Figure 22*) contains:

- Request flags (*Table 3* and *Table 5*)
- Inventory command code (01h, *Table 9*)
- AFI, if the AFI flag is set
- Mask length
- Mask value
- 2-byte CRC (*Figure 15*)

In case of errors in the Inventory request frame, the LRI64 does not generate any answer.

The response frame (*Figure 23*) contains:

- Response flags (*Table 6*)
- DSFID
- Unique ID
- 2-byte CRC (*Figure 15*)

Figure 22. Inventory, request frame format

Request SOF	Request Flags	Command Code	Optional AFI	Mask Length	Mask Value	2-Byte CRC	Request EOF
	8 bits	8 bits 01h	8 bits	8 bits	0 to 8 bytes	16 bits	

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Figure 23. Inventory, response frame format

Response SOF	Response Flags	DSFID	UID	2-Byte CRC	Response EOF
	8 bits	8 bits	64 bits	16 bits	

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18.2 Stay Quiet

The Stay Quiet command is always executed in Addressed mode (the Address_Flag is set to 1).

The Request frame (*Figure 24*) contains:

- Request flags (22h, as described in *Table 3* and *Table 4*)
- Stay Quiet command code (02h, *Table 9*)
- Unique ID
- 2-byte CRC (*Figure 15*)

When receiving the Stay Quiet command, the LRI64 enters the Quiet state and does *not* send back a response. There is *no* response to the Stay Quiet command.

When in the Quiet state:

- the LRI64 does not process any request in which the Inventory_flag is set
- the LRI64 responds to commands in the Addressed mode if the UID matches

The LRI64 exits the Quiet state when it is taken to the Power Off state (*Figure 19*).

Figure 24. Stay Quiet, request frame format

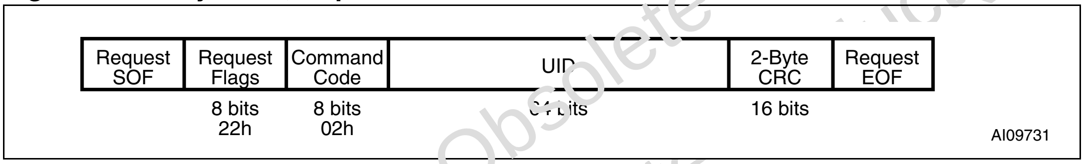
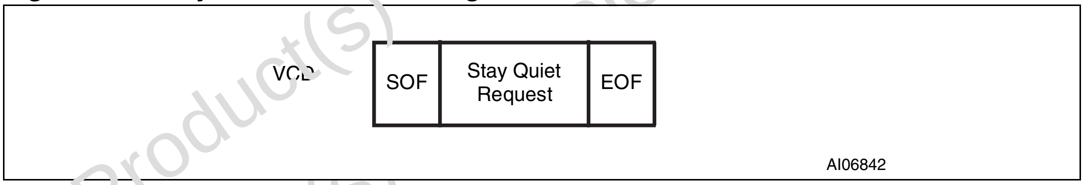


Figure 25. Stay Quiet frame exchange between VCD and LRI64



18.3 Read Single Block

When receiving the Read Single Block command, the LRI64 reads the requested block and sends back its 8-bit value in the response. The Option_Flag is supported. The Read Single Block can be issued in both addressed and non addressed modes.

The request frame (*Figure 26*) contains:

- Request flags (*Table 3* and *Table 4*)
- Read Single Block command code (20h, *Table 9*)
- Unique ID (Optional)
- Block number
- 2-byte CRC (*Figure 15*)

If there is no error, at the LRI64, the response frame (*Figure 27*) contains:

- Response flags (*Table 6*)
- Block locking status, if Option_Flag is set
- 1 byte of block data (*Table 10*)
- 2-byte CRC (*Figure 15*)

Otherwise, if there is an error, the response frame (*Figure 28*) contains:

- Response flags (01h, *Table 6*)
- Error code (0Fh, *Table 7*)
- 2-byte CRC (*Figure 15*)

Table 10. Block lock status

Bit	Name	Value	Description
0	Block locked	0	Current block not locked
		1	Current block locked
1 to 7	RFU	0	

Figure 26. Read Single Block, request frame format

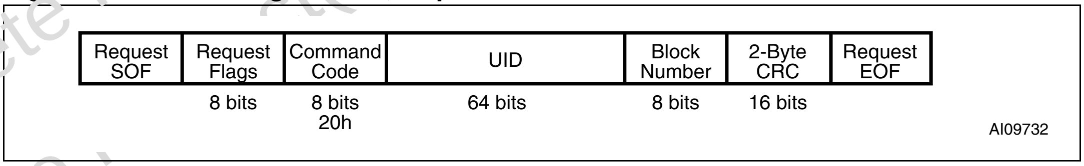


Figure 27. Read Single Block, response frame format, when Error_Flag is *not* set

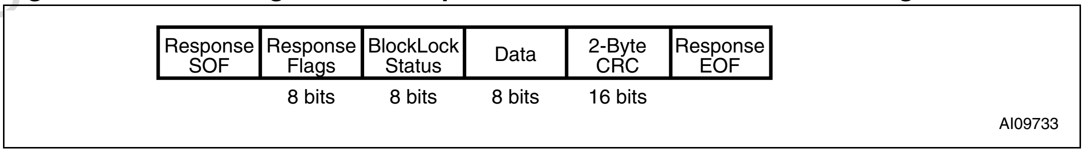


Figure 28. Read Single Block, response frame format, when Error_Flag is set

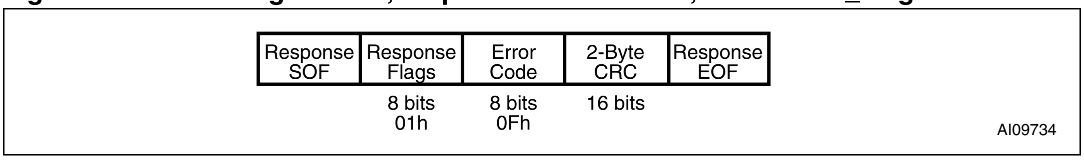
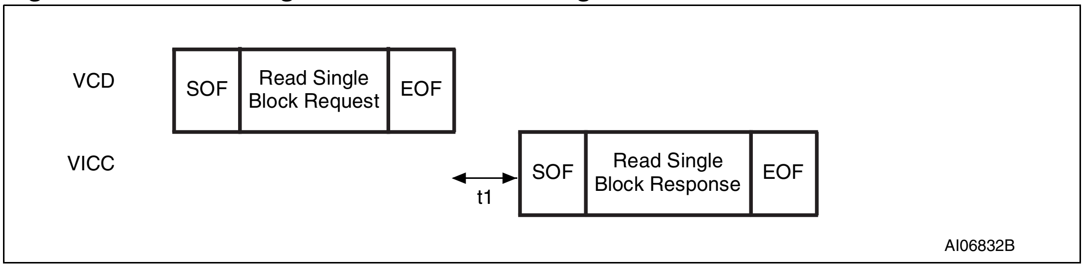


Figure 29. READ Single Block frame exchange between VCD and LRI64



18.4 Write Single Block

When receiving the Write Single Block command, the LRI64 writes the requested block with the data contained in the request and report the success of the operation in the response. The Option_Flag is not supported and must be set to 0. The Write Single Block can be issued in both addressed and non addressed modes.

During the write cycle t_W, no modulation shall occur, otherwise the LRI64 may program the data incorrectly in the memory.

The request frame (*Figure 30*) contains:

- Request flags (*Table 3* and *Table 4*)
- Write Single Block command code (21h, *Table 9*)
- Unique ID (Optional)
- Block number
- Data
- 2-byte CRC (*Figure 15*)

If there is no error, at the LRI64, an empty response frame (*Figure 31*) is sent back after the write cycle, containing no parameters. It just contains:

- Response flags (*Table 6*)
- 2-byte CRC (*Figure 15*)

Otherwise, if there is an error, the response frame (*Figure 32*) contains:

- Response flags (01h, *Table 6*)
- Error Code (0Fh, *Table 7*)
- 2-byte CRC (*Figure 15*)

Figure 30. Write Single Block, request frame format

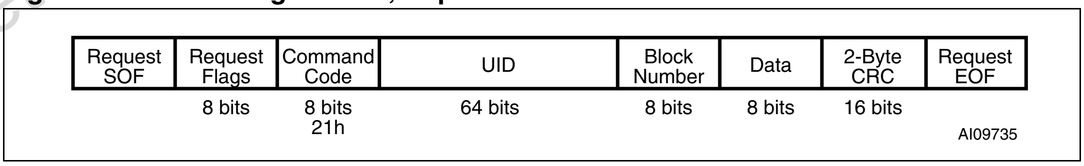


Figure 31. Write Single Block, response frame format, when Error_Flag is *not* set

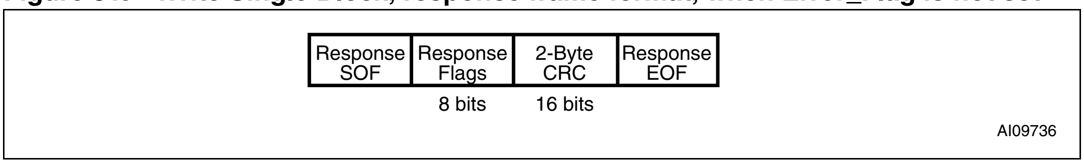


Figure 32. Write Single Block, response frame format, when Error_Flag is set

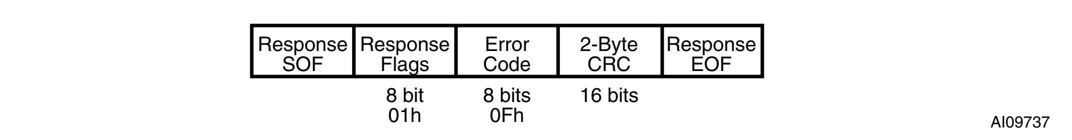
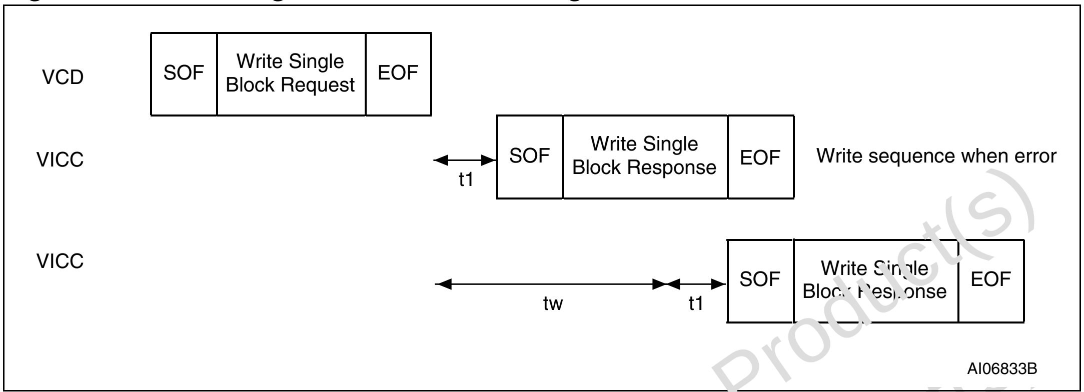


Figure 33. Write Single Block frame exchange between VCD and LRI64



18.5 Get System Info

When receiving the Get System Info command, the LRI64 send back its information data in the response.The Option_Flag is not supported and must be set to 0. The Get System Info can be issued in both addressed and non addressed modes.

The request frame (*Figure 26*) contains:

- Request flags (*Table 3* and *Table 4*)
- Get System Info command code (2Bh, *Table 9*)
- Unique ID (Optional)
- 2-byte CRC (*Figure 15*)

If there is no error, at the LRI64, the response frame (*Figure 27*) contains:

- Response flags (*Table 6*)
- Information flags set to 0Fh, indicating the four information fields that are present (DSFID, AFI, Memory Size, IC Reference)
- Unique ID
- DSFID value (as written in block 9)
- AFI value (as written in block 8)
- Memory size: for the LRI64, there are 15 blocks (0Eh) of 1 byte (00h).
- IC Reference: only the 6 most significant bits are used. The product code of the LRI64 is 00 0101_b=5_d
- 2-byte CRC (*Figure 15*)

Otherwise, if there is an error, the response frame (*Figure 28*) contains:

- Response flags (01h, *Table 6*)
- Error Code (0Fh, *Table 7*)
- 2-byte CRC (*Figure 15*)

Figure 34. Get System Info, request frame format

Request SOF	Request Flags	Command Code	UID	2-Byte CRC	Request EOF
	8 bits	8 bits 2Bh	64 bits	16 bits	

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Figure 35. Get System Info, response frame format, when Error_Flag is *not* set

Response SOF	Response Flags	Information Flags	UID	DSFID	AFI	Memory Size	IC Ref	2-Byte CRC	Response EOF
	8 bits 00h	8 bits 0Fh	64 bits	8 bits	8 bits	16 bits 000Eh	8 bits 000101xxb	16 bits	

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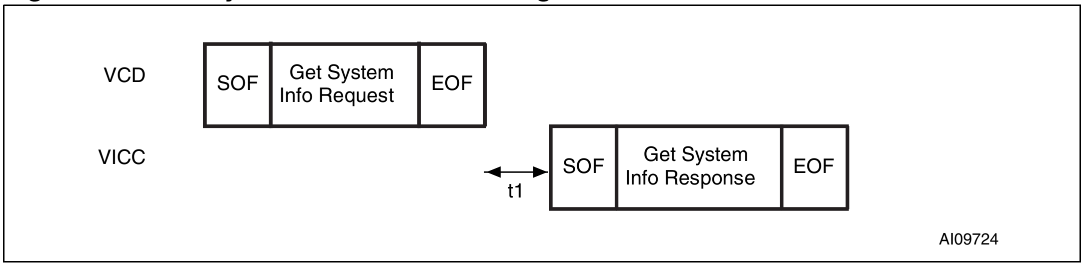
Figure 36. Get System Info, response frame format, when Error_Flag is set

Response SOF	Response Flags	Error Code	2-Byte CRC	Response EOF
	8 bits 01h	8 bits 0Fh	16 bits	

AI09740

Figure 37. Get System Info frame exchange between VCD and LRI64



19 Maximum rating

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 11. Absolute maximum ratings

Symbol	Parameter		Min.	Max.	Unit
T_{STG}	Storage temperature	UFDFPN8	–65	150	°C
		Wafer (kept in its antistatic bag)	15	25	
t_{STG}	Storage time	Wafer (kept in its antistatic bag)		23	months
I_{CC}	Supply current on AC0 / AC1		–20	20	mA
V_{MAX}	Input voltage on AC0 / AC1		–7	7	V
V_{ESD}	Electrostatic discharge voltage[1]	UFDFPN8 (HBM)[2]	–1000	1000	V
		UFDFPN8 (MM)[3]	–100	100	V

1. Mil. Std. 883 - Method 3015
2. Human body model.
3. Machine model.

20 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 12. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient operating temperature	–20	85	°C

Figure 38. LRI64 synchronous timing, transmit and receive

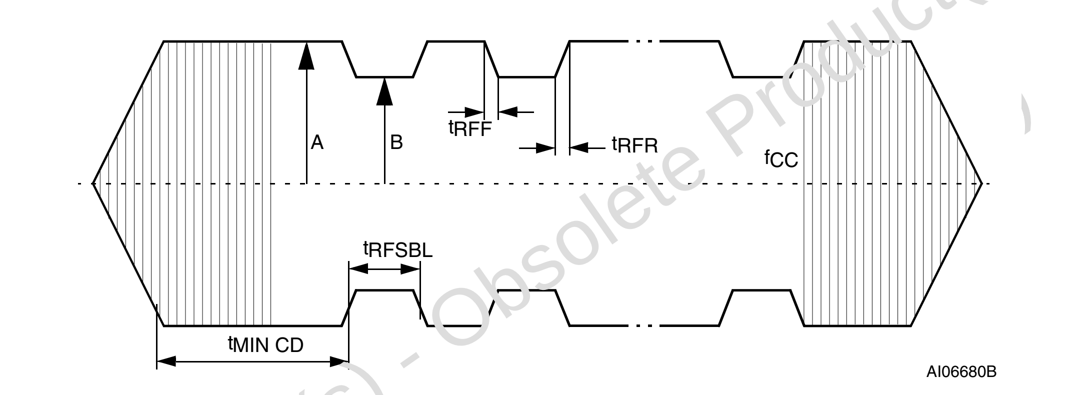


Figure 38 shows an ASK modulated signal, from the VCD to the LRI64. The test condition for the AC/DC parameters are:

- Close coupling condition with tester antenna (1mm)
- Gives LRI64 performance on tag antenna

Table 13. DC characteristics

Symbol	Parameter		Test conditions(1)	Min.	Typ.	Max.	Unit
V_{CC}	Regulated voltage			1.5		3.0	V
V_{RET}	Retromodulated induced voltage		ISO10373-7	10			mV
I_{CC}	Supply current	Read	V_{CC} = 3.0 V			50	µA
		Write	V_{CC} = 3.0 V			150	µA
C_{TUN}	Internal tuning capacitor		f=13.56 MHz for W4/1		21		pF
			f=13.56 MHz for W4/2		28.5		pF
			f=13.56 MHz for W4/3		97		pF

1. T_A = –20 to 85 °C

Table 14. AC characteristics

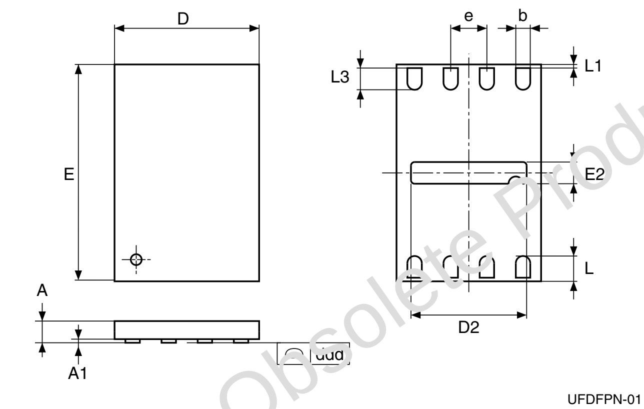
Symbol	Parameter	Test conditions[1],[2]	Min.	Typ.	Max.	Unit
f_C	External RF signal frequency		13.553	13.56	13.567	MHz
$MI_{CARRIER}$	10% carrier modulation index	MI=(A-B)/(A+B)	10		30	%
t_{RFR}, t_{RFF}	10% rise and fall time		0		3.0	µs
t_{RFSBL}	10% minimum pulse width for bit		7.1		9.44	µs
t_{JIT}	Bit pulse jitter		–2		+2	µs
t_{MINCD}	Minimum time from carrier generation to first data	From H-field min		0.1	1	ms
f_{SH}	Subcarrier frequency high	$f_C/32$		423.75		kHz
t_1	Time for LRI64 response	$4352/f_C$	313	320.9	322	µs
t_2	Time between commands	$4224/f_C$	309	311.5	314	µs
t_W	Programming time	$93297/f_C$			6.88	ms

1. T_A = –20 to 85 °C
2. All timing measurements were performed on a reference antenna with the following characteristics:
External size: 75 mm x 48 mm
Number of turns: 6
Width of conductor: 1 mm
Space between 2 conductors: 0.4 mm
Value of the tuning capacitor: 28.5 pF (LRI64-W4)
Value of the coil: 4.3 µH
Tuning Frequency: 14.4 MHz.

21 Package mechanical data

In order to meet environmental requirements, ST offers the LRI64 in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of second-level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.
The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*.

Figure 39. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 × 3 mm, package outline



1. Drawing is not to scale.

Table 15. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 × 3 mm, package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	0.55	0.45	0.6	0.0217	0.0177	0.0236
A1	0.02	0	0.05	0.0008	0	0.002
b	0.25	0.2	0.3	0.0098	0.0079	0.0118
D	2	1.9	2.1	0.0787	0.0748	0.0827
D2	1.6	1.5	1.7	0.063	0.0591	0.0669
E	3	2.9	3.1	0.1181	0.1142	0.122
E2	0.2	0.1	0.3	0.0079	0.0039	0.0118
e	0.5	-	-	0.0197	-	-
L	0.45	0.4	0.5	0.0177	0.0157	0.0197
L1			0.15			0.0059
L3		0.3			0.0118	
ddd[2]	0.08			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

22 Part numbering

Table 16. Ordering information scheme

Example: LRI64 - W4 / 2 GE

Device type

LRI64

Package

W4 = 180 µm ± 15 µm unsawn wafer

SBN18 = 180 µm ± 15 µm bumped and sawn wafer on 8-inch frame

MBTG = UFDFPN8 (MLP8), tape & reel packing, ECOPACK®, lead-free, RoHS compliant, Sb_2O_3-free and TBBA-free(1)

Tuning capacitance

1 = 21 pF

2 = 28.5 pF

3 = 97 pF

Customer code given by ST

GE = generic product

xx = customer code after personalization

1. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Appendix A Algorithm for pulsed slots

The following pseudo-code describes how the anticollision could be implemented on the VCD, using recursive functions.

```
function push (mask, address); pushes on private stack
function pop (mask, address); pops from private stack
function pulse_next_pause; generates a power pulse
function store(LRI64_UID); stores LRI64_UID

function poll_loop (sub_address_size as integer)
  pop (mask, address)
  mask = address & mask; generates new mask
            ; send the request
  mode = anticollision
  send_Request (Request_cmd, mode, mask length, mask value)
  for sub_address = 0 to (2^sub_address_size - 1)
    pulse_next_pause
    if no_collision_is_detected ; LRI64 is inventoried
      then
        store (LRI64_UID)
      else ; remember a collision was detected
        push(mask,address)
      endif
    next sub_address

  if stack_not_empty ; if some collisions have been detected and
    then   ; not yet processed, the function calls itself
      poll_loop (sub_address_size); recursively to process the
last stored collision
    endif
end poll_loop

main_cycle:
  mask = null
  address = null
  push (mask, address)
  poll_loop(sub_address_size)
end_main_cycle
```

Appendix B C-example to calculate or check the CRC16 according to ISO/IEC 13239

The cyclic redundancy check (CRC) is calculated on all data contained in a message, from the start of the flags through to the end of Data. This CRC is used from VCD to LRI64 and from LRI64 to VCD.

To add extra protection against shifting errors, a further transformation on the calculated CRC is made. The One's Complement of the calculated CRC is the value attached to the message for transmission.

For checking of received messages the 2 CRC bytes are often also included in the re-calculation, for ease of use. In this case, given the expected value for the generated CRC is the residue of F0B8h

Table 17. CRC definition

CRC definition					
CRC Type	**Length**	**Polynomial**	**Direction**	**Preset**	**Residue**
ISO/IEC 13239	16 bits	$X^{16} + X^{12} + X^5 + 1$ = 0x8408	Backward	FFFFh	F0B8h

22.1 CRC calculation example

This example in C language illustrates one method of calculating the CRC on a given set of bytes comprising a message.

```
#define  POLYNOMIAL0x8408//  x^16 + x^12 + x^5 + 1
#define  PRESET_VALUE0xFFFF
#define  CHECK_VALUE0xF0B8

#define  NUMBER_OF_BYTES4// Example: 4 data bytes
#define  CALC_CRC1
#define  CHECK_CRC0

void main()
{
 unsigned int  current_crc_value;
 unsigned char array_of_databytes[NUMBER_OF_BYTES + 2] = {1, 2, 3,
4, 0x91, 0x39};
  int            number_of_databytes = NUMBER_OF_BYTES;
  int            calculate_or_check_crc;
  int            i, j;
  calculate_or_check_crc = CALC_CRC;
// calculate_or_check_crc = CHECK_CRC;// This could be an other
example
  if (calculate_or_check_crc == CALC_CRC)
  {
      number_of_databytes = NUMBER_OF_BYTES;
  }
```

```
  else    // check CRC
  {
      number_of_databytes = NUMBER_OF_BYTES + 2;
  }

  current_crc_value = PRESET_VALUE;

  for (i = 0; i < number_of_databytes; i++)
  {
      current_crc_value = current_crc_value ^ ((unsigned
int)array_of_databytes[i]);

      for (j = 0; j < 8; j++)
      {
          if (current_crc_value & 0x0001)
          {
              current_crc_value = (current_crc_value >> 1) ^
POLYNOMIAL;
          }
          else
          {
              current_crc_value = (current_crc_value >> 1);
          }
      }
  }

  if (calculate_or_check_crc == CALC_CRC)
  {
      current_crc_value = ~current_crc_value;

      printf ("Generated CRC is 0x%04X\n", current_crc_value);

      // current_crc_value is now ready to be appended to the data
stream
      // (first LSByte, then MSByte)
  }
  else   // check CRC
  {
      if (current_crc_value == CHECK_VALUE)
      {
          printf ("Checked CRC is ok (0x%04X)\n",
current_crc_value);
      }
      else
      {
          printf ("Checked CRC is NOT ok (0x%04X)\n",
current_crc_value);
      }
  }
}
```

Appendix C Application family identifier (AFI) coding

AFI (application family identifier) represents the type of application targeted by the VCD and is used to extract from all the LRI64 present only the LRI64 meeting the required application criteria.

It is programmed by the LRI64 issuer (the purchaser of the LRI64). Once locked, it can not be modified.

The most significant nibble of AFI is used to code one specific or all application families, as defined in *Table 18*.

The least significant nibble of AFI is used to code one specific or all application subfamilies. Subfamily codes different from 0 are proprietary.

Table 18. AFI coding(1)

AFI most significant nibble	AFI least significant nibble	Meaning LRI64 Devices respond from	Examples / Note
0	0	All families and subfamilies	No applicative preselection
x	0	All subfamilies of family X	Wide applicative preselection
x	y	Only the Yth subfamily of family X	
0	y	Proprietary subfamily Y only	
1	0, y	Transport	Mass transit, bus, airline, etc.
2	0, y	Financial	IEP, banking, retail, etc.
3	0, y	Identification	Access Control, etc.
4	0, y	Telecommunication	Public telephony, GSM, etc.
5	0, y	Medical	
6	0, y	Multimedia	Internet services, etc.
7	0, y	Gaming	
8	0, y	Data storage	Portable Files, etc.
9	0, y	Item management	
A	0, y	Express parcels	
B	0, y	Postal services	
C	0, y	Airline bags	
D	0, y	RFU	
E	0, y	RFU	
F	0, y	RFU	

1. x and y each represent any single-digit hexadecimal value between 1 and F

Revision history

Table 19. Document revision history

Date	Revision	Changes
27-Aug-2003	1.0	First Issue
16-Jul-2004	2.0	First public release of full datasheet
22-Sep-2004	3.0	Values changed for t_W, t_1 and t_2
11-Jul-2005	4.0	Added MLP package information.
7-Sept-2005	5.0	Modified Option_Flag information in *Get System Info* command and added ISO 18000-3 Mode 1 compliance.
19-Feb-2007	6	Document reformatted. UFDPFN8 package specifications updated (see *Table 15: UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 × 3 mm, package mechanical data*). ST offers the LRI64 in ECOPACK® compliant UFDPFN8 packages. C_{TUN} value for W4/3 added to *Table 13: DC characteristics*. Small text changes.
01-Apr-2008	7	Small text changes. V_{ESD} for MLP package added to *Table 11: Absolute maximum ratings*. UFDFPN8 inch values calculated from millimeters rounded to four decimal digits (see *Table 15: UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 × 3 mm, package mechanical data*).
28-Aug-2008	8	LRI64 products are no longer delivered in A1 inlays and A6 and A7 antennas. T_{STG} added for UFDPFN8 package in *Table 11: Absolute maximum ratings*. *Table 16: Ordering information scheme* clarified.