

ADC0804S030/040/050

Single 8 bits ADC, up to 30 MHz, 40 MHz or 50 MHz

Rev. 03 — 2 July 2012

Product data sheet

1. General description

The ADC0806030/040/050 are a family of 8-bit high-speed, low-power Analog-to-Digital Converters (ADC) for professional video and other applications. It converts the analog input signal into 8-bit binary coded digital signals at a maximum sampling rate of 50 MHz. All digital inputs and outputs are Transistor-Transistor Logic (TTL) and CMOS compatible, although a low-level sine wave clock input signal can also be used.

The device requires an external source to drive its reference ladder. If the application requires that the reference is driven via internal sources, IDT recommends you use one of the ADC1003S030/040/050 family.

2. Features

- 8-bit resolution
- Sampling rate up to 50 MHz
- DC sampling allowed
- One clock cycle conversion only
- High signal-to-noise ratio over a large analog input frequency range (7.8 effective bits at 4.43 MHz full-scale input at $f_{clk} = 40$ MHz)
- No missing codes guaranteed
- In-Range (IR) CMOS output
- TTL and CMOS levels compatible digital inputs
- 3 V to 5 V CMOS digital outputs
- Low-level AC clock input signal allowed
- External reference voltage regulator
- Power dissipation only 175 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required

3. Applications

- Video data digitizing
- Radar
- Transient signal analysis
- $\Sigma\Delta$ modulators
- Medical imaging
- Barcode scanner
- Global Positioning System (GPS) receiver



- Cellular base stations

4. Quick reference data

Table 1. Quick reference data

$V_{CCA} = V3$ to $V4 = 4.75$ V to 5.25 V; $V_{CCD} = V11$ to $V12$ and $V28$ to $V27 = 4.75$ V to 5.25 V;
 $V_{CCO} = V13$ to $V14 = 3.0$ V to 5.25 V; AGND and DGND shorted together; $T_{amb} = 0$ °C to 70 °C;
 typical values measured at $V_{CCA} = V_{CCD} = 5$ V and $V_{CCO} = 3.3$ V, $V_{i(a)(p-p)} = 2.0$ V; $C_L = 15$ pF and
 $T_{amb} = 25$ °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output supply voltage		3.0	3.3	5.25	V
I_{CCA}	analog supply current		-	18	24	mA
I_{CCD}	digital supply current		-	16	21	mA
I_{CCO}	output supply current	$f_{clk} = 40$ MHz; ramp input	-	1	2	mA
INL	integral non-linearity	$f_{clk} = 40$ MHz ramp input	-	± 0.2	± 0.5	LSB
DNL	differential non-linearity	$f_{clk} = 40$ MHz ramp input	-	± 0.12	± 0.22	LSB
$f_{clk(max)}$	maximum clock frequency	ADC0804S030TS	30	-	-	MHz
		ADC0804S040TS	40	-	-	MHz
		ADC0804S050TS	50	-	-	MHz
P_{tot}	total power dissipation	$f_{clk} = 40$ MHz; ramp input	-	175	247	mW

5. Ordering information

Table 2. Ordering information

Type number	Package			Sampling frequency (MHz)
	Name	Description	Version	
ADC0804S030TS	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1	30
ADC0804S040TS	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1	40
ADC0804S050TS	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1	50

6. Block diagram

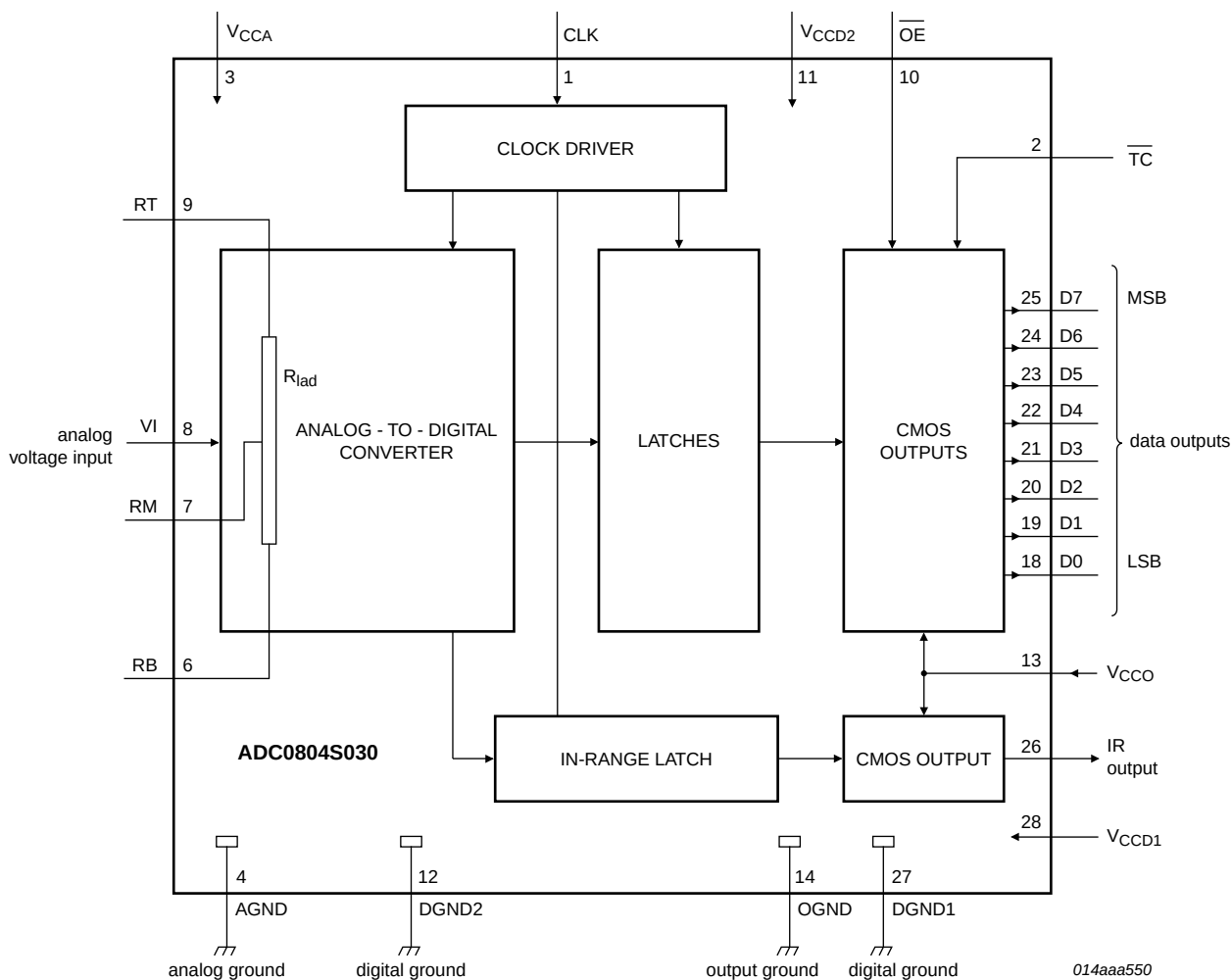


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

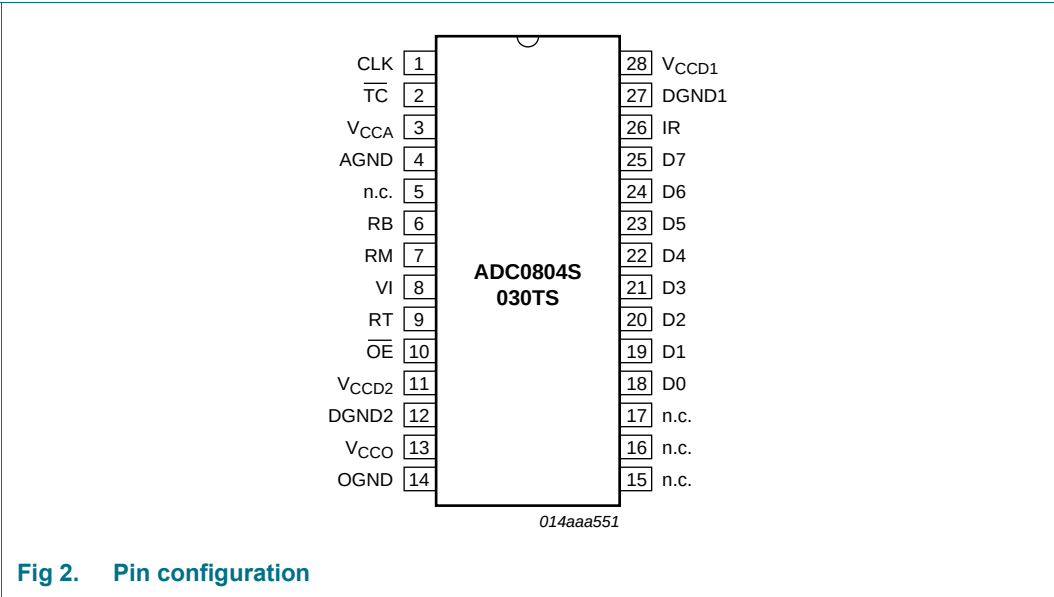


Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
CLK	1	clock input
$\overline{TC}$	2	two's complement input (active LOW)
V_{CCA}	3	analog supply voltage (5 V)
AGND	4	analog ground
n.c.	5	not connected
RB	6	reference voltage BOTTOM input
RM	7	reference voltage MIDDLE
VI	8	analog input voltage
RT	9	reference voltage TOP input
$\overline{OE}$	10	output enable input (CMOS level input, active LOW)
V_{CCD2}	11	digital supply voltage 2 (5 V)
DGND2	12	digital ground 2
V_{CCO}	13	supply voltage for output stages (3 V to 5 V)
OGND	14	output ground
n.c.	15	not connected
n.c.	16	not connected
n.c.	17	not connected
D0	18	data output; bit 0 (Least Significant Bit (LSB))
D1	19	data output; bit 1

Table 3. Pin description ...continued

Symbol	Pin	Description
D2	20	data output; bit 2
D3	21	data output; bit 3
D4	22	data output; bit 4
D5	23	data output; bit 5
D6	24	data output; bit 6
D7	25	data output; bit 7 (Most Significant Bit (MSB))
IR	26	in-range data output
DGND1	27	digital ground 1
V _{CCD1}	28	digital supply voltage 1 (5 V)

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CCA}	analog supply voltage	[1]	−0.3	+7.0	V
V _{CCD}	digital supply voltage	[1]	−0.3	+7.0	V
V _{CCO}	output supply voltage	[1]	−0.3	+7.0	V
ΔV_{CC}	supply voltage difference	V _{CCA} − V _{CCD}	−1.0	+1.0	V
		V _{CCD} − V _{CCO}	−1.0	+4.0	V
		V _{CCA} − V _{CCO}	−1.0	+4.0	V
V _I	input voltage	referenced to AGND	−0.3	+7.0	V
V _{i(clk)(p-p)}	peak-to-peak clock input voltage	referenced to DGND	-	V _{CCD}	V
I _O	output current		-	10	mA
T _{stg}	storage temperature		−55	+150	°C
T _{amb}	ambient temperature		−40	+85	°C
T _j	junction temperature		-	150	°C

[1] The supply voltages V_{CCA}, V_{CCD} and V_{CCO} may have any value between −0.3 V and +7.0 V provided that the supply voltage differences ΔV_{CC} are respected.

9. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	110	K/W

10. Characteristics

Table 6. Characteristics

$V_{CCA} = V3$ to $V4 = 4.75$ V to 5.25 V; $V_{CCD} = V11$ to $V12$ and $V28$ to $V27 = 4.75$ V to 5.25 V;
 $V_{CCO} = V13$ to $V14 = 3.0$ V to 5.25 V; AGND and DGND shorted together; $T_{amb} = 0$ °C to 70 °C; typical values measured at
 $V_{CCA} = V_{CCD} = 5$ V and $V_{CCO} = 3.3$ V, $V_{I(a)(p-p)} = 2.0$ V; $C_L = 15$ pF and $T_{amb} = 25$ °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output supply voltage		3.0	3.3	5.25	V
ΔV_{CC}	supply voltage difference	$V_{CCA} - V_{CCD}$	-0.20	-	+0.20	V
		$V_{CCA} - V_{CCO}$	-0.20	-	+2.25	V
		$V_{CCD} - V_{CCO}$	-0.20	-	+2.25	V
I_{CCA}	analog supply current		-	18	24	mA
I_{CCD}	digital supply current		-	16	21	mA
I_{CCO}	output supply current	$f_{clk} = 40$ MHz; ramp input	-	1	2	mA
P_{tot}	total power dissipation	$f_{clk} = 40$ MHz; ramp input	-	175	247	mW
Inputs						
Clock input CLK (referenced to DGND) ^[1]						
V_{IL}	LOW-level input voltage		0	-	0.8	V
V_{IH}	HIGH-level input voltage		2	-	V_{CCD}	V
I_{IL}	LOW-level input current	$V_{clk} = 0.8$ V	-1	-	+1	μA
I_{IH}	HIGH-level input current	$V_{clk} = 2$ V	-	2	10	μA
Z_i	input impedance	$f_{clk} = 40$ MHz	-	2	-	kΩ
C_i	input capacitance		-	2	-	pF
$\overline{OE}$ and $\overline{TC}$ (referenced to DGND); see Table 8						
V_{IL}	LOW-level input voltage		0	-	0.8	V
V_{IH}	HIGH-level input voltage		2	-	V_{CCD}	V
I_{IL}	LOW-level input current	$V_{IL} = 0.8$ V	-1	-	-	μA
I_{IH}	HIGH-level input current	$V_{IH} = 2.0$ V	-	-	1	μA
V_I (analog input voltage referenced to AGND)						
I_{IL}	LOW-level input current	$V_I = V_{RB} = 1.3$ V	-	0	-	μA
I_{IH}	HIGH-level input current	$V_I = V_{RT} = 3.67$ V	-	35	-	μA
Z_i	input impedance	$f_i = 4.43$ MHz	-	8	-	kΩ
C_i	input capacitance		-	5	-	pF
Reference voltages for the resistor ladder; see Table 7						
V_{RB}	voltage on pin RB		1.2	1.3	2.45	V
V_{RT}	voltage on pin RT		3.2	3.67	$V_{CCA} - 0.8$	V

Table 6. Characteristics

$V_{CCA} = V3 \text{ to } V4 = 4.75 \text{ V to } 5.25 \text{ V}$; $V_{CCD} = V11 \text{ to } V12 \text{ and } V28 \text{ to } V27 = 4.75 \text{ V to } 5.25 \text{ V}$;
 $V_{CCO} = V13 \text{ to } V14 = 3.0 \text{ V to } 5.25 \text{ V}$; AGND and DGND shorted together; $T_{amb} = 0 \text{ }^{\circ}\text{C to } 70 \text{ }^{\circ}\text{C}$; typical values measured at
 $V_{CCA} = V_{CCD} = 5 \text{ V}$ and $V_{CCO} = 3.3 \text{ V}$, $V_{i(a)(p-p)} = 2.0 \text{ V}$; $C_L = 15 \text{ pF}$ and $T_{amb} = 25 \text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ref(dif)}$	differential reference voltage	$V_{RT} - V_{RB}$	2.0	2.37	3.0	V
I_{ref}	reference current	$V_{RT} - V_{RB} = 2.37 \text{ V}$	-	9.7	-	mA
R_{lad}	ladder resistance		-	245	-	Ω
TC_{Rlad}	ladder resistor temperature coefficient		-	456	-	m Ω /K
V_{offset}	offset voltage	BOTTOM; $V_{RT} - V_{RB} = 2.37 \text{ V}$	[2] -	175	-	mV
		TOP; $V_{RT} - V_{RB} = 2.37 \text{ V}$	[2] -	175	-	mV
$V_{i(a)(p-p)}$	peak-to-peak analog input voltage		[3] 1.7	2.02	2.55	V

Digital outputs D7 to D0 and IR (referenced to OGND)

V_{OL}	LOW-level output voltage	$I_{OL} = 1 \text{ mA}$	0	-	0.5	V
V_{OH}	HIGH-level output voltage	$I_{OH} = -1 \text{ mA}$	$V_{CCO} - 0.5$	-	V_{CCO}	V
I_o	output current	in 3-state mode; $0.5 \text{ V} < V_O < V_{CCO}$	-20	-	+20	μA

Switching characteristics; Clock input CLK; see Figure 4^[1]

$f_{clk(max)}$	maximum clock frequency	ADC0804S030TS	30	-	-	MHz
		ADC0804S040TS	40	-	-	MHz
		ADC0804S050TS	50	-	-	MHz
$t_{w(ck)H}$	HIGH clock pulse width	full effective bandwidth	8.5	-	-	ns
$t_{w(ck)L}$	LOW clock pulse width	full effective bandwidth	5.5	-	-	ns

Analog signal processing**Linearity**

INL	integral non-linearity	$f_{clk} = 40 \text{ MHz}$; ramp input	-	± 0.2	± 0.5	LSB
DNL	differential non-linearity	$f_{clk} = 40 \text{ MHz}$; ramp input	-	± 0.12	± 0.22	LSB
E_{offset}	offset error	middle code; $V_{RB} = 1.3 \text{ V}$; $V_{RT} = 3.67 \text{ V}$	-	± 0.25	-	LSB
E_G	gain error	from device to device; $V_{RB} = 1.3 \text{ V}$; $V_{RT} = 3.67 \text{ V}$	[4] -	± 0.1	-	%

Bandwidth ($f_{clk} = 40 \text{ MHz}$)

B	bandwidth	full-scale sine wave	[5] -	15	-	MHz
		75 % full-scale sine wave	-	20	-	MHz
		small signal at mid-scale; $V_i = \pm 10 \text{ LSB}$ at code 512	-	350	-	MHz
$t_{s(LH)}$	LOW to HIGH settling time	full-scale square wave; see Figure 6	[6] -	1.5	3.0	ns
$t_{s(HL)}$	HIGH to LOW settling time		-	1.5	3.0	ns

Table 6. Characteristics

$V_{CCA} = V3$ to $V4 = 4.75$ V to 5.25 V; $V_{CCD} = V11$ to $V12$ and $V28$ to $V27 = 4.75$ V to 5.25 V;
 $V_{CCO} = V13$ to $V14 = 3.0$ V to 5.25 V; AGND and DGND shorted together; $T_{amb} = 0$ °C to 70 °C; typical values measured at
 $V_{CCA} = V_{CCD} = 5$ V and $V_{CCO} = 3.3$ V, $V_{i(a)(p-p)} = 2.0$ V; $C_L = 15$ pF and $T_{amb} = 25$ °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Harmonics (f _{clk} = 40 MHz); see Figure 7 and 8						
α _{1H}	first harmonic level	f _i = 4.43 MHz	-	-	0	dB
α _{2H}	second harmonic level	f _i = 4.43 MHz	-	-75	-65	dB
α _{3H}	third harmonic level	f _i = 4.43 MHz	-	-72	-65	dB
THD	total harmonic distortion	f _i = 4.43 MHz	-	-65	-	dB
Signal-to-noise ratio; see Figure 7 and 8 ^[7]						
S/N	signal-to-noise ratio	full scale; without harmonics; f _{clk} = 40 MHz; f _i = 4.43 MHz	46	49	-	dB
Effective number of bits ^[7]						
ENOB	effective number of bits	ADC0804S030TS (f _{clk} = 30 MHz)				
		f _i = 4.43 MHz	-	7.8	-	bits
		f _i = 7.5 MHz	-	7.8	-	bits
		ADC0804S040TS (f _{clk} = 40 MHz)				
		f _i = 4.43 MHz	-	7.8	-	bits
		f _i = 7.5 MHz	-	7.8	-	bits
		f _i = 10 MHz	-	7.8	-	bits
		f _i = 15 MHz	-	7.4	-	bits
		ADC0804S050TS (f _{clk} = 50 MHz)				
		f _i = 4.43 MHz	-	7.8	-	bits
		f _i = 7.5 MHz	-	7.8	-	bits
		f _i = 10 MHz	-	7.8	-	bits
		f _i = 15 MHz	-	7.3	-	bits
Two-tone intermodulation ^[8]						
α _{IM}	intermodulation suppression	f _{clk} = 40 MHz	-	-69	-	dB
Bit error rate						
BER	bit error rate	f _{clk} = 40 MHz; f _i = 4.43 MHz; V _I = ±16 LSB at code 512	-	10 ⁻¹³	-	times/ samples
Differential gain ^[9]						
G _{dif}	differential gain	f _{clk} = 40 MHz; PAL modulated ramp	-	0.8	-	%

Table 6. Characteristics

$V_{CCA} = V3$ to $V4 = 4.75$ V to 5.25 V; $V_{CCD} = V11$ to $V12$ and $V28$ to $V27 = 4.75$ V to 5.25 V;
 $V_{CCO} = V13$ to $V14 = 3.0$ V to 5.25 V; AGND and DGND shorted together; $T_{amb} = 0$ °C to 70 °C; typical values measured at
 $V_{CCA} = V_{CCD} = 5$ V and $V_{CCO} = 3.3$ V, $V_{i(a)(p-p)} = 2.0$ V; $C_L = 15$ pF and $T_{amb} = 25$ °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Differential phase^[9]						
ϕ_{dif}	differential phase	$f_{clk} = 40$ MHz; PAL modulated ramp	-	0.4	-	deg
Timing ($f_{clk} = 40$ MHz; $C_i = 15$ pF); see Figure 4^[10]						
$t_{d(s)}$	sampling delay time		-	3	-	ns
$t_{h(o)}$	output hold time		4	-	-	ns
$t_{d(o)}$	output delay time	$V_{CCO} = 4.75$ V	-	10	13	ns
		$V_{CCO} = 3.15$ V	-	12	15	ns
C_L	load capacitance		-	-	15	pF
3-state output delay times; see Figure 5						
t_{dZH}	float to active HIGH delay time		-	5.5	8.5	ns
t_{dZL}	float to active LOW delay time		-	12	15	ns
t_{dHZ}	active HIGH to float delay time		-	19	24	ns
t_{dLZ}	active LOW to float delay time		-	12	15	ns

[1] In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 0.5 ns.

[2] Analog input voltages producing code 0 up to and including code 255:

- V_{offset} BOTTOM is the difference between the analog input which produces data equal to 00 and the reference voltage on pin RB (V_{RB}) at $T_{amb} = 25$ °C.
- V_{offset} TOP is the difference between the reference voltage on pin RT (V_{RT}) and the analog input which produces data outputs equal to code 255 at $T_{amb} = 25$ °C.

[3] To ensure the optimum linearity performance of such a converter architecture the lower and upper extremities of the converter reference resistor ladder are connected to pins RB and RT via offset resistors R_{OB} and R_{OT} as shown in Figure 3.

- The current flowing into the resistor ladder is $I = \frac{V_{RT} - V_{RB}}{R_{OB} + R_L + R_{OT}}$ and the full-scale input range at the converter, to cover code 0

$$\text{to 255 is } V_I = R_L \times I_L = \frac{R_L}{R_{OB} + R_L + R_{OT}} \times (V_{RT} - V_{RB}) = 0.852 \times (V_{RT} - V_{RB})$$

- Since R_L , R_{OB} and R_{OT} have similar behavior with respect to process and temperature variation, the ratio $\frac{R_L}{R_{OB} + R_L + R_{OT}}$

will be kept reasonably constant from device to device. Consequently, the variation of the output codes at a given input voltage depends mainly on the difference $V_{RT} - V_{RB}$ and its variation with temperature and supply voltage. When several ADCs are connected in parallel and fed with the same reference source, the matching between each of them is optimized.

$$[4] \quad E_G = \frac{(V_{I023} - V_0) - V_{i(p-p)}}{V_{i(p-p)}} \times 100$$

[5] The analog bandwidth is defined as the maximum input sine wave frequency which can be applied to the device. No glitches greater than 0.5 LSB, neither any significant attenuation are observed in the reconstructed signal.

[6] The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square wave signal) in order to sample the signal and obtain correct output data.

- [7] Effective bits are obtained via a Fast Fourier transform (FFT) treatment taking 8000 acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half the clock frequency (Nyquist frequency). Conversion to Signal-to-Noise-And-Distortion (SINAD) ratio: $SINAD = ENOB \times 6.02 + 1.76 \text{ dB}$.
- [8] Intermodulation measured relative to either tone with analog input frequencies of 4.43 MHz and 4.53 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full-scale to the converter.
- [9] Measurement carried out using video analyzer VM700A, where the video analog signal is reconstructed through a digital-to-analog converter.
- [10] Output data acquisition: the output data is available after the maximum delay time of $t_{d(0)}$. For 50 MHz version IDT recommend the lowest possible output load.

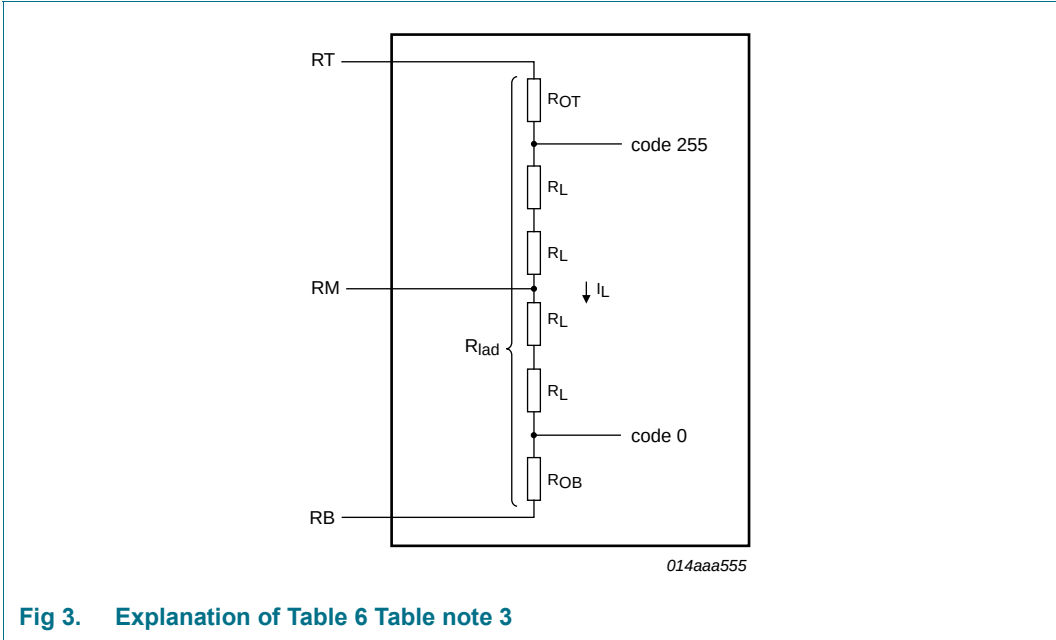


Fig 3. Explanation of Table 6 Table note 3

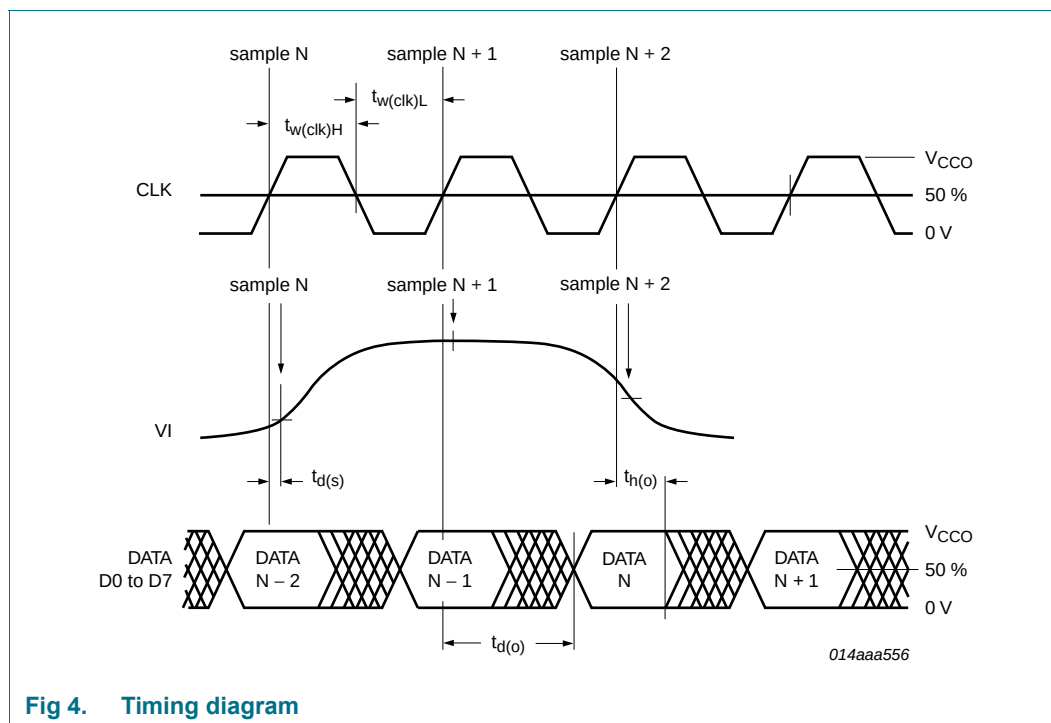
11. Additional information relating to Table 6

Table 7. Output coding and input voltage (typical values; referenced to AGND, $V_{RB} = 1.3 \text{ V}$, $V_{RT} = 3.67 \text{ V}$)

Code	$V_{i(a)(p-p)}$ (V)	IR	Binary outputs D7 to D0	Two's complement outputs D7 to D0
Underflow	< 1.475	0	0000 0000	10 0000 00
0	1.475	1	0000 0000	10 0000 00
1	-	1	0000 0001	10 0000 01
↓	-	↓	↓	↓
254	-	1	1111 1110	01 1111 10
255	3.495	1	1111 1111	01 1111 11
Overflow	> 3.495	0	1111 1111	01 1111 11

Table 8. Mode selection

TC	OE	D7 to D0	IR
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

**Fig 4. Timing diagram**

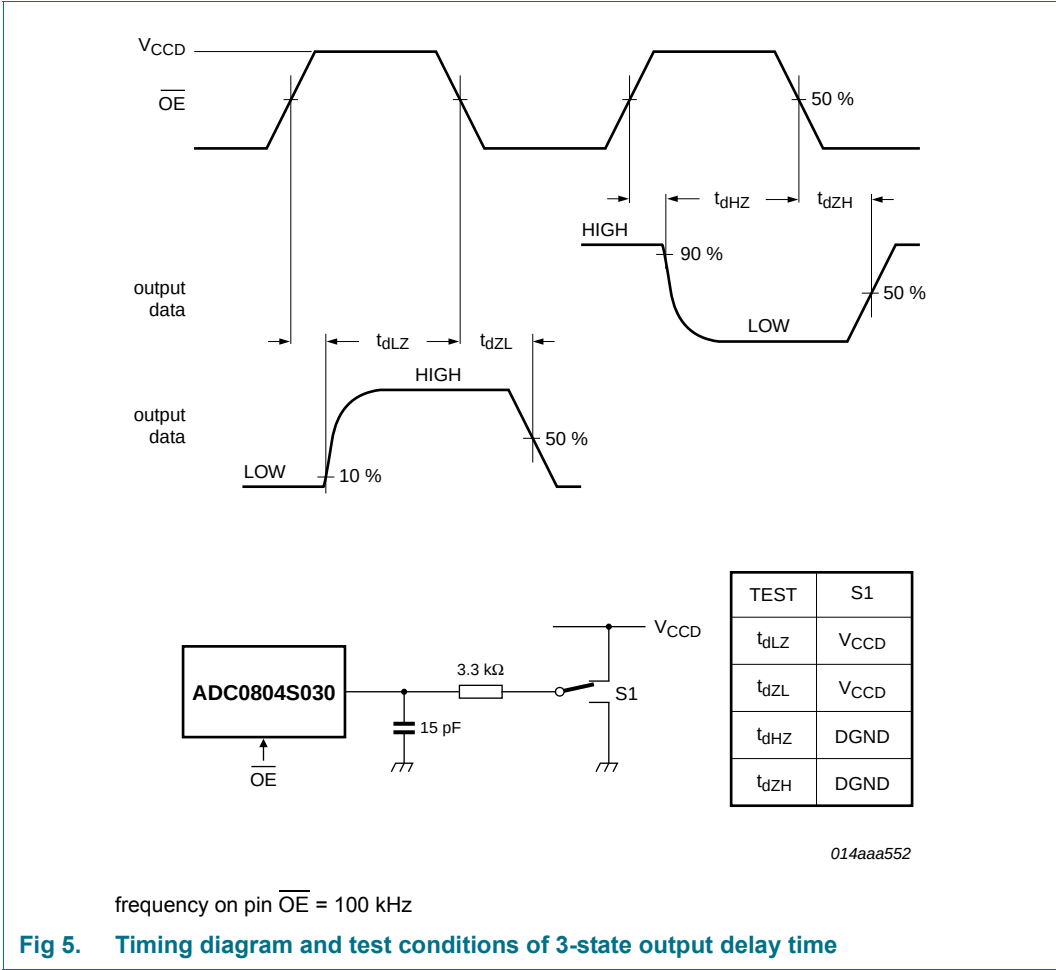


Fig 5. Timing diagram and test conditions of 3-state output delay time

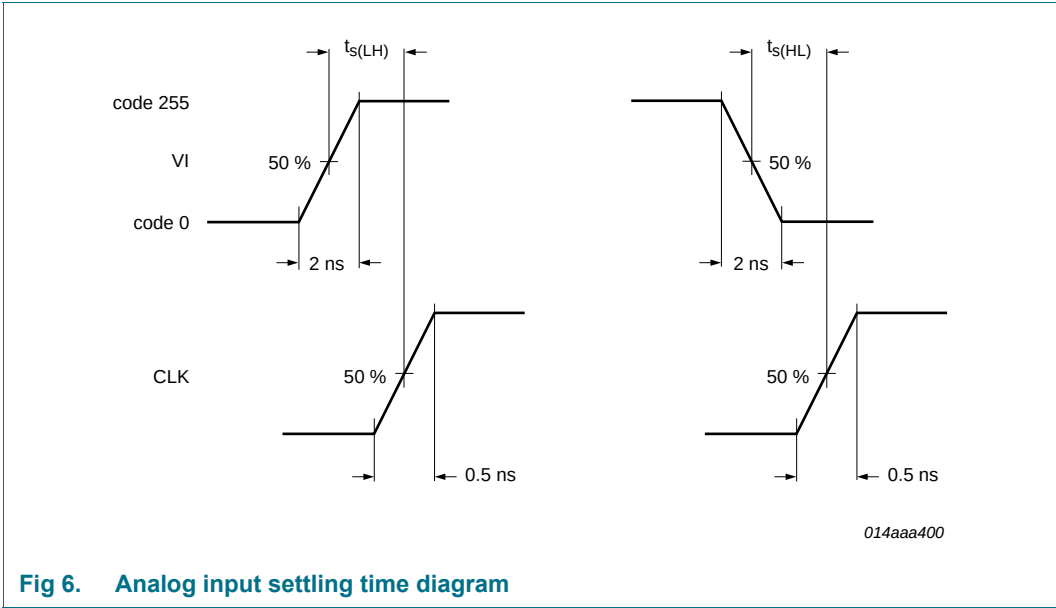
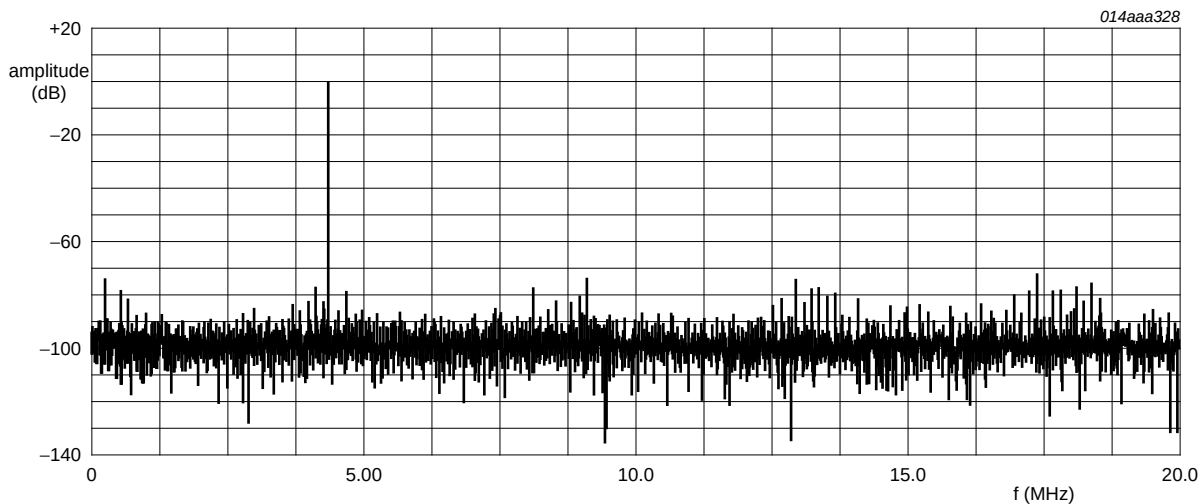


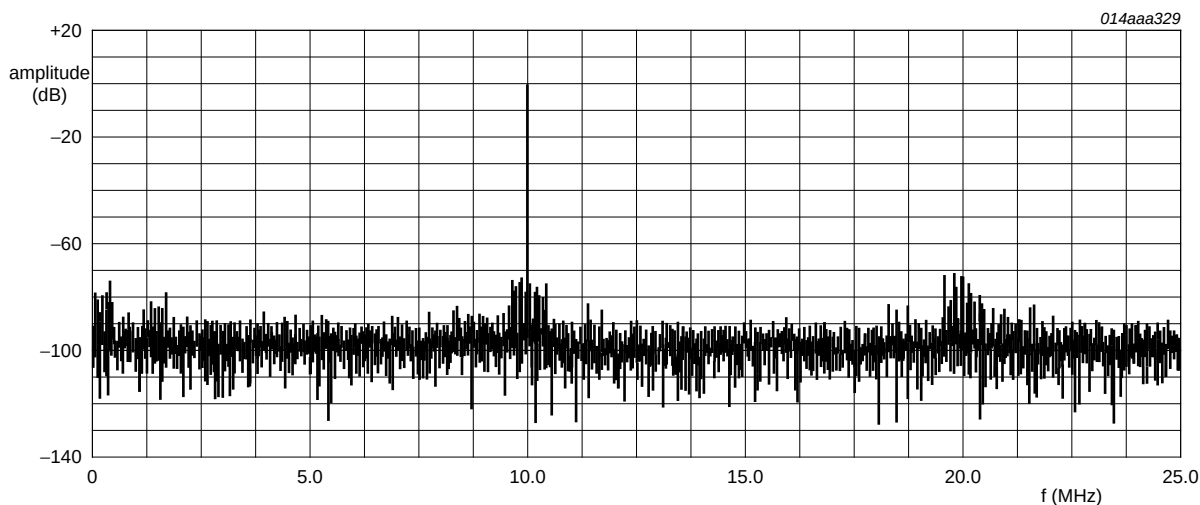
Fig 6. Analog input settling time diagram



Effective bits: 7.84; THD = -71.8 dB.

Harmonic levels (dB): 2nd = -83.19; 3rd = -78.09; 4th = -78.72; 5th = -78.33; 6th = -77.55.

Fig 7. Typical fast Fourier transform ($f_{\text{clk}} = 40 \text{ MHz}$; $f_i = 4.43 \text{ MHz}$)



Effective bits: 7.79; THD = -62.96 dB.

Harmonic levels (dB): 2nd = -71.38; 3rd = -71.54; 4th = -74.14; 5th = -65.15; 6th = -77.16.

Fig 8. Typical fast Fourier transform ($f_{\text{clk}} = 50 \text{ MHz}$; $f_i = 10 \text{ MHz}$)

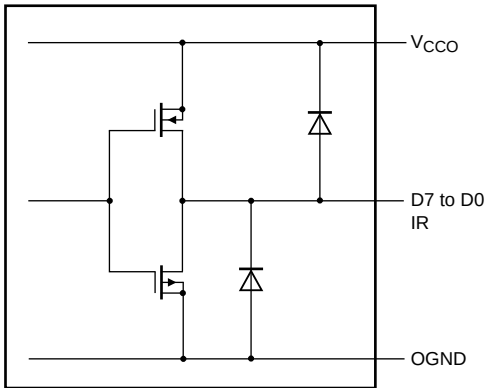


Fig 9. CMOS data and in-range outputs

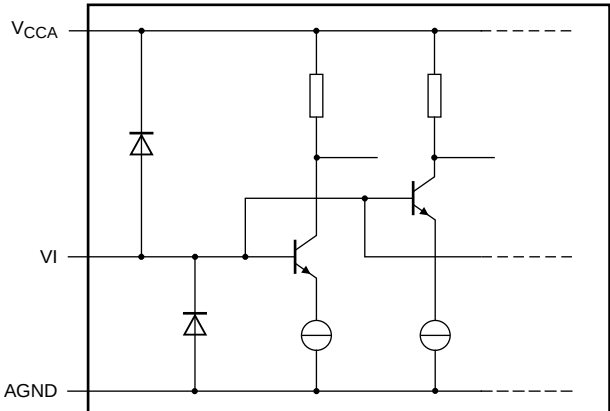


Fig 10. Analog inputs

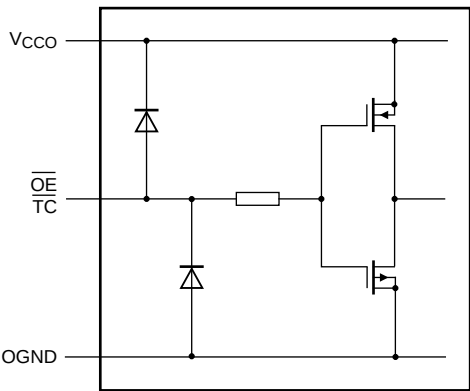


Fig 11. $\overline{OE}$ and $\overline{TC}$ input

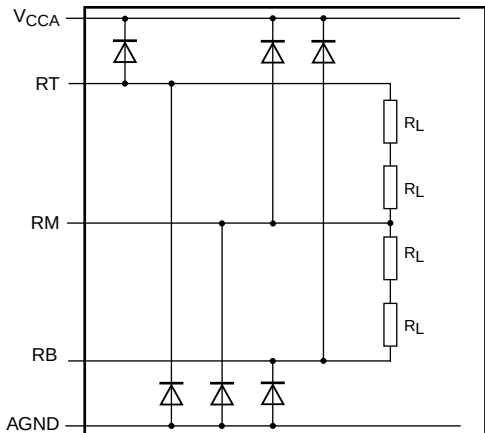


Fig 12. RB, RM and RT

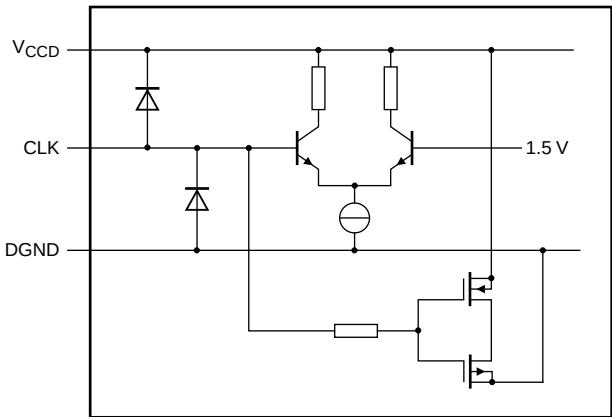
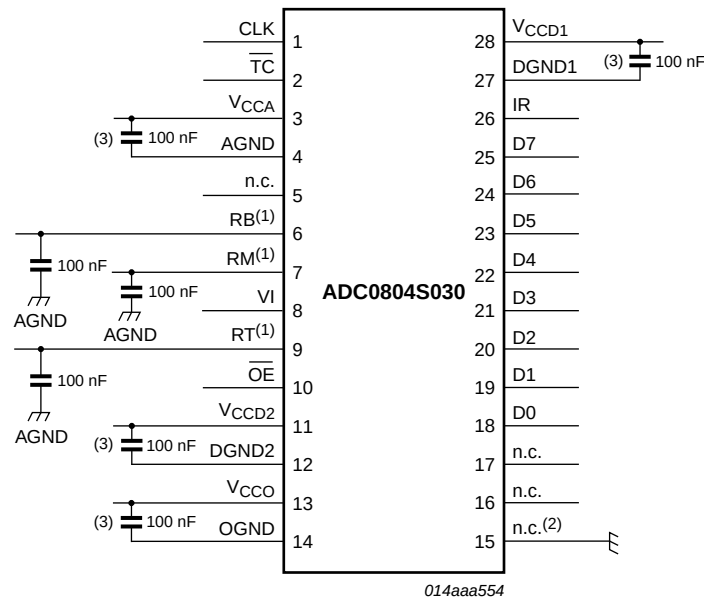


Fig 13. CLK input

12. Application information



The analog and digital supplies should be separated and well decoupled

A user manual is available that describes the demonstration board that uses the version ADC0804S030/040/050/ family with an application environment.

- (1) RB, RM and RT are decoupled to AGND.
- (2) Pin 15 may be connected to DGND in order to prevent noise influence.
- (3) Decoupling capacitor for supplies; must be placed close to the device.

Fig 14. Application diagram

12.1 Alternative parts

The following alternative parts are also available:

Table 9. Alternative parts

Type number	Description		Sampling frequency
ADC1004S030	Single 10 bits ADC	[1]	30 MHz
ADC1004S040	Single 10 bits ADC	[1]	40 MHz
ADC1004S050	Single 10 bits ADC	[1]	50 MHz
ADC1003S030	Single 10 bits ADC	[1]	30 MHz, with internal reference regulator
ADC1003S040	Single 10 bits ADC	[1]	40 MHz, with internal reference regulator
ADC1003S050	Single 10 bits ADC	[1]	50 MHz, with internal reference regulator
ADC1005S060	Single 10 bits ADC	[1]	60 MHz

[1] Pin to pin compatible

13. Package outline

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm

SOT341-1

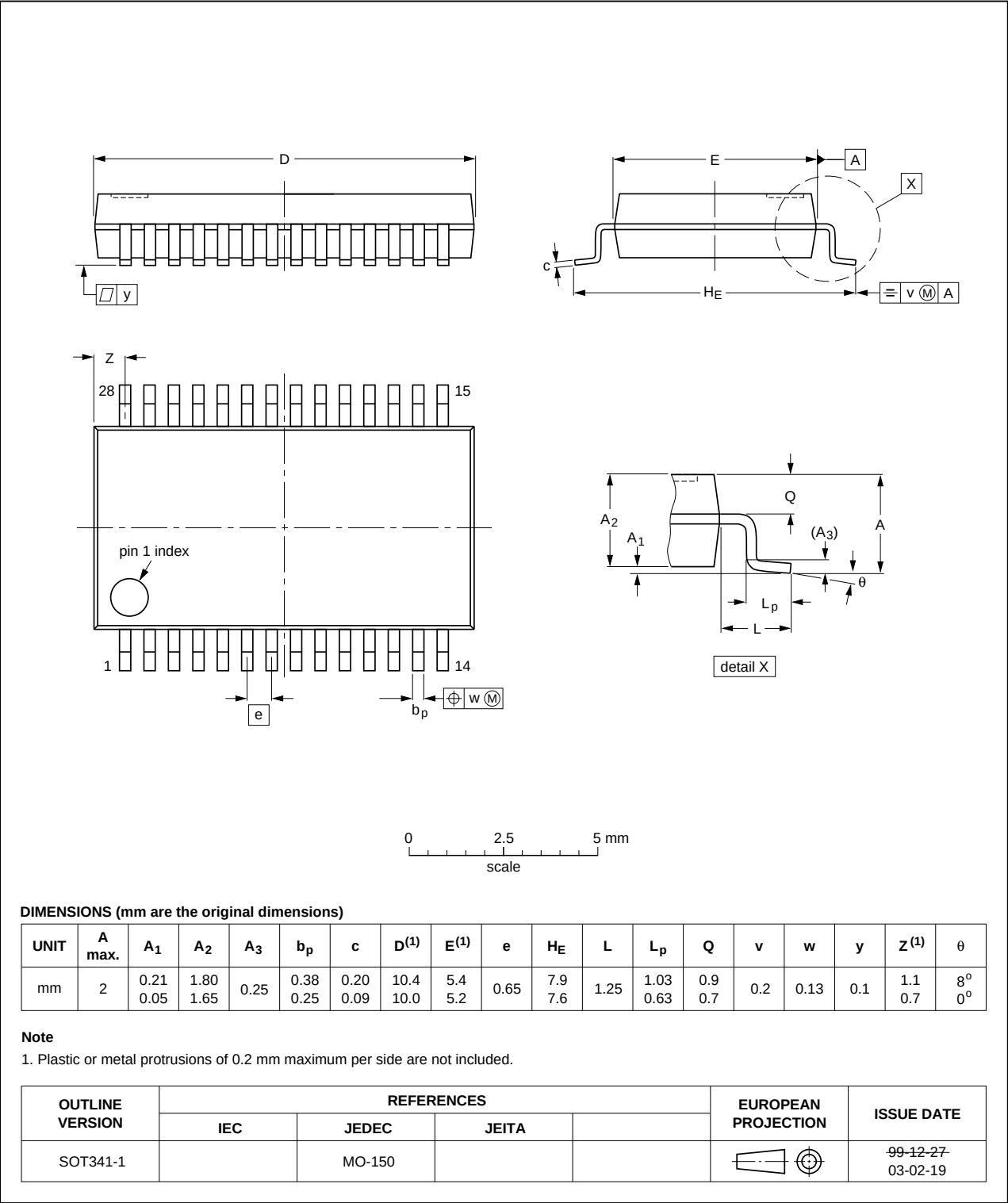


Fig 15. SOT341-1 (SSOP28)

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ADC0804S030_040_050_3	20120702	Product data sheet	-	ADC0804S030_040_050_2
ADC0804S030_040_050_2	20080814	Product data sheet	-	ADC0804S030_040_050_1
Modifications:				
• Paragraph added to Section 1. • Corrections to descriptions of rows RB and RM in Table 3. • Corrections to Table 6. • Corrections to Figure 9, 10 and 12.				
ADC0804S030_040_050_1	20080616	Product data sheet	-	-

15. Contact information

For more information or sales office addresses, please visit: <http://www.idt.com>

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