

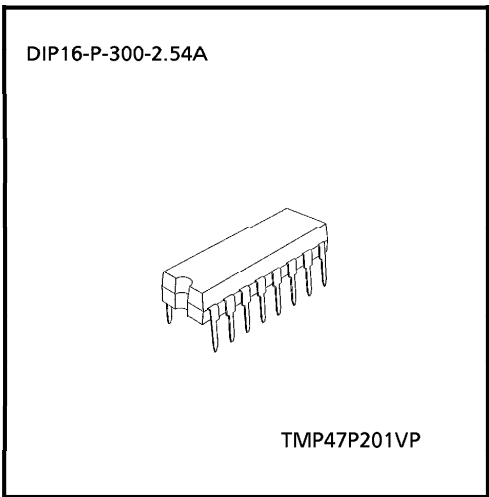
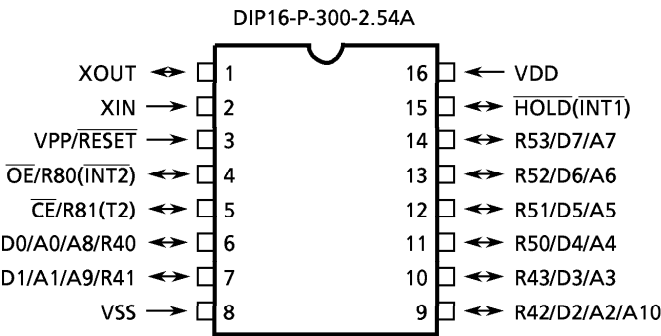
CMOS 4-BIT MICROCONTROLLER

TMP47P201VP

The 47P201V is the system evaluation LSI of 47C101/201 with 16K bits one-time PROM. The 47P201V programs / verifies using an adapter socket to connect with PROM programmer, as it is in TMM27256AD. In addition, the 47P201V and the 47C101/201 are pin compatible. The 47P201V operates as the same as the 47C101/201 by programming to the internal PROM.

| PART No.    | ROM                 | RAM         | PACKAGE           | ADAPTER SOCKET |
|-------------|---------------------|-------------|-------------------|----------------|
| TMP47P201VP | OTP<br>2048 × 8-bit | 128 × 4-bit | DIP16-P-300-2.54A | BM1187         |

PIN ASSIGNMENT (TOP VIEW)



## PIN FUNCTION

The 47P201V has MCU mode and PROM mode.

## (1) MCU mode

The 47C101/201 and the 47P201V are pin compatible.

## (2) PROM mode

| PIN NAME          | INPUT / OUTPUT | FUNCTIONS                                     | PIN NAME (MCU mode) |
|-------------------|----------------|-----------------------------------------------|---------------------|
| D0 / A0 / A8      | I/O            | Data inputs/outputs or Address inputs         | R40                 |
| D1 / A1 / A9      |                |                                               | R41                 |
| D2 / A2 / A10     |                |                                               | R42                 |
| D3 / A3           |                |                                               | R43                 |
| D4 / A4           |                |                                               | R50                 |
| D5 / A5           |                |                                               | R51                 |
| D6 / A6           |                |                                               | R52                 |
| D7 / A7           |                |                                               | R53                 |
| $\overline{OE}$   | Input          | Output Enable input                           | R80                 |
| $\overline{CE}$   |                | Chip Enable input                             | R81                 |
| VPP               | Power supply   | + 12.5 V / 5 V (Program supply voltage)       | $\overline{RESET}$  |
| VCC               |                | + 5 V                                         | VDD                 |
| VSS               |                | 0 V                                           | VSS                 |
| $\overline{HOLD}$ | Input          | PROM mode setting pin. Be fixed to low level. | $\overline{HOLD}$   |
| XIN               | Input          | Input the clock from the external oscillator. |                     |
| XOUT              | Input          | PROM control input                            |                     |

## OPERATIONAL DESCRIPTION

The following is an explanation of hardware configuration and operation in relation to the 47P201V. The 47P201V is the same as the 47C101/201 except that an OTP is used instead of a built-in mask ROM.

### 1. OPERATION mode

The 47P201V has an MCU mode and a PROM mode.

#### 1.1 MCU mode

The MCU mode is set by attaching a resonator between the XIN and XOUT pins. Operation in the MCU mode is the same as for the 47C101/201. In the 47P201V, RC oscillation is impossible.

##### 1.1.1 Program Memory

The program storage area is the same as for the 47C201. Don't use the addresses 400 to 7FF<sub>H</sub> when using the 47P101V to check 47C101 operation.

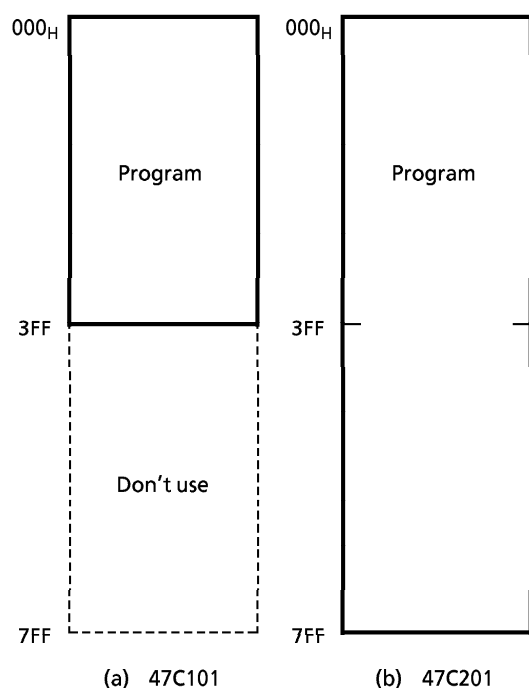


Figure 1-1. Program Area

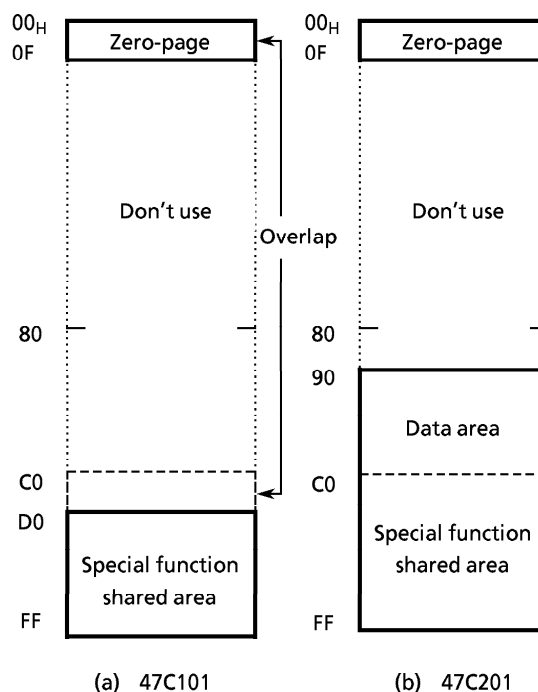


Figure 1-2. RAM Address Assignment

##### 1.1.2 Data Memory

The 47P201V has 128×4-bit of data memory (RAM). When the 47P201V is used as the 47C101/201 evaluator, programming should be performed assuming that the RAM is assigned to address 00 to 0F<sub>H</sub> and D0 to FF<sub>H</sub> for 47C101, and 00 to 0F<sub>H</sub> and 90 to FF<sub>H</sub> for 47C201 as show in Figure 1-2. When the BM4721A (emulator) is used as the 47C101/201 evaluator, it is same.

Further, zero-page (addresses 00 to 0F<sub>H</sub>) and special function shared area (stack location 0-3) are overlapped on the 47C101.

### 1.1.3 Input/Output Circuitry

(1) Control pins

This is the same as I/O code FA of the 47C101/201. In the 47P201V, RC oscillator is impossible. Connecting the resonator or inputting the external clock to XIN pin are required when using as evaluator of I/O code FD, FE.

(2) I/O Ports

The input/output circuit of the 47P201V is the same as I/O code FA or FD of the 47C101/201. External resistance, for example, is required when using as evaluator of other I/O codes (FB, FE).

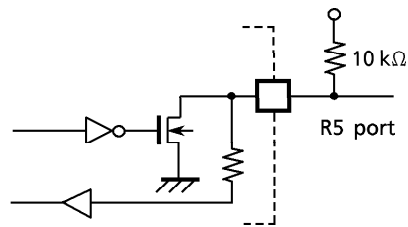


Figure 1-3. I/O code and external circuitry

## 1.2 PROM mode

The 47P201V enters PROM mode by sending external clock signal from XIN pin when XOUT pin is at low level. In PROM mode, programs can be written or verified using a general-purpose PROM writer with an adapter socket (BM1187) being attached.

With the 47P201V, the PROM address input and data input/output use the same port. PROM mode control signal (XOUT) is used for switching between two functions. XOUT pin becomes control signal input after PROM mode is completed.

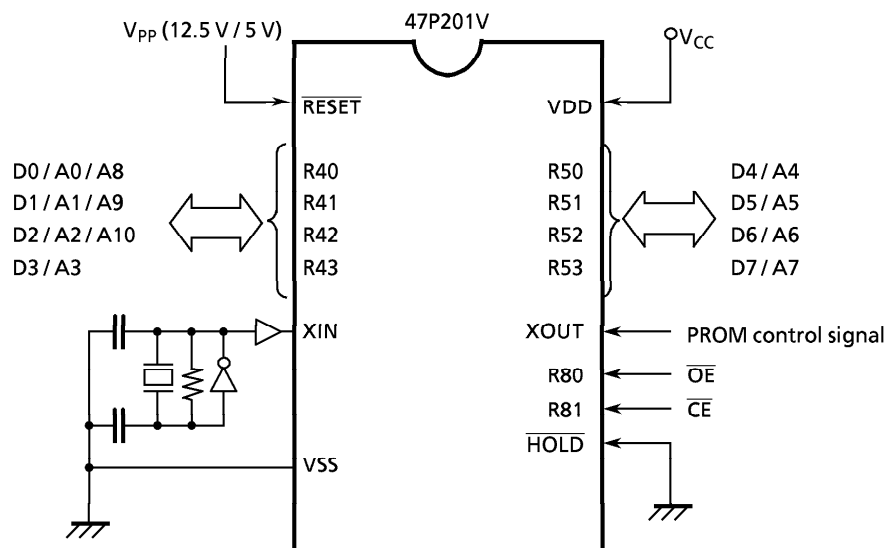


Figure 1-4. Setting for PROM mode

### 1.2.1 Program Writing

When writing a program, set a ROM type to "27256A" (programming voltage : 12.5 V) . Since the 47P201V has a 2048 × 8-bit internal PROM (000 to 7FF<sub>H</sub>) , set a stop address of a PROM writer to "7FF<sub>H</sub>" . For a general-purpose PROM writer, use the writer which does not have or can release an electric signature mode.

**Note.** When the data written to OTP is same as the data of PROM programmer, there is the possibility that the security writing can not be executed, which is depended on the types of PROM programmers.

In this case, set the data of PROM programmer to "00" and execute the security writing after writing the data to OTP.

### 1.2.2 High Speed Programming Mode

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+ 12.5 V) is applied to the  $V_{PP}$  terminal with  $V_{CC} = 6\text{ V}$  and  $\overline{CE} = V_{IH}$ .

The programming is achieved by applying a single low level 1ms pulse the  $\overline{CE}$  input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with  $V_{CC} = V_{PP} = 5\text{ V}$ .

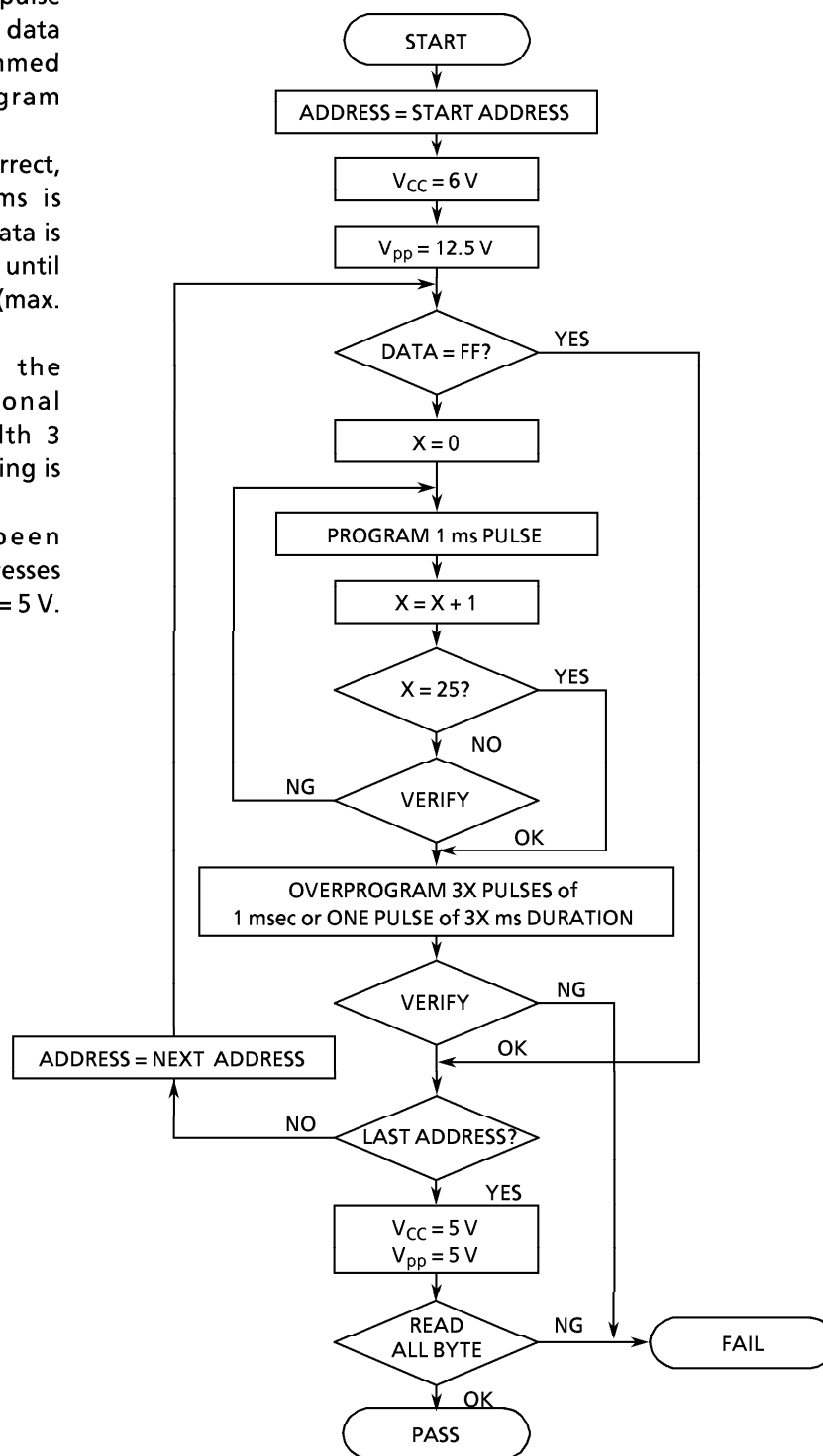


Figure 1-4. FLOW CHART

## ELECTRICAL CHARACTERISTICS

## ABSOLUTE MAXIMUM RATINGS

(V<sub>SS</sub> = 0 V)

| PARAMETER                                    | SYMBOL                   | PINS                                   | RATING                         | UNIT |
|----------------------------------------------|--------------------------|----------------------------------------|--------------------------------|------|
| Supply Voltage                               | V <sub>DD</sub>          |                                        | – 0.3 to 6.5                   | V    |
| Program Voltage                              | V <sub>PP</sub>          | RESET/VPP                              | – 0.3 to 13.0                  | V    |
| Input Voltage                                | V <sub>IN</sub>          |                                        | – 0.3 to V <sub>DD</sub> + 0.3 | V    |
| Output Voltage                               | V <sub>OUT</sub>         |                                        | – 0.3 to V <sub>DD</sub> + 0.3 | V    |
| Output Current (Per 1 pin)                   | I <sub>OUT1</sub>        | Port R4                                | 30                             | mA   |
|                                              | I <sub>OUT2</sub>        | Ports R5, R8, $\overline{\text{HOLD}}$ | 3.2                            |      |
| Output Current (Total)                       | $\Sigma I_{\text{OUT1}}$ | Port R4                                | 60                             | mA   |
| Power Dissipation [T <sub>opr</sub> = 70 °C] | PD                       |                                        | 300                            | mW   |
| Soldering Temperature (time)                 | T <sub>sld</sub>         |                                        | 260 (10 s)                     | °C   |
| Storage Temperature                          | T <sub>stg</sub>         |                                        | – 55 to 125                    | °C   |
| Operating Temperature                        | T <sub>opr</sub>         |                                        | – 30 to 70                     | °C   |

## RECOMMENDED OPERATING CONDITIONS

(V<sub>SS</sub> = 0 V, T<sub>opr</sub> = – 30 to 70 °C)

| PARAMETER          | SYMBOL           | PINS                    | CONDITIONS                     | Min.                   | Max.                   | UNIT |
|--------------------|------------------|-------------------------|--------------------------------|------------------------|------------------------|------|
| Supply Voltage     | V <sub>DD</sub>  |                         | f <sub>c</sub> = 6.0 MHz       | 4.5                    | 5.5                    | V    |
|                    |                  |                         | f <sub>c</sub> = 4.2 MHz       | 2.7                    |                        |      |
|                    |                  |                         | HOLD mode                      | 2.0                    |                        |      |
| Input High Voltage | V <sub>IH1</sub> | Except Hysteresis Input | In the normal operating area   | V <sub>DD</sub> × 0.7  | V <sub>DD</sub>        | V    |
|                    | V <sub>IH2</sub> | Hysteresis Input        |                                | V <sub>DD</sub> × 0.75 |                        |      |
|                    | V <sub>IH3</sub> |                         | In the HOLD mode               | V <sub>DD</sub> × 0.9  |                        |      |
| Input Low Voltage  | V <sub>IL1</sub> | Except Hysteresis Input | In the normal operating area   | 0                      | V <sub>DD</sub> × 0.3  | V    |
|                    | V <sub>IL2</sub> | Hysteresis Input        |                                |                        | V <sub>DD</sub> × 0.25 |      |
|                    | V <sub>IL3</sub> |                         | In the HOLD mode               |                        | V <sub>DD</sub> × 0.1  |      |
| Clock Frequency    | f <sub>c</sub>   | XIN, XOUT               | V <sub>DD</sub> = 4.5 to 5.5 V | 0.4                    | 6.0                    | MHz  |
|                    |                  |                         | V <sub>DD</sub> = 2.7 to 5.5 V |                        | 4.2                    |      |

## D.C. CHARACTERISTICS

(V<sub>SS</sub> = 0 V, T<sub>opr</sub> = – 30 to 70 °C)

| PARAMETER                                           | SYMBOL           | PINS                    | CONDITIONS                                             | Min. | Typ. | Max. | UNIT |
|-----------------------------------------------------|------------------|-------------------------|--------------------------------------------------------|------|------|------|------|
| Hysteresis Voltage                                  | V <sub>HS</sub>  | Hysteresis Input        |                                                        | –    | 0.7  | –    | V    |
| Input Current                                       | I <sub>IN1</sub> | RESET, HOLD             | V <sub>DD</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V / 0 V | –    | –    | ± 2  | μA   |
|                                                     | I <sub>IN2</sub> | Open drain output ports |                                                        |      |      |      |      |
| Input Resistance                                    | R <sub>IN</sub>  | RESET                   |                                                        | 100  | 220  | 450  | KΩ   |
| Output Leakage Current                              | I <sub>LO</sub>  | Open drain output ports | V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub> = 5.5 V      | –    | –    | 2    | μA   |
| Output Low Voltage                                  | V <sub>OL</sub>  | Except XOUT and port R4 | V <sub>DD</sub> = 4.5 V, I <sub>OL</sub> = 1.6 mA      | –    | –    | 0.4  | V    |
| Output Low Current                                  | I <sub>OL1</sub> | Port R4                 | V <sub>DD</sub> = 4.5 V, V <sub>OL</sub> = 1.0 V       | –    | 20   | –    | mA   |
| Supply Current<br>(in the Normal<br>operating mode) | I <sub>DD</sub>  |                         | V <sub>DD</sub> = 5.5 V, f <sub>c</sub> = 4 MHz        | –    | 2    | 4    | mA   |
|                                                     |                  |                         | V <sub>DD</sub> = 3.0 V, f <sub>c</sub> = 4 MHz        | –    | 1    | 2    |      |
|                                                     |                  |                         | V <sub>DD</sub> = 3.0 V, f <sub>c</sub> = 400 kHz      | –    | 0.5  | 1    |      |
| Supply Current<br>(in the HOLD<br>operating mode)   | I <sub>DDH</sub> |                         | V <sub>DD</sub> = 5.5 V                                | –    | 0.5  | 10   | μA   |

Note 1. Typ. values show those at T<sub>opr</sub> = 25 °C, V<sub>DD</sub> = 5 V.

Note 2. Input Current I<sub>IN1</sub> : The current through resistor is not included.

Note 3. Supply Current : V<sub>IN</sub> = 5.3 V / 0.2 V (V<sub>DD</sub> = 5.5 V) or 2.8 V / 0.2 V (V<sub>DD</sub> = 3.0 V)

## A.C. CHARACTERISTICS

(V<sub>SS</sub> = 0 V, T<sub>opr</sub> = – 30 to 70 °C)

| PARAMETER                    | SYMBOL           | CONDITIONS                   | Min. | Typ. | Max. | UNIT |
|------------------------------|------------------|------------------------------|------|------|------|------|
| Instruction Cycle Time       | t <sub>cy</sub>  | VDD = 4.5 to 5.5 V           | 1.3  | –    | 20   | μs   |
|                              |                  | VDD = 2.7 to 5.5 V           | 1.9  |      |      |      |
| High level Clock pulse Width | t <sub>WCH</sub> | For external clock operation | 80   | –    | –    | ns   |
| Low level Clock pulse Width  | t <sub>WCL</sub> |                              |      |      |      |      |

## RECOMMENDED OSCILLATING CONDITIONS

(V<sub>SS</sub> = 0 V, V<sub>DD</sub> = 2.7 to 5.5 V, T<sub>opr</sub> = – 30 to 70 °C)

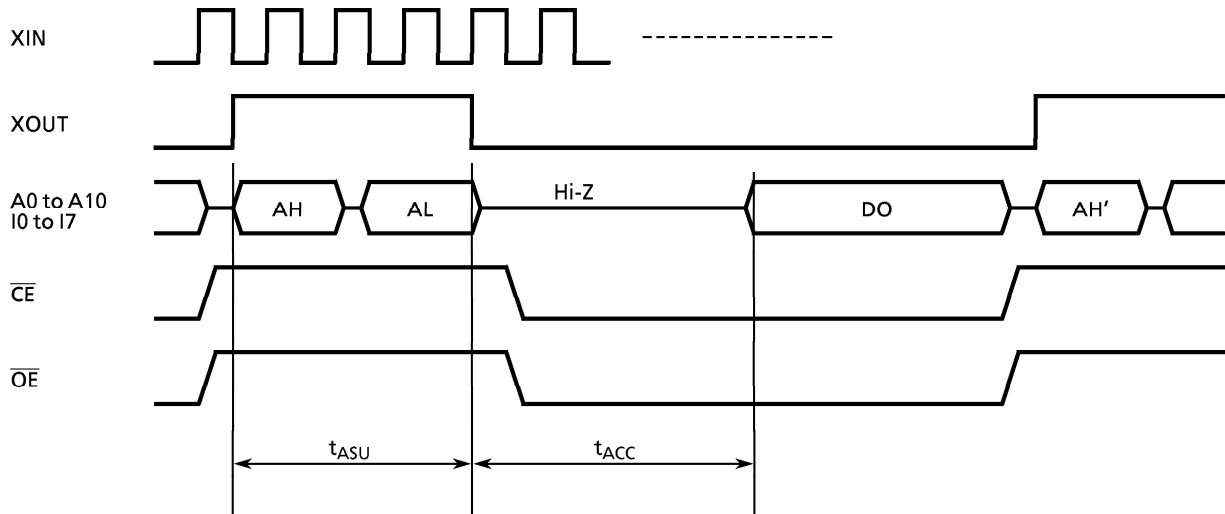
Recommended oscillating conditions of the 47P201V are equal to the 47C101/201's but RC oscillation is impossible.

## DC/AC CHARACTERISTICS

(V<sub>SS</sub> = 0 V)

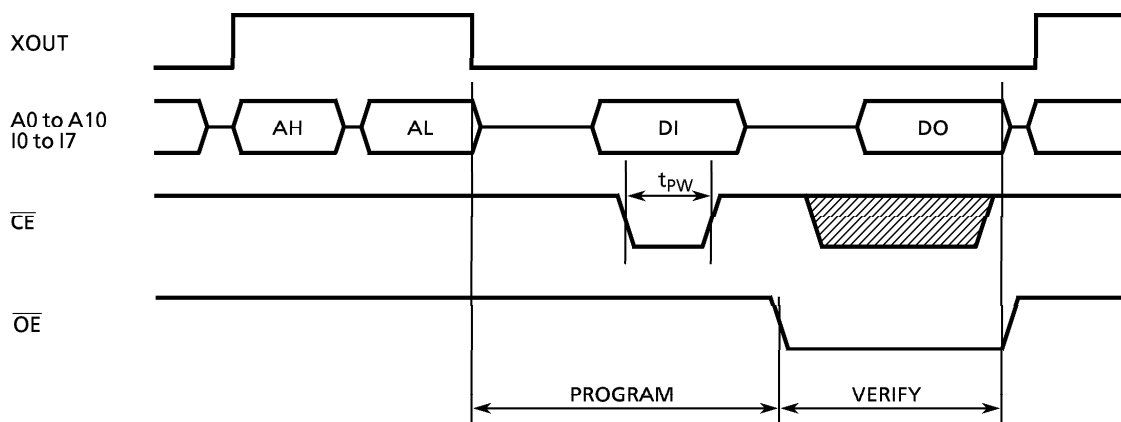
## (1) Read Operation

| PARAMETER                 | SYMBOL           | CONDITION                      | Min.                  | Typ. | Max.                  | UNIT |
|---------------------------|------------------|--------------------------------|-----------------------|------|-----------------------|------|
| Output Level High Voltage | V <sub>IH4</sub> |                                | V <sub>CC</sub> × 0.7 | –    | V <sub>CC</sub>       | V    |
| Output Level Low Voltage  | V <sub>IL4</sub> |                                | 0                     | –    | V <sub>CC</sub> × 0.3 | V    |
| Supply Voltage            | V <sub>CC</sub>  |                                | 4.75                  | –    | 6.0                   | V    |
| Programming Voltage       | V <sub>PP</sub>  |                                |                       |      |                       |      |
| Address Set-up Time       | t <sub>ASU</sub> |                                | 350                   | –    | –                     | ns   |
| Address Access Time       | t <sub>ACC</sub> | V <sub>CC</sub> = 5.0 ± 0.25 V | –                     | –    | 300                   | ns   |



## (2) High Speed Programming Operation

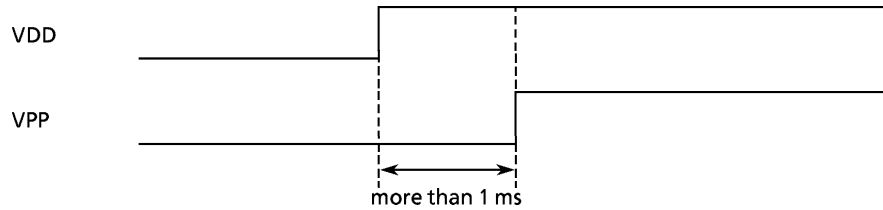
| PARAMETER                     | SYMBOL    | CONDITION                 | Min.                | Typ.  | Max.                | UNIT |
|-------------------------------|-----------|---------------------------|---------------------|-------|---------------------|------|
| Input High Voltage            | $V_{IH4}$ |                           | $V_{CC} \times 0.7$ | —     | $V_{CC}$            | V    |
| Input Low Voltage             | $V_{IL4}$ |                           | 0                   | —     | $V_{CC} \times 0.3$ | V    |
| Supply Voltage                | $V_{CC}$  |                           | 4.75                | —     | 6.0                 | V    |
| $V_{PP}$ Power Supply Voltage | $V_{PP}$  |                           | 12.00               | 12.50 | 13.00               | V    |
| Programming Pulse Width       | $t_{PW}$  | $V_{CC} = 6.0 \pm 0.25$ V | 0.95                | 1.0   | 1.05                | ms   |



(Note) DO ; Data output (I0 to I7), AL ; Address input (A0 to A7)  
 DI ; Data input (I0 to I7), AH ; Address input (A8 to A10)

*Note. There are some PROM programmer types which cannot program OTP.*

*In TMP47P201V, VPP pin is also used as RESET pin. To set a mode, REST/VPP pin must be set to "low" during 1 ms and more after the rising of power-on and the rising of VDD electrical power.*



Recommende EPROM programmer

TYPE

R4945 (ADVANTEST)

UNISITE (DATA I/O)

AF - 9706 (ANDO)

PECKER - 11 (AVAL DATA)