

## 74F164A Serial-In, Parallel-Out Shift Register

### General Description

The 74F164A is a high-speed 8-bit serial-in/parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs LOW independent of the clock. The 74F164A is a faster version of the 74F164.

### Features

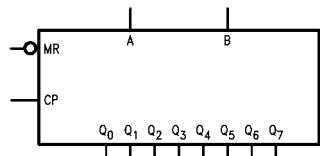
- Typical shift frequency of 90 MHz
- Asynchronous Master Reset
- Gated serial data input
- Fully synchronous data transfers
- 74F164A is a faster version of the 74F164

### Ordering Code:

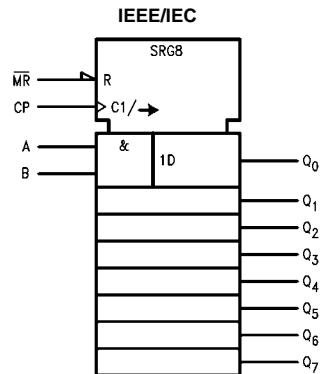
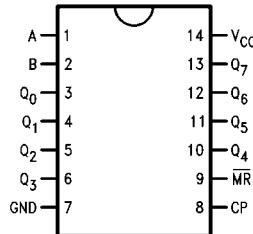
Order Number	Package Number	Package Description
74F164ASC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74F164ASJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F164APC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



## Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
A, B	Data Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/-0.6 mA
MR	Master Reset Input (Active LOW)	1.0/1.0	20 $\mu$ A/-0.6 mA
$Q_0-Q_7$	Outputs	50/33.3	-1 mA/20 mA

## Functional Description

The 74F164A is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into  $Q_0$  the logical AND of the two data inputs ( $A \cdot B$ ) that existed before the rising clock edge. A LOW level on the Master Reset ( $\overline{MR}$ ) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

## Mode Select Table

Operating Mode	Inputs		Outputs	
	$\overline{MR}$	A B	$Q_0$	$Q_1-Q_7$
Reset (Clear)	L	X X	L	L-L
Shift	H	I I	L	$q_0-q_6$
	H	I h	L	$q_0-q_6$
	H	h I	L	$q_0-q_6$
	H	h h	H	$q_0-q_6$

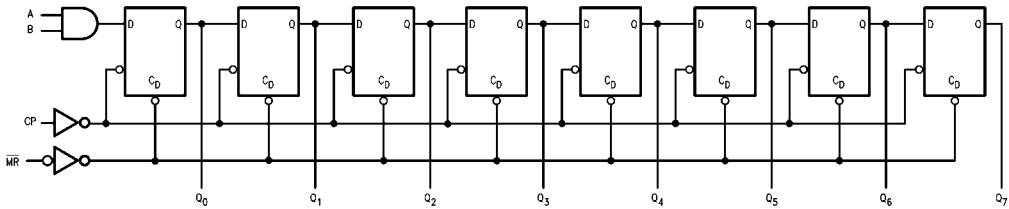
H(h) = HIGH Voltage Levels

L(l) = LOW Voltage Levels

X = Immaterial

$q_n$  = Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
$V_{CC}$ Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 1)	-0.5V to +7.0V
Input Current (Note 1)	-30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with $V_{CC} = 0V$ )	
Standard Output	-0.5V to $V_{CC}$
3-STATE Output	-0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated $I_{OL}$ (mA)
ESD Last Passing Voltage (Min)	4000V

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

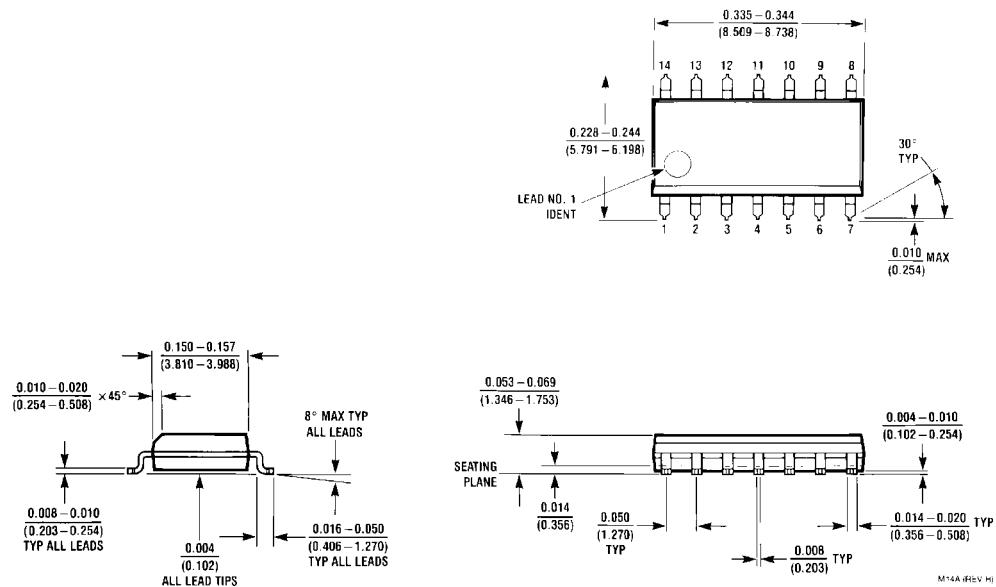
Symbol	Parameter	Min	Typ	Max	Units	$V_{CC}$	Conditions
$V_{IH}$	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
$V_{IL}$	Input LOW Voltage		0.8		V		Recognized as a LOW Signal
$V_{CD}$	Input Clamp Diode Voltage		-1.2		V	Min	$I_{IN} = -18$ mA
$V_{OH}$	Output HIGH Voltage	10% $V_{CC}$	2.5		V	Min	$I_{OH} = -1$ mA
		5% $V_{CC}$	2.7				$I_{OH} = -1$ mA
$V_{OL}$	Output LOW Voltage	10% $V_{CC}$		0.5	V	Min	$I_{OL} = 20$ mA
$I_{IH}$	Input HIGH Current			5.0	$\mu$ A	Max	$V_{IN} = 2.7V$
$I_{BVI}$	Input HIGH Current Breakdown Test			7.0	$\mu$ A	Max	$V_{IN} = 7.0V$
$I_{CEX}$	Output HIGH Leakage Current			50	$\mu$ A	Max	$V_{OUT} = V_{CC}$
$V_{ID}$	Input Leakage Test	4.75			V	0.0	$I_{ID} = 1.9$ $\mu$ A All other pins grounded
$I_{OD}$	Output Leakage Circuit Current			3.75	$\mu$ A	0.0	$V_{IOD} = 150$ mV All other pins grounded
$I_{IL}$	Input LOW Current			-0.6	mA	Max	$V_{IN} = 0.5V$
$I_{OS}$	Output Short-Circuit Current	-60		-150	mA	Max	$V_{OUT} = 0V$
$I_{CC}$	Power Supply Current		35	55	mA	Max	CP = HIGH $\overline{MR}$ = GND, A, B = GND

## AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^\circ C$ $V_{CC} = +5.0V$ $C_L = 50 pF$			$T_A = -55^\circ C$ to $+125^\circ C$ $V_{CC} = 5.0V$ $C_L = 50 pF$			$T_A = 0^\circ C$ to $+70^\circ C$ $V_{CC} = 5.0V$ $C_L = 50 pF$			Units
		Min	Typ	Max	Min	Max	Min	Max	Min	Max	
$t_{MAX}$	Maximum Clock Frequency	80	120		60		80				MHz
$t_{PLH}$	Propagation Delay CP to $Q_n$	3.0	4.8	7.5	2.5	9.0	3.0	7.5	3.5	8.0	ns
$t_{PHL}$	Propagation Delay MR to $Q_n$	3.5	5.0	8.0	3.0	8.5	3.5	8.0			
		5.0	7.0	10.0	4.0	12.5	5.0	10.5			ns

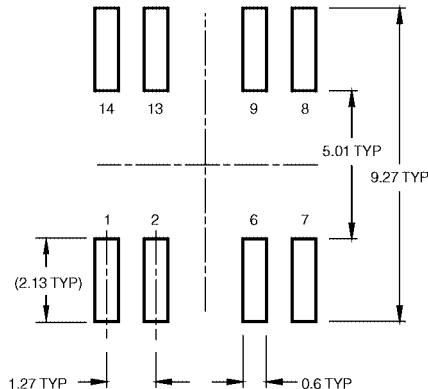
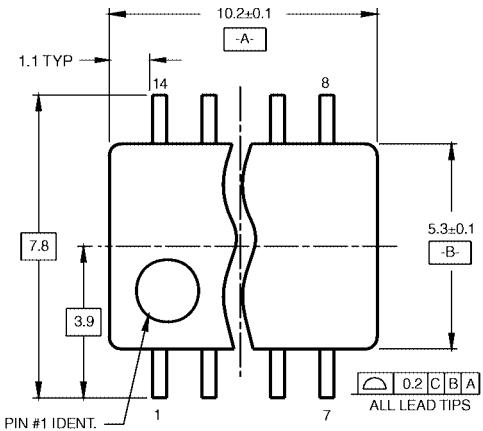
## AC Operating Requirements

Symbol	Parameter	$T_A = +25^\circ C$ $V_{CC} = +5.0V$			$T_A = -55^\circ C$ to $+125^\circ C$ $V_{CC} = 5.0V$			$T_A = 0^\circ C$ to $+70^\circ C$ $V_{CC} = 5.0V$			Units	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	4.5		5.5		4.5						
$t_S(L)$	A or B to CP	4.0		4.0		4.0						
$t_H(H)$	Hold Time, HIGH or LOW	1.0		1.0		1.0						
$t_H(L)$	A or B to CP	1.0		1.0		1.0						
$t_W(H)$	CP Pulse Width	4.0		4.0		4.0						
$t_W(L)$	HIGH or LOW	7.0		7.0		7.0						
$t_W(L)$	MR Pulse Width, LOW	4.0		5.0		4.0						
$t_{REC}$	Recovery Time MR to CP	5.0		6.5		5.0						

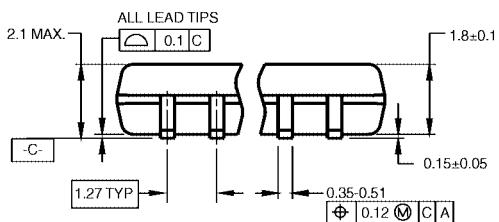
**Physical Dimensions** inches (millimeters) unless otherwise noted

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow  
Package Number M14A

## **Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



#### LAND PATTERN RECOMMENDATION

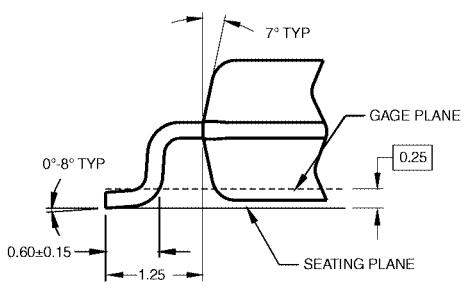
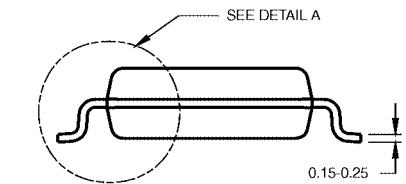


DIMENSIONS ARE IN MILLIMETERS

**NOTES:**

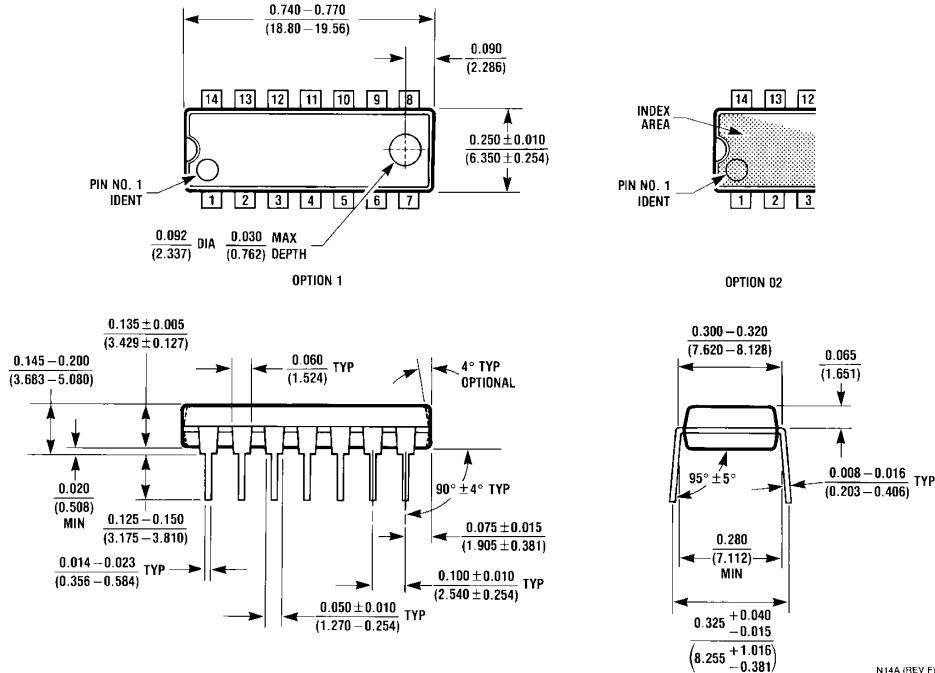
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- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1



**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M14D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide  
Package Number N14A

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