

**POWER MANAGEMENT****Description**

The SC198 is a high-efficiency, dual synchronous buck converter designed for use in low power applications. Each converter is capable of supplying up to 600mA of average current at one of eight programmable output voltages commonly used as microprocessor supply voltages.

The SC198 uses a single control logic block for the two converters, but their controls can be set independently. The SC198 employs a flexible clocking scheme that allows the user to use the fixed internal 1MHz oscillator or synchronize the clock to an external source. The device also has an optional power-save mode that optimizes efficiency for light loads.

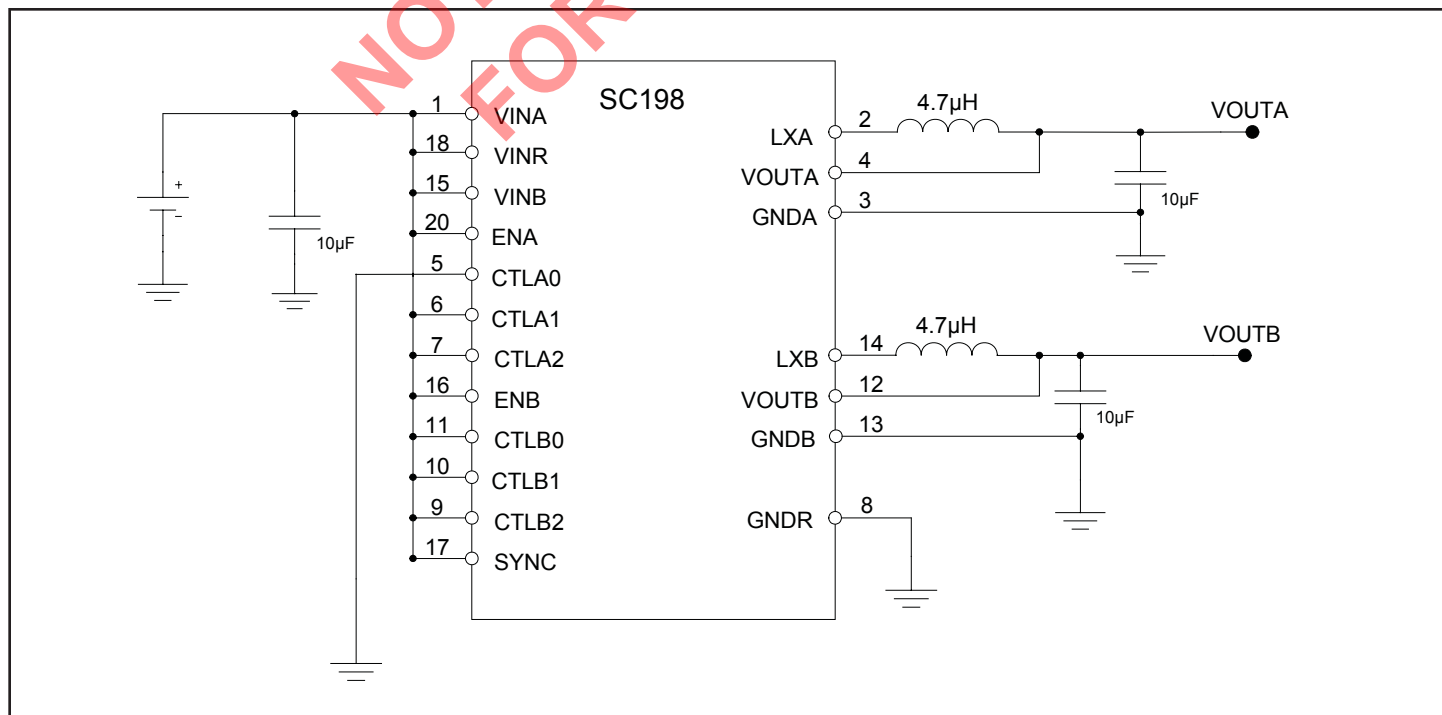
The SC198 provides output voltage flexibility while conserving board space by using control pins to select the output voltage instead of external resistor voltage divider circuits. This eliminates at least four parts from the traditional dual buck converter bill of materials.

**Features**

- ◆ Dual buck converters with independent control
- ◆ High efficiency - over 90% peak
- ◆ 8 programmable output voltages
- ◆ Input voltage range between 2.7V to 5.5V
- ◆ Fixed-frequency operation - 1MHz
- ◆ Optional SYNC clock input
- ◆ Optional power-save under light-load conditions
- ◆ Shutdown current <1 $\mu$ A
- ◆ Soft-start to limit in-rush current
- ◆ 4mm x 4mm MLPQ package

**Applications**

- ◆ Mobile phones
- ◆ Cordless phones
- ◆ MP3 players
- ◆ Digital cameras
- ◆ PDAs
- ◆ Single li-ion cell or (3) NiMH/NiCd cell devices
- ◆ Digital multimedia broadcast (DMB) devices
- ◆ Portable gaming systems

**Typical Application Circuit**

## POWER MANAGEMENT

### Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

Parameter	Symbol	Maximum	Units
VIN	$V_{IN}$	-0.3 to 7	V
EN, SYNC Input	$V_{EN}, V_{SYNC}$	-0.3 to $V_{IN} + 0.3$	V
LXA and LXB Voltages	$V_{LXA}, V_{LXB}$	-1 to $V_{IN} + 1$	V
VOUT	$V_{OUT}$	-0.3 to $V_{IN} + 0.3$	V
CTLA0, CTLA1, CTLA2, CTLB0, CTLB1 & CTLB2 Voltages		-0.3 to $V_{IN} + 0.3$	V
Output Short Circuit to GND	$t_{SC}$	Indefinite	s
LXA and LXB Currents	$I_{LXA}$ and $I_{LXB}$	1.2	A
Thermal Impedance (Junction to Ambient) <sup>(1)</sup>	$\theta_{JA}$	40	°C/W
Operating Ambient Temperature	$T_A$	-40 to +85	°C
Maximum Junction Temperature	$T_J$	150	°C
Storage Temperature	$T_S$	-65 to +150	°C
Reflow Solder Temperature	$T_{PKG}$	260	°C
ESD Protection Level <sup>(2)</sup>	$V_{ESD}$	2	kV

Note:

(1) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad as per JESD51 standards.

(2) Tested according to JEDEC standard JESD22-A114-B.

### Electrical Characteristics

Unless otherwise noted:  $V_{IN} = 3.6V$ ,  $SYNC = V_{IN}$ ,  $L = 4.7\mu H$ ,  $C = 10\mu F$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ . Typical values are at  $T_A = 25^\circ C$ .

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Range	$V_{IN}$		2.7		5.5	V
VOUT Accuracy <sup>(1)</sup>	$\Delta V_{OUT}$	$I_{OUT} = 10mA$ to $600mA$	-3		3	%
Line Regulation	$V_{LINEREG}$	$V_{IN} = 2.7$ to $5.5V$ , $V_{OUT} = 1.8V$ , $I_{OUT} = 300mA$			0.2	%/V
Load Regulation	$V_{LOADREG}$	$I_{OUT} = 10mA$ to $600mA$			0.0008	%/mA
Minimum Duty Cycle	$DC_{MIN}$				18	%
LXA, LXB Current Limit	$I_{LIM}$		0.9			A
Quiescent Current	$I_Q$	$I_{OUT} = 0mA$ , $SYNC = 0$ , $ENA$ , $ENB = V_{IN}$			50	$\mu A$
Shutdown Current	$I_{SD}$	$ENA$ , $ENB = 0$ , $LXA$ , $LXB = Open$		0.1	1	$\mu A$
LXA and LXB Leakage Current	$I_{LXA}, I_{LXB}$	$V_{IN} = 5.5V$ , $LX = 0V$ , PMOS		0.1	1	$\mu A$
		$V_{IN} = 5.5V$ , $LX = V_{IN}$ , NMOS	-2	0.1		$\mu A$

**POWER MANAGEMENT**
**Electrical Characteristics (Cont.)**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
P-Channel On Resistance	$R_{\text{DSP}}$	$I_{\text{LXA}}, I_{\text{LXB}} = 100\text{mA}$		0.35		$\Omega$
N-Channel On Resistance	$R_{\text{DSN}}$	$I_{\text{LXA}}, I_{\text{LXB}} = 100\text{mA}$		0.25		$\Omega$
Start-Up Time	$t_{\text{START}}$				5	ms
Oscillator Frequency	$f_{\text{OSC}}$		0.85	1.1	1.25	MHz
SYNC Frequency (upper)	$f_{\text{SYNCU}}$		1.25			MHz
SYNC Frequency (lower)	$f_{\text{SYNCL}}$				0.75	MHz
Thermal Shutdown	$T_{\text{HI}}$			145		$^{\circ}\text{C}$
Thermal Shutdown Hysteresis	$T_{\text{HYSR}}$			10		$^{\circ}\text{C}$
UVLO Threshold	$V_{\text{UVL}}$	Decreasing $V_{\text{IN}}$	2.4	2.5	2.6	V
UVLO Hysteresis	$V_{\text{UVLHYS}}$			50		mV
Logic Input High <sup>(2)</sup>	$V_{\text{IH}}$		1.6			V
Logic Input Low <sup>(2)</sup>	$V_{\text{IL}}$				0.6	V

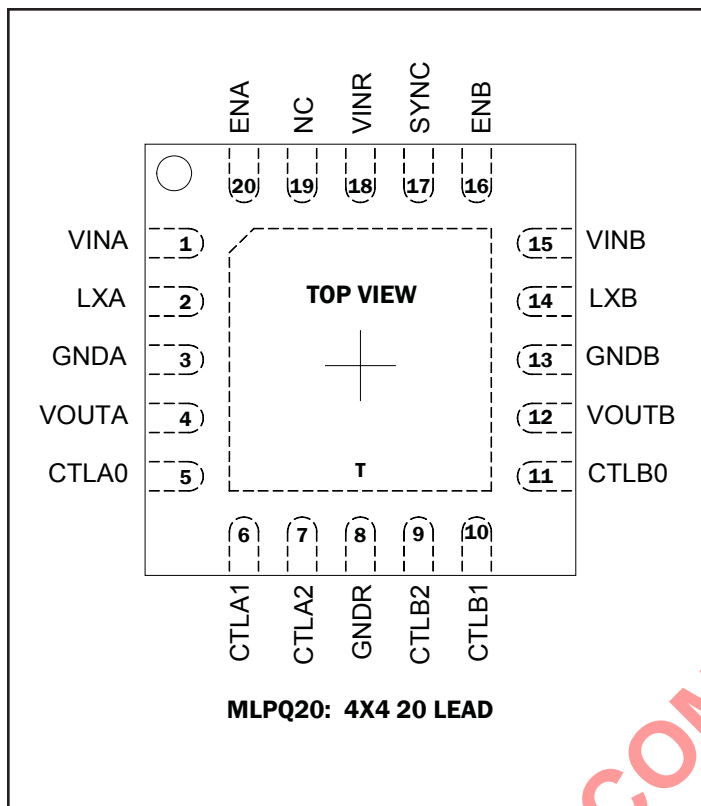
Notes:

(1) See Output Voltage Options table in the Application Information section.

(2) For ENA, ENB, SYNC, CTLA0, CTLA1, CTLA2, CTLB0, CTLB1, CTLB2.

## POWER MANAGEMENT

### Pin Configuration



### Ordering Information

DEVICE	PACKAGE
SC198MLTRT <sup>(1)(2)</sup>	MLPQ-20
SC198EVB	Evaluation Board

#### Notes:

- (1) Available in tape and reel only. A reel contains 3,000 devices.
- (2) Available in lead-free package only. Device is WEEE and RoHS compliant.

### Marking Information



## POWER MANAGEMENT

### Pin Descriptions

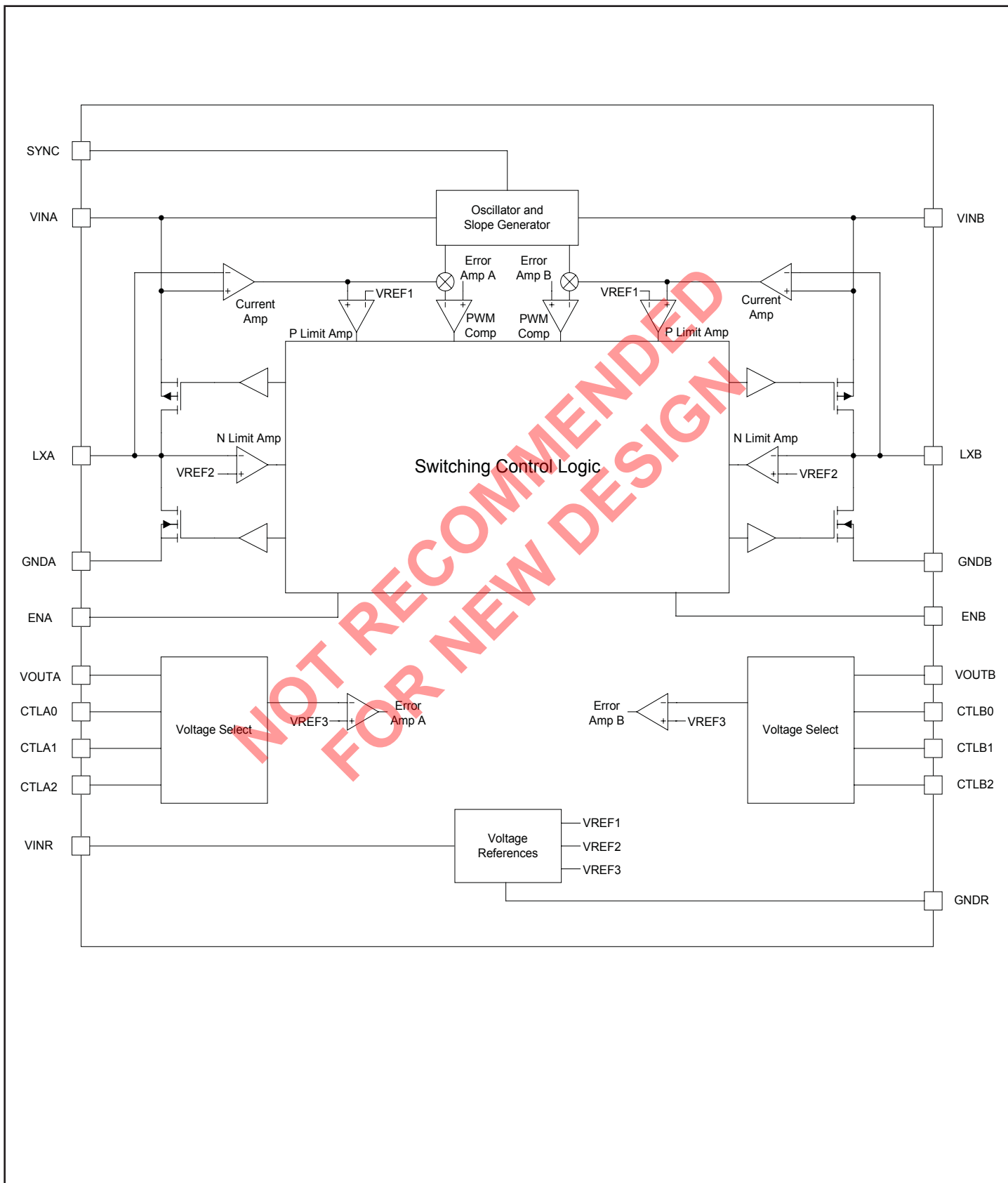
Pin #	Pin Name	Pin Function
1	VINA	Input power supply voltage converter A
2	LXA	Connection point for the inductor on converter A
3	GNDA	Ground reference to converter A
4	VOUTA	Feedback control input for converter A
5	CTLA0	Voltage select control pin 0 for output A (see Table A — Output Voltage Options). <sup>(1)</sup>
6	CTLA1	Voltage select control pin 1 for output A (see Table A — Output Voltage Options). <sup>(1)</sup>
7	CTLA2	Voltage select control pin 2 for output A (see Table A — Output Voltage Options). <sup>(1)</sup>
8	GNDR	Ground for reference supply
9	CTLB2	Voltage select control pin 2 for output B (see Table A — Output Voltage Options). <sup>(1)</sup>
10	CTLB1	Voltage select control pin 1 for output B (see Table A — Output Voltage Options). <sup>(1)</sup>
11	CTLB0	Voltage select control pin 0 for output B (see Table A — Output Voltage Options). <sup>(1)</sup>
12	VOUTB	Feedback control input for converter B
13	GNDB	Ground reference for converter B
14	LXB	Connection point for the inductor on converter B
15	VINB	Input power supply voltage for converter B
16	ENB	Enable pin for output B
17	SYNC	Oscillator synchronization input - connect to VIN for forced PWM mode, ground for power-save mode or connect to an external clock for frequency synchronization.
18	VINR	Reference supply input
19	NC	Not connected
20	ENA	Enable pin for output A
T	THERMAL PAD	Thermal pad for heatsinking purposes — connect to ground plane using multiple vias — not connected internally

Note:

(1) All CTL pins must be pulled high or low for proper operation.

## POWER MANAGEMENT

### Block Diagram



## POWER MANAGEMENT

### Applications Information

#### SC198 Detailed Description

The SC198 is a dual step-down, pulse-width modulated DC-DC converter with programmable output voltage and power-save mode. This device has a 1MHz internal oscillator that can be used during forced PWM mode or power-save mode (PSAVE).

#### Operation

During normal operation, the PMOS switch is activated on each rising edge of the internal oscillator. Current feedback for the switching regulator is through the PMOS current path, and it is amplified and summed with the internal slope compensation network. The voltage feedback loop uses an internal feedback divider. The on-time is determined by comparing the summed current feedback and the output of the error amplifier. The period is set by the onboard oscillator or by an external clock attached to the SYNC/PWM pin. When synchronizing to an external frequency, the SC198 operates in PWM mode only. The device has an internal synchronous NMOS rectifier and does not require a Schottky diode on the LX pin. The device is designed to operate as a buck converter in PWM mode with a fixed frequency of 1MHz. At light loads the part can enter PSAVE mode to maximize efficiency.

#### Output Filter

The SC198 converter also has internal loop compensation. The internal compensation is designed to work with a certain output filter corner frequency defined by the equation:

$$f_c = \frac{1}{2\pi\sqrt{L \times C}}$$

When selecting output filter components, the LC product should not vary over a wide range. Selection of smaller inductor and capacitor values will move the corner frequency, potentially impacting system stability. Due to this issue the practical lower limit for the inductor value is 4.7μH. The internal compensation is designed to operate with a single-pole output filter,  $L = 4.7\mu\text{H}$  and  $C_{\text{OUT}} = 10\mu\text{F}$ .

#### Programmable Output Voltage

The SC198 has three control pins per output to allow the user to select a voltage level from eight predetermined output voltage levels (see Table A, Output Voltage Options below). The output voltage can be selected at any time, including while the output is enabled and loaded.

Table A – Output Voltage Options

Programmable Output Voltage			
CTLA2/B2	CTLA1/B1	CTLA0/B0	Nominal Output Voltage (V)
0	0	0	1
0	0	1	1.2
0	1	0	1.375
0	1	1	1.4
1	0	0	1.5
1	0	1	1.575
1	1	0	1.8
1	1	1	1.875

#### Continuous Conduction and Oscillator Synchronization

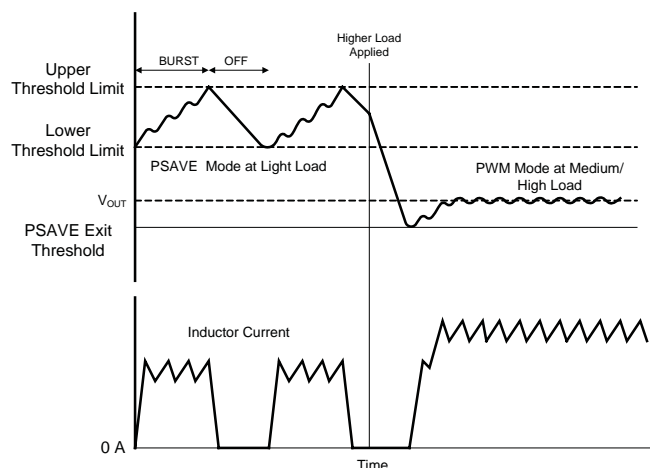
The SC198 is designed to operate in a continuous conduction mode, where it maintains a fixed frequency. When the SYNC pin is tied high, the part runs under control of the internal oscillator in PWM mode. The part can be synchronized to an external clock by connecting a clock signal to the SYNC pin. The part synchronizes to the rising edge of the clock.

#### Power-Save Mode Operation

The SC198 has a power-save mode (PSAVE) which may be selected by tying the SYNC pin to GND. Selecting PSAVE mode enables automatic activation of PSAVE mode at light loads, thus maximizing efficiency across the full load range. The SC198 will automatically detect the load current at which it should enter PSAVE mode. The SC198 is optimized to track maximum efficiency with respect to  $V_{\text{IN}}$ .

## POWER MANAGEMENT

### Applications Information (Cont.)



#### PSAVE Operation

In PSAVE mode,  $V_{OUT}$  regulation is controlled by bursts in switching. While the output voltage is between the low and high voltage thresholds, switching is stopped to reduce loss in the regulator due to switching. When the voltage drops to the lower threshold, the switch bursts at a fixed on time until the upper threshold is met. At this point the output voltage is allowed to ramp down to the lower threshold again without switching to conserve power. In the PSAVE mode, less switching is used. Less switching results in less power loss which can be seen in the difference of efficiency between PWM mode and PSAVE mode at light loads.

The PSAVE switching burst frequency is controlled such that the inductor current ripple during the burst is similar to that in PWM mode. The minimum switching frequency during this period is limited to 650kHz.

The SC198 automatically detects when to exit PSAVE mode. The device sets a maximum peak current in PSAVE mode, and then detects when  $V_{OUT}$  falls due to the load increasing above the level that the peak current will support.

For the SC198 to exit PSAVE mode, the load must be increased, which causes  $V_{OUT}$  to decrease until the PSAVE exit threshold is reached. PSAVE levels are set high to minimize the undershoot when the SC198 exits PSAVE.

#### Protection Features

The SC198 provides the following protection features:

- Thermal Shutdown
- Current Limit
- Over-Voltage Protection
- Soft-Start

#### Thermal Shutdown

The device has a thermal shutdown feature to protect the SC198 if the junction temperature exceeds 145°C. In thermal shutdown the on-chip power devices are disabled, tri-stating the LX output. Switching will resume when the temperature drops by 10°C. During this time if the output voltage decreases by more than 60% of its programmed value, a soft-start will be invoked.

#### Current Limit

The PMOS and NMOS power devices of the buck switcher stage are protected by current limit functions. In the case of a short to ground on the output, the part enters frequency foldback mode, that causes the switching frequency to divide by a factor determined by the output voltage. This prevents the inductor current from "staircasing".

#### Over-Voltage Protection

Over-voltage protection is provided on the SC198. Hysteresis is provided to prevent toggling in and out of operation.

#### Soft-Start

The soft-start mode operates by limiting the current through the inductor and controlling the switching frequency. The current limit is increased over several milliseconds in discrete steps. This has the desired effect of limiting in-rush current from the input supply. The soft-start mode is cancelled once the output reaches regulation. Soft-start is only re-enabled by power cycling, toggling enable, UVLO event, or shutdown.



## POWER MANAGEMENT

### Applications Information (Cont.)

#### Inductor Selection

The SC198 was designed for optimum performance when using a 4.7μH inductor. The magnitude of the inductor current ripple is dependent on the inductor value and can be determined by the following equation:

$$\Delta I_L = \frac{V_{OUT}}{L \times f_{OSC}} \left( 1 + \frac{V_{OUT}}{V_{IN}} \right)$$

This equation demonstrates the relationship between input voltage, output voltage, and inductor ripple current. The inductor should also have a low DCR to minimize the conduction losses and maximize efficiency. The minimum DC current rating of the inductor should be equal to the maximum load current plus half of the inductor current ripple as shown by the following equation:

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

Final inductor selection will depend on various design considerations such as efficiency, EMI, size and cost. Table B lists some manufacturers of practical inductor options.

#### Capacitor Selection

##### Input Capacitor

The source input current to a buck converter is non-continuous. To prevent large input voltage ripple a low ESR ceramic capacitor is required. A minimum value of 4.7μF should be used for sufficient input voltage filtering and a 22μF MLCC may be used for optimum input voltage filtering.

##### Output Capacitor

A 4.7μF ceramic capacitor is the minimum recommended for the output filter capacitor. A capacitor value of at least 10μF is recommended if the part will be used in power-save mode. Output voltage ripple is dominated by the filter capacitance ESR as shown in the following equation:

$$V_{OUT(P-P)} = \Delta I_L \times ESR_{COUT}$$

Capacitors with X7R or X5R ceramic dielectric are strongly recommended for their low ESR and superior temperature and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them unsuitable for this application. Table C lists some manufacturers of recommended capacitor options.

## POWER MANAGEMENT

### Applications Information (Cont.)

**Table B — Recommended Inductors**

Manufacturer	Part Number	Value $\mu\text{H}$	DCR $\Omega$	Rated Current A	Tolerance %	Dimensions (L×W×H) mm
Coilcraft	LPO6610-472ML <sup>(1)</sup>	4.7	0.20	1.1	±20	6.60 × 5.50 × 1.10
	1812PS-472KLB	4.7	0.11	2.10	±20	5.87 × 4.89 × 3.81
TDK	VLCF4020T-4R7N1R2	4.7	0.098	1.0	±30	4 × 4 × 2
BI Technologies	HM66-304R7LF	4.7	0.072	1.32	±20	4.7 × 4.7 × 3.0

Note:

(1) This inductor was used while obtaining data for the Typical Characteristics Section.

**Table C — Recommended Capacitors**

Manufacturer	Part Number	Value $\mu\text{F}$	Rated Voltage VDC	Type	Case Size
Murata	GRM21BR60J226ME39	22	6.3	X5R	0805
	GRM188R60J106ME47	10	6.3	X5R	0603
	GRM188R60J475KE19	4.7	6.3	X5R	0603
AVX	08056D107MAT2A	10	6.3	X5R	0805

## POWER MANAGEMENT

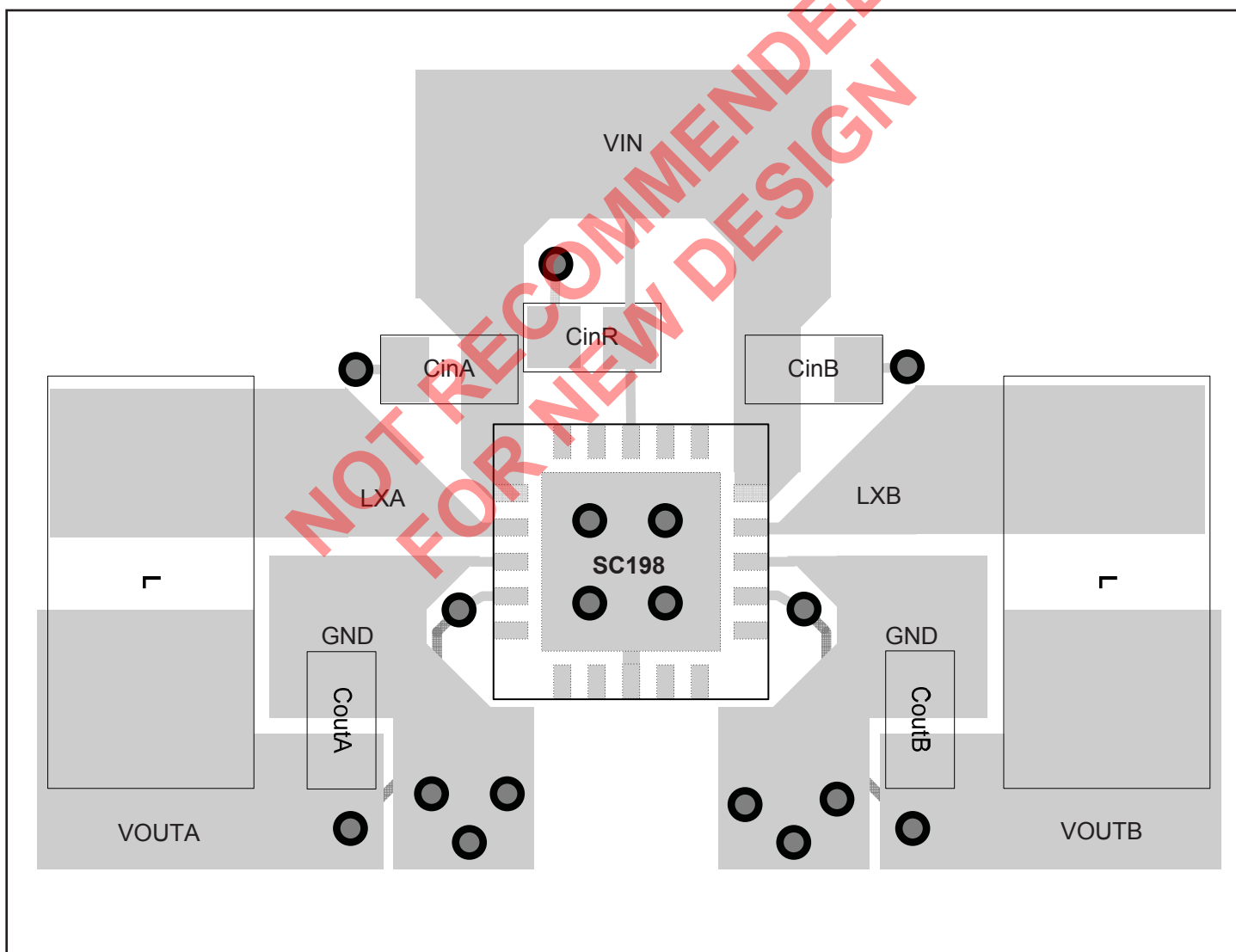
### Applications Information (Cont.)

#### PCB Layout Considerations

Poor layout can degrade the performance of the DC-DC converter and can be a contributory factor in EMI problems, ground bounce, thermal issues, and resistive voltage losses. Poor regulation and instability can result.

The following design rules are recommended:

1. Place the inductor and filter capacitors as close to the device as possible and use short wide traces between the power components.
2. Route the output voltage feedback path away from inductor and LX node to minimize noise and magnetic interference.
3. Use a ground plane to further reduce noise interference on sensitive circuit nodes.

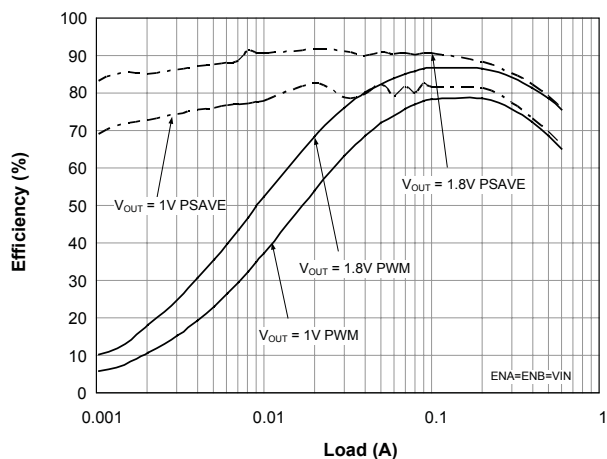


Note:  
Control pin routings are not shown.

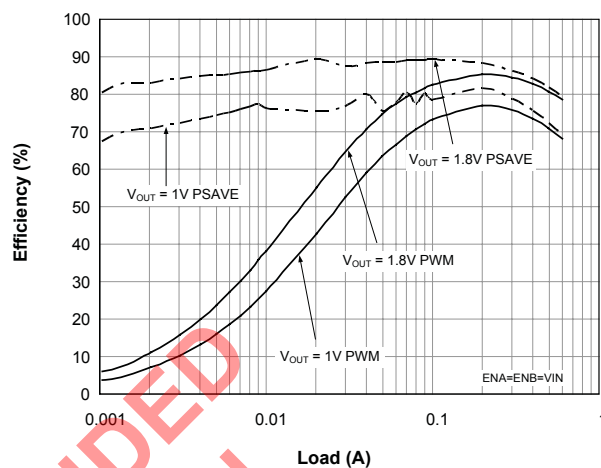
## POWER MANAGEMENT

### Typical Characteristics

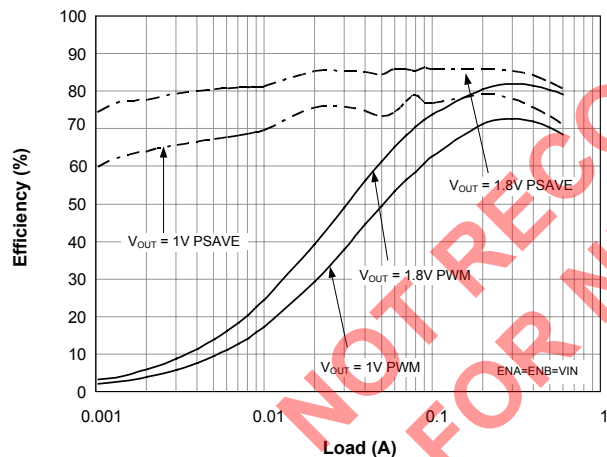
Efficiency vs. Load @ 2.7V<sub>IN</sub>



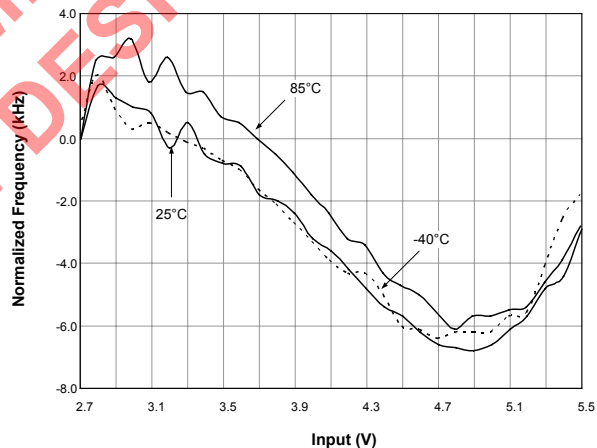
Efficiency vs. Load @ 3.6V<sub>IN</sub>



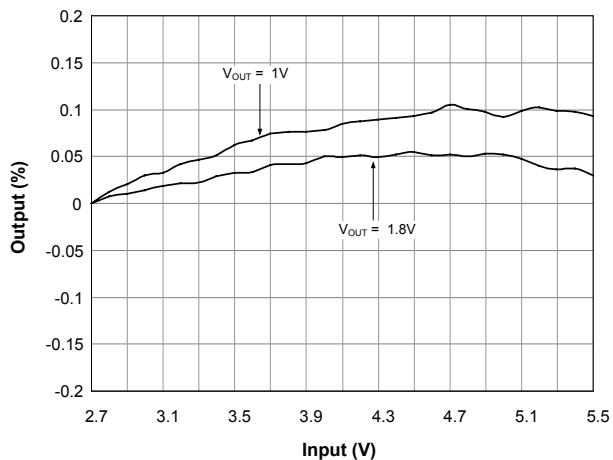
Efficiency vs. Load @ 5.5V<sub>IN</sub>



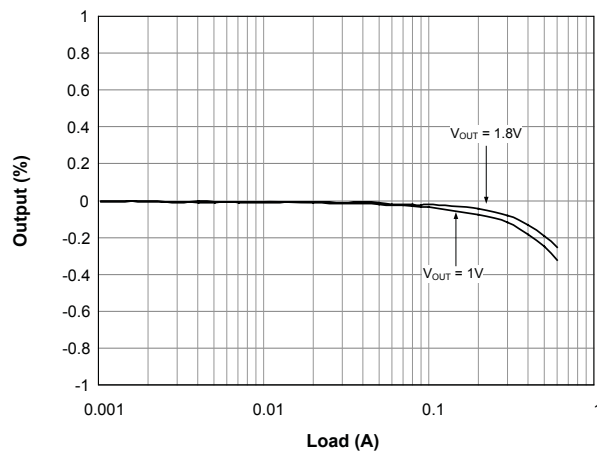
Oscillator Frequency vs. Input Voltage

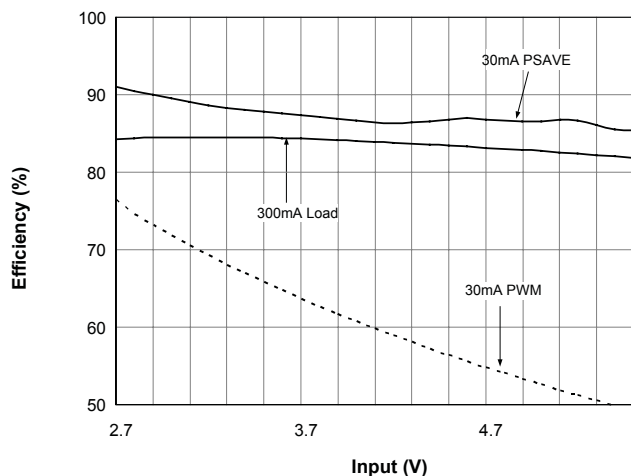
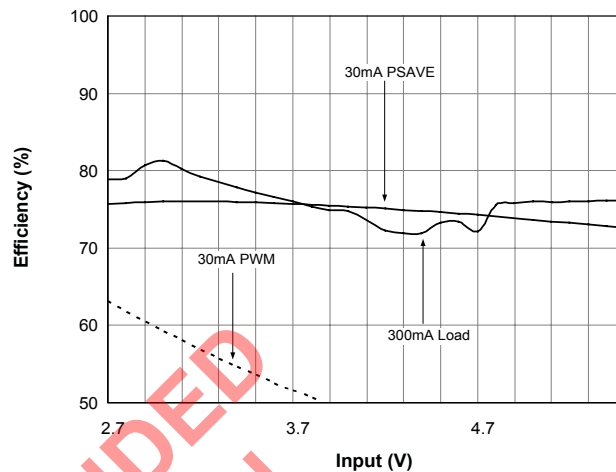
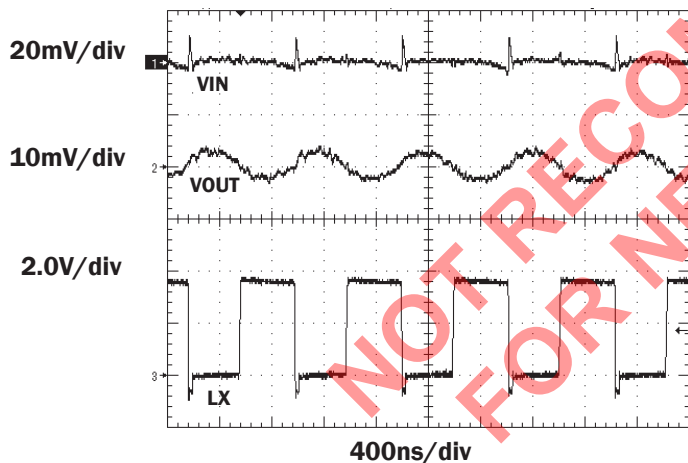
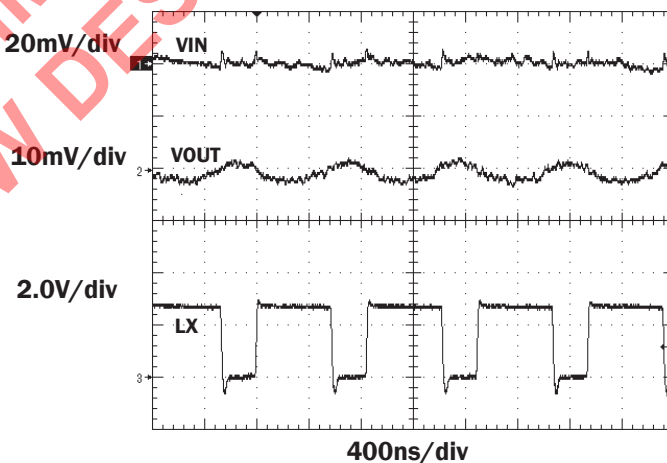
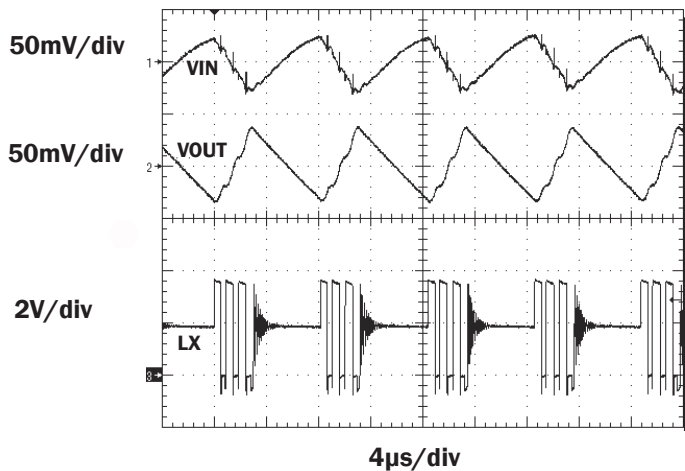
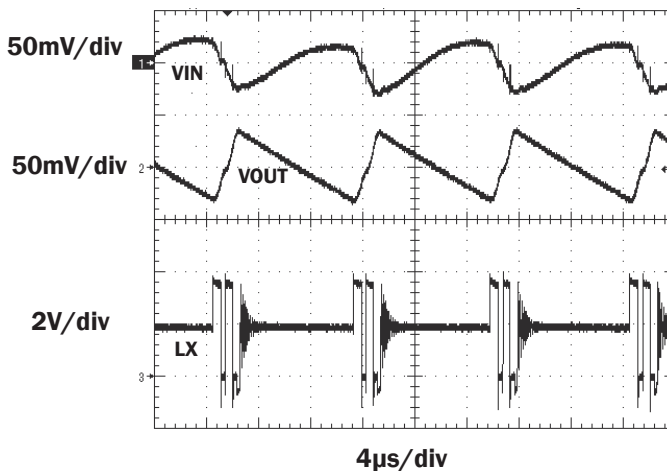


Line Regulation at 300mA<sub>OUT</sub>



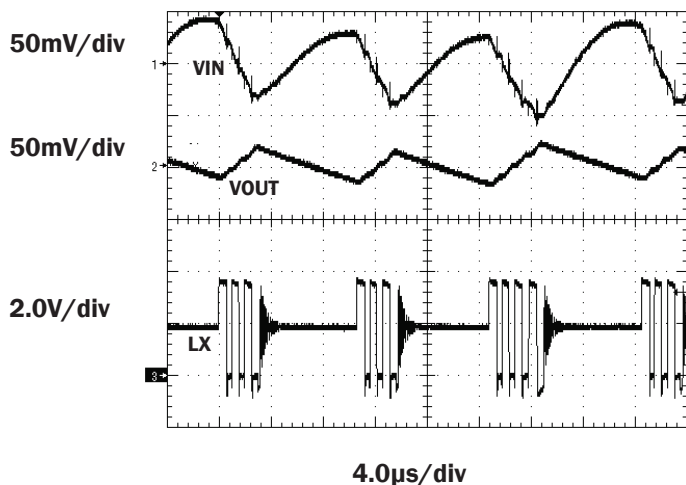
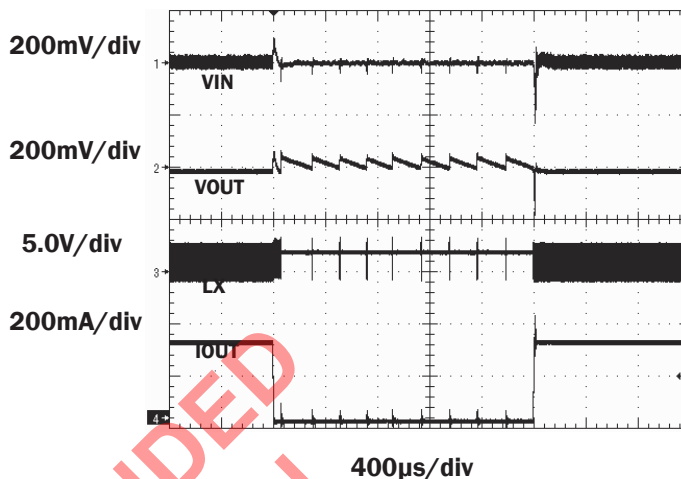
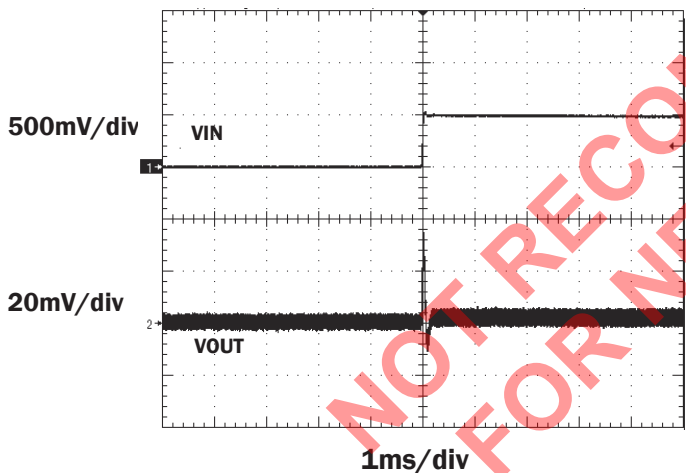
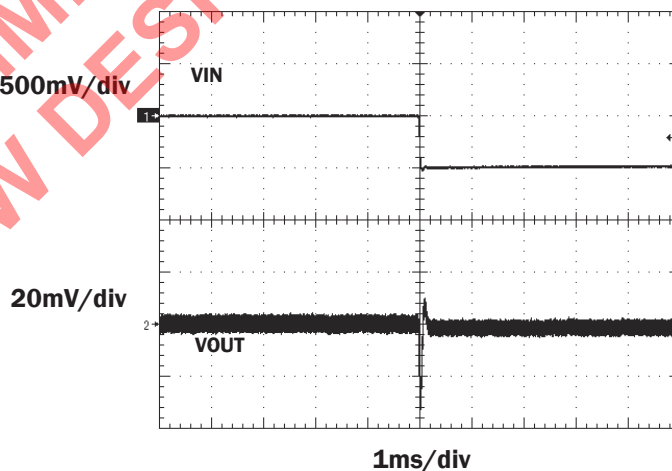
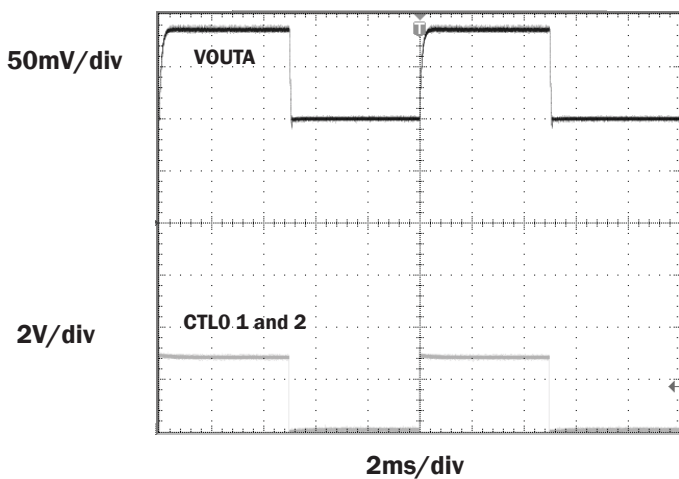
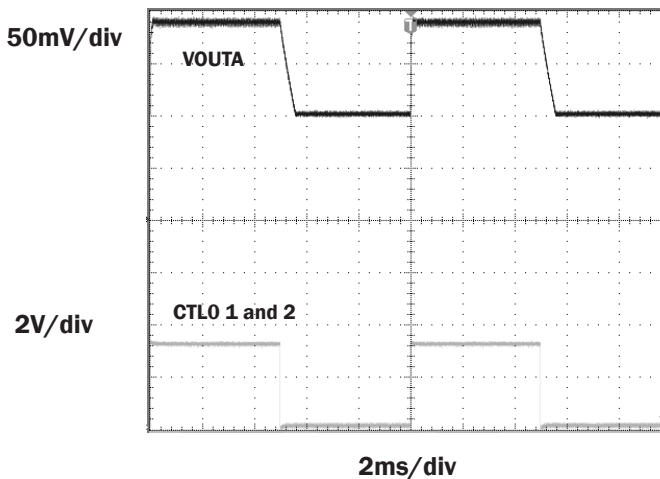
Load Regulation at 3.6V<sub>IN</sub> (PWM)



**POWER MANAGEMENT**
**Typical Characteristics (Cont.)**
**Efficiency vs. Line @  $V_{OUT} = 1.8V$** 

**Efficiency vs. Line @  $V_{OUT} = 1V$** 

**Output Ripple for  $V_{IN} = 3.6V$  and  $V_{OUT} = 1.8V$  @  $I_{OUT} = 50mA$** 

**Output Ripple for  $V_{IN} = 3.6V$  and  $V_{OUT} = 1.8V$  @  $I_{OUT} = 10mA$** 

**PSAVE @ 50mA Load**

**PSAVE @ 30mA Load**


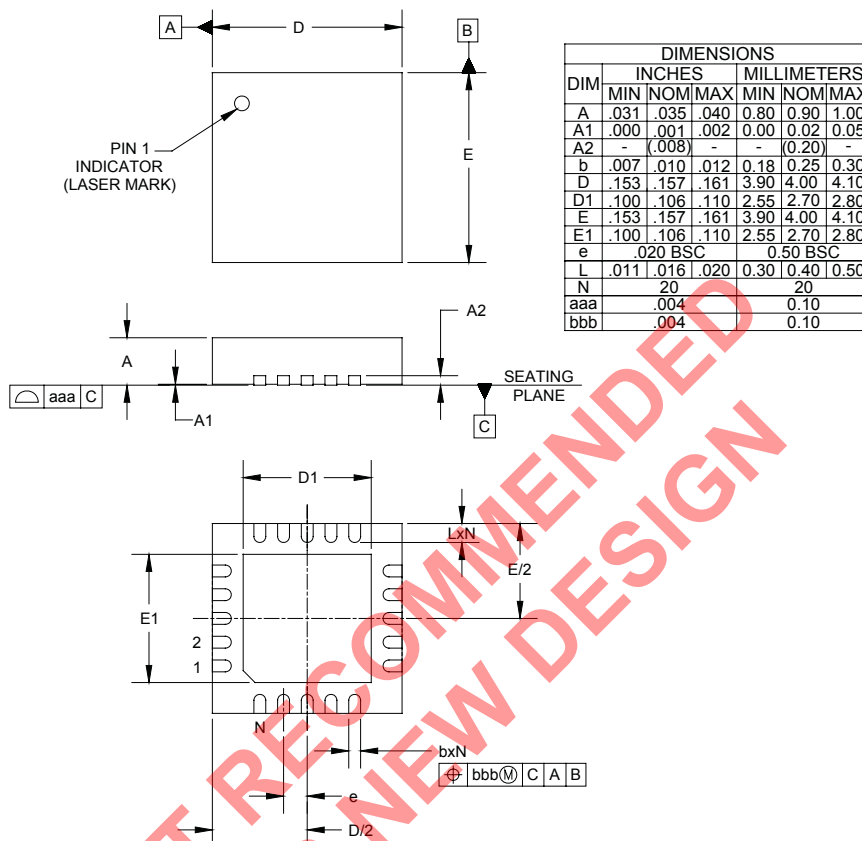
# POWER MANAGEMENT

## Typical Characteristics (Cont.)

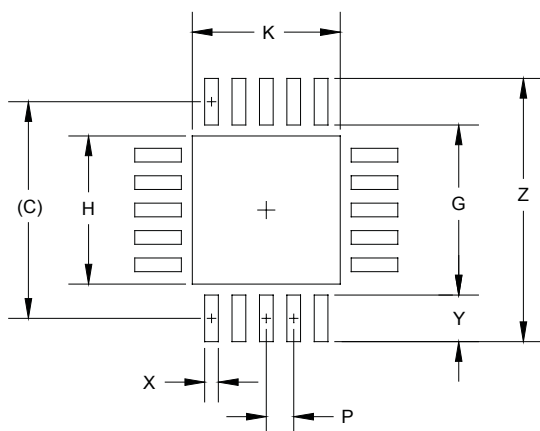
**PSAVE @ 50mA Load with  $C_{OUT} = 22\mu F$** 

**Transient Step in PSAVE**

**Input Transient Step from 3.1V to 3.6V**

**Input Transient Step from 3.6V to 3.1V**

**Output Transient @ PWM**

**Output Transient in PSAVE**


POWER MANAGEMENT

Outline Drawing - MLPQ-20 4 x 4



- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
  2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

**POWER MANAGEMENT**
**Land Pattern - MLPQ-20 4 x 4**


DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.155)	(3.95)
G	.122	3.10
H	.106	2.70
K	.106	2.70
P	.021	0.50
X	.010	0.25
Y	.033	0.85
Z	.189	4.80

**NOTES:**

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

**Contact Information**

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