

R1LV1616H-I Series

Wide Temperature Range Version
16 M SRAM (1-Mword $\times$ 16-bit)

REJ03C0195-0100Z

Rev. 1.00

Apr.22.2004

Description

The R1LV1616H-I Series is 16-Mbit static RAM organized 1-Mword $\times$ 16-bit. R1LV1616H-I Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is packaged in 48-pin plastic TSOPI for high density surface mounting.

Features

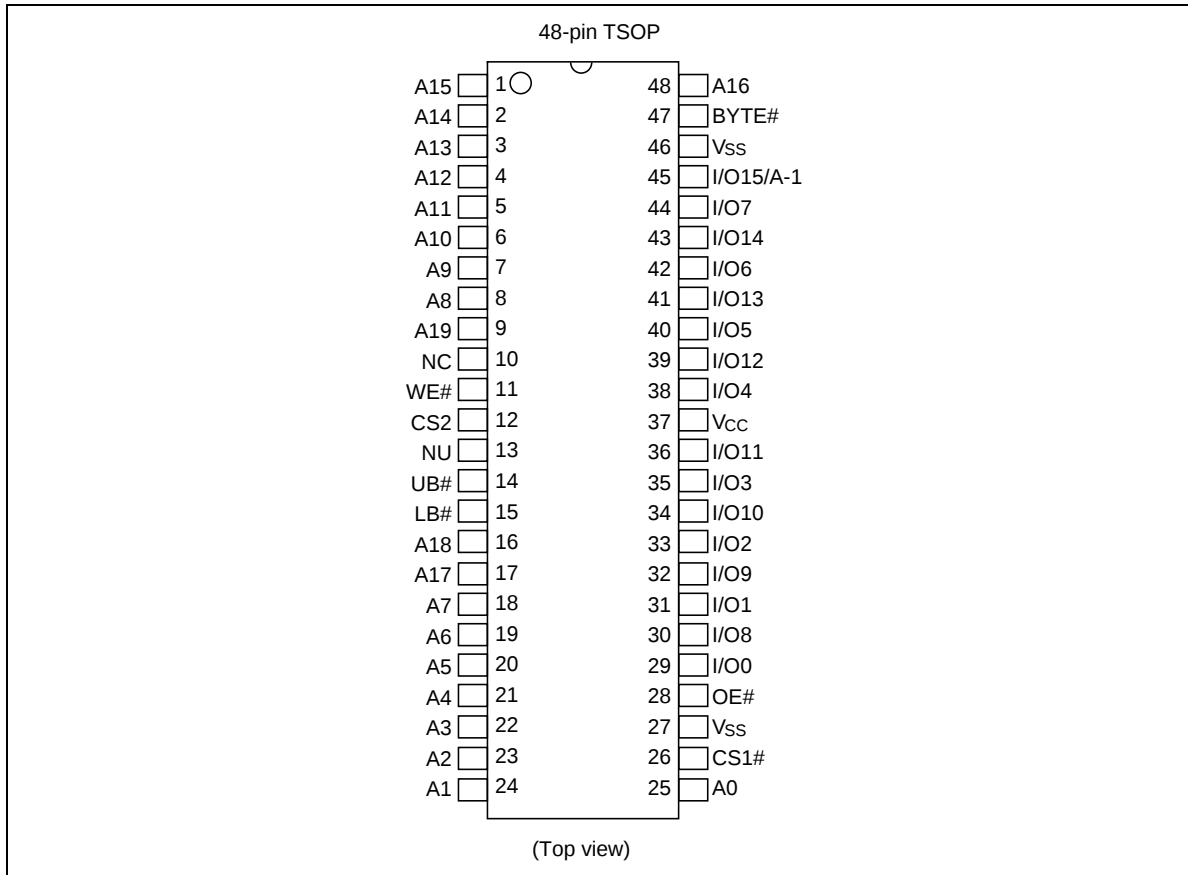
- Single 3.0 V supply: 2.7 V to 3.6 V
- Fast access time: 45/55 ns (max)
- Power dissipation:
 - Active: 9 mW/MHz (typ)
 - Standby: 1.5 μ W (typ)
- Completely static memory.
 - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
 - Three state output
- Battery backup operation.
 - 2 chip selection for battery backup
- Temperature range: -40 to $+85^{\circ}\text{C}$

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Ordering Information

Type No.	Access time	Package
R1LV1616HSA-4LI	45 ns	48-pin plastic TSOP1 (48P3R-B)
R1LV1616HSA-4SI	45 ns	
R1LV1616HSA-5SI	55 ns	

Pin Arrangement

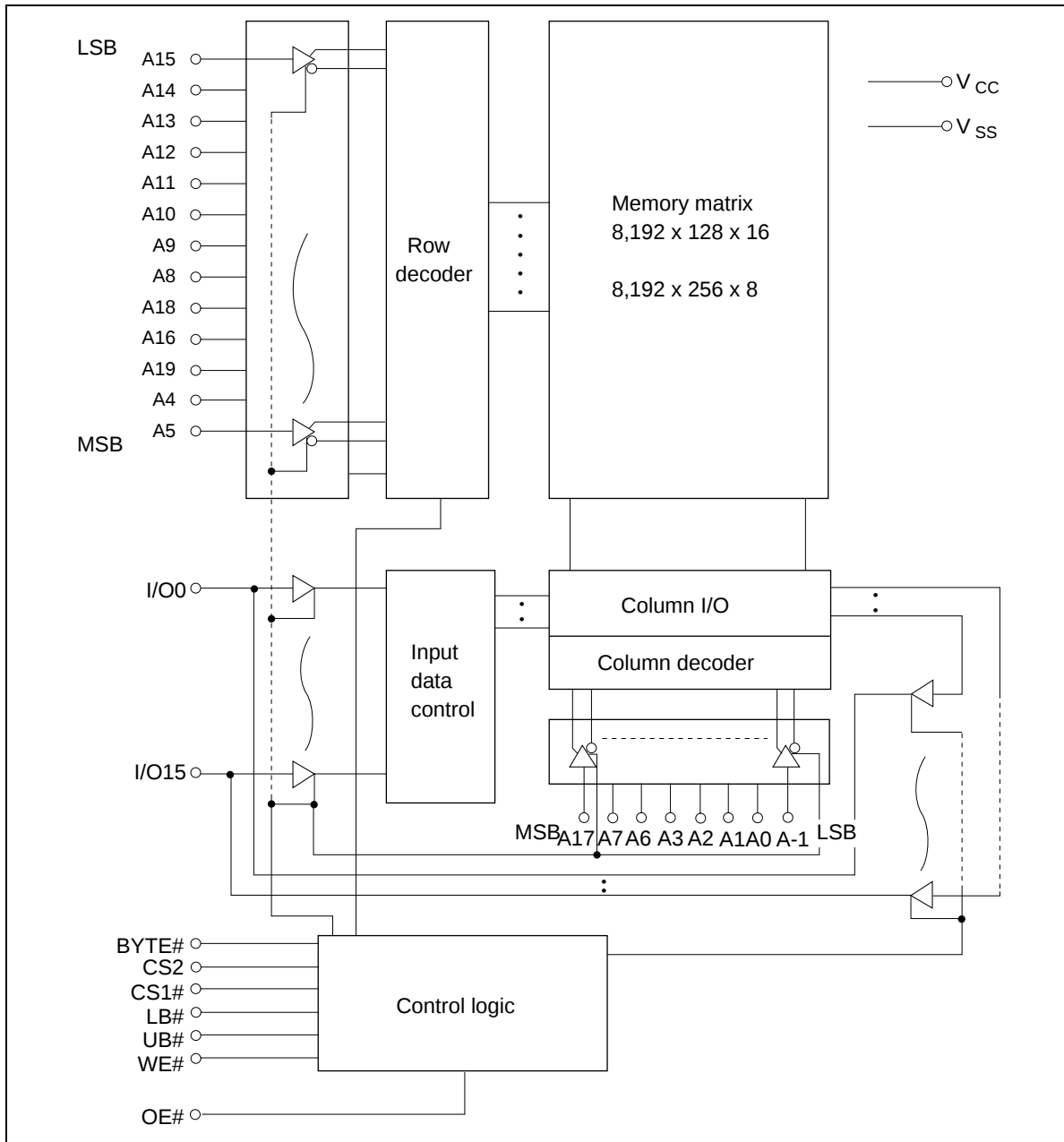


Pin Description (TSOP)

Pin name	Function
A0 to A19	Address input (word mode)
A-1 to A19	Address input (byte mode)
I/O0 to I/O15	Data input/output
CS1# ($\overline{\text{CS1}}$)	Chip select 1
CS2	Chip select 2
WE# ($\overline{\text{WE}}$)	Write enable
OE# ($\overline{\text{OE}}$)	Output enable
LB# ($\overline{\text{LB}}$)	Lower byte select
UB# ($\overline{\text{UB}}$)	Upper byte select
BYTE# ($\overline{\text{BYTE}}$)	Byte enable
V _{CC}	Power supply
V _{SS}	Ground
NC	No connection
NU* ¹	Not used (test mode pin)

Note: 1. This pin should be connected to a ground (V_{SS}), or not be connected (open).

Block Diagram (TSOP)



Operation Table (TSOP)

Byte mode

CS1#	CS2	WE#	OE#	UB#	LB#	BYTE#	I/O0 to I/O7	I/O8 to I/O14	I/O15	Operation
H	×	×	×	×	×	L	High-Z	High-Z	High-Z	Standby
×	L	×	×	×	×	L	High-Z	High-Z	High-Z	Standby
L	H	H	L	×	×	L	Dout	High-Z	A-1	Read
L	H	L	×	×	×	L	Din	High-Z	A-1	Write
L	H	H	H	×	×	L	High-Z	High-Z	High-Z	Output disable

Note: H: V_{IH} , L: V_{IL} , ×: V_{IH} or V_{IL}

Word mode

CS1#	CS2	WE#	OE#	UB#	LB#	BYTE#	I/O0 to I/O7	I/O8 to I/O14	I/O15	Operation
H	×	×	×	×	×	H	High-Z	High-Z	High-Z	Standby
×	L	×	×	×	×	H	High-Z	High-Z	High-Z	Standby
×	×	×	×	H	H	H	High-Z	High-Z	High-Z	Standby
L	H	H	L	L	L	H	Dout	Dout	Dout	Read
L	H	H	L	H	L	H	Dout	High-Z	High-Z	Lower byte read
L	H	H	L	L	H	H	High-Z	Dout	Dout	Upper byte read
L	H	L	×	L	L	H	Din	Din	Din	Write
L	H	L	×	H	L	H	Din	High-Z	High-Z	Lower byte write
L	H	L	×	L	H	H	High-Z	Din	Din	Upper byte write
L	H	H	H	×	×	H	High-Z	High-Z	High-Z	Output disable

Note: H: V_{IH} , L: V_{IL} , ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	-0.5* ¹ to $V_{CC} + 0.3$ * ²	V
Power dissipation	P_T	1.0	W
Storage temperature range	Tstg	-55 to +125	°C
Storage temperature range under bias	Tbias	-40 to +85	°C

Notes: 1. V_T min: -2.0 V for pulse half-width ≤ 10 ns.
2. Maximum voltage is +4.6 V.

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.2	—	$V_{CC} + 0.3$	V	
Input low voltage	V_{IL}	-0.3	—	0.6	V	1
Ambient temperature range	Ta	-40	—	+85	°C	

Note: 1. V_{IL} min: -2.0 V for pulse half-width ≤ 10 ns.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions*2	
Input leakage current	I _{LI}	—	—	1	μA	Vin = V _{SS} to V _{CC}	
Output leakage current	I _{LO}	—	—	1	μA	CS1# = V _{IH} or CS2 = V _{IL} or OE# = V _{IH} or WE# = V _{IL} or LB# = UB# = V _{IH} , V _{I/O} = V _{SS} to V _{CC}	
Operating current	I _{CC}	—	—	20	mA	CS1# = V _{IL} , CS2 = V _{IH} , Others = V _{IH} / V _{IL} , I _{I/O} = 0 mA	
Average operating current	I _{CC1} (READ)	—	22* ¹	35	mA	Min. cycle, duty = 100%, I _{I/O} = 0 mA, CS1# = V _{IL} , CS2 = V _{IH} , WE# = V _{IH} , Others = V _{IH} /V _{IL}	
	I _{CC1}	—	30* ¹	50	mA	Min. cycle, duty = 100%, I _{I/O} = 0 mA, CS1# = V _{IL} , CS2 = V _{IH} , Others = V _{IH} /V _{IL}	
	I _{CC2} * ³ (READ)	—	3* ¹	8	mA	Cycle time = 70 ns, duty = 100%, I _{I/O} = 0 mA, CS1# = V _{IL} , CS2 = V _{IH} , WE# = V _{IH} , Others = V _{IH} /V _{IL} Address increment scan or decrement scan	
	I _{CC2} * ³	—	20* ¹	30	mA	Cycle time = 70 ns, duty = 100%, I _{I/O} = 0 mA, CS1# = V _{IL} , CS2 = V _{IH} , Others = V _{IH} /V _{IL} Address increment scan or decrement scan	
	I _{CC3}	—	3* ¹	8	mA	Cycle time = 1 μs, duty = 100%, I _{I/O} = 0 mA, CS1# ≤ 0.2 V, CS2 ≥ V _{CC} − 0.2 V V _{IH} ≥ V _{CC} − 0.2 V, V _{IL} ≤ 0.2 V	
Standby current	I _{SB}	—	0.1* ¹	0.5	mA	CS2 = V _{IL}	
Standby current	-4SI -5SI	I _{SB1}	—	0.5* ¹	8	μA	0 V ≤ Vin (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS1# ≥ V _{CC} − 0.2 V, CS2 ≥ V _{CC} − 0.2 V or
	-4LI	I _{SB1}	—	0.5* ¹	25	μA	(3) LB# = UB# ≥ V _{CC} − 0.2 V, CS2 ≥ V _{CC} − 0.2 V, CS1# ≤ 0.2 V Average value
Output high voltage	V _{OH}	2.4	—	—	V	I _{OH} = −1 mA	
	V _{OH}	V _{CC} − 0.2	—	—	V	I _{OH} = −100 μA	
Output low voltage	V _{OL}	—	—	0.4	V	I _{OL} = 2 mA	
	V _{OL}	—	—	0.2	V	I _{OL} = 100 μA	

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- Notes: 1. Typical values are at $V_{CC} = 3.0\text{ V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.
2. $\text{BYTE\#} \geq V_{CC} - 0.2\text{ V}$ or $\text{BYTE\#} \leq 0.2\text{ V}$
3. I_{CC2} is the value measured while the valid address is increasing or decreasing by one bit.
Word mode: LSB (least significant bit) is A0.
Byte mode: LSB (least significant bit) is A-1.

Capacitance

($T_a = +25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	C_{in}	—	—	8	pF	$V_{in} = 0\text{ V}$	1
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O} = 0\text{ V}$	1

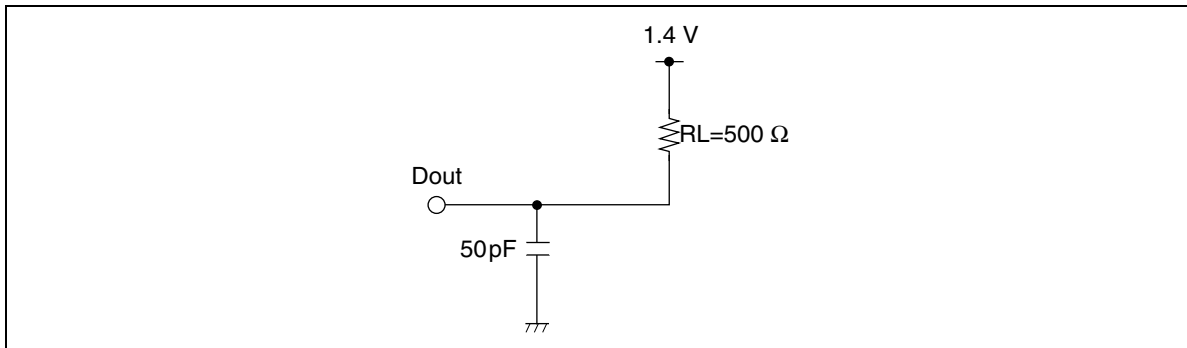
Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics

($T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.7$ V to 3.6 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: $V_{IL} = 0.4$ V, $V_{IH} = 2.4$ V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.4 V
- Output load: See figures (Including scope and jig)



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Read Cycle

Parameter	Symbol	R1LV1616H-I				Unit	Notes
		-4SI, -4LI		-5SI			
		Min	Max	Min	Max		
Read cycle time	t _{RC}	45	—	55	—	ns	
Address access time	t _{AA}	—	45	—	55	ns	
Chip select access time	t _{ACS1}	—	45	—	55	ns	
	t _{ACS2}	—	45	—	55	ns	
Output enable to output valid	t _{OE}	—	30	—	35	ns	
Output hold from address change	t _{OH}	10	—	10	—	ns	
LB#, UB# access time	t _{BA}	—	45	—	55	ns	
Chip select to output in low-Z	t _{CLZ1}	10	—	10	—	ns	2, 3
	t _{CLZ2}	10	—	10	—	ns	2, 3
LB#, UB# enable to low-Z	t _{BLZ}	5	—	5	—	ns	2, 3
Output enable to output in low-Z	t _{OLZ}	5	—	5	—	ns	2, 3
Chip deselect to output in high-Z	t _{CHZ1}	0	20	0	20	ns	1, 2, 3
	t _{CHZ2}	0	20	0	20	ns	1, 2, 3
LB#, UB# disable to high-Z	t _{BHZ}	0	15	0	20	ns	1, 2, 3
Output disable to output in high-Z	t _{OHZ}	0	15	0	20	ns	1, 2, 3

Write Cycle

		R1LV1616H-I					
		-4SI, -4LI		-5SI			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	t _{WC}	45	—	55	—	ns	
Address valid to end of write	t _{AW}	45	—	50	—	ns	
Chip selection to end of write	t _{CW}	45	—	50	—	ns	5
Write pulse width	t _{WP}	35	—	40	—	ns	4
LB#, UB# valid to end of write	t _{BW}	45	—	50	—	ns	
Address setup time	t _{AS}	0	—	0	—	ns	6
Write recovery time	t _{WR}	0	—	0	—	ns	7
Data to write time overlap	t _{DW}	25	—	25	—	ns	
Data hold from write time	t _{DH}	0	—	0	—	ns	
Output active from end of write	t _{OW}	5	—	5	—	ns	2
Output disable to output in high-Z	t _{OHZ}	0	15	0	20	ns	1, 2
Write to output in high-Z	t _{WHZ}	0	15	0	20	ns	1, 2

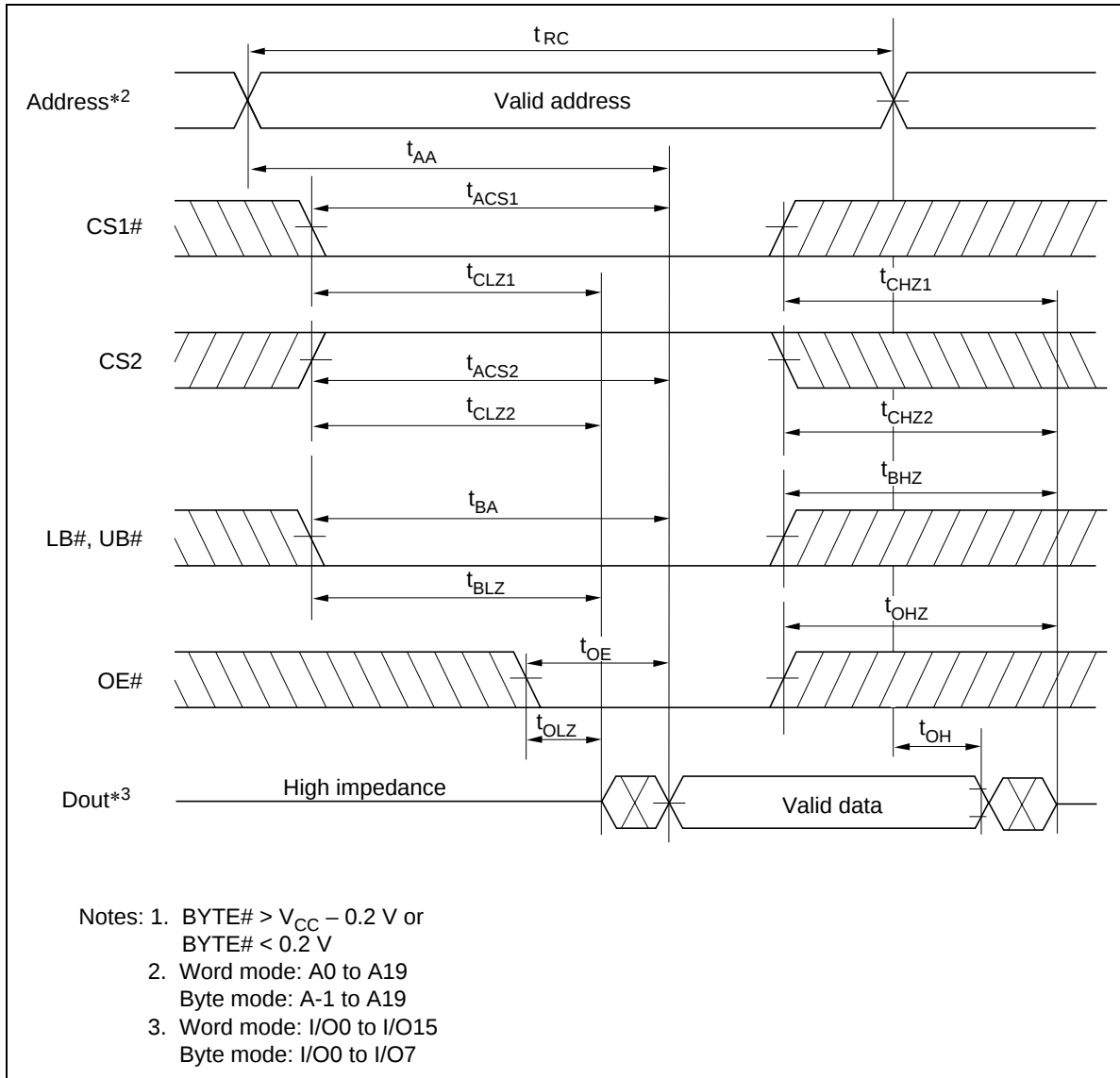
Byte Control

Parameter	Symbol	R1LV1616H-I				Unit	Notes
		-4SI, -4LI		-5SI			
		Min	Max	Min	Max		
BYTE# setup time	t _{BS}	5	—	5	—	ms	
BYTE# recovery time	t _{BR}	5	—	5	—	ms	

- Notes:
1. t_{CHZ} , t_{OHZ} , t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
 2. This parameter is sampled and not 100% tested.
 3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
 4. A write occurs during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#. A write begins at the latest transition among CS1# going low, CS2 going high, WE# going low and LB# going low or UB# going low. A write ends at the earliest transition among CS1# going high, CS2 going low, WE# going high and LB# going high or UB# going high. t_{WP} is measured from the beginning of write to the end of write.
 5. t_{CW} is measured from the later of CS1# going low or CS2 going high to the end of write.
 6. t_{AS} is measured from the address valid to the beginning of write.
 7. t_{WR} is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle.

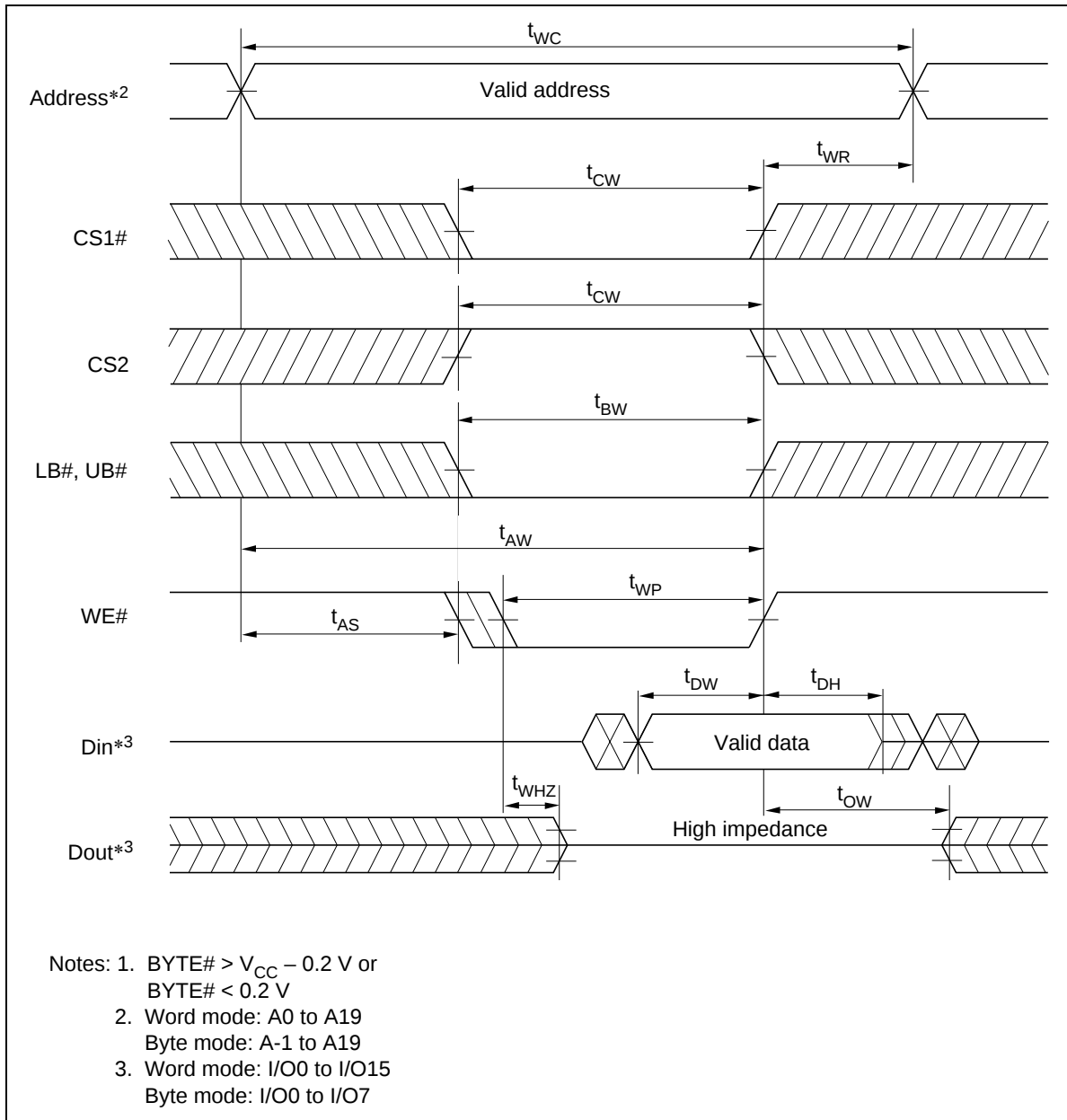
Timing Waveform

Read Cycle*¹

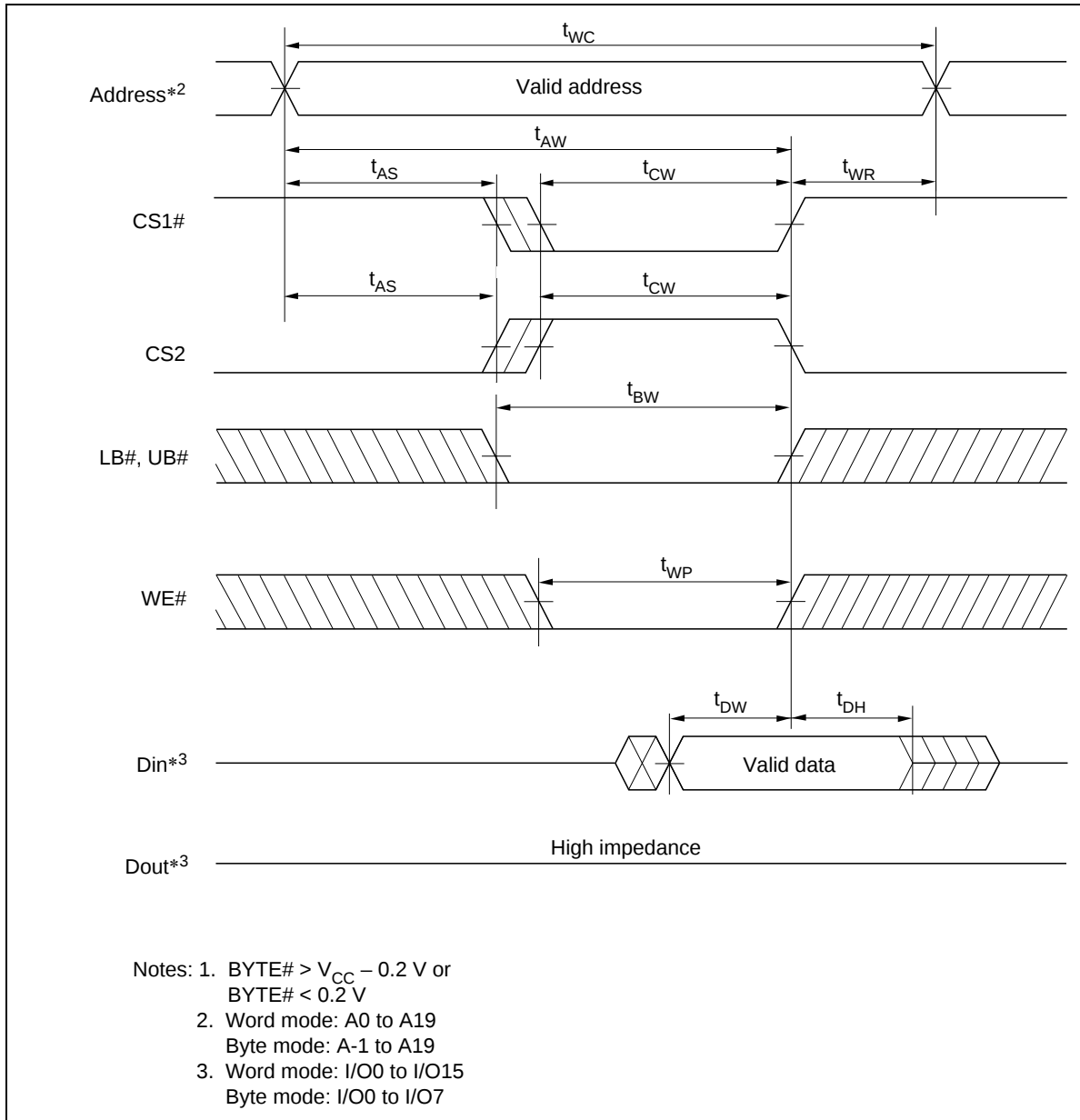


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Write Cycle (1)*¹ (WE# Clock)

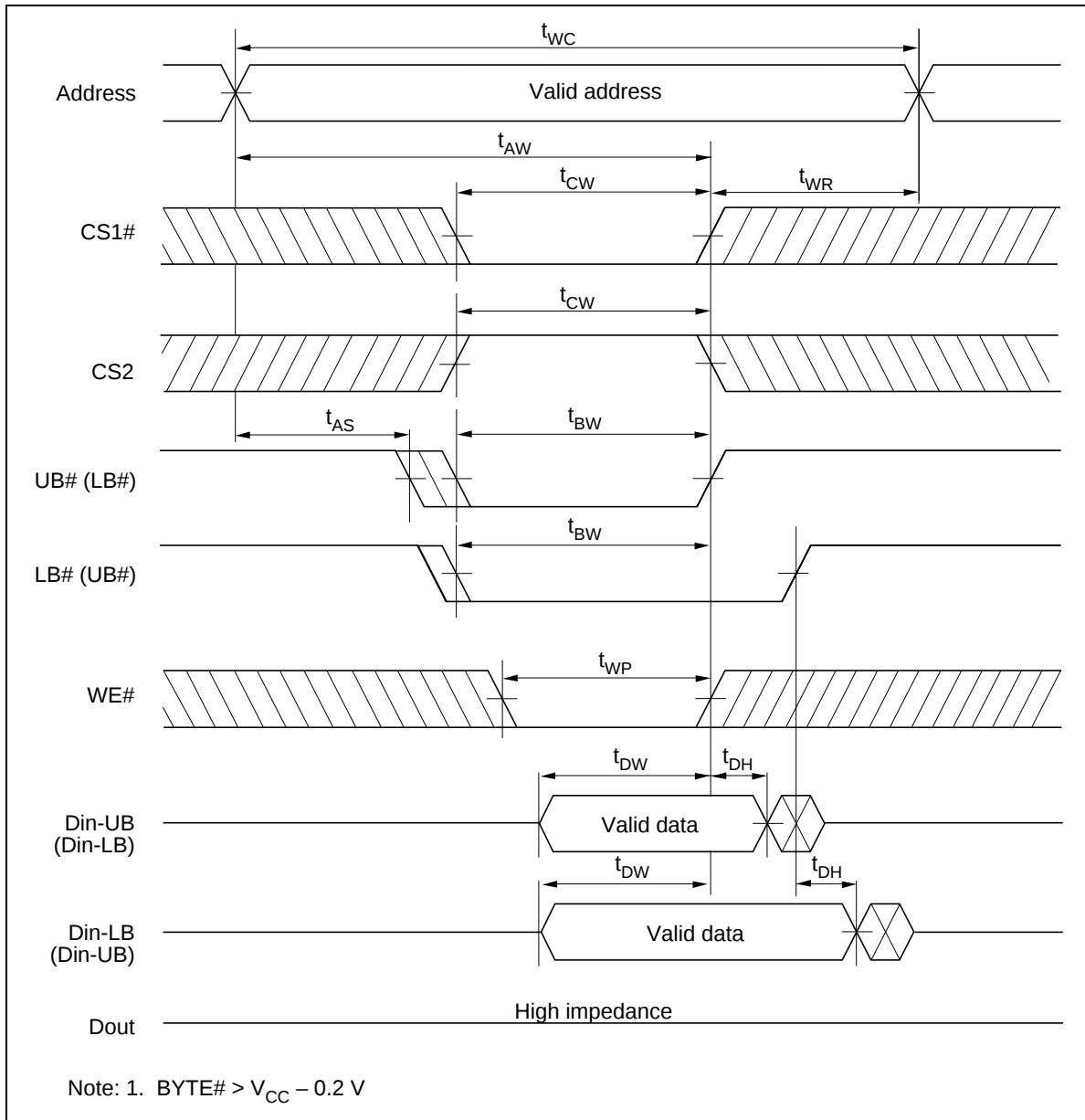


Write Cycle (2)*¹ (CS1#, CS2 Clock, OE# = V_{IH})

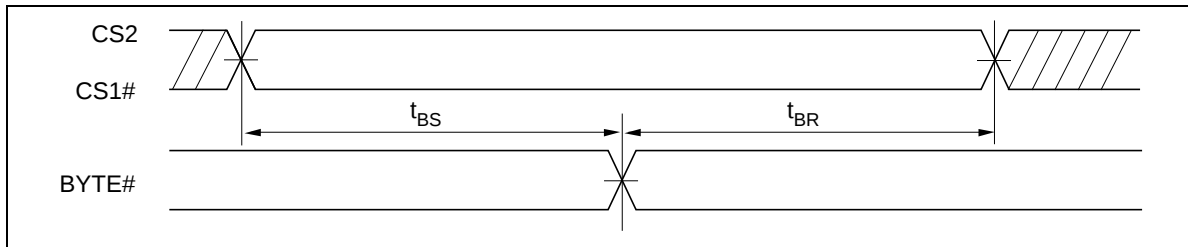


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Write Cycle (3)*¹ (LB#, UB# Clock, OE# = V_{IH})



Byte Control (TSOP)



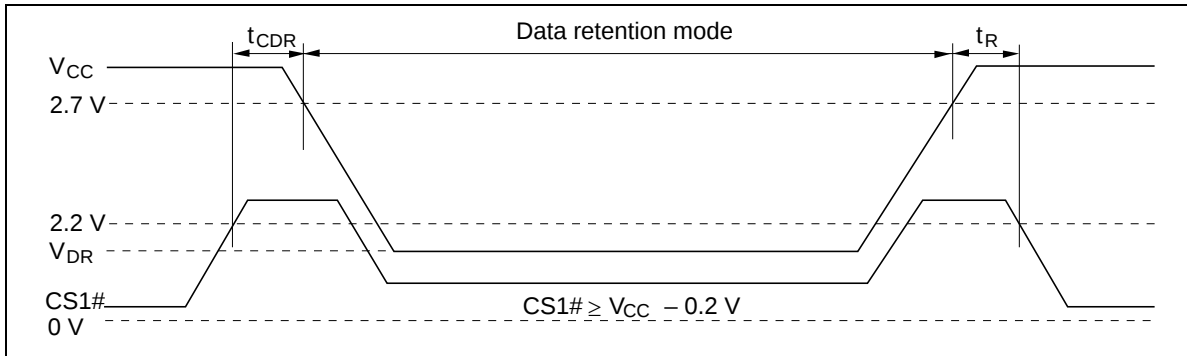
Low V_{CC} Data Retention Characteristics

(Ta = -40 to +85°C)

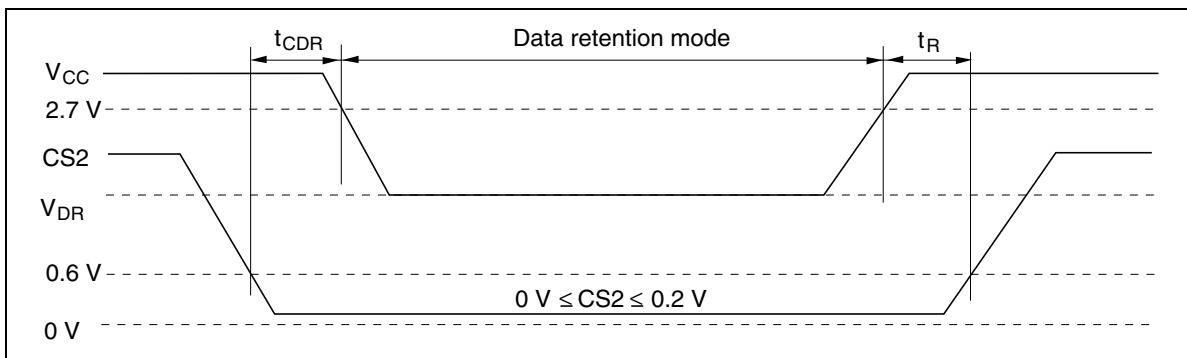
Parameter		Symbol	Min	Typ	Max	Unit	Test conditions* ^{2, 3}
V _{CC} for data retention		V _{DR}	1.5	—	3.6	V	V _{in} ≥ 0 V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V _{CC} − 0.2 V, CS1# ≥ V _{CC} − 0.2 V or (3) LB# = UB# ≥ V _{CC} − 0.2 V, CS2 ≥ V _{CC} − 0.2 V, CS1# ≤ 0.2 V
Data retention current	-4SI -5SI	I _{CCDR}	—	0.5* ¹	8	μA	V _{CC} = 3.0 V, V _{in} ≥ 0 V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V _{CC} − 0.2 V, CS1# ≥ V _{CC} − 0.2 V or (3) LB# = UB# ≥ V _{CC} − 0.2 V, CS2 ≥ V _{CC} − 0.2 V, CS1# ≤ 0.2 V
	-4LI	I _{CCDR}	—	0.5* ¹	25	μA	Average value
Chip deselect to data retention time		t _{CDR}	0	—	—	ns	See retention waveforms
Operation recovery time		t _R	5	—	—	ms	

Notes: 1. Typical values are at $V_{CC} = 3.0$ V, Ta = +25°C and not guaranteed.2. BYTE# $\geq V_{CC} - 0.2$ V or BYTE# ≤ 0.2 V3. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer, LB#, UB# buffer and Din buffer. If CS2 controls data retention mode, Vin levels (address, WE#, OE#, CS1#, LB#, UB#, I/O) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be CS2 $\geq V_{CC} - 0.2$ V or 0 V $\leq$ CS2 $\leq$ 0.2 V. The other input levels (address, WE#, OE#, LB#, UB#, I/O) can be in the high impedance state.

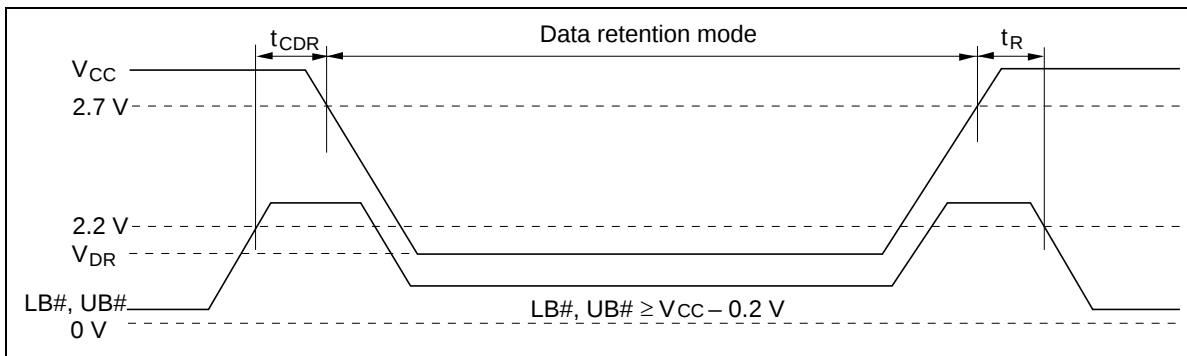
Low V_{CC} Data Retention Timing Waveform (1) (CS1# Controlled)



Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



Low V_{CC} Data Retention Timing Waveform (3) (LB#, UB# Controlled)



Revision History

R1LV1616H-I Series Data Sheet

Rev.	Date	Contents of Modification	
		Page	Description
1.00	Apr. 22, 2004	—	Initial issue

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