8-bit high-speed analog-to-digital converter TDF8704

FEATURES

- 8-bit resolution
- Sampling rate up to 50 MHz
- Extended temperature range (−40 to +85 °C)
- High signal-to-noise ratio over a large analog input frequency range (7.4 effective bits at 4.43 MHz full-scale input at f_{CLK} = 50 MHz)
- Binary 3-state TTL outputs
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- Stable internal reference voltage regulator included
- Power dissipation only 360 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

- General purpose high-speed analog-to-digital conversion for extended temperature applications
- Automotive
- RF, satellite and GPS
- Medical
- General industrial
- Digital video (VCR, TV and satellite).

GENERAL DESCRIPTION

The TDF8704T is an 8-bit high-speed analog-to-digital converter (ADC) for general industrial applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are TTL compatible, although a low-level AC clock input signal is allowed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	37	tbf	mA
I_{CCD}	digital supply current		–	18	tbf	mA
I_{CCO}	output stages supply current		–	17	tbf	mA
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
AILE	AC integral linearity error	note 1	–	–	±2	LSB
f_{CLK}	maximum conversion rate		50	–	–	MHz
P_{tot}	total power dissipation		–	360	tbf	mW

Note

1. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK} = 50 MHz).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE				
	PINS	PIN POSITION	MATERIAL	CODE	SAMPLING FREQUENCY (MHz)
TDF8704T/2	24	SO24	plastic	SOT137A	20
TDF8704T/4	24	SO24	plastic	SOT137A	40
TDF8704T/5	24	SO24	plastic	SOT137A	50

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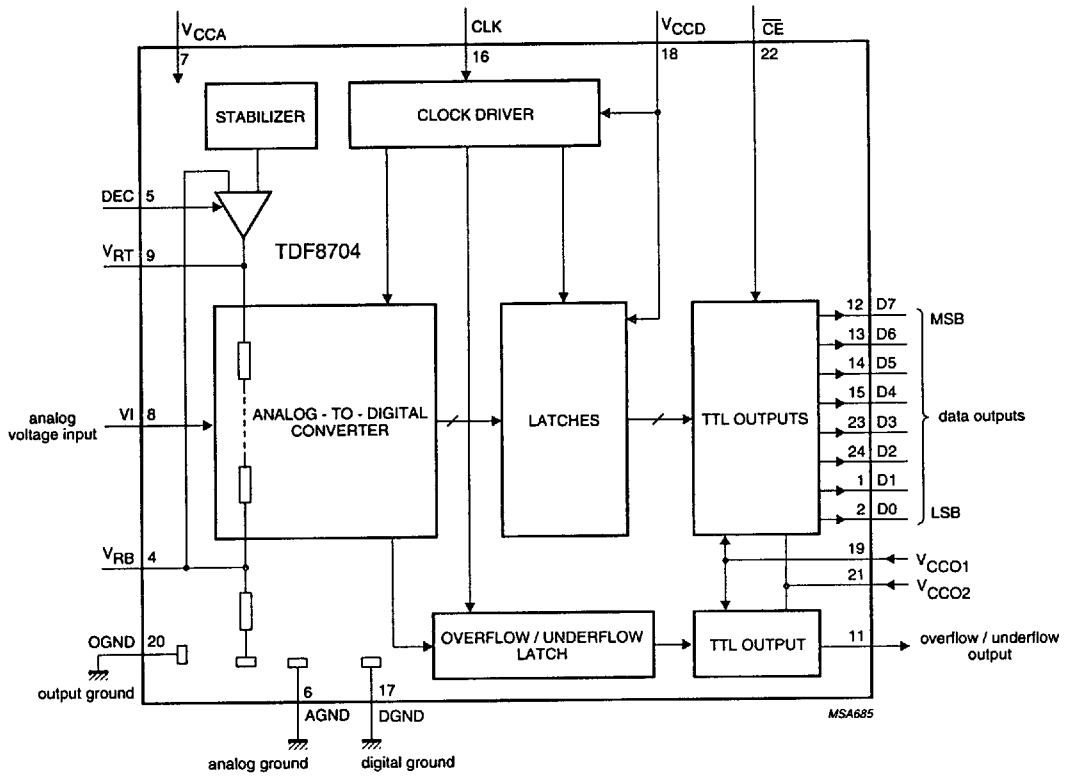

Fig.1 Block diagram.

8-bit high-speed analog-to-digital converter TDF8704

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output, bit 1
D0	2	data output; bit 0 (LSB)
n.c.	3	not connected
V_{RB}	4	reference voltage bottom (decoupling)
DEC	5	decoupling input (internal stabilization loop decoupling)
AGND	6	analog ground
V_{CCA}	7	positive supply voltage for analog circuits (+5 V)
VI	8	analog voltage input
V_{RT}	9	reference voltage top (decoupling)
n.c.	10	not connected
O/UF	11	overflow/underflow data output
D7	12	data output; bit 7 (MSB)
D6	13	data output; bit 6
D5	14	data output; bit 5
D4	15	data output; bit 4
CLK	16	clock input
DGND	17	digital ground
V_{CCD}	18	positive supply voltage for digital circuits (+5 V)
V_{CCO1}	19	positive supply voltage for output stages 1 (+5 V)
OGND	20	output ground
V_{CCO2}	21	positive supply voltage for output stages 2 (+5 V)
$\overline{CE}$	22	chip enable input (TTL level input, active LOW)
D3	23	data output; bit 3
D2	24	data output; bit 2

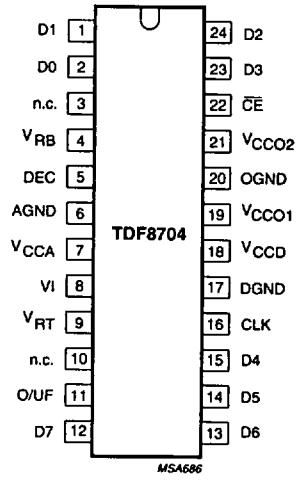

Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage		−0.3	7.0	V
V_{CCD}	digital supply voltage		−0.3	7.0	V
V_{CCO}	output stages supply voltage		−0.3	7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCO} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCA} - V_{CCO}$	supply voltage differences		−1.0	1.0	V
V_{VI}	input voltage range	referenced to AGND	−0.3	7.0	V
$V_{CLK(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	−	V_{CCD}	V
I_O	output current		−	+10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
T_j	junction temperature		−	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient in free air	75 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS (see Tables 1 and 2)

$V_{CCA} = V_7 - V_6 = 4.75$ V to 5.25 V; $V_{CCD} = V_{18} - V_{20} = 4.75$ V to 5.25 V; $V_{CCO} = V_{19} - V_{20} = 4.75$ V to 5.25 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.25$ V to +0.25 V; $V_{CCO} - V_{CCD} = -0.25$ V to +0.25 V; $V_{CCA} - V_{CCD} = -0.25$ V to +0.25 V; $T_{amb} = -40$ °C to +85 °C; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = V_{CCO1} = V_{CCO2} = 5$ V and $T_{amb} = 25$ °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	37	tbf	mA
I_{CCD}	digital supply current		–	18	tbf	mA
I_{CCO}	output stage supply current	all outputs LOW	–	17	tbf	mA
Inputs						
Clock input; CLK (referenced to DGND)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_{CLK} = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_{CLK} = 2.7$ V	–	–	100	µA
		$V_{CLK} = V_{CCD}$	–	–	300	µA
Z_i	input impedance	$f_{CLK} = 50$ MHz	–	2	–	kΩ
C_i	input capacitance	$f_{CLK} = 50$ MHz	–	4.5	–	pF
Input $\overline{CE}$ (referenced to DGND)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.2	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_{IL} = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_{IH} = 2.7$ V	–	–	20	µA
VI (analog input voltage referenced to AGND) (see Figs 3 and 4)						
$V_{VI(B)}$	input voltage (bottom)		tbf	1.23	tbf	V
$V_{VI(0)}$	input voltage	output code = 0	tbf	1.46	tbf	V
$V_{OS(B)}$	offset voltage (bottom)	$V_{VI(0)} - V_{VI(B)}$	tbf	–	tbf	V
$V_{VI(T)}$	input voltage (top)		tbf	3.41	tbf	V
$V_{VI(255)}$	input voltage	output code = 255	tbf	3.31	tbf	V
$V_{OS(T)}$	offset voltage (top)	$V_{VI(T)} - V_{VI(255)}$	tbf	–	tbf	V
$V_{VI(p-p)}$	input voltage amplitude (peak-to-peak value)		tbf	1.85	tbf	V
I_{IL}	LOW level input current	$V_{VI} = 1.23$ V	–	0	–	µA
I_{IH}	HIGH level input current	$V_{VI} = 3.41$ V	60	150	300	µA
Z_i	input impedance	$f_i = 4.43$ MHz	–	10	–	kΩ
C_i	input capacitance	$f_i = 4.43$ MHz	–	14	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference resistance						
R_{ref}	reference resistance	V_{RT} to V_{RB}	–	220	–	Ω
Outputs						
Digital outputs (D7 - D0) (referenced to DGND)						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = −0.4 mA	2.7	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	−20	–	+20	μA
Switching characteristics (note 1; see Fig.3)						
f_{CLK}	maximum clock frequency	TDF8704T/2	20	–	–	MHz
		TDF8704T/4	40	–	–	MHz
		TDF8704T/5	50	–	–	MHz
t_{CPH}	clock pulse width HIGH		7	–	–	ns
t_{CPL}	clock pulse width LOW		7	–	–	ns
Analog signal processing (f_{CLK} = 50 MHz)						
G_d	differential gain	note 2	–	0.6	–	%
ϕ_d	differential phase	note 2	–	0.8	–	deg
f_t	fundamental harmonics (full-scale)	f_i = 4.43 MHz	–	–	0	dB
f_{all}	harmonics (full-scale), all components	f_i = 4.43 MHz	–	−60	–	dB
SVRR1	supply voltage ripple rejection	note 3	–	−28	−25	dB
SVRR2	supply voltage ripple rejection	note 3	–	1	2.5	%/V
Transfer function						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
AILE	AC integral linearity error	note 4	–	–	±2	LSB
Effective bits; note 5						
EB	TDF8704T/2 (f_{CLK} = 20 MHz)	f_i = 2.5 MHz	–	7.7	–	bits
		f_i = 4.43 MHz	–	7.6	–	bits
	TDF8704T/4 (f_{CLK} = 40 MHz)	f_i = 4.43 MHz	–	7.5	–	bits
		f_i = 7.5 MHz	–	7.3	–	bits
	TDF8704T/5 (f_{CLK} = 50 MHz)	f_i = 4.43 MHz	–	7.4	–	bits
		f_i = 7.5 MHz	–	7.2	–	bits

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (note 6; see Figs 3 to 5; f_{CLK} = 50 MHz)						
t_{dS}	sampling delay		–	–	2	ns
t_{HD}	output hold time		5	–	–	ns
t_d	output delay time		–	12	15	ns
t_{dZH}	3-state output delay times	enable-to-HIGH	–	19	tbf	ns
t_{dZL}	3-state output delay times	enable-to-LOW	–	16	tbf	ns
t_{dHZ}	3-state output delay times	disable-to-HIGH	–	14	tbf	ns
t_{dLZ}	3-state output delay times	disable-to-LOW	–	9	tbf	ns

Notes

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 1 ns.
2. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.
3. Supply voltage ripple rejection:
   - SVRR1; variation of the input voltage producing output code 127 for supply voltage variation of 1 V: SVRR1 = 20 log ($\Delta V_{VI(127)}$ / ΔV_{CCA})
   - SVRR2; relative variation of the full-scale range of analog input for a supply voltage variation of 1 V: SVR2 = $\{\Delta(V_{VI(0)} - V_{VI(255)}) / (V_{VI(0)} - V_{VI(255)})\} \div \Delta V_{CCA}$.
4. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK} = 50 MHz).
5. Effective bits are obtained via a Fast Fourier Transformer (FFT) treatment taking 4K acquisition points per period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to SNR: SNR (dB) = EB x 6.02 + 1.76.
6. Output data acquisition:
   - Output data is available after the maximum delay of t_d.

Table 1 Output coding and input voltage (typical values; referenced to AGND).

			BINARY OUTPUT BITS							
STEP	$V_{VI(p-p)}$	O/UF	D7	D6	D5	D4	D3	D2	D1	D0
underflow	< 1.46	1	0	0	0	0	0	0	0	0
0	1.46	0	0	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
254	•	0	1	1	1	1	1	1	1	0
255	3.31	0	1	1	1	1	1	1	1	1
overflow	> 3.316	1	1	1	1	1	1	1	1	1

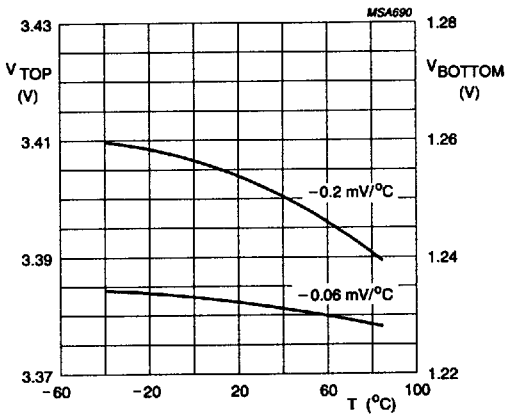

Fig.3 Influence of ambient temperature on V_{TOP} and V_{BOTTOM} under 5 V supply.

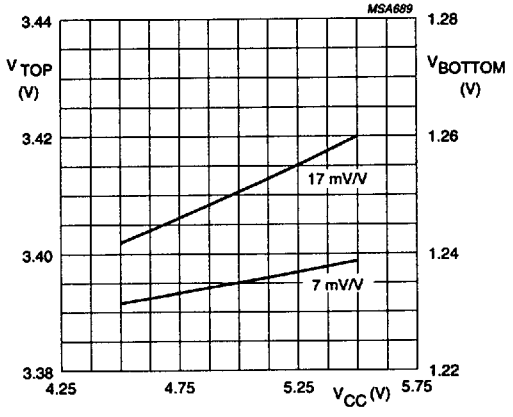

Fig.4 Influence of supply voltage on V_{TOP} and V_{BOTTOM} under 25 °C ambient temperature.

Table 2 Mode selection.

$\overline{CE}$	D7 to D0	O/UF
1	high impedance	high impedance
0	active; binary	active

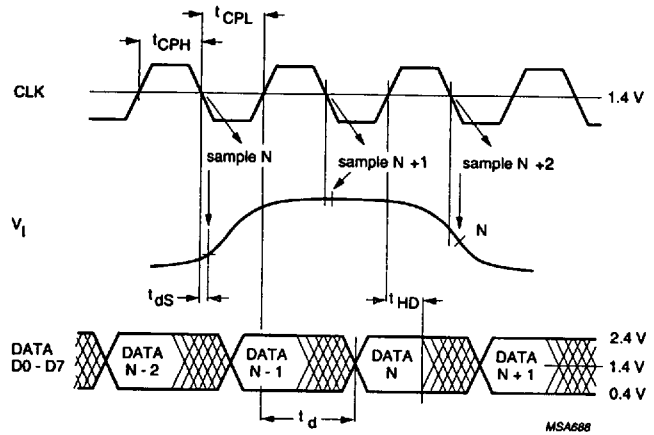

Fig.5 Timing diagram.

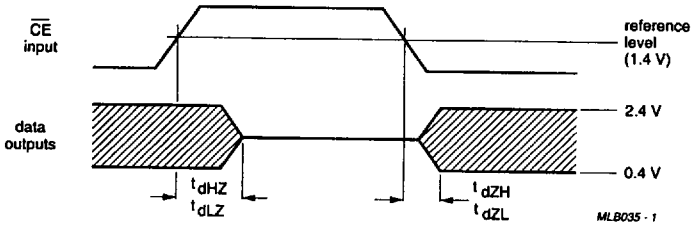

Fig.6 3-state delay timing diagram.

INTERNAL PIN CONFIGURATIONS

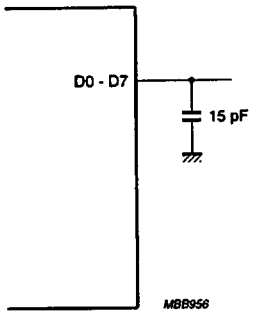

Fig.7 Load circuit for timing measurement.

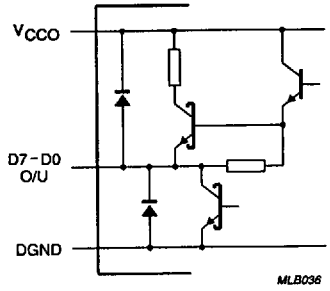

Fig.8 TTL data and overflow/underflow outputs.

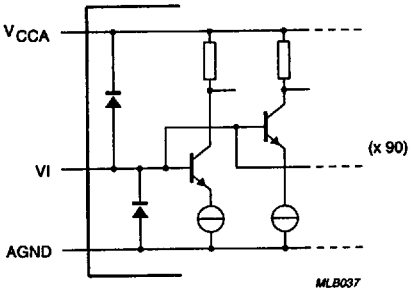

Fig.9 Analog inputs.

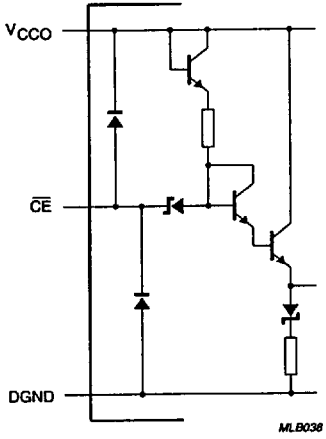

Fig.10 $\overline{CE}$ (3-state) input.

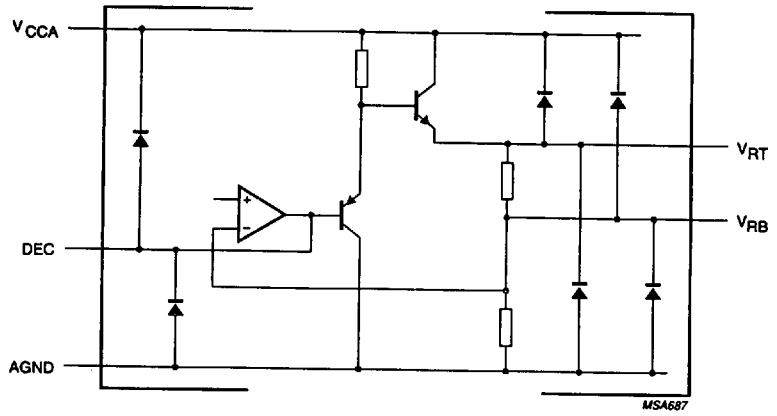

Fig.11 V_{RB}, V_{RT} and DEC.

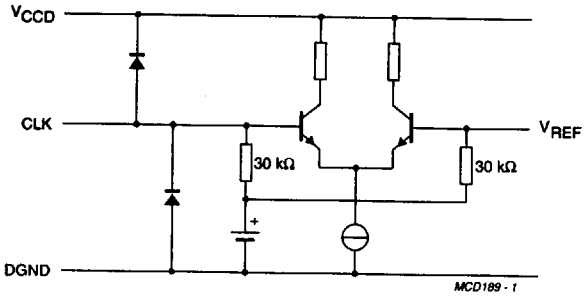

Fig.12 CLK input.

APPLICATION INFORMATION

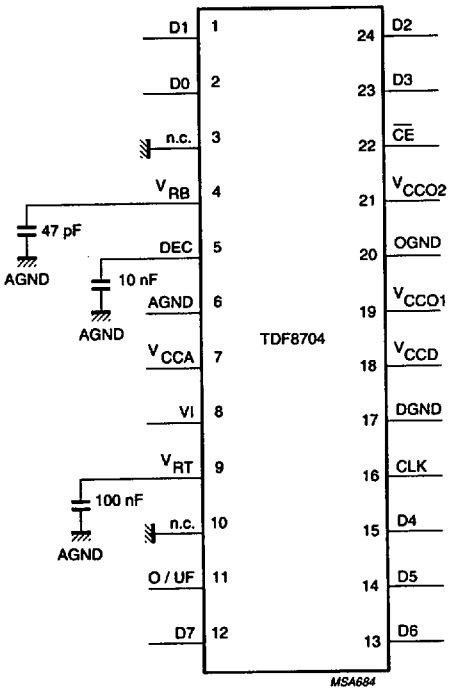

Fig.13 Application diagram.

Notes to Fig.13

1. V_{RB} and V_{RT} are decoupling pins for the internal reference ladder; do not draw current from these pins in order to achieve good linearity.
2. Analog and digital supplies should be separated and decoupled.
3. Pins 3 and 10 should be connected to DGND in order to prevent noise influence.