

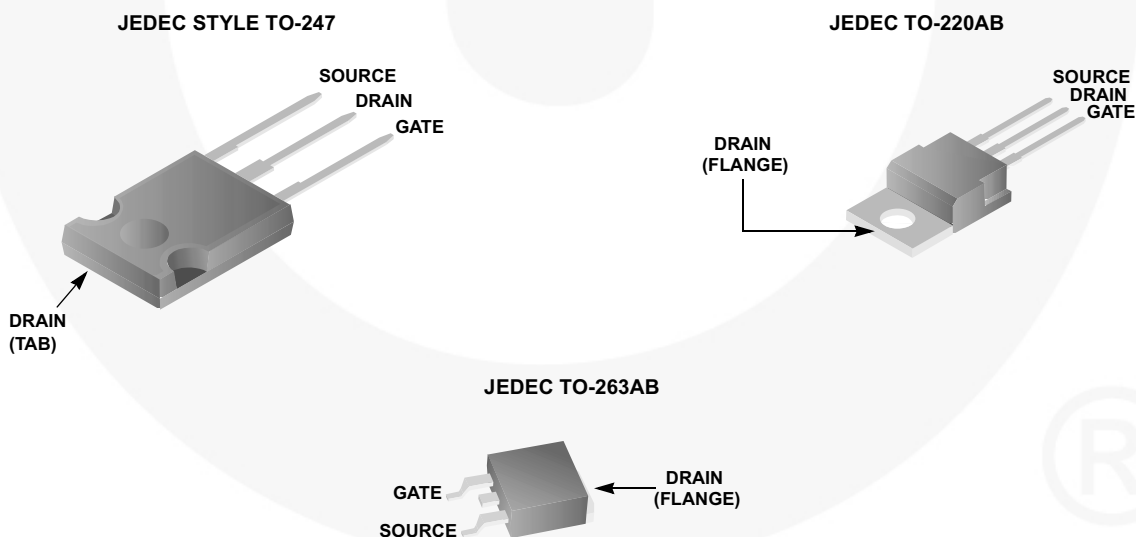
N-Channel UltraFET Power MOSFET
55 V, 75 A, 7 mΩ

These N-Channel power MOSFETs are manufactured using the innovative UltraFET process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

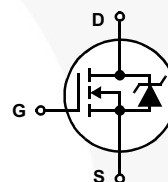
Formerly developmental type TA75345.

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF75345G3	TO-247	75345G
HUF75345P3	TO-220AB	75345P
HUF75345S3ST	TO-263AB	75345S

Packaging

Features

- 75A, 55V
- Simulation Models
 - Temperature Compensated PSpice® and SABER™ Models
 - Thermal Impedance SPICE and SABER Models Available on the WEB at: www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
 - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol


Product reliability information can be found at <http://www.fairchildsemi.com/products/discrete/reliability/index.html>

For severe environments, see our Automotive HUF series.

All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

HUF75345G3, HUF75345P3, HUF75345S3S

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

			UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	55	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	55	V
Gate to Source Voltage	V_{GS}	± 20	V
Drain Current			
Continuous (Figure 2)	I_D	75	A
Pulsed Drain Current	I_{DM}	Figure 4	
Pulsed Avalanche Rating	E_{AS}	Figure 6	
Power Dissipation	P_D	325	W
Derate Above 25°C		2.17	W/ $^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^\circ\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 11)	55	-	-	V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 50V, V _{GS} = 0V	-	-	1	μA	
		V _{DS} = 45V, V _{GS} = 0V, T _C = 150°C	-	-	250	μA	
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V	-	-	±100	nA	
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 10)	2	-	4	V	
Drain to Source On Resistance	r _{DS(ON)}	I _D = 75A, V _{GS} = 10V (Figure 9)	-	0.006	0.007	Ω	
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	R _{θJC}	(Figure 3)	-	-	0.46	°C/W	
Thermal Resistance Junction to Ambient	R _{θJA}	TO-247	-	-	30	°C/W	
		TO-220, TO-263	-	-	62	°C/W	
SWITCHING SPECIFICATIONS (V _{GS} = 10V)							
Turn-On Time	t _{ON}	V _{DD} = 30V, I _D ≅ 75A, R _L = 0.4Ω, V _{GS} = 10V, R _{GS} = 2.5Ω	-	-	195	ns	
Turn-On Delay Time	t _{d(ON)}		-	14	-	ns	
Rise Time	t _r		-	118	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	42	-	ns	
Fall Time	t _f		-	26	-	ns	
Turn-Off Time	t _{OFF}		-	-	98	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 20V	V _{DD} = 30V, I _D ≅ 75A, R _L = 0.4Ω I _{g(REF)} = 1.0mA (Figure 13)	-	220	275	nC
Gate Charge at 10V	Q _{g(10)}	V _{GS} = 0V to 10V		-	125	165	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 2V		-	6.8	10	nC
Gate to Source Gate Charge	Q _{gs}			-	14	-	nC
Gate to Drain “Miller” Charge	Q _{gd}			-	58	-	nC

HUF75345G3, HUF75345P3, HUF75345S3S

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CAPACITANCE SPECIFICATIONS						
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$ (Figure 12)	-	4000	-	pF
Output Capacitance	C_{OSS}		-	1450	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	450	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 75\text{A}$	-	-	1.25	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 75\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	55	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 75\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	80	nC

Typical Performance Curves

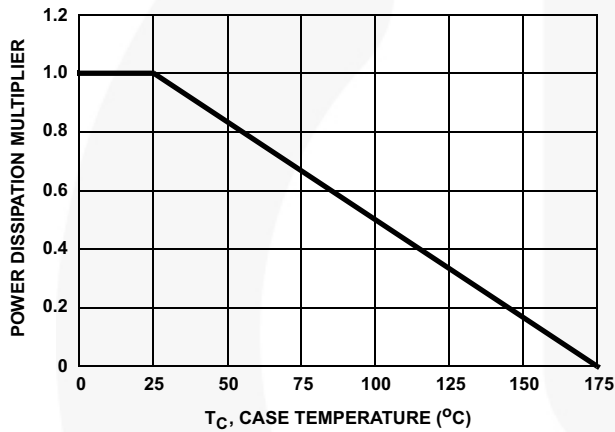


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

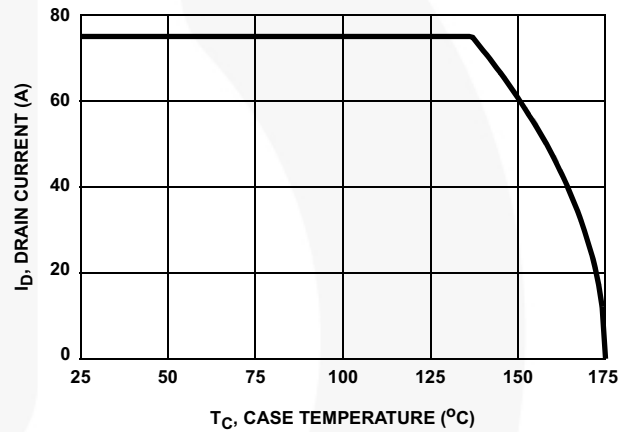


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

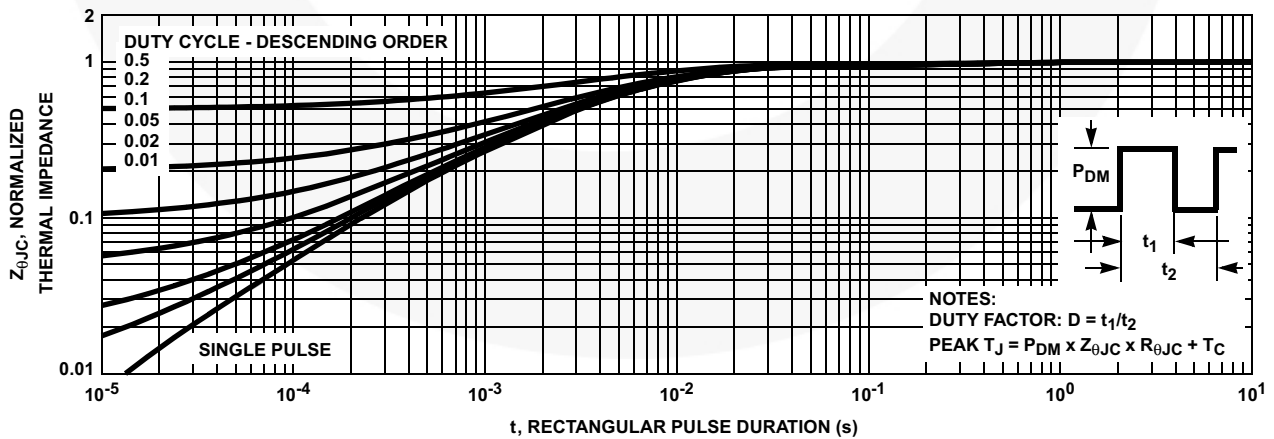


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves (Continued)

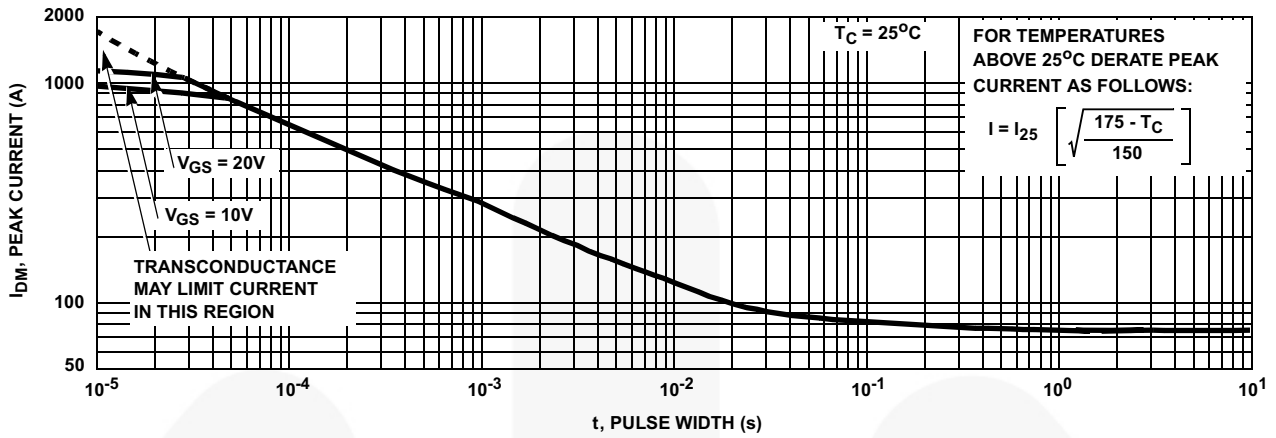


FIGURE 4. PEAK CURRENT CAPABILITY

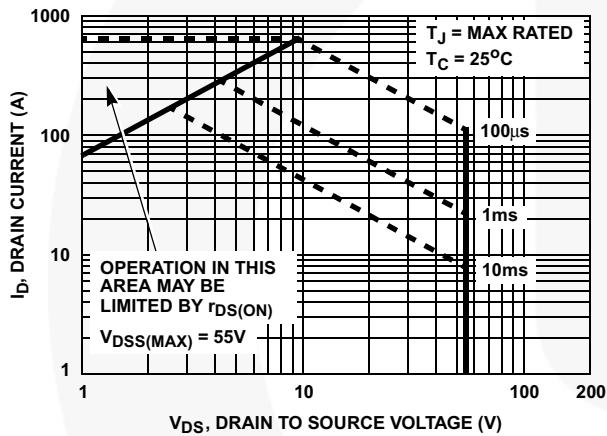
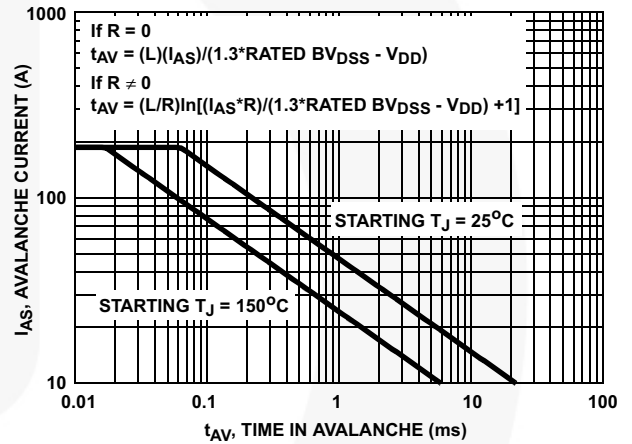


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

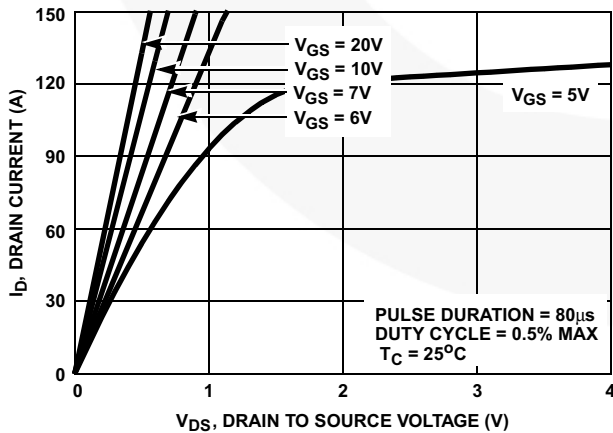


FIGURE 7. SATURATION CHARACTERISTICS

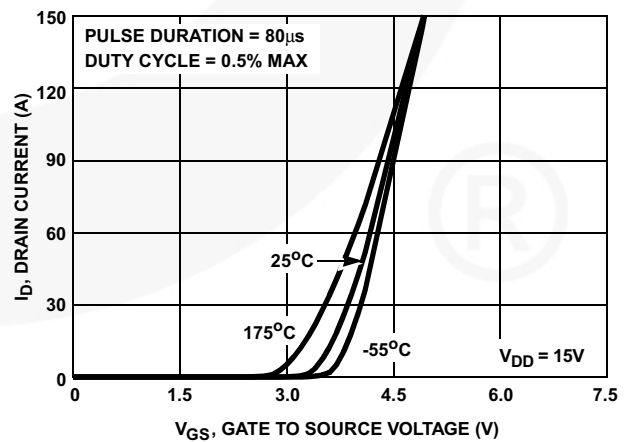


FIGURE 8. TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

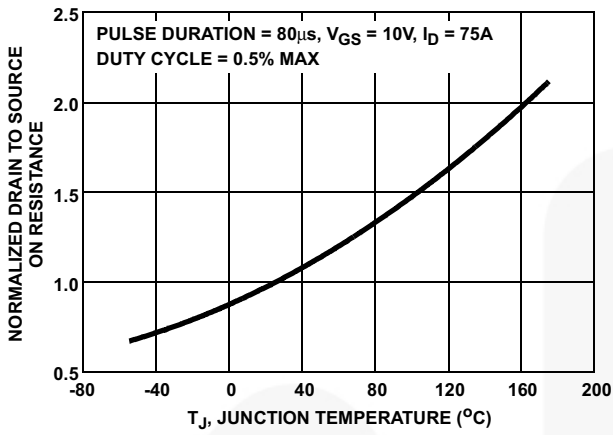


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

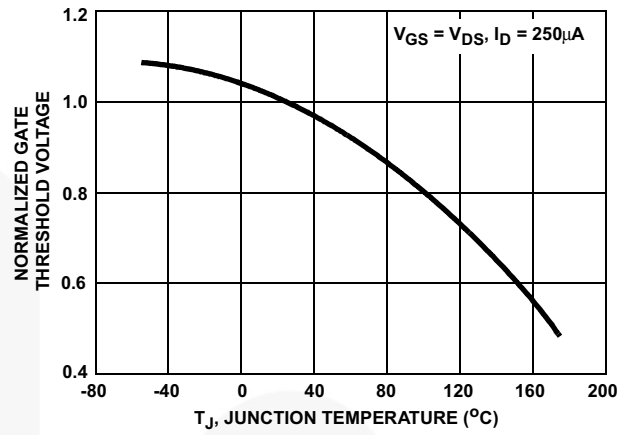


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

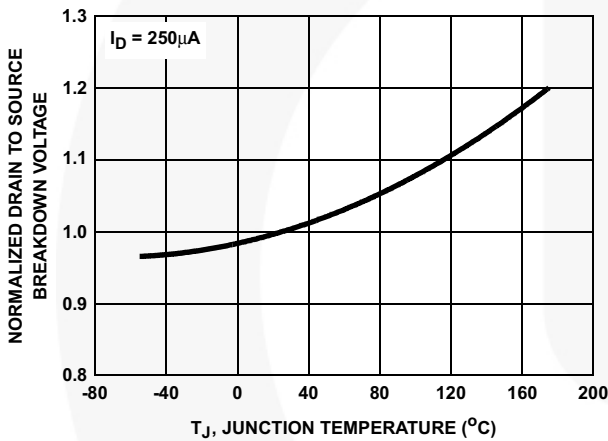


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

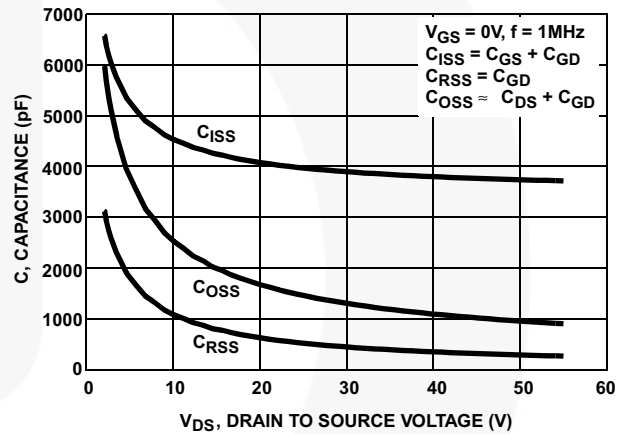
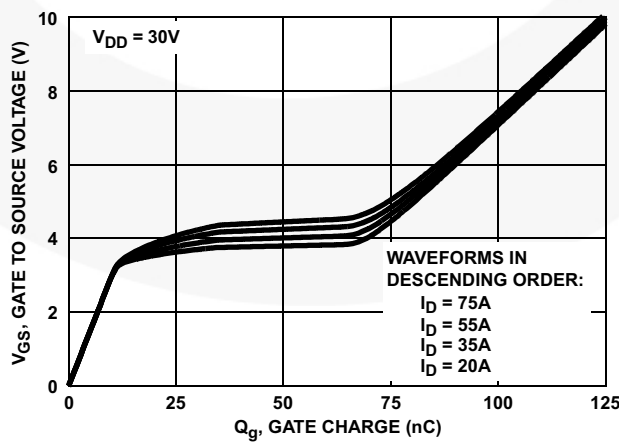


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

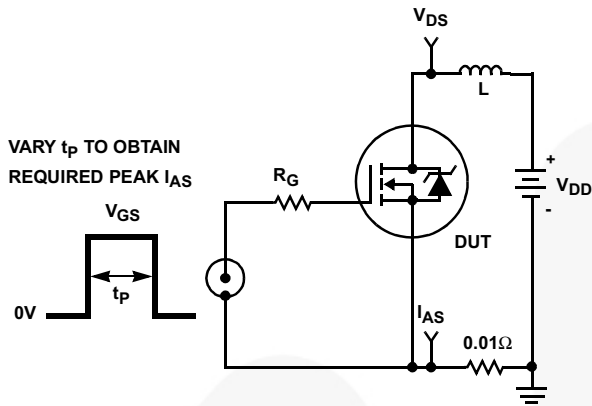


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

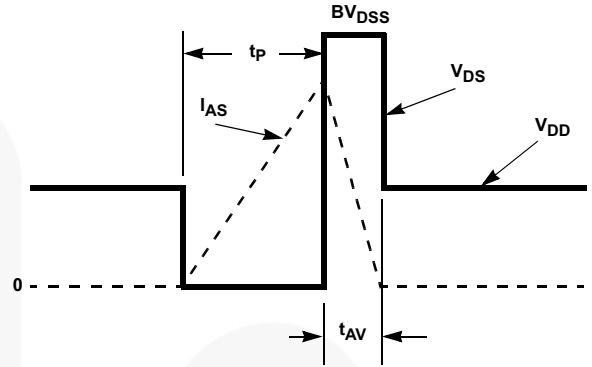


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

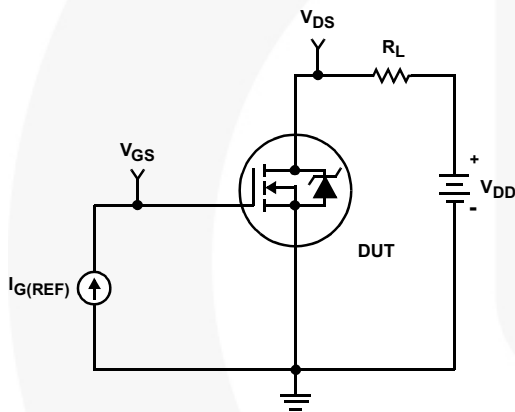


FIGURE 16. GATE CHARGE TEST CIRCUIT

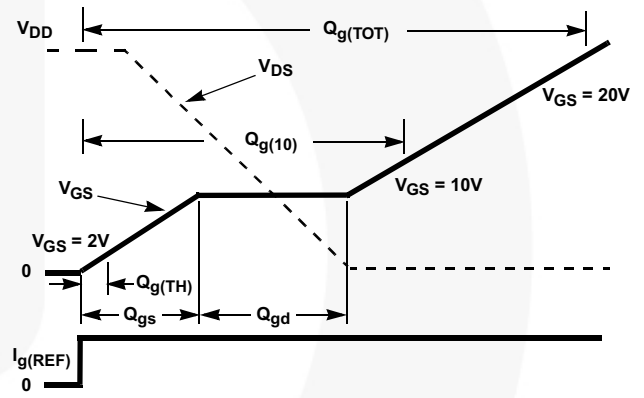


FIGURE 17. GATE CHARGE WAVEFORM

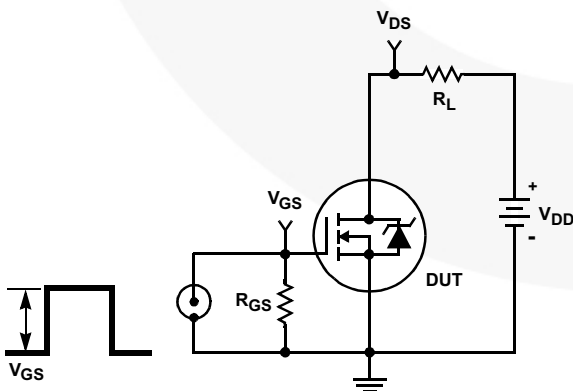


FIGURE 18. SWITCHING TIME TEST CIRCUIT

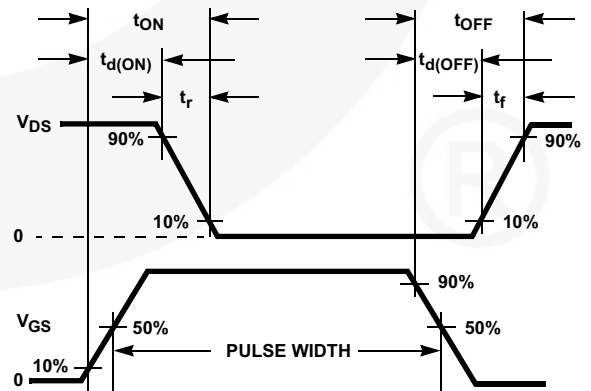


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

HUF75345G3, HUF75345P3, HUF75345S3S

SABER Electrical Model

REV 3 February 1999

template huf75345 n2, n1, n3

electrical n2, n1, n3

```
{
var i iscl
d..model dbodymod = (is = 6e-12, xti = 5, cjo = 5.5e-9, tt = 5.9e-8, m=0.5, vj=0.75)
d..model dbreakmod = ()
d..model dplcapmod = (cjo = 6.75e-9, is = 1e-30, m = 0.88, vj = 1.45, fc=0.5)
m..model mmedmod = (type=_n, vto = 2.93, kp = 13.75, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 3.23, kp = 96, is=1e-30, tox=1,
lambda = 0.06)
m..model mweakmod = (type=_n, vto = 2.35, kp = 0.02, is = 1e-30, tox = 1)
sw_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = -9, voff = -4)
sw_vcsp..model s1bmod = (ron = 1e-5, roff = 0.1, von = -4, voff = -9)
sw_vcsp..model s2amod = (ron = 1e-5, roff = 0.1, von = 0, voff = 0.5)
sw_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = 0.5, voff = 0)
```

c.ca n12 n8 = 5.55e-9

c.cb n15 n14 = 5.55e-9

c.cin n6 n8 = 3.45e-9

d.dbody n7 n71 = model=dbodymod

d.dbreak n72 n11 = model=dbreakmod

d.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1e-9

l.lgate n1 n9 = 2.6e-9

l.lsource n3 n7 = 1.1e-9

k.k1 i(l.lgate) i(l.lsource) = i(l.lgate), i(l.lsource), 0.0085

m.mmed n16 n6 n8 n8 = model=mmedmod, l = 1u, w = 1u

m.mstrong n16 n6 n8 n8 = model=mstrongmod, l = 1u, w = 1u

m.mweak n16 n21 n8 n8 = model=mweakmod, l = 1u, w = 1u

res.rbreak n17 n18 = 1, tc1 = 8e-4, tc2 = 4e-6

res.rbody n71 n5 = 1.4e-3, tc1 = 2.75e-3, tc2 = 5e-6

res.rdbreak n72 n5 = 2.8e-2, tc1 = -4e-3, tc2 = 1e-6

res.rdrain n50 n16 = 1e-4, tc1 = 1.5e-1, tc2 = 6.5e-4

res.rgate n9 n20 = 0.36

res.rldrain n2 n5 = 10

res.rlgate n1 n9 = 26

res.rlsource n3 n7 = 11

res.rslc1 n5 n51 = 1e-6, tc1 = 1e-4, tc2 = 1.05e-6

res.rslc2 n5 n50 = 1e3

res.rsource n8 n7 = 3.15e-3, tc1 = 1e-3, tc2 = 0

res.rvtemp n18 n19 = 1, tc1 = -2.75e-3, tc2 = 1.45e-6

res.rvthres n22 n8 = 1, tc1 = -1.5e-3, tc2 = -2.6e-5

spe.ebreak n11 n7 n17 n18 = 56.7

spe.eds n14 n8 n5 n8 = 1

spe.egs n13 n8 n6 n8 = 1

spe.esg n6 n10 n6 n8 = 1

spe.evtemp n20 n6 n18 n22 = 1

spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod

sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod

sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod

sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc = 1

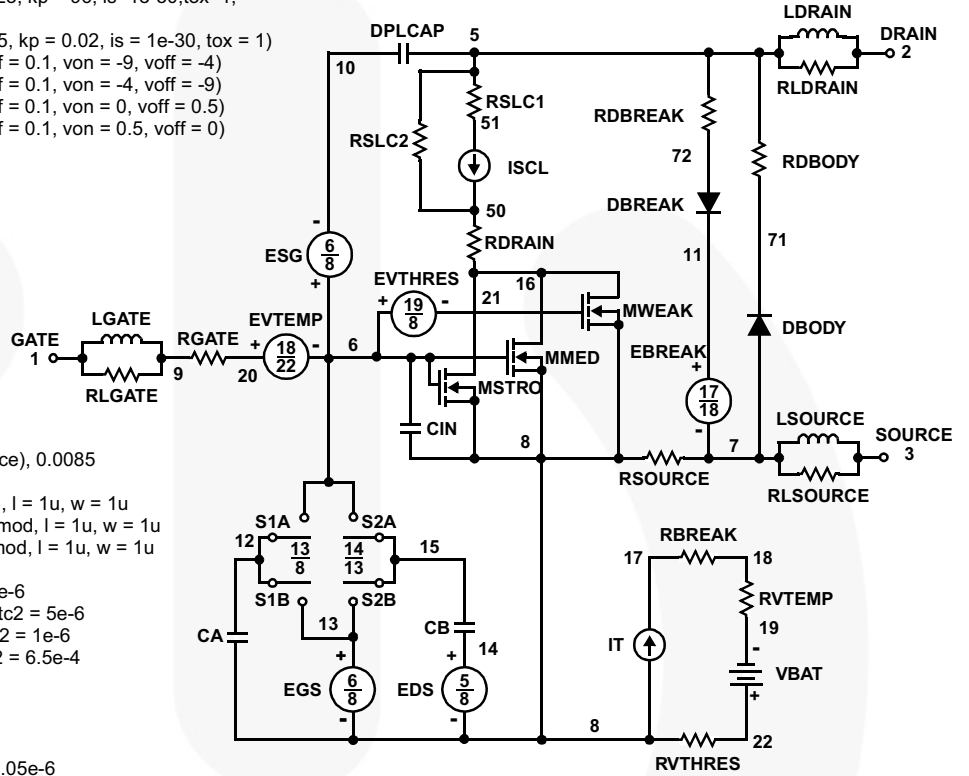
equations {

i (n51->n50) + = iscl

iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/500))** 3.5))

}

}



SPICE Thermal Model

REV 5 February 1999

HUF75345

CTHERM1 th 6 6.3e-3
CTHERM2 6 5 1.5e-2
CTHERM3 5 4 2.0e-2
CTHERM4 4 3 3.0e-2
CTHERM5 3 2 8.0e-2
CTHERM6 2 tl 1.5e-1

RTHERM1 th 6 5.0e-3
RTHERM2 6 5 1.8e-2
RTHERM3 5 4 5.0e-2
RTHERM4 4 3 8.5e-2
RTHERM5 3 2 1.0e-1
RTHERM6 2 tl 1.1e-1

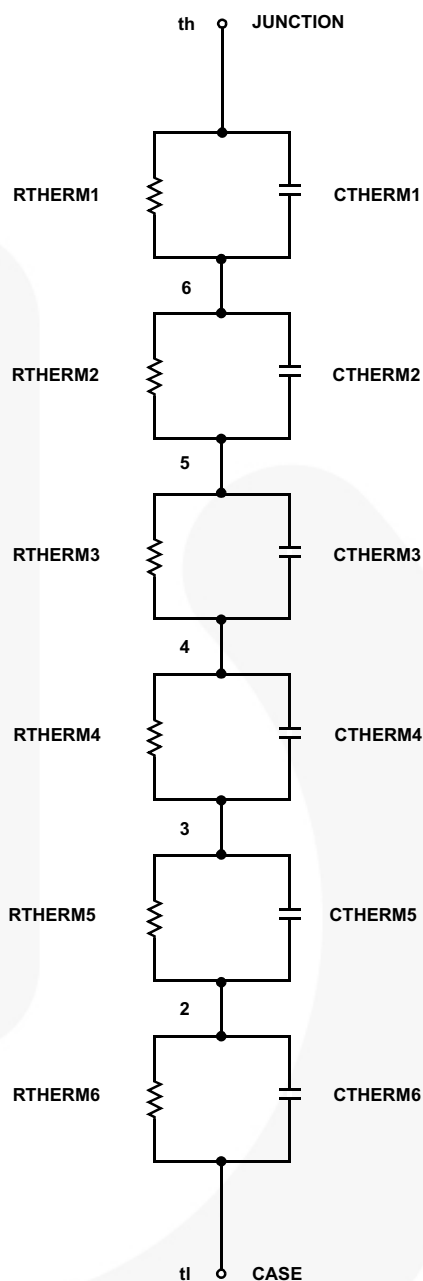
SABER Thermal Model

SABER thermal model HUF75345

template thermal_model th tl
thermal_c th, tl

```
{
  ctherm.ctherm1 th 6 = 6.3e-3
  ctherm.ctherm2 6 5 = 1.5e-2
  ctherm.ctherm3 5 4 = 2.0e-2
  ctherm.ctherm4 4 3 = 3.0e-2
  ctherm.ctherm5 3 2 = 8.0e-2
  ctherm.ctherm6 2 tl = 1.5e-1
```

```
  rtherm.rtherm1 th 6 = 5.0e-3
  rtherm.rtherm2 6 5 = 1.8e-2
  rtherm.rtherm3 5 4 = 5.0e-2
  rtherm.rtherm4 4 3 = 8.5e-2
  rtherm.rtherm5 3 2 = 1.0e-1
  rtherm.rtherm6 2 tl = 1.1e-1
}
```



Mechanical Dimensions

TO-220 3L

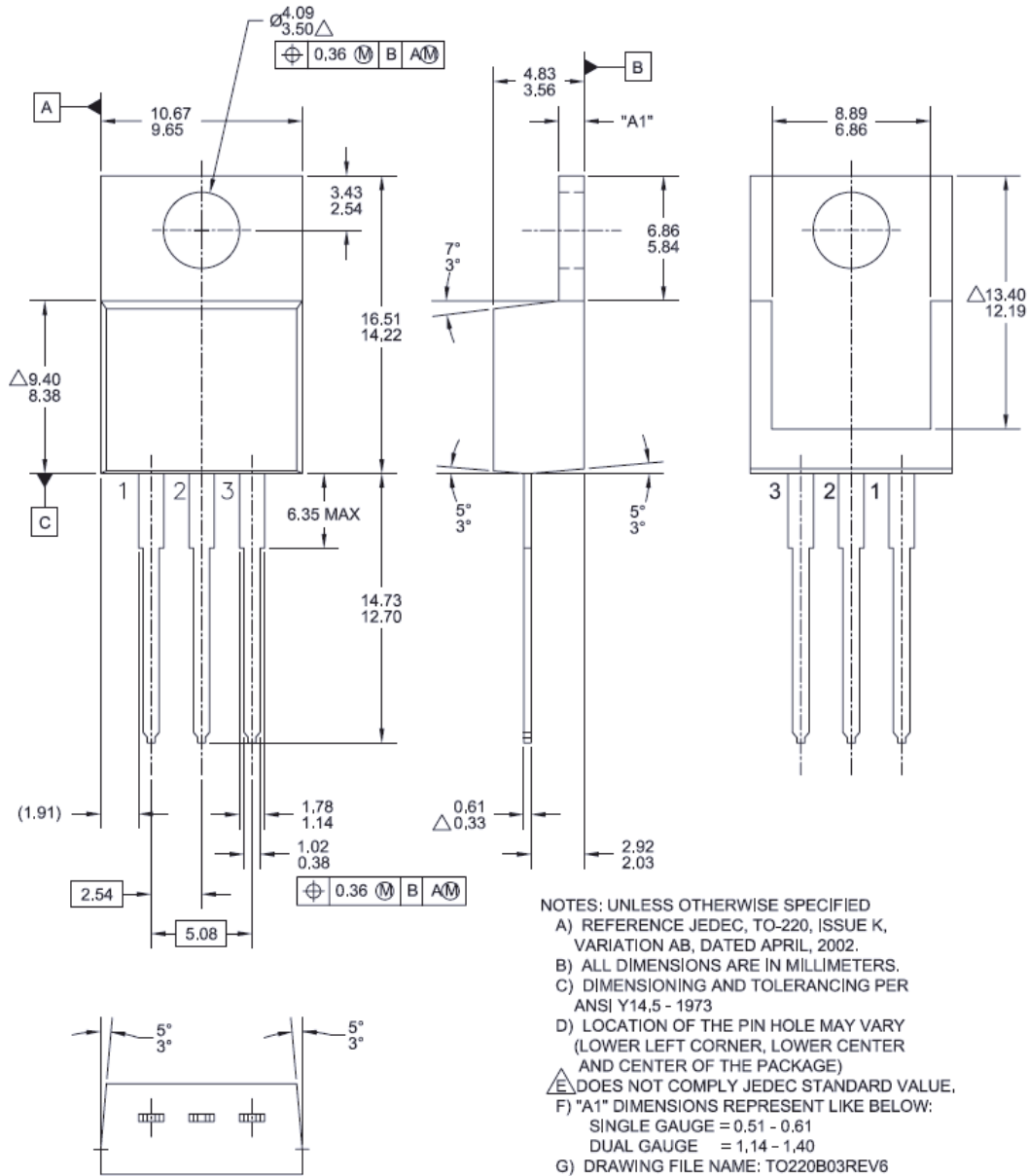


Figure 20. TO-220, Molded, 3Lead, Jedec Variation AB

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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Dimension in Millimeters



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CorePLUS™	Green FPS™	QS™	TinyBuck®
CorePOWER™	Green FPS™ e-Series™	Quiet Series™	TinyCalc™
CROSSVOLT™	Gmax™	RapidConfigure™	TinyLogic®
CTL™	GTO™	ISOPLANAR™	TINYOPTO™
Current Transfer Logic™	IntelliMAX™	Saving our world, 1mW/W/kW at a time™	TinyPower™
DEUXPEED®	ISOPLANAR™	SignalWise™	TinyPWM™
Dual Cool™	Marking Small Speakers Sound Louder and Better™	SmartMax™	TinyWire™
EcoSPARK®	MegaBuck™	SMART START™	TranSiC™
EfficientMax™	MICROCOUPLER™	Solutions for Your Success™	TriFault Detect™
ESBC™	MicroFET™	SPM®	TRUECURRENT®*
	MicroPak™	STEALTH™	µSerDes™
Fairchild®	MicroPak2™	SuperFET®	
Fairchild Semiconductor®	MillerDrive™	SuperSOT™-3	UHC®
FACT Quiet Series™	MotionMax™	SuperSOT™-6	Ultra FRFET™
FACT®	mWSaver®	SuperSOT™-8	UniFET™
FAST®	OptoHiT™	SupreMOS®	VCX™
FastvCore™	OPTOLOGIC®	SyncFET™	VisualMax™
FETBench™	OPTOPLANAR®		VoltagePlus™
FPS™			XS™

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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