

+/- 15kV ESD Protected, +3V to +5.5V, Low Power, 250kbps, RS-232 Transmitters/Receivers

The Intersil ICL32X7E devices are 3V to 5.5V powered RS-232 transmitters (five)/receivers (three) which meet EIA/TIA-232 and V.28/V.24 specifications, even at $V_{CC} = 3.0V$. Additionally, they provide $\pm 15kV$ ESD protection (IEC61000-4-2 Air Gap) and $\pm 15kV$ Human Body Model protection on transmitter outputs and receiver inputs (RS-232 pins). Targeted applications are ISDN Terminal Adaptors, PDAs, Palmtops, peripherals, and notebook and laptop computers where the low operational, and even lower standby, power consumption is critical. The ICL3217E's efficient on-chip charge pumps, coupled with an automatic powerdown function, reduces the standby supply current to a $1\mu A$ trickle. Small footprint packaging, and the use of small, low value capacitors ensure board space savings as well. Data rates greater than 250kbps are guaranteed at worst case load conditions. This family is fully compatible with 3.3V-only systems, mixed 3.3V and 5V systems, and 5V-only systems, and is a lower power, pin-for-pin replacement for '207E and '237E type devices.

The **ICL3217E** features an **automatic powerdown** function which powers down the on-chip power-supply and driver circuits. This occurs when an attached peripheral device is shut off or the RS-232 cable is removed, conserving system power automatically, without changes to the hardware or operating system. The ICL3217E powers up again when a valid RS-232 voltage is applied to any receiver input.

Table 1 summarizes the features of the devices represented by this data sheet, while application Note AN9863 summarizes the features of each device comprising the ICL32XXE 3V family.

Features

- Pb-Free Available as an Option (see Ordering Info)
- ESD Protection for RS-232 I/O Pins to $\pm 15kV$ (IEC61000)
- 5V Lower Power Replacement for MAX207E, HIN207E, HIN237E
- Meets EIA/TIA-232 and V.28/V.24 Specifications at 3V
- Latch-Up Free
- On-Chip Voltage Converters Require Only Four External $0.1\mu F$ Capacitors
- RS-232 Compatible with $V_{CC} = 2.7V$
- Automatic Powerdown ($I_{CC} = 1\mu A$, ICL3217E Only)
- Receiver Hysteresis For Improved Noise Immunity
- Guaranteed Minimum Data Rate 250kbps
- Guaranteed Minimum Slew Rate $6V/\mu s$
- Wide Power Supply Range Single +3V to +5.5V

Applications

- Battery Powered, Hand-Held, and Portable Equipment
- Laptop Computers, Notebooks, Palmtops
- Modems, Printers and other Peripherals
- ISDN Terminal Adaptors and Set Top Boxes
- Related Literature
 - Technical Brief TB363, *Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)*

Pinout

ICL3207E, ICL3217E (SOIC, SSOP)
TOP VIEW

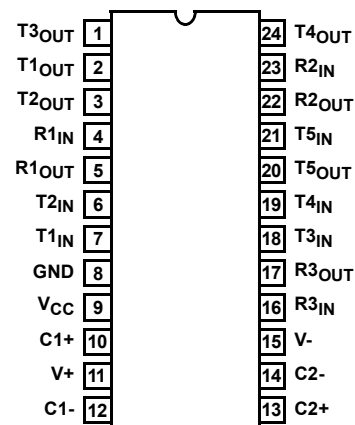


TABLE 1. SUMMARY OF FEATURES

PART NUMBER	NO. OF TX	NO. OF RX	NO. OF MONITOR RX (ROUTB)	DATA RATE (kbps)	RX ENABLE FUNCTION?	MANUAL POWER-DOWN?	AUTOMATIC POWERDOWN FUNCTION?
ICL3207E	5	3	0	250	NO	NO	NO
ICL3217E (No longer available or supported)	5	3	0	250	NO	NO	YES

Pin Descriptions

PIN	FUNCTION
V _{CC}	System power supply input (3.0V to 5.5V).
V+	Internally generated positive transmitter supply (+5.5V).
V-	Internally generated negative transmitter supply (-5.5V).
GND	Ground connection.
C1+	External capacitor (voltage doubler) is connected to this lead.
C1-	External capacitor (voltage doubler) is connected to this lead.
C2+	External capacitor (voltage inverter) is connected to this lead.
C2-	External capacitor (voltage inverter) is connected to this lead.
T _{IN}	TTL/CMOS compatible transmitter inputs.
T _{OUT}	±15kV ESD Protected, RS-232 level (nominally ±5.5V) transmitter outputs.
R _{IN}	±15kV ESD Protected, RS-232 compatible receiver inputs.
R _{OUT}	TTL/CMOS level receiver outputs.

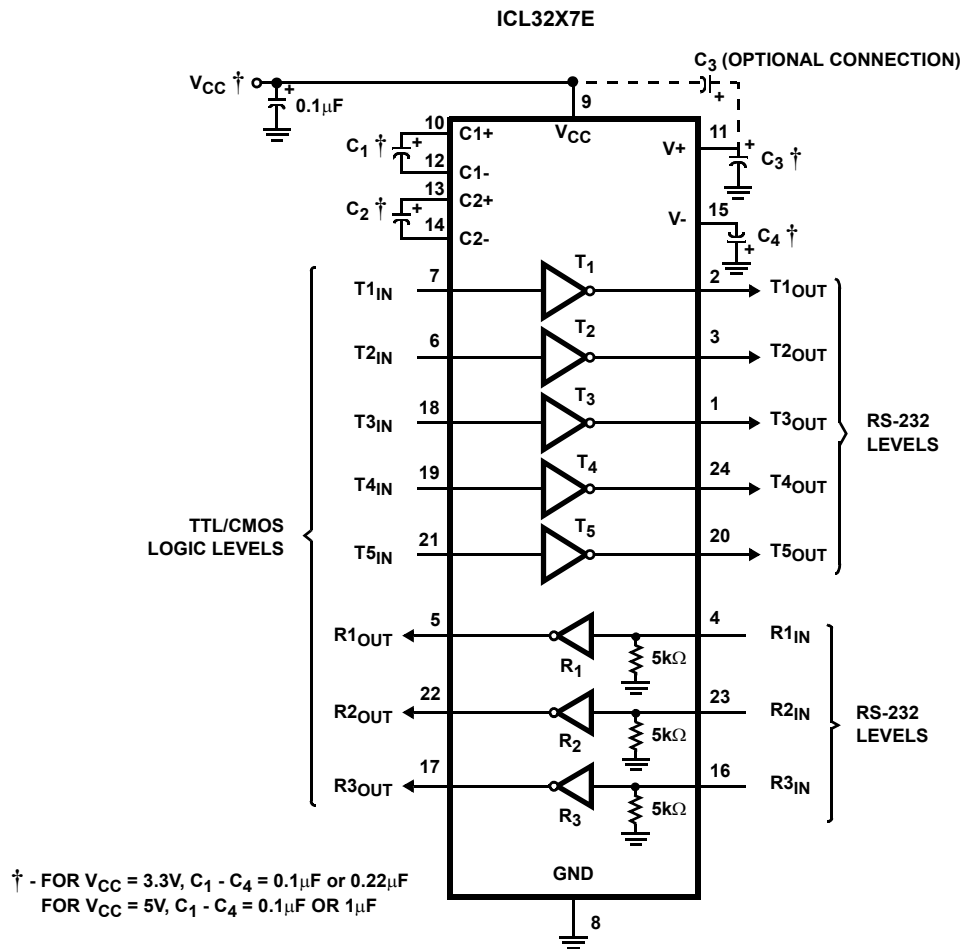
Ordering Information

PART NUMBER (Notes 1, 2)	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ICL3207ECAZ	0 to 70	24 Ld SSOP	M24.209
ICL3207ECBZ	0 to 70	24 Ld SOIC	M24.3
ICL3217ECAZ (No longer available, recommended replacement: ICL3238ECAZ)	0 to 70	24 Ld SSOP	M24.209
ICL3217ECBZ (No longer available, recommended replacement: ICL3238ECAZ)	0 to 70	24 Ld SOIC	M24.3
ICL3217EIAZ (No longer available, recommended replacement: ICL3238ECAZ)	-40 to 85	24 Ld SSOP	M24.209
ICL3217EIBZ (No longer available, recommended replacement: ICL3238ECAZ)	-40 to 85	24 Ld SOIC	M24.3

NOTES:

1. Most surface mount devices are available on tape and reel; add "-T" to suffix.
2. Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Typical Operating Circuit



Absolute Maximum Ratings

V _{CC} to Ground	-0.3V to 6V
V ₊ to Ground	-0.3V to 7V
V ₋ to Ground	+0.3V to -7V
V ₊ to V ₋	14V
Input Voltages	
T _{IN}	-0.3V to 6V
R _{IN}	±25V
Output Voltages	
T _{OUT}	±13.2V
R _{OUT}	-0.3V to V _{CC} + 0.3V
Short Circuit Duration	
T _{OUT}	Continuous
ESD Rating	See Specification Table

Thermal Information

Thermal Resistance (Typical, Note 3)	θ _{JA} (°/W)
24 Ld SOIC Package	75
24 Ld SSOP Package	100
Maximum Junction Temperature (Plastic Package)	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) (Lead Tips Only)	300°C

Operating Conditions

Temperature Range	
ICL32X7ECX	0°C to 70°C
ICL32X7EIX	-40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Test Conditions: V_{CC} = 3V to 5.5V, C₁ - C₄ = 0.1μF; Unless Otherwise Specified.
Typicals are at T_A = 25°C

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Supply Current, Automatic Powerdown	All R _{IN} Open (ICL3217E Only)	25	-	1.0	10	μA
Supply Current, Automatic Powerdown Disabled	All Outputs Unloaded	25	-	0.3	1.0	mA
TRANSMITTER INPUTS AND RECEIVER OUTPUTS						
Input Logic Threshold Low	T _{IN}	Full	-	-	0.8	V
Input Logic Threshold High	T _{IN}	V _{CC} = 3.3V	Full	2.0	-	V
		V _{CC} = 5.0V	Full	2.4	-	V
Input Leakage Current	T _{IN}	Full	-	±0.01	±1.0	μA
Output Leakage Current (ICL3217E Only)		Full	-	±0.05	±10	μA
Output Voltage Low	I _{OUT} = 1.6mA	Full	-	-	0.4	V
Output Voltage High	I _{OUT} = -1.0mA	Full	V _{CC} -0.6	V _{CC} -0.1	-	V
AUTOMATIC POWERDOWN (ICL3217E Only)						
Receiver Input Thresholds to Enable Transmitters	ICL3217E Powers Up (Figure 4)	Full	-2.7	-	2.7	V
Receiver Input Thresholds to Disable Transmitters	ICL3217E Powers Down (Figure 4)	Full	-0.3	-	0.3	V
Receiver Threshold to Transmitters Enabled Delay (t _{WU})		25	-	100	-	μs
Receiver Positive or Negative Threshold to Transmitters Disabled Delay		25	-	30	-	μs
RECEIVER INPUTS						
Input Voltage Range		Full	-25	-	25	V
Input Threshold Low	V _{CC} = 3.3V	25	0.6	1.2	-	V
	V _{CC} = 5.0V	25	0.8	1.5	-	V
Input Threshold High	V _{CC} = 3.3V	25	-	1.5	2.4	V
	V _{CC} = 5.0V	25	-	1.8	2.4	V

Electrical Specifications Test Conditions: $V_{CC} = 3V$ to $5.5V$, $C_1 - C_4 = 0.1\mu F$; Unless Otherwise Specified.
Typicals are at $T_A = 25^\circ C$ (Continued)

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS	
Input Hysteresis		25	-	0.3	-	V	
Input Resistance		25	3	5	7	kΩ	
TRANSMITTER OUTPUTS							
Output Voltage Swing	All Transmitter Outputs Loaded with 3kΩ to Ground	Full	±5.0	±5.4	-	V	
Output Resistance	V _{CC} = V+ = V- = 0V, Transmitter Output = ±2V	Full	300	10M	-	Ω	
Output Short-Circuit Current		Full	-	±35	±60	mA	
Output Leakage Current (ICL3217E Only)	V _{OUT} = ±12V, V _{CC} = 0V or 3V to 5.5V In Automatic Powerdown	Full	-	-	±25	μA	
TIMING CHARACTERISTICS							
Maximum Data Rate (One Transmitter Switching)	V _{CC} = 3.15V, C ₁ - C ₄ = 0.1μF, R _L = 3kΩ, C _L = 1000pF		Full	250	500	-	kbps
	V _{CC} = 3.0V, C ₁ - C ₄ = 0.22μF, R _L = 3kΩ, C _L = 1000pF		Full	250	286	-	kbps
	V _{CC} ≥ 4.5V, C ₁ - C ₄ = 0.1μF, R _L = 3kΩ, C _L = 1000pF		Full	250	310	-	kbps
Receiver Propagation Delay	Receiver Input to Receiver Output, C _L = 150pF	t _{PHL}	25	-	0.3	-	μs
		t _{PLH}	25	-	0.3	-	μs
Transmitter Skew	t _{PHL} - t _{PLH}		Full	-	200	1000	ns
Receiver Skew	t _{PHL} - t _{PLH}		Full	-	100	500	ns
Transition Region Slew Rate	V _{CC} = 3.3V, R _L = 3kΩ to 7kΩ, Measured From +3V to -3V or -3V to +3V	C _L = 200pF to 2500pF	25	4	15	30	V/μs
		C _L = 200pF to 1000pF	25	6	15	30	V/μs
ESD PERFORMANCE							
RS-232 Pins (T _{OUT} , R _{IN})	IEC61000-4-2, Air-Gap Discharge Method		25	-	±15	-	kV
	IEC61000-4-2, Contact Discharge Method		25	-	±8	-	kV
	Human Body Model		25	-	±15	-	kV
All Other Pins	Human Body Model		25	-	±2	-	kV

Detailed Description

The ICL32X7E interface ICs operate from a single $+3V$ to $+5.5V$ power supply, guarantee a 250kbps minimum data rate, require only four small external $0.1\mu F$ capacitors, feature low power consumption, and meet all EIA RS-232C and V.28 specifications. The circuit is divided into three sections: charge pump, transmitters and receivers.

Charge-Pump

Intersil's new ICL32XXE family utilizes regulated on-chip dual charge pumps as voltage doublers, and voltage inverters to generate $\pm 5.5V$ transmitter supplies from a V_{CC} supply as low as $3V$. This allows these devices to maintain RS-232 compliant output levels over the $\pm 10\%$ tolerance range of $3.3V$ powered systems. The efficient on-chip power supplies require only four small, external $0.1\mu F$ capacitors for the voltage doubler and inverter functions at $V_{CC} = 3.3V$. See the *Capacitor Selection* section, and Table 3 for capacitor recommendations for other operating conditions. The charge pumps operate discontinuously (i.e., they turn off as soon as the V_+ and V_- supplies are pumped up to the nominal values), resulting in significant power savings.

Transmitters

The transmitters are proprietary, low dropout, inverting drivers that translate TTL/CMOS inputs to EIA/TIA-232 output levels. Coupled with the on-chip $\pm 5.5V$ supplies, these transmitters deliver true RS-232 levels over a wide range of single supply system voltages.

ICL3217E transmitter outputs disable and assume a high impedance state when the device enters the automatic powerdown mode. These outputs may be driven to $\pm 12V$ when disabled.

Both devices guarantee a 250kbps data rate for full load conditions ($3k\Omega$ and $1000pF$), $V_{CC} \geq 3.0V$, with one transmitter operating at full speed. Under more typical conditions of $V_{CC} \geq 3.3V$, $R_L = 3k\Omega$, and $C_L = 250pF$, one transmitter easily operates at 800kbps.

Transmitter inputs float if left unconnected, and may cause I_{CC} increases. Connect unused inputs to GND for the best performance.

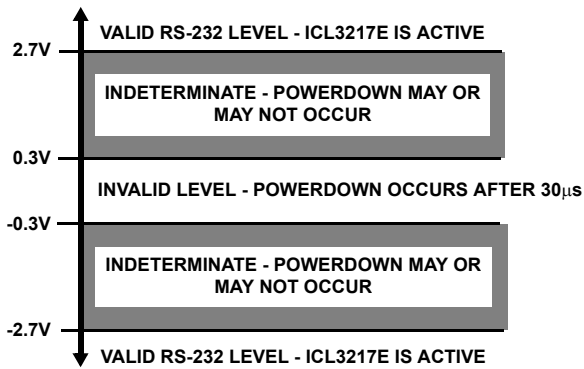


FIGURE 4. DEFINITION OF VALID RS-232 RECEIVER LEVELS

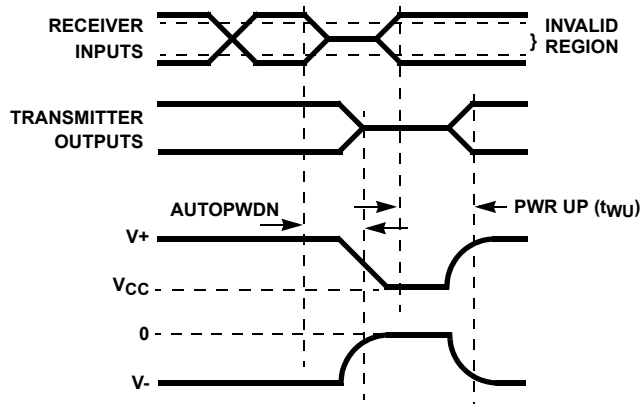


FIGURE 5. AUTOMATIC POWERDOWN TIMING DIAGRAM

This automatic powerdown feature provides additional system power savings without changes to the existing operating system or hardware.

Utilizing power management circuitry, to power down the rest of the communication circuitry (e.g., the UART) when the ICL3217E powers down, produces even greater power savings. Connecting a transition detector to the V- pin (see Figure 3) is an easy way for the power management logic to determine when the ICL3217E enters and exits powerdown.

Capacitor Selection

The charge pumps require 0.1µF, or greater, capacitors for 3.3V operation. With 0.1µF capacitors, five percent tolerance supplies (e.g., 3.14V minimum) deliver greater than ±5V transmitter swings at full data rate, while ten percent tolerance supplies (e.g., 2.97V minimum) deliver ±4.95V transmitter swings. If greater than ±5V transmitter swings are required with a 10% tolerance 3.3V supply, 0.22µF capacitors are recommended (see Table 3). Existing 5V applications typically utilize either 0.1µF or 1µF capacitors, and the ICL32X7E works well with either value. New 5V designs should use 0.22µF capacitors for the best results. For other supply voltages refer to Table 3 for capacitor values. Do not use values smaller than those listed in Table 3. Increasing the capacitor values (by a factor of two)

reduces ripple on the transmitter outputs and slightly reduces power consumption. C₂, C₃, and C₄ can be increased without increasing C₁'s value, however, do not increase C₁ without also increasing C₂, C₃, and C₄ to maintain the proper ratios (C₁ to the other capacitors).

When using minimum required capacitor values, make sure that capacitor values do not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's equivalent series resistance (ESR) usually rises at low temperatures and it influences the amount of ripple on V₊ and V₋.

TABLE 3. REQUIRED CAPACITOR VALUES

V _{CC} (V)	C ₁ (µF)	C ₂ , C ₃ , C ₄ (µF)
3.15 to 3.6	0.1	0.1
3.0 to 3.6	0.22	0.22
4.5 to 5.5	0.1 to 1.0	0.1 to 1.0
3.0 to 5.5	0.22	0.22

Power Supply Decoupling

In most circumstances a 0.1µF bypass capacitor is adequate. In applications that are particularly sensitive to power supply noise, decouple V_{CC} to ground with a capacitor of the same value as the charge-pump capacitor C₁. Connect the bypass capacitor as close as possible to the IC.

Transmitter Outputs when Exiting Powerdown

Figure 6 shows the response of two ICL3217E transmitter outputs when exiting powerdown mode. As they activate, the two transmitter outputs properly go to opposite RS-232 levels, with no glitching, ringing, nor undesirable transients. Each transmitter is loaded with 3kΩ in parallel with 2500pF. Note that the transmitters enable only when the magnitude of the supplies exceed approximately 3V.

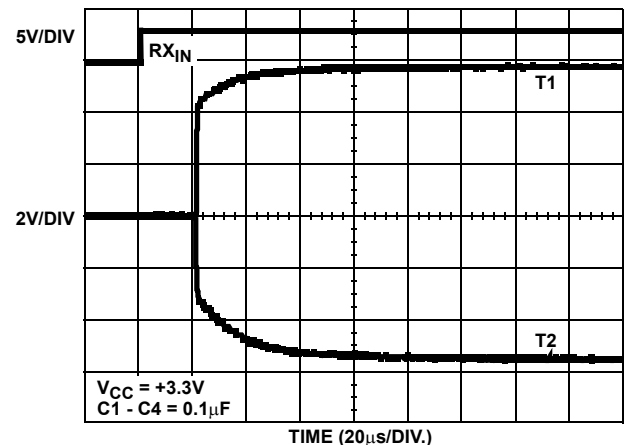


FIGURE 6. TRANSMITTER OUTPUTS WHEN EXITING POWERDOWN (ICL3217E ONLY)

Operation down to 2.7V

ICL32X7E transmitter outputs meet RS-562 levels ($\pm 3.7V$) with V_{CC} as low as 2.7V. RS-562 levels typically ensure interoperability with RS-232 devices.

High Data Rates

The ICL32XX maintain the RS-232 $\pm 5V$ minimum transmitter output voltages even at high data rates. Figure 7 details a transmitter loopback test circuit, and Figure 8 illustrates the loopback test result at 120kbps. For this test, all transmitters were simultaneously driving RS-232 loads in parallel with 1000pF, at 120kbps. Figure 9 shows the loopback results for a single transmitter driving 1000pF and an RS-232 load at 250kbps. The static transmitters were also loaded with an RS-232 receiver.

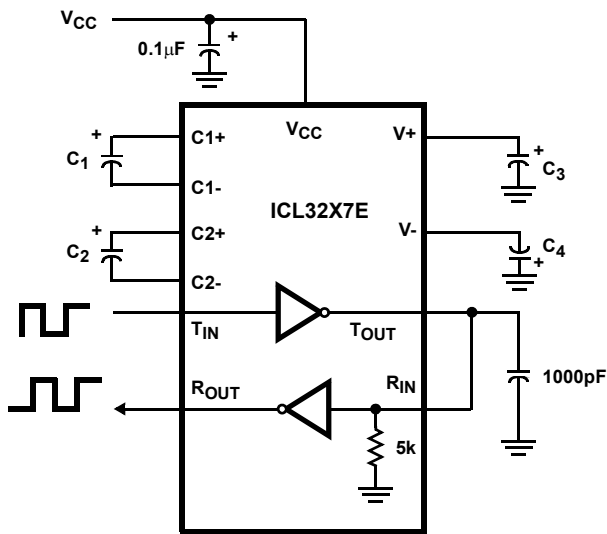


FIGURE 7. TRANSMITTER LOOPBACK TEST CIRCUIT

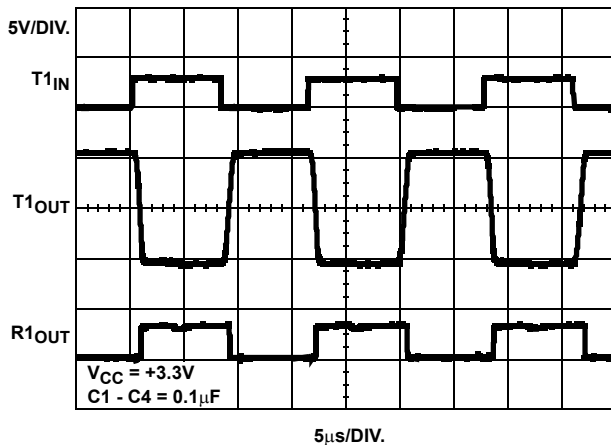


FIGURE 8. LOOPBACK TEST AT 120kbps

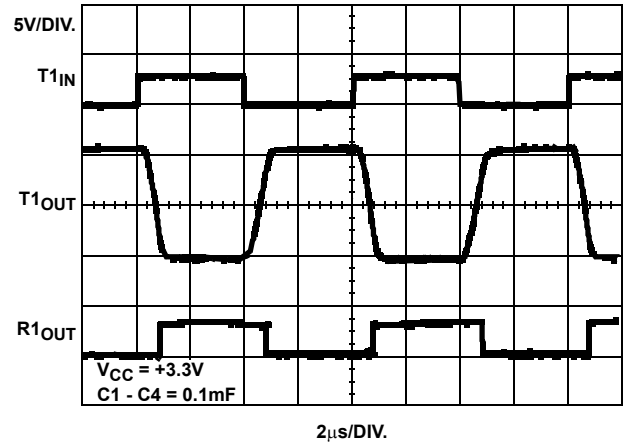


FIGURE 9. LOOPBACK TEST AT 250kbps

Interconnection with 3V and 5V Logic

The ICL32X7E directly interface with 5V CMOS and TTL logic families. Nevertheless, with the ICL32X7E at 3.3V, and the logic supply at 5V, AC, HC, and CD4000 outputs can drive ICL32X7E inputs, but ICL32X7E outputs do not reach the minimum V_{IH} for these logic families. See Table 4 for more information.

TABLE 4. LOGIC FAMILY COMPATIBILITY WITH VARIOUS SUPPLY VOLTAGES

SYSTEM POWER-SUPPLY VOLTAGE (V)	V_{CC} SUPPLY VOLTAGE (V)	COMPATIBILITY
3.3	3.3	Compatible with all CMOS families.
5	5	Compatible with all TTL and CMOS logic families.
5	3.3	Compatible with ACT and HCT CMOS, and with TTL. ICL32X7E outputs are incompatible with AC, HC, and CD4000 CMOS inputs.

$\pm 15kV$ ESD Protection

All pins on ICL32XX devices include ESD protection structures, but the ICL32X7E incorporate advanced structures which allow the RS-232 pins (transmitter outputs and receiver inputs) to survive ESD events up to $\pm 15kV$. The RS-232 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, protect without allowing any latchup mechanism to activate, and don't interfere with RS-232 signals as large as $\pm 25V$.

Human Body Model (HBM) Testing

As the name implies, this test method emulates the ESD event delivered to an IC during human handling. The tester delivers the charge through a 1.5k Ω current limiting resistor, making the test less severe than the IEC61000 test which utilizes a 330 Ω limiting resistor. The HBM method determines an IC's ability to withstand the ESD transients typically present during handling and manufacturing. Due to the random nature of these events, each pin is tested with respect to all other pins. The RS-232 pins on "E" family devices can withstand HBM ESD events to ± 15 kV.

IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-232 pins in this case), and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than

the HBM test. The extra ESD protection built into this device's RS-232 pins allows the design of equipment meeting level 4 criteria without the need for additional board level protection on the RS-232 port.

AIR-GAP DISCHARGE TEST METHOD

For this test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc., so it is difficult to obtain repeatable results. The "E" device RS-232 pins withstand ± 15 kV air-gap discharges.

CONTACT DISCHARGE TEST METHOD

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ± 8 kV. All "E" family devices survive ± 8 kV contact discharges on the RS-232 pins.

Typical Performance Curves $V_{CC} = 3.3V$, $T_A = 25^\circ C$

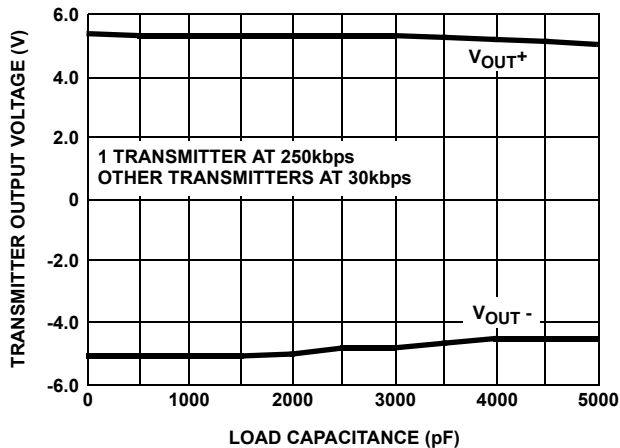


FIGURE 10. TRANSMITTER OUTPUT VOLTAGE vs LOAD CAPACITANCE

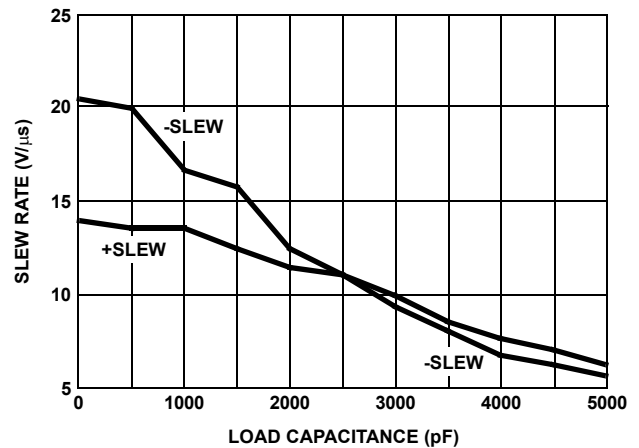


FIGURE 11. SLEW RATE vs LOAD CAPACITANCE

Typical Performance Curves $V_{CC} = 3.3V$, $T_A = 25^\circ C$ (Continued)

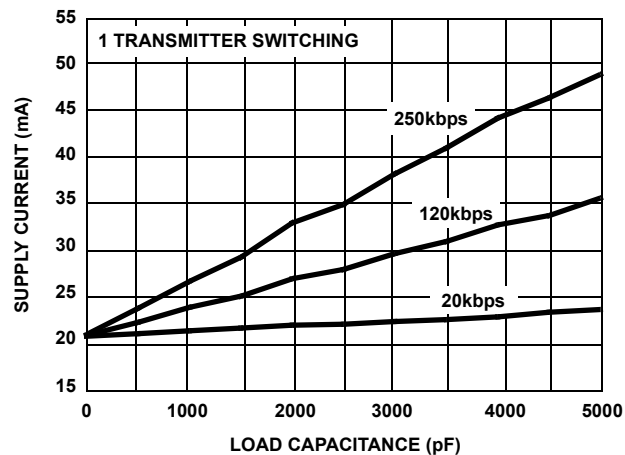


FIGURE 12. SUPPLY CURRENT vs LOAD CAPACITANCE WHEN TRANSMITTING DATA

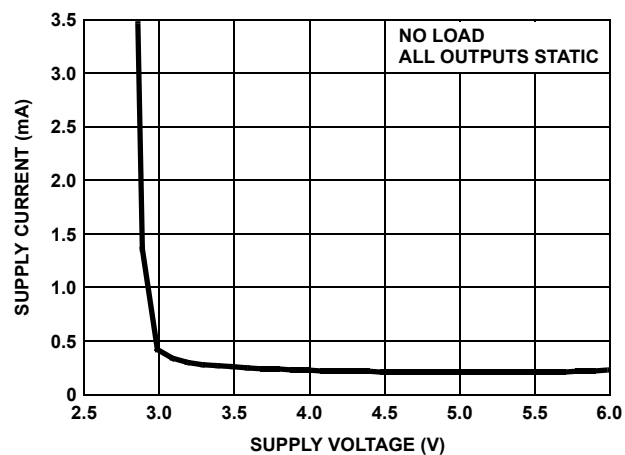


FIGURE 13. SUPPLY CURRENT vs SUPPLY VOLTAGE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

ICL3207E: 469

ICL3217E: 488

PROCESS:

Si Gate CMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
August 21, 2015	FN4914.6	Updated Ordering Information table on page 2. Added Revision History and About Intersil sections. Updated Package Outline Drawing M24.3 to the latest revision updates are as follows: -Revision 0 to Revision 1, Removed μ symbol which is overlapping the alpha symbol in the diagram. -Revision 1 to Revision 2, Updated to new POD standard by removing table listing dimensions and putting dimensions on drawing. Added Land Pattern.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

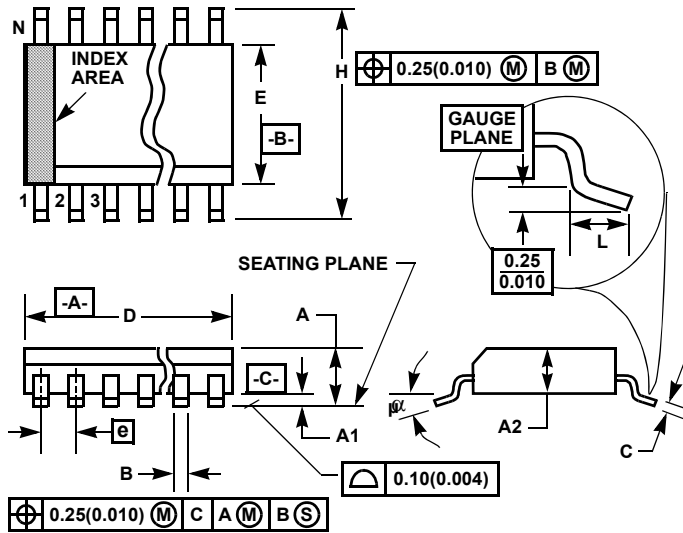
Reliability reports are also available from our website at www.intersil.com/support

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9001** quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site www.intersil.com

Shrink Small Outline Plastic Packages (SSOP)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M24.209 (JEDEC MO-150-AG ISSUE B) 24 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.312	0.334	7.90	8.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	24		24		7
α	0°	8°	0°	8°	-

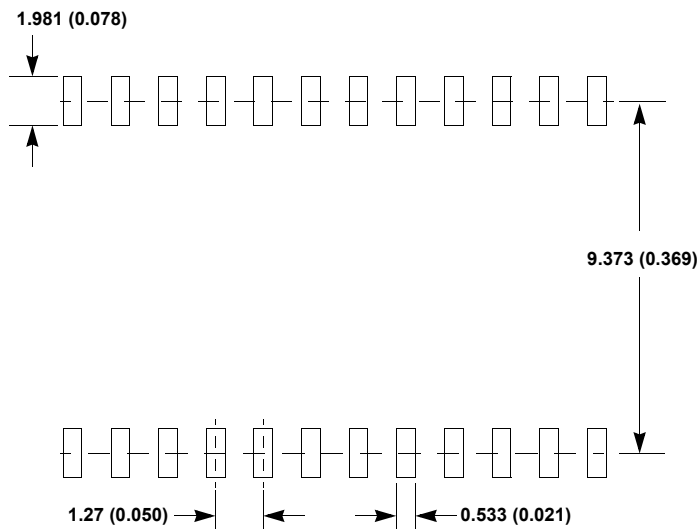
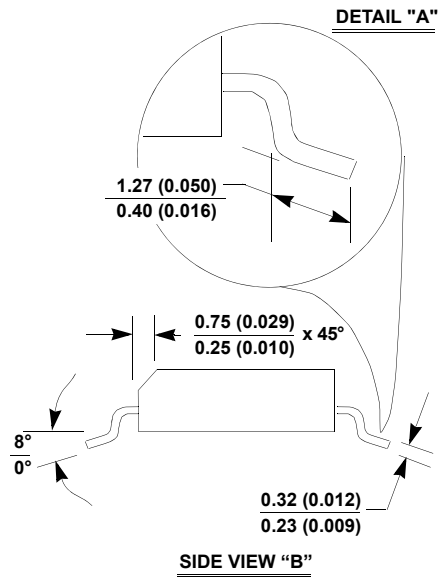
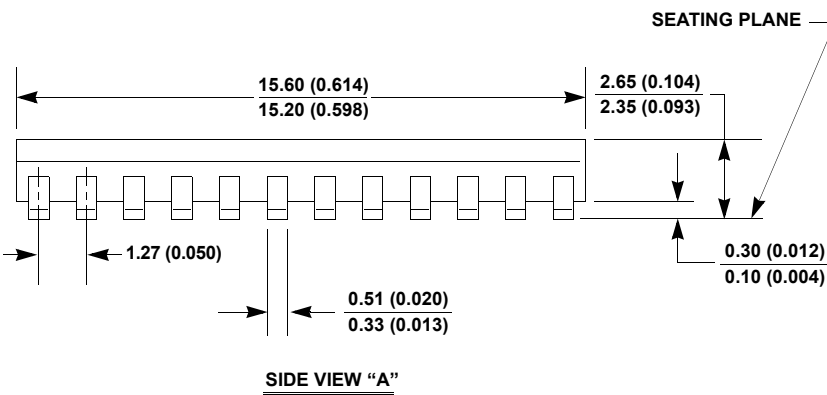
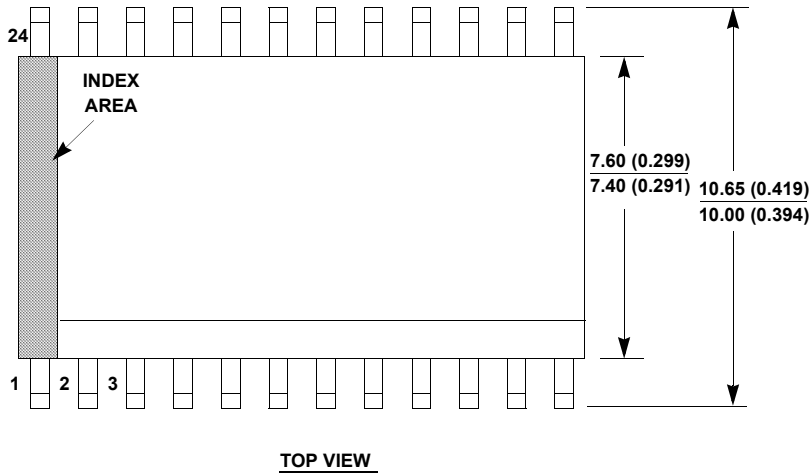
Rev. 1 3/95

Package Outline Drawing

M24.3

24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE (SOIC)

Rev 2, 3/11



NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions in () are not necessarily exact.
8. This outline conforms to JEDEC publication MS-013-AD ISSUE C.