

TOSHIBA CMOS Digital Integrated Circuit   Silicon Monolithic

# **TC7MH4040FK**

## **12-Stage Ripple-Carry Binary Counter**

The TC7MH4040FK is an advanced high speed CMOS 12-stage ripple-carry binary counter fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent bipolar schottky TTL while maintaining the CMOS low power dissipation.

Setting CLR to high resets the counter to low.

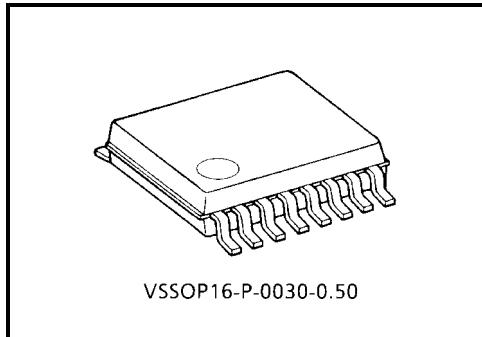
A negative transition on the CK input brings one increment into the counter.

This counter provides all divided output stages, and at Q12, a 1/4096 divided frequency will be output.

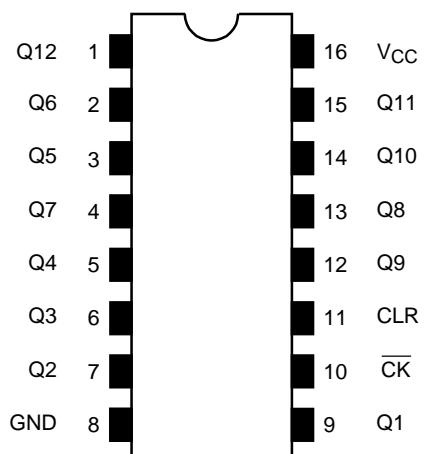
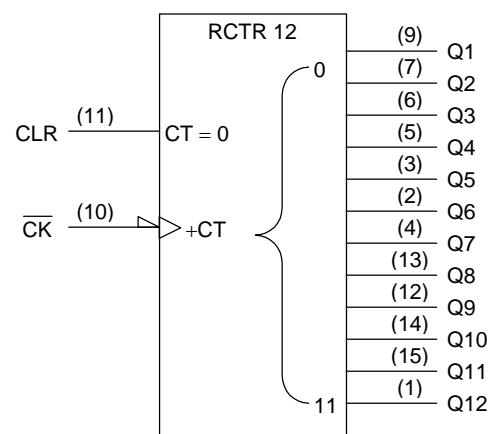
An input protection circuit ensures that 0 to 7 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

## **Features**

- High speed:  $f_{max} = 210$  MHz (typ.) ( $V_{CC} = 5$  V)
- Low power dissipation:  $I_{CC} = 4$   $\mu$ A (max) ( $T_a = 25^\circ C$ )
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$  (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC\ (opr)} = 2\sim 5.5$  V
- Low noise:  $V_{OLP} = 1.5$  V (max)
- Pin and function compatible with 74HC4040



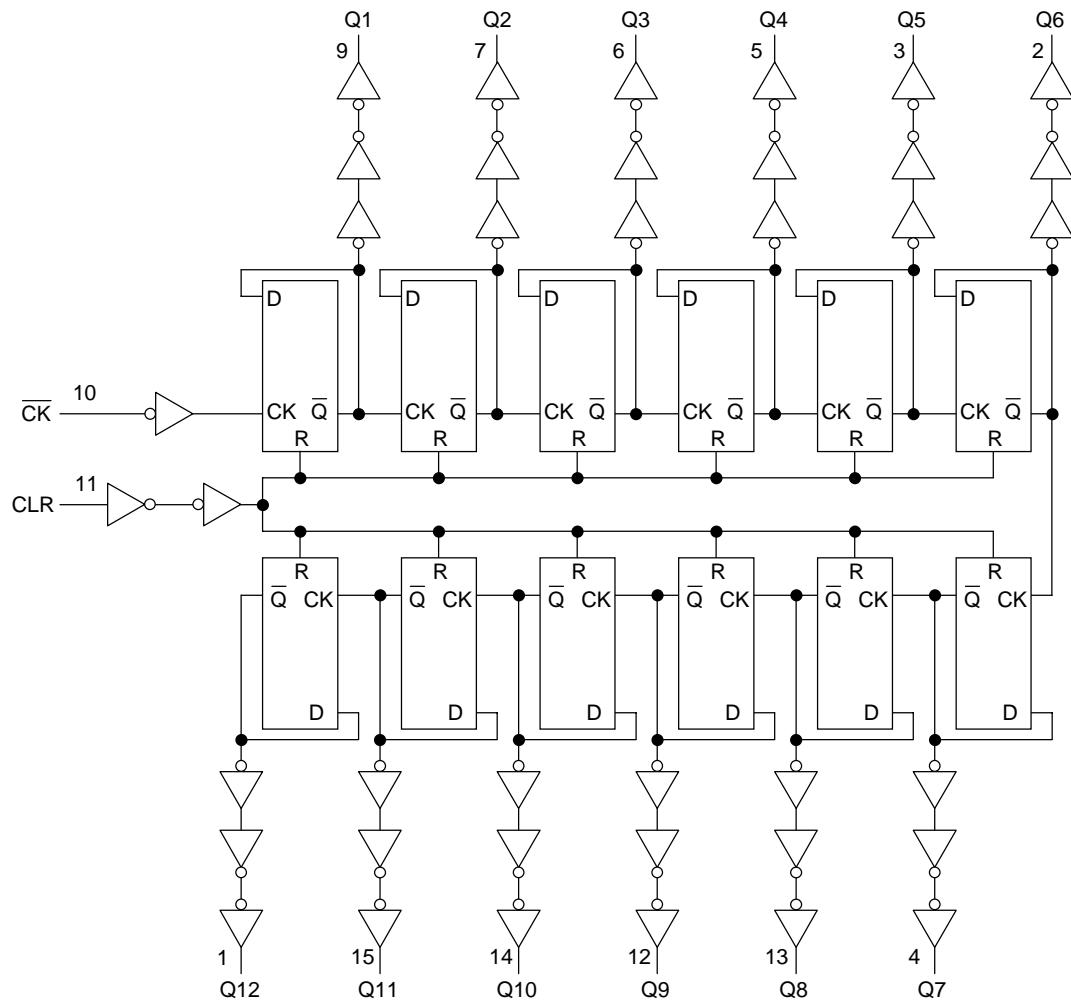
Weight: 0.02 g (typ.)

**Pin Assignment (top view)****IEC Logic Level****Truth Table**

$\overline{CK}$	CLR	Outputs
X	H	All outputs = "L"
	L	No change
	L	Advance to next stage

X: Don't care

## System Diagram



## Maximum Ratings

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5~7.0	V
DC input voltage	$V_{IN}$	-0.5~7.0	V
DC output voltage	$V_{OUT}$	-0.5~ $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	-20	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 100$	mA
Power dissipation	$P_D$	180	mW
Storage temperature	$T_{stg}$	-65~150	°C

## Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2.0~5.5	V
Input voltage	$V_{IN}$	0~5.5	V
Output voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating temperature	$T_{opr}$	-40~85	°C
Input rise and fall time	$dt/dv$	0~100 ( $V_{CC} = 3.3 \pm 0.3$ V)	ns/V
		0~20 ( $V_{CC} = 5 \pm 0.5$ V)	

## Electrical Characteristics

## DC Characteristics

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40~85°C		Unit	
			$V_{CC}$ (V)	Min	Typ.	Max	Min		
Input voltage	High level	$V_{IH}$	—	2.0	1.50	—	—	1.50	V
				3.0~5.5	$V_{CC} \times 0.7$	—	—	$V_{CC} \times 0.7$	
	Low level	$V_{IL}$	—	2.0	—	—	0.50	—	
				3.0~5.5	—	—	$V_{CC} \times 0.3$	—	
Output voltage	High level	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu A$	2.0	1.9	2.0	—	V
					3.0	2.9	3.0	—	
					4.5	4.4	4.5	—	
				$I_{OH} = -4 mA$	3.0	2.58	—	2.48	
				$I_{OH} = -8 mA$	4.5	3.94	—	3.80	
	Low level	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu A$	2.0	—	0	0.1	
					3.0	—	0	0.1	
					4.5	—	0	0.1	
				$I_{OL} = 4 mA$	3.0	—	0.36	—	
				$I_{OL} = 8 mA$	4.5	—	0.36	—	
Input leakage current	$I_{IN}$	$V_{IN} = 5.5$ V or GND	0~5.5	—	—	$\pm 0.1$	—	$\pm 1.0$	μA
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	—	40.0	μA

Timing Requirements (Input:  $t_r = t_f = 3$  ns)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40~85°C		Unit
			$V_{CC}$ (V)	Typ.	Limit	Limit	
Minimum pulse width ( $\overline{CK}$ )	$t_w$ (L) $t_w$ (H)	—	3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum pulse width (CLR)	$t_w$ (H)	—	3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum removal time	$t_{rem}$	—	3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	5.0	5.0	

AC Characteristics (Input:  $t_r = t_f = 3$  ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40~85°C		Unit
			V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Typ.	Max	
Propagation delay time ( $\overline{C_K} - Q_1$ )	$t_{pLH}$ $t_{pHL}$	—	3.3 ± 0.3	15	—	7.5	11.9	1.0 14.0
				50	—	10.0	15.4	1.0 17.5
			5.0 ± 0.5	15	—	4.8	7.3	1.0 8.5
				50	—	6.3	9.3	1.0 10.5
Propagation delay time ( $Q_n - Q_{n+1}$ )	$\Delta t_{pd}$	—	3.3 ± 0.3	50	—	2.4	4.4	1.0 5.0
			5.0 ± 0.5	50	—	1.6	3.1	1.0 3.5
Propagation delay time (CLR - Q)	$t_{pHL}$	—	3.3 ± 0.3	15	—	8.3	12.8	1.0 15.0
				50	—	10.8	16.3	1.0 18.5
			5.0 ± 0.5	15	—	5.6	8.6	1.0 10.0
				50	—	7.1	10.6	1.0 12.0
Maximum clock frequency	$f_{max}$	—	3.3 ± 0.3	15	75	140	—	75 —
				50	55	80	—	50 —
			5.0 ± 0.5	15	150	210	—	125 —
				50	95	125	—	80 —
Input capacitance	C <sub>IN</sub>	—	—	—	—	4	10	— 10 pF
Power dissipation capacitance	C <sub>PD</sub>	(Note)	—	—	21	—	—	— pF

Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

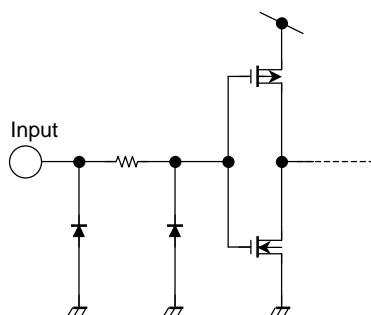
Average operating current can be obtained by the equation:

$$I_{CC} (\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Noise Characteristics (Input:  $t_r = t_f = 3$  ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			V <sub>CC</sub> (V)	Typ.	Limit	
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50 pF	5.0	1.2	1.5	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	C <sub>L</sub> = 50 pF	5.0	-1.2	-1.5	V
Minimum high level dynamic input voltage V <sub>IH</sub>	V <sub>IHD</sub>	C <sub>L</sub> = 50 pF	5.0	—	3.5	V
Minimum low level dynamic input voltage V <sub>IL</sub>	V <sub>ILD</sub>	C <sub>L</sub> = 50 pF	5.0	—	1.5	V

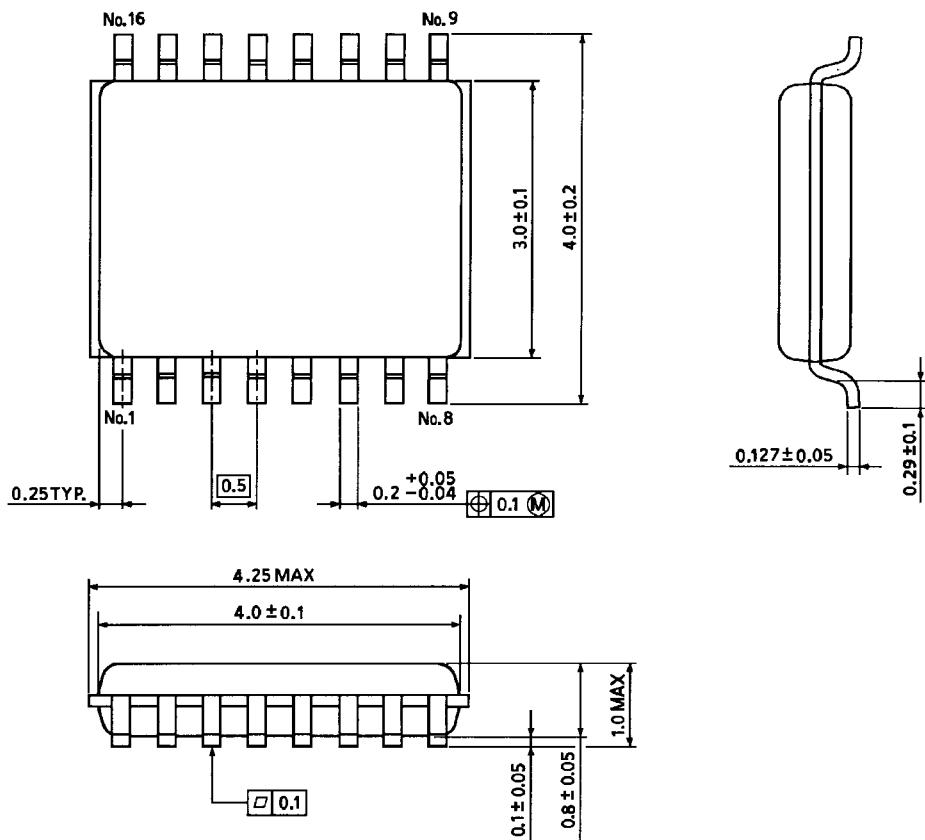
## Input Equivalent Circuit



**Package Dimensions**

VSSOP16-P-0030-0.50

Unit : mm



Weight: 0.02 g (typ.)

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