

# EH3525TS-5.000M

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## REGULATORY COMPLIANCE (Data Sheet downloaded on Dec 26, 2018)


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## ITEM DESCRIPTION

Quartz Crystal Clock Oscillators XO (SPXO) HCMOS/TTL (CMOS) 5.0Vdc 4 Pad 3.2mm x 5.0mm Ceramic Surface Mount (SMD) 5.000MHz  $\pm 25$ ppm 0°C to +70°C

## ELECTRICAL SPECIFICATIONS

|                                       |                                                                                                                                                                                                                                        |
|---------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Nominal Frequency                     | 5.000MHz                                                                                                                                                                                                                               |
| Frequency Tolerance/Stability         | $\pm 25$ ppm Maximum (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°C, Shock, and Vibration) |
| Aging at 25°C                         | $\pm 5$ ppm/year Maximum                                                                                                                                                                                                               |
| Operating Temperature Range           | 0°C to +70°C                                                                                                                                                                                                                           |
| Supply Voltage                        | 5.0Vdc $\pm 10\%$                                                                                                                                                                                                                      |
| Input Current                         | 50mA Maximum (No Load)                                                                                                                                                                                                                 |
| Output Voltage Logic High (Voh)       | 2.4Vdc Minimum with TTL Load, Vdd-0.4Vdc Minimum with HCMOS Load (IOH = -16mA)                                                                                                                                                         |
| Output Voltage Logic Low (Vol)        | 0.4Vdc Maximum with TTL Load, 0.5Vdc Maximum with HCMOS Load (IOL = +16mA)                                                                                                                                                             |
| Rise/Fall Time                        | 6nSec Maximum (Measured at 0.8Vdc to 2.0Vdc with TTL Load or at 20% to 80% of waveform with HCMOS Load)                                                                                                                                |
| Duty Cycle                            | 50 $\pm 10\%$ (Measured at 1.4Vdc with TTL Load or at 50% of waveform with HCMOS Load)                                                                                                                                                 |
| Load Drive Capability                 | 10TTL Load or 50pF HCMOS Load Maximum                                                                                                                                                                                                  |
| Output Logic Type                     | CMOS                                                                                                                                                                                                                                   |
| Pin 1 Connection                      | Tri-State (Disabled Output: High Impedance)                                                                                                                                                                                            |
| Tri-State Input Voltage (Vih and Vil) | +2.2Vdc Minimum to enable output, +0.8Vdc Maximum to disable output (High Impedance), No Connect to enable output.                                                                                                                     |
| Absolute Clock Jitter                 | $\pm 250$ pSec Maximum, $\pm 100$ pSec Typical                                                                                                                                                                                         |
| One Sigma Clock Period Jitter         | $\pm 50$ pSec Maximum, $\pm 30$ pSec Typical                                                                                                                                                                                           |
| Start Up Time                         | 10mSec Maximum                                                                                                                                                                                                                         |
| Storage Temperature Range             | -55°C to +125°C                                                                                                                                                                                                                        |

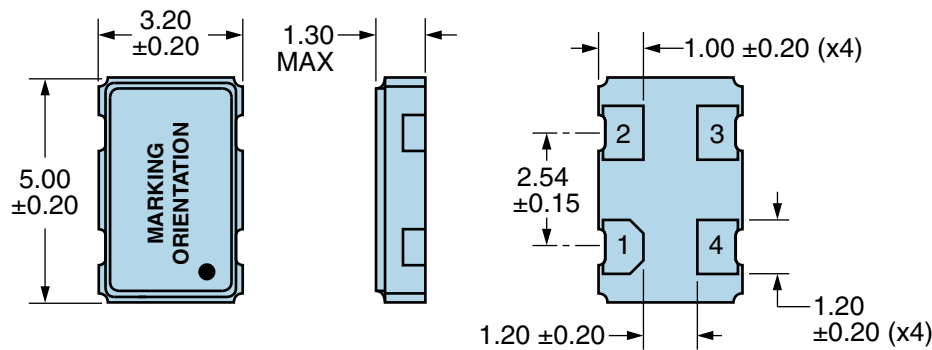
## ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

|                              |                                       |
|------------------------------|---------------------------------------|
| Fine Leak Test               | MIL-STD-883, Method 1014, Condition A |
| Gross Leak Test              | MIL-STD-883, Method 1014, Condition C |
| Mechanical Shock             | MIL-STD-202, Method 213, Condition C  |
| Resistance to Soldering Heat | MIL-STD-202, Method 210               |
| Resistance to Solvents       | MIL-STD-202, Method 215               |
| Solderability                | MIL-STD-883, Method 2003              |
| Temperature Cycling          | MIL-STD-883, Method 1010              |
| Vibration                    | MIL-STD-883, Method 2007, Condition A |

EH3525TS-5.000M

[Click part number to visit Part Number Details page](#)

MECHANICAL DIMENSIONS (all dimensions in millimeters)

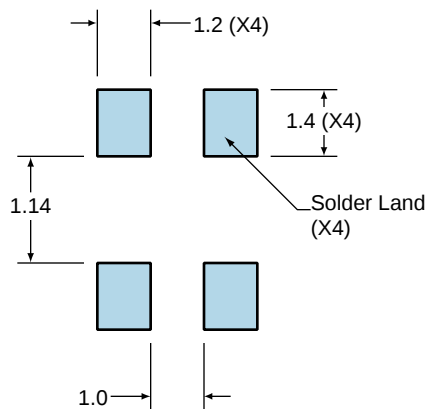


| PIN | CONNECTION         |
|-----|--------------------|
| 1   | Tri-State          |
| 2   | Ground/Case Ground |
| 3   | Output             |
| 4   | Supply Voltage     |

| LINE | MARKING                                                          |
|------|------------------------------------------------------------------|
| 1    | <b>E5.0000</b><br><i>E=Ecliptek Designator</i>                   |
| 2    | <b>XXXXXX</b><br><i>XXXXXX=Ecliptek Manufacturing Identifier</i> |

Suggested Solder Pad Layout

All Dimensions in Millimeters



All Tolerances are ±0.1

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[Click part number to visit Part Number Details page](#)

OUTPUT WAVEFORM & TIMING DIAGRAM



EH3525TS-5.000M

[Click part number to visit Part Number Details page](#)

Test Circuit for TTL Output

| Output Load Drive Capability | R <sub>L</sub> Value (Ohms) | C <sub>L</sub> Value (pF) |
|------------------------------|-----------------------------|---------------------------|
| 10TTL                        | 390                         | 15                        |
| 5TTL                         | 780                         | 15                        |
| 2TTL                         | 1100                        | 6                         |
| 10LSTTL                      | 2000                        | 15                        |
| 1TTL                         | 2200                        | 3                         |

Table 1: R<sub>L</sub> Resistance Value and C<sub>L</sub> Capacitance Value Vs. Output Load Drive Capability



- Note 1: An external 0.1μF low frequency tantalum bypass capacitor in parallel with a 0.01μF high frequency ceramic bypass capacitor close to the package ground and V<sub>DD</sub> pin is required.
- Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.
- Note 3: Capacitance value C<sub>L</sub> includes sum of all probe and fixture capacitance.
- Note 4: Resistance value R<sub>L</sub> is shown in Table 1. See applicable specification sheet for 'Load Drive Capability'.
- Note 5: All diodes are MM74VHC00, MM74VHC14, or equivalent.

# EH3525TS-5.000M

[Click part number to visit Part Number Details page](#)

## Test Circuit for CMOS Output



Note 1: An external  $0.1\mu\text{F}$  low frequency tantalum bypass capacitor in parallel with a  $0.01\mu\text{F}$  high frequency ceramic bypass capacitor close to the package ground and  $V_{DD}$  pin is required.

Note 2: A low capacitance ( $<12\text{pF}$ ), 10X attenuation factor, high impedance ( $>10\text{Mohms}$ ), and high bandwidth ( $>300\text{MHz}$ ) passive probe is recommended.

Note 3: Capacitance value  $C_L$  includes sum of all probe and fixture capacitance.