

HD74ALVC1G79

Single Positive Edge-triggered D-type Flip Flop

REJ03D0126–0300Z
(Previous ADE-205-637B (Z))
Rev.3.00
Nov.12.2003

Description

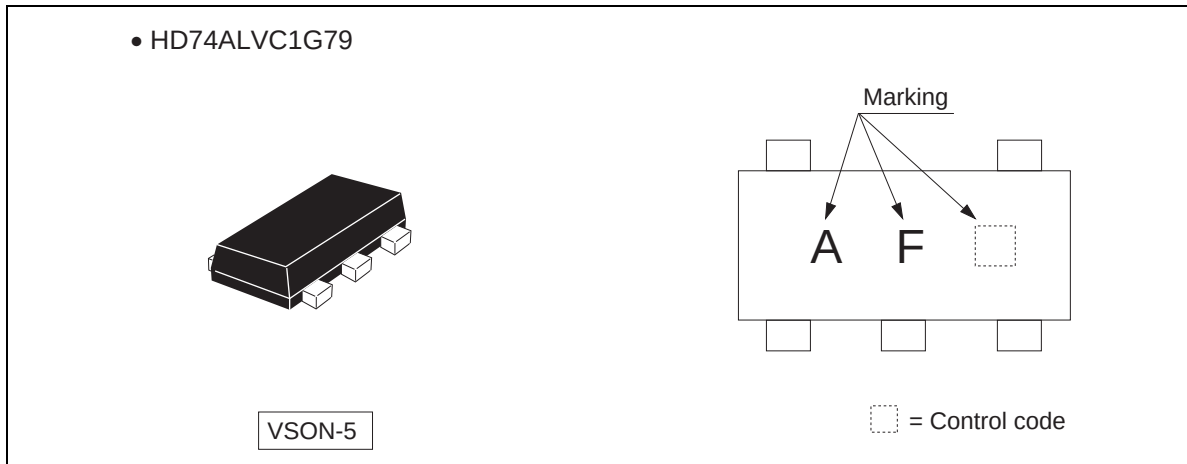
The HD74ALVC1G79 has D-type flip flop in a 5 pin package. The input data is transferred to the output at the rising edge of clock pulse CLK. Low voltage and high-speed operation is suitable for the battery powered products (e.g., notebook computers), and the low power consumption extends the battery life.

Features

- The basic gate function is lined up as Renesas uni logic series.
- Supplied on emboss taping for high-speed automatic mounting.
- Supply voltage range : 1.2 to 3.6 V
Operating temperature range : -40 to +85°C
- All inputs V_{IH} (Max.) = 3.6 V (@ V_{CC} = 0 V to 3.6 V)
All outputs V_O (Max.) = 3.6 V (@ V_{CC} = 0 V)
- Output current ± 2 mA (@ V_{CC} = 1.2 V)
 ± 4 mA (@ V_{CC} = 1.4 V to 1.6 V)
 ± 6 mA (@ V_{CC} = 1.65 V to 1.95 V)
 ± 18 mA (@ V_{CC} = 2.3 V to 2.7 V)
 ± 24 mA (@ V_{CC} = 3.0 V to 3.6 V)
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74ALVC1G79VSE	VSON-5 pin	TNP-5DV	VS	E (3,000 pcs/reel)

Outline and Article Indication

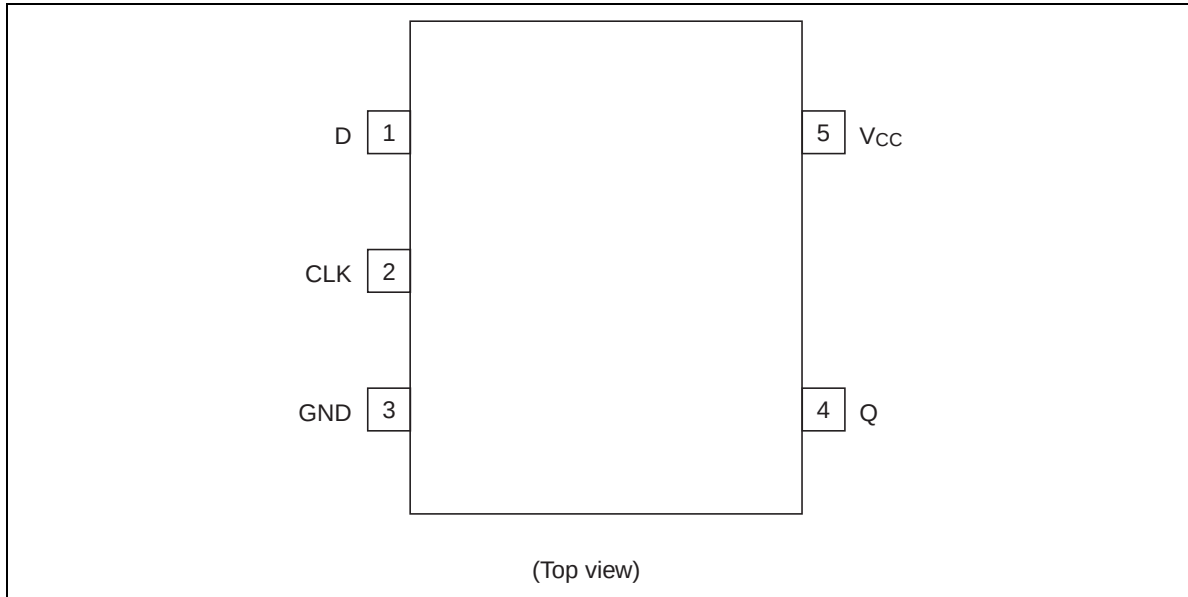


Function Table

Inputs		Output Q
CLK	D	
↑	H	H
↑	L	L
L	X	Q ₀

H: High level
 L: Low level
 X: Immaterial
 ↑: Low to high transition
 Q₀: Level of Q before the indicated steady input conditions was established.

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	-0.5 to 4.6	V	
Input voltage range ^{*1}	V_I	-0.5 to 4.6	V	
Output voltage range ^{*1, 2}	V_O	-0.5 to $V_{CC}+0.5$ -0.5 to 4.6	V	Output : H or L V_{CC} : OFF
Input clamp current	I_{IK}	-50	mA	$V_I < 0$
Output clamp current	I_{OK}	± 50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	± 50	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	± 100	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air) ^{*3}	P_T	200	mW	
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$	

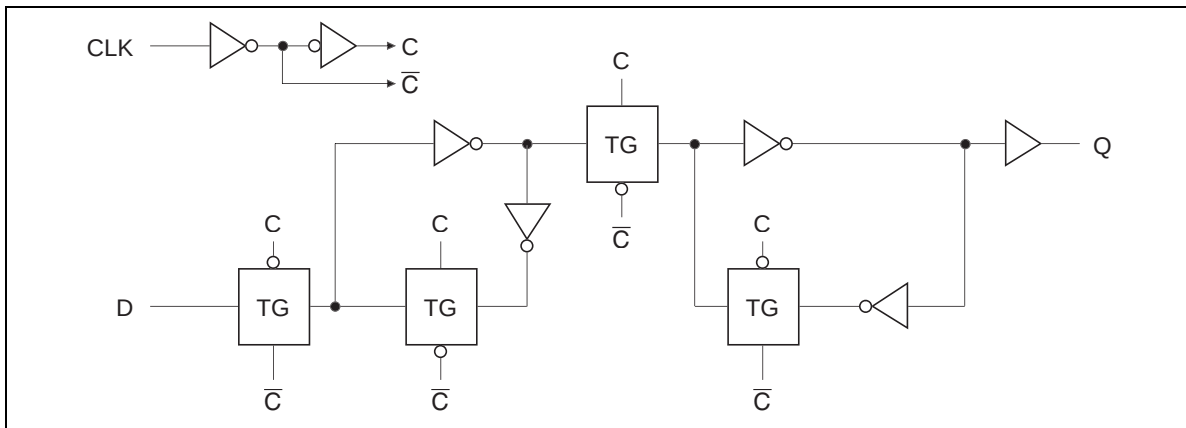
- Notes:
- The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.
 - 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation was calculated using a junction temperature of 150°C .

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	1.2	3.6	V	
Input voltage range	V_I	0	3.6	V	
Output voltage range	V_O	0	V_{CC}	V	
Output current	I_{OH}	—	−2	mA	$V_{CC} = 1.2\text{ V}$
		—	−4		$V_{CC} = 1.4\text{ V}$
		—	−6		$V_{CC} = 1.65\text{ V}$
		—	−18		$V_{CC} = 2.3\text{ V}$
		—	−24		$V_{CC} = 3.0\text{ V}$
	I_{OL}	—	2		$V_{CC} = 1.2\text{ V}$
		—	4		$V_{CC} = 1.4\text{ V}$
		—	6		$V_{CC} = 1.65\text{ V}$
		—	18		$V_{CC} = 2.3\text{ V}$
		—	24		$V_{CC} = 3.0\text{ V}$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	20	ns / V	$V_{CC} = 1.2\text{ to }2.7\text{ V}$
		0	10		$V_{CC} = 3.3\pm 0.3\text{ V}$
Operating free-air temperature	T_a	−40	85	°C	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



Electrical Characteristics

(T_a = -40 to 85°C)

Item	Symbol	V _{CC} (V) *	Min	Typ	Max	Unit	Test conditions
Input voltage	V _{IH}	1.2	V _{CC} ×0.75	—	—	V	
		1.4 to 1.6	V _{CC} ×0.7	—	—		
		1.65 to 1.95	V _{CC} ×0.7	—	—		
		2.3 to 2.7	1.7	—	—		
		3.0 to 3.6	2.0	—	—		
	V _{IL}	1.2	—	—	V _{CC} ×0.25		
		1.4 to 1.6	—	—	V _{CC} ×0.3		
		1.65 to 1.95	—	—	V _{CC} ×0.3		
		2.3 to 2.7	—	—	0.7		
		3.0 to 3.6	—	—	0.8		
Output voltage	V _{OH}	Min to Max	V _{CC} -0.2	—	—	V	I _{OH} = -100 μA
		1.2	0.9	—	—		I _{OH} = -2 mA
		1.4	1.1	—	—		I _{OH} = -4 mA
		1.65	1.2	—	—		I _{OH} = -6 mA
		2.3	1.7	—	—		I _{OH} = -18 mA
		3.0	2.2	—	—		I _{OH} = -24 mA
	V _{OL}	Min to Max	—	—	0.2		I _{OL} = 100 μA
		1.2	—	—	0.3		I _{OL} = 2 mA
		1.4	—	—	0.3		I _{OL} = 4 mA
		1.65	—	—	0.3		I _{OL} = 6 mA
		2.3	—	—	0.55		I _{OL} = 18 mA
		3.0	—	—	0.55		I _{OL} = 24 mA
Input current	I _{IN}	3.6	—	—	±5	μA	V _{IN} = 3.6 V or GND
Quiescent supply current	I _{CC}	3.6	—	—	10	μA	V _{IN} = V _{CC} or GND, I _O = 0
Output leakage current	I _{OFF}	0	—	—	5	μA	V _{IN} or V _O = 0 to 3.6 V
Input capacitance	C _{IN}	3.3	—	4.0	—	pF	V _{IN} = V _{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

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Switching Characteristics

($T_a = -40$ to 85°C)

$V_{CC} = 1.2\text{ V}$

Item	Symbol	Min	Typ	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Maximum clock frequency	$f_{\max}$	—	200	—	MHz	$C_L = 15\text{ pF}$		
Propagation delay time	t_{PLH} t_{PHL}	—	7.0	—	ns	$C_L = 15\text{ pF}$	CLK	Q
Setup time	t_{su}	—	4.5	—	ns		D	
Hold time	t_h	—	−4.5	—	ns			
Pulse width	t_w	—	2.0	—	ns		CLK "H" or "L"	

$V_{CC} = 1.5 \pm 0.1\text{ V}$

Item	Symbol	Min	Typ	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Maximum clock frequency	$f_{\max}$	100	350	—	MHz	$C_L = 15\text{ pF}$		
Propagation delay time	t_{PLH} t_{PHL}	2.0	—	8.0	ns	$C_L = 15\text{ pF}$	CLK	Q
Setup time	t_{su}	4.5	—	—	ns		D	
Hold time	t_h	0.0	—	—	ns			
Pulse width	t_w	3.5	—	—	ns		CLK "H" or "L"	

$V_{CC} = 1.8 \pm 0.15\text{ V}$

Item	Symbol	Min	Typ	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Maximum clock frequency	$f_{\max}$	160	350	—	MHz	$C_L = 30\text{ pF}$		
Propagation delay time	t_{PLH} t_{PHL}	1.5	—	7.0	ns	$C_L = 30\text{ pF}$	CLK	Q
Setup time	t_{su}	3.5	—	—	ns		D	
Hold time	t_h	0.0	—	—	ns			
Pulse width	t_w	2.5	—	—	ns		CLK "H" or "L"	

Switching Characteristics (cont)

$$V_{CC} = 2.5 \pm 0.2 \text{ V}$$

Item	Symbol	Min	Typ	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Maximum clock frequency	$f_{\max}$	160	400	—	MHz	$C_L = 30 \text{ pF}$		
Propagation delay time	t_{PLH} t_{PHL}	1.0	—	4.0	ns	$C_L = 30 \text{ pF}$	CLK	Q
Setup time	t_{su}	2.5	—	—	ns		D	
Hold time	t_h	0.0	—	—	ns			
Pulse width	t_w	2.5	—	—	ns		CLK "H" or "L"	

$$V_{CC} = 3.3 \pm 0.3 \text{ V}$$

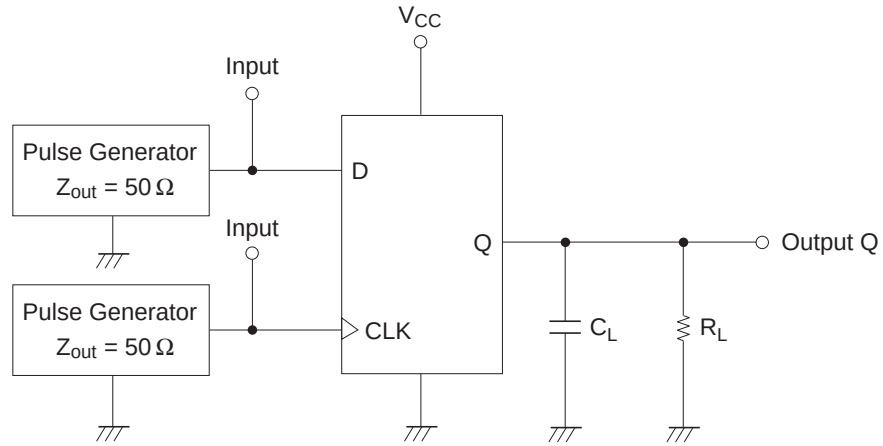
Item	Symbol	Min	Typ	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Maximum clock frequency	$f_{\max}$	200	450	—	MHz	$C_L = 30 \text{ pF}$		
Propagation delay time	t_{PLH} t_{PHL}	1.0	—	3.0	ns	$C_L = 30 \text{ pF}$	CLK	Q
Setup time	t_{su}	2.0	—	—	ns		D	
Hold time	t_h	0.0	—	—	ns			
Pulse width	t_w	2.0	—	—	ns		CLK "H" or "L"	

Operating Characteristics

$$(T_a = 25^\circ\text{C})$$

Item	Symbol	V_{CC} (V)	Min	Typ	Max	Unit	Test conditions
Power dissipation capacitance	C_{PD}	1.5	—	7.5	—	pF	$f = 10 \text{ MHz}$
		1.8	—	7.5	—		
		2.5	—	8.0	—		
		3.3	—	11.0	—		

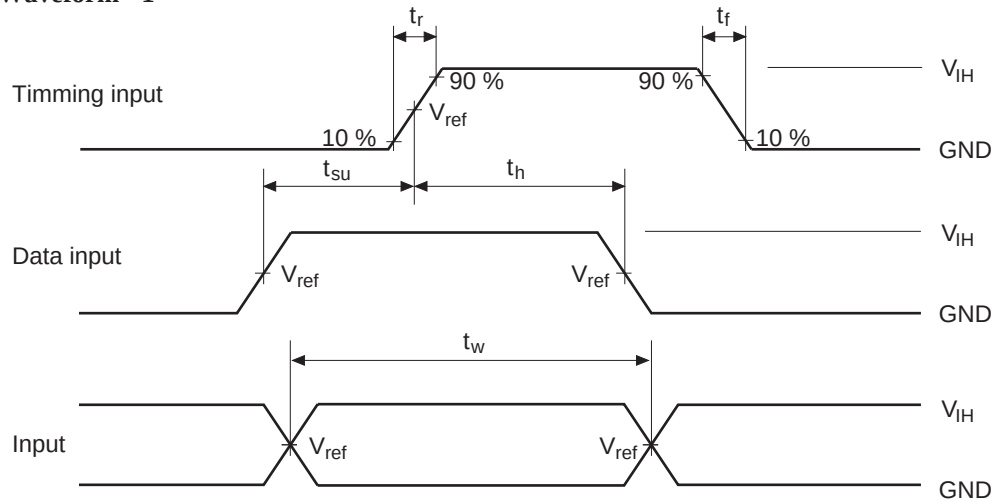
Test Circuit



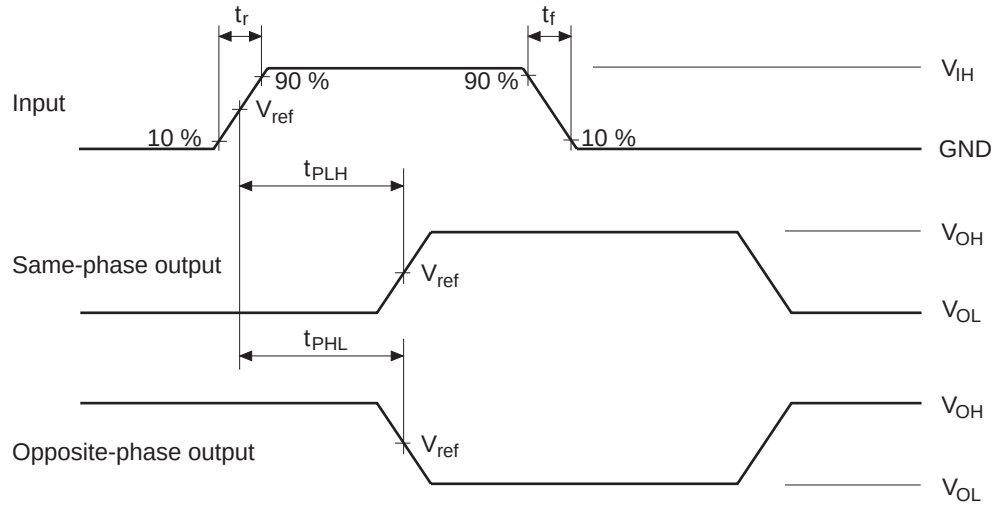
Symbol	$V_{CC} = 1.2\text{ V},$ $1.5 \pm 0.1\text{ V}$	$V_{CC} = 1.8 \pm 0.15\text{ V}$	$V_{CC} = 2.5 \pm 0.2\text{ V},$ $3.3 \pm 0.3\text{ V}$
R_L	2.0 k Ω	1.0 k Ω	500 Ω
C_L	15 pF	30 pF	30 pF

Note: C_L includes probe and jig capacitance.

• Waveform - 1



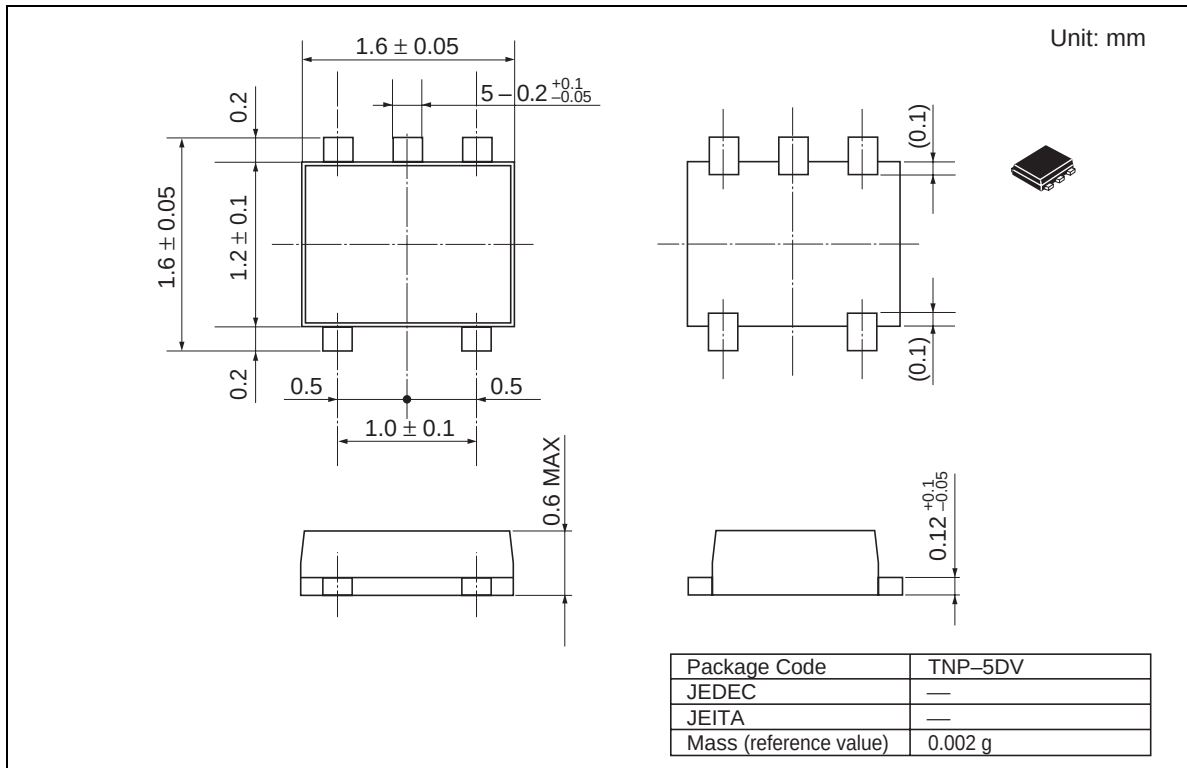
• Waveform - 2



Symbol	$V_{CC} = 1.2 \text{ V},$ $1.5 \pm 0.1 \text{ V},$ $1.8 \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \pm 0.3 \text{ V}$
t_r / t_f	2.0 ns	2.5 ns	2.5 ns
V_{IH}	V_{CC}	V_{CC}	2.7 V
V_{ref}	50%	50%	1.5 V

Note: Input waveform : PRR = 10 MHz, duty cycle 50%

Package Dimensions



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