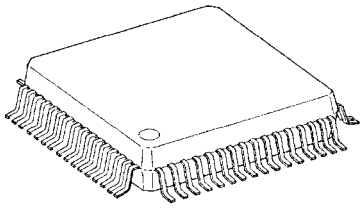
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC9298F,TC9298FB

LCD Driver with On-Chip Key Input

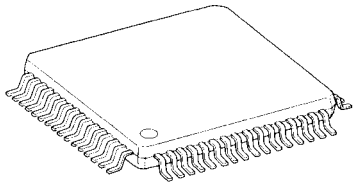
TC9298F and TC9298FB is an LCD driver with on-chip key input, which is controlled using serial data.

TC9298F



QFP64-P-1414-0.80A

TC9298FB



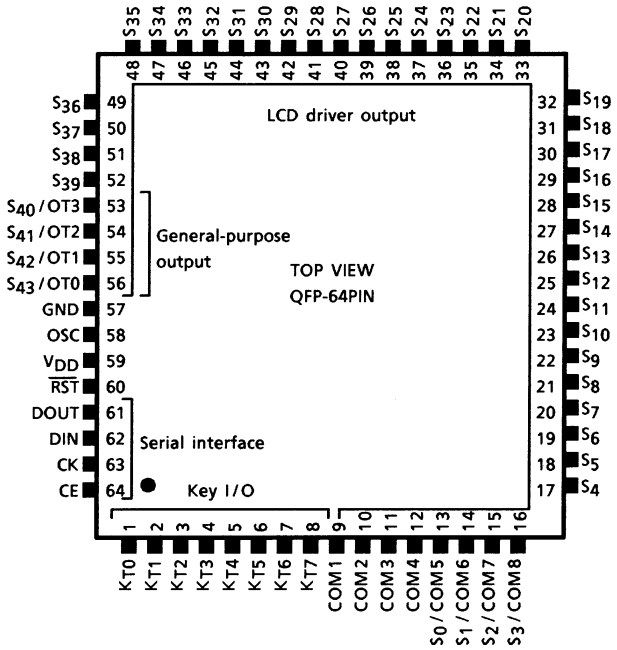
QFP64-P-1212-0.65

Weight
QFP64-P-1414-0.80A: 1.10 g (typ.)
QFP64-P-1212-0.65: 0.45 g (typ.)

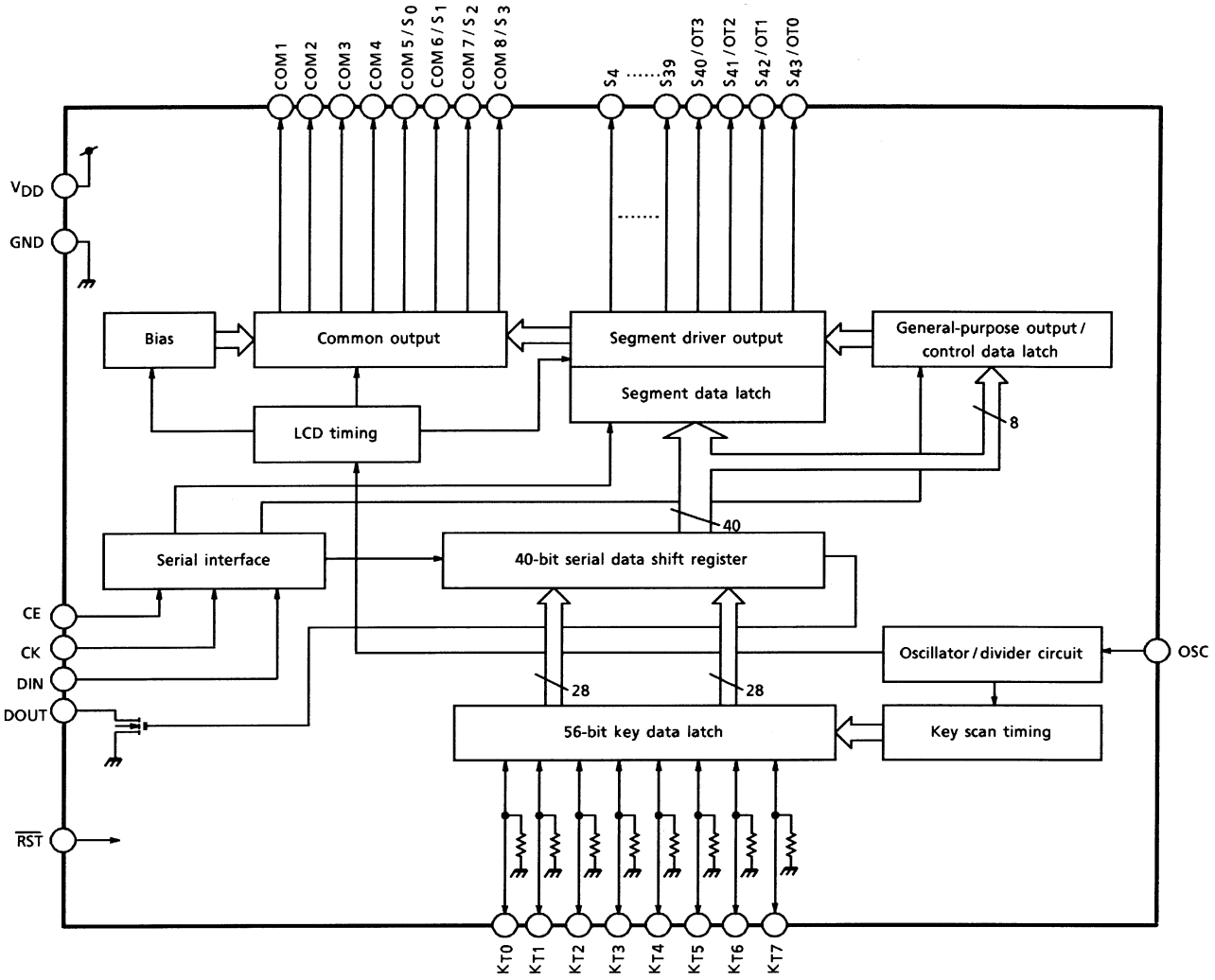
Features

- Supports switching between 1/4 and 1/8 duty and 1/3 and 1/4 bias.
- Displays up to 176 segments in 1/4 duty mode; up to 320 segments in 1/8 duty mode.
- All display segments can be turned on or off. Outputs from the S40 to S43 pins can be switched between segment output and LED driver output.
- Supports input from 28 keys as standard. Externally connecting diodes supports input from up to 56 keys.
- Four-wire configuration employed for connecting to the controller.

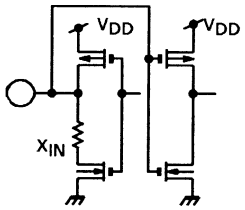
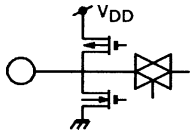
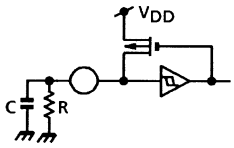
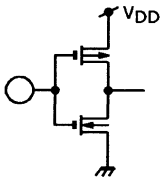
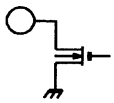
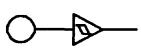
Pin Assignment (top view)



Block Diagram



Pin Functions

Pin No.	Symbol	Pin Name	Function	Remarks
59	V_{DD}	Power pin	Power is applied to these pins. Normally 5 V is supplied. Power-on reset resets system at power on or V_{DD} < 2.0 V (typical).	—
57	GND	Ground pin		
1~8	KT_0~KT_7	Key scan I/O pins	Key scan signal I/O pins. Data can be input from 28 keys (standard) by a key matrix with other key scan I/O pins. Connecting external diodes enables data to be input from up to 56 keys. At a fixed cycle, a pin is set to output and the other pins are set to input. The pin set to output outputs high level; the others are pulled down to low level by built-in pull-down resistors.	
9~12	COM1~ COM4	Common output pins	Common signal output pins for LCD. When set to 1/4 duty, can display up to 176 segments by a key matrix of COM1 to COM4 and S_0 to S_{43}; when set to 1/8 duty, can display up to 320 segments by a key matrix of COM1 to COM8 and S_4 to S_{43}. When set to 1/8 duty, S_0 to S_3 are used as COM5 to COM8.	
13~16	S_0/COM5~ S_3/COM8	Segment output pins /common output pins		
17~52	S_4~S_{39}	Segment output pins	Segment signal output pins for LCD. When set to 1/4 duty, can display up to 176 segments by a key matrix of COM1 to COM4 and S_0 to S_{43}; when set to 1/8 duty, can display up to 320 segments by a key matrix of COM1 to COM8 and S_4 to S_{43}. S_{40} to S_{43} are also used as general-purpose output pins. When set to general-purpose output, S_{40} to S_{43} output CMOS outputs.	
53~56	S_{40}/OT3~ S_{43}/OT0	Segment output pins /general-purpose output pins		
58	OSC	CR oscillator pin	Connecting C and R generates the system clock. The oscillation frequency is expressed as follows: $f_{osc} \simeq 1.41/(C \cdot R)$ [Hz] For example, where C = 0.01 μF and R = 27 kΩ $f_{osc} \simeq 5.22$ kHz	
60	$\overline{RST}$	Reset input pin	Reset signal input pin for device system reset. While the $\overline{RST}$ input is at low level, stops the oscillator, resetting all internal data. At the same time, fixes the LCD output pins to low level. Since the power-on reset circuit is incorporated, for normal use, connect the RST pin to V_{DD}.	
61	DOUT	Data output pin	Serial interface pins. Used to transfer to and from the controller, display data, key input data, and data for controlling these data. While the CE pin is at low level, disables data transfer. Setting the CE pin to high level inputs or outputs data to or from the DIN/DOUT pin in sync with the clock input to the CK pin. All input pins incorporate Schmitt circuits. The DOUT pin is N-channel open drain output.	
62	DIN	Data input pin		
63	CK	Clock input pin		
64	CE	Chip enable input pin		

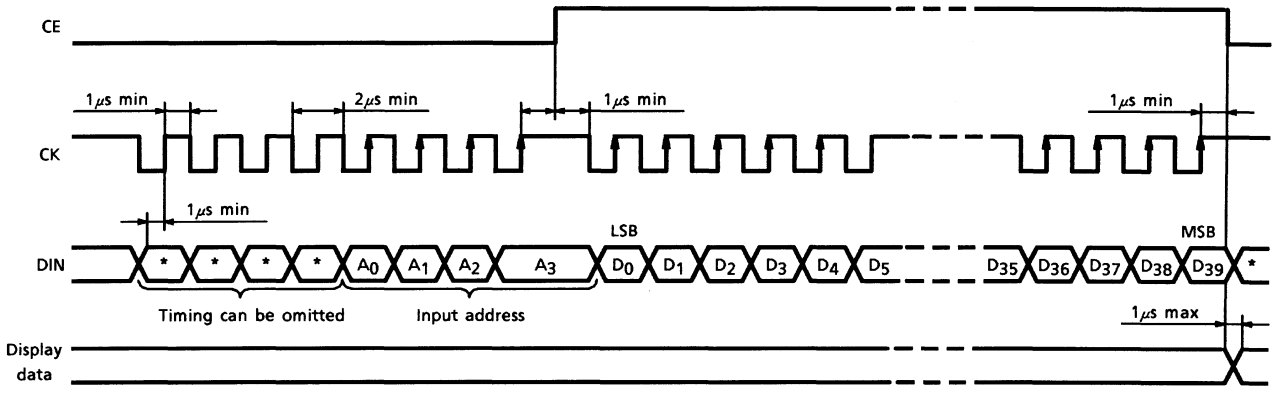
The Contents of Address Data

Duty	Can be Omitted				A0	A1	A2	A3	Address (HEX)	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8~D_{11}	D_{12}~D_{15}	D_{16}~D_{28}	D_{29}~D_{39}
1/4	*	*	*	*	0	0	0	0	0	S_9 to S_0 display data											
										S_9				S_8				S_7	S_6	S_5~S_0	
										COM4	COM3	COM2	COM1	COM4	COM3	COM2	COM1	COM4, 3, 2, 1	COM4, 3, 2, 1	COM4, 3, 2, 1	
	*	*	*	*	1	0	0	0	1	S_{19} to S_{10} display data											
										S_{19}				S_{18}				S_{17}	S_{16}	S_{15}~S_{10}	
										COM4	COM3	COM2	COM1	COM4	COM3	COM2	COM1	COM4, 3, 2, 1	COM4, 3, 2, 1	COM4, 3, 2, 1	
	*	*	*	*	0	1	0	0	2	S_{29} to S_{20} display data											
	*	*	*	*	1	1	0	0	3	S_{39} to S_{30} display data											
	*	*	*	*	0	0	1	0	4	S_{43} to S_{40} display data											Input prohibited
1/8	*	*	*	*	0	0	0	0	0	S_8 to S_4 display data											
										S_8								S_7		S_6~S_4	
										COM8	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM8, 7, 6, 5, 4, 3, 2, 1		COM8~COM1	
	*	*	*	*	1	0	0	0	1	S_{13} to S_9 display data											
										S_{13}								S_{12}		S_{11}~S_9	
										COM8	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM8, 7, 6, 5, 4, 3, 2, 1		COM8~COM1	
	*	*	*	*	0	1	0	0	2	S_{18} to S_{14} display data											
	*	*	*	*	1	1	0	0	3	S_{23} to S_{19} display data											
	*	*	*	*	0	0	1	0	4	S_{28} to S_{24} display data											
	*	*	*	*	1	0	1	0	5	S_{33} to S_{29} display data											
	*	*	*	*	0	1	1	0	6	S_{38} to S_{34} display data											
	*	*	*	*	1	1	1	0	7	S_{43} to S_{39} display data											
—	*	*	*	*	0	0	0	1	8	EX-OSC	0	0	DUTY	Segment/general-purpose output switching				Input prohibited			
														S_{43}/OT0	S_{42}/OT1	S_{41}/OT2	S_{40}/OT3				
	*	*	*	*	1	0	0	1	9	RBIAS	Display control			General-purpose output control				Input prohibited			
											LT	BL	OP	OT0	OT1	OT2	OT3				
	*	*	*	*	0	1	0	1	A	Key data output											Undefined
										K_{ON}	K_{01}	K_{02}	K_{03}	K_{04}	K_{05}	K_{06}	K_{07}	K_{08}~K_{11}	K_{12}~K_{15}	K_{12}~K_{15}	
	*	*	*	*	1	1	0	1	B	Expanded key data output											Undefined
										K_{ON}	K_{29}	K_{30}	K_{31}	K_{32}	K_{33}	K_{34}	K_{35}	K_{36}~K_{39}	K_{40}~K_{43}	K_{44}~K_{56}	

Description of Operation

1. Display and Control Data Input Format

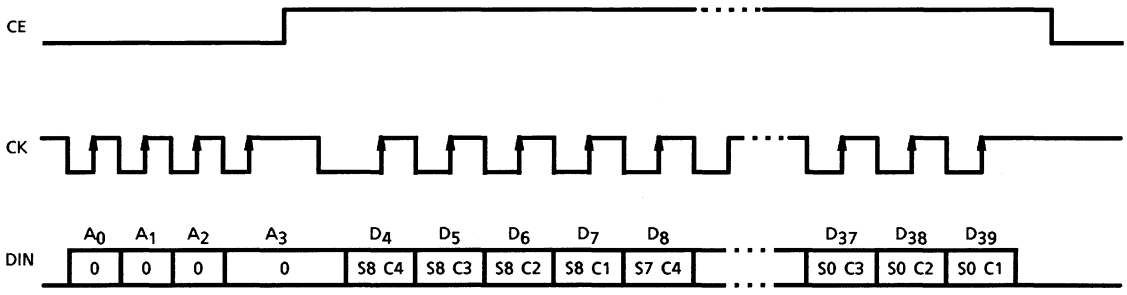
- The display and control data input timing is as follows.



*: Don't care

- Set all display data bits for outputting the segments to be used.
- The display data for outputting unused segments need not be set, but only on the LSB side.
- At input the DOUT pin goes to high impedance.

(example) At 1/4 duty, if the address for setting the data is set to 0H, segment output pins from S0 to S8 are used and S9 is not, the S9 display data can be omitted as shown below.



(1) Display control data bit

This bit sets the display on/off. In accordance with the setting, the waveform corresponding to display on/off is output to a segment output pin. Setting the bit to 1 outputs display on waveform; setting the bit to 0, display off waveform.

First specify an address from 0H~4H at 1/4 duty or an address from 0H~7H at 1/8 duty, then set the data for each segment in sequence, starting from the segment's upper bit.

If any segments remain unused, the data settings can be omitted from the highest segment output pins.

0	Display off
1	Display on

Note 1: After a reset these data are undefined.

(2) Duty control bit (DUTY)

The DUTY bit controls the switching between 1/4 and 1/8 duty. Setting this bit to 0 selects 1/4 duty; to 1 selects 1/8 duty.

Selecting 1/4 duty switches the S0/COM5~S3/COM8 pins to segment output pins S0~S3. Selecting 1/8 duty switches the S0/COM5~S3/COM8 pins to common output pins COM5~COM8.

To set the data, specify the address as 8H.

	A_0	A_1	A_2	A_3	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Address 8H	0	0	0	1		0	0	DUTY				

(Note 2)		
	0	1/4 DUTY, 1/3 BIAS
	1	1/8 DUTY, 1/4 BIAS

Note 2: After a reset these data are cleared to 0.

(3) Bias resistance control bit (RBIAS)

This bit controls the resistance (RBIAS) value for generating the bias voltage.

At 1/4 duty and 1/3 bias, writing 0 to the bit sets RBIAS = 4 kΩ, while writing 1 to the bit sets RBIAS = 2 kΩ.

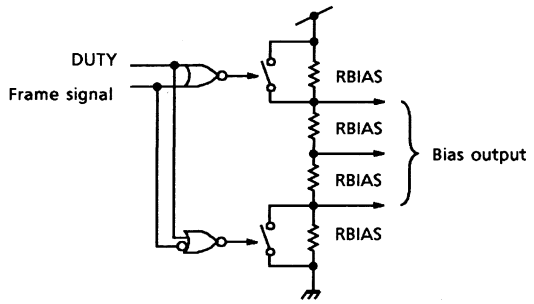
At 1/8 duty and 1/4 bias, writing 0 to the bit sets RBIAS = 2 kΩ, while writing 1 to the bit sets RBIAS = 1 kΩ.

To set the data, specify the address as 9H.

If setting RBIAS to 0 increases the noise on the LCD driver output waveform and adversely affects the display, set RBIAS to 1 to reduce the noise.

	A_0	A_1	A_2	A_3	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Address 9H	1	0	0	1	RBIAS							

DUTY	LCD DRIVER MODE	RBIAS	RBIAS RESISTANCE (TYP.)
0	1/4 DUTY 1/3 BIAS	0	4kΩ (×3)
		1	2kΩ (×3)
1	1/8 DUTY 1/4 BIAS	0	2kΩ (×4)
		1	1kΩ (×4)



(configuration of bias circuit)

Note 3: After a reset these data are cleared to 0.

(4) All-on/all-off control bits (BL/LT)

The BL/LT bits turn each display to all-on or all-off. Setting both bits to 0 outputs standard display data to each segment output pin. Setting BL to 1 outputs the display off waveform to all the segment output pins. Setting BL to 1 outputs the display on waveform to all the segment output pins.

When all-on or all-off is set, the previous display data are held. There is no need to set the display data again. New data can also be set during the all-on or all-off states.

To set the data, specify the address as 9H.

	A_0	A_1	A_2	A_3	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Address 9H	1	0	0	1		LT	BL					

(Note 4)

LT	BL	DISPLAY
0	0	Standard display
1		All on
0	1	All off (Note 5)
1		

Note 4: After a reset these data are cleared to 0.

Note 5: When BL and LT are both set to 1, BL takes priority.

(5) Operation control bit (OP)

The OP bit starts/stops the LCD driver and key scan functions.

Setting OP to 0 stops the oscillation and fixes the LCD driver output pins and the key scan input/output pins to Low.

After operations are turned off, the previous data of all data bits are held. New data can also be set while the operations are off.

A reset clears the OP bit to 0 and turns off the LCD driver and key scanner operations. While the operations are off, initialize the control data and display data.

To set the data, specify the address as 9H.

	A_0	A_1	A_2	A_3	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Address 9H	1	0	0	1				OP				

(Note 6)

0	Operations off
1	Operations on

Note 6: After a reset these data are cleared to 0.

(6) External clock input control bit (EX-OSC)

The EX-OSC bit selects oscillator operation or external clock input.

Setting this bit to 0 operates the oscillator circuit with external CR.

Setting the bit to 1 sets the OSC pin as a CMOS input pin with Schmitt circuit and inputs an external clock as the system clock. Use this pin at such times as when using an output clock from a microcontroller.

To set the data, specify the address as 8H.

	A_0	A_1	A_2	A_3	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Address 8H	0	0	0	1	EX-OSC	0	0					

(Note 7)

0	CR oscillation
1	External clock

Note 7: After a reset these data are cleared to 0.

(7) Segment/general-purpose output switching bits (S43/OT0~S40/OT3) and general-purpose output control bits (OT0~OT3)

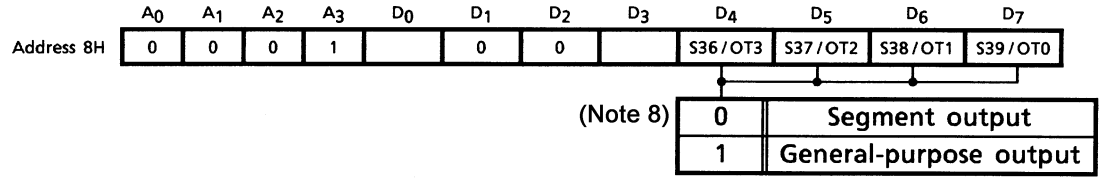
The segment/general-purpose output switching bits switch between segment output and general-purpose output. Setting 0 selects segment output; setting 1 selects general-purpose output. When segment output is selected, a display on/off waveform corresponding to the display data is output. When general-purpose output is selected, the general-purpose output control bit sets the output status.

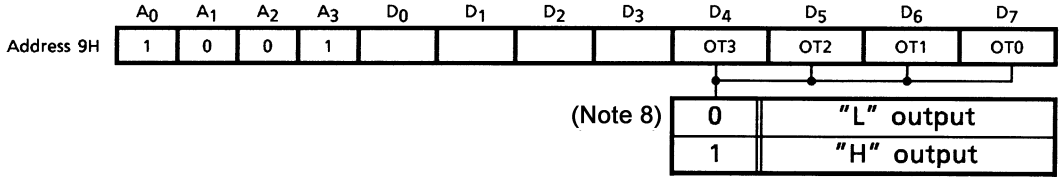
Setting the general-purpose output control bit to 0 outputs Low. Setting the bit to 1 outputs High.

When segment output is selected, the corresponding general-purpose output control data are invalid. When general-purpose output is selected, the corresponding segment output display data are invalid.

To set the segment/general-purpose output switching bits, specify the address as 8H.

To set the general-purpose output control bits, specify the address as 9H.





Note 8: After a reset these data are cleared to 0.

(8) Key data bits (K_{ON}, K_{01}~K_{56})

These are the key data bits of the key matrix. The K_{ON} bit shows whether the key input is on or off. The K_{01}~K_{56} bits, each corresponding to a key, show which key is being pressed.

Key input sets K_{ON} to 1. No key input sets K_{ON} to 0. A key input corresponding to K_{01}~K_{56} sets the relevant K_{01}~K_{56} bit to 1. No key input corresponding to K_{01}~K_{56} sets the relevant K_{01}~K_{56} bit to 0.

K_{ON} Bit

0	No key input
1	Key input

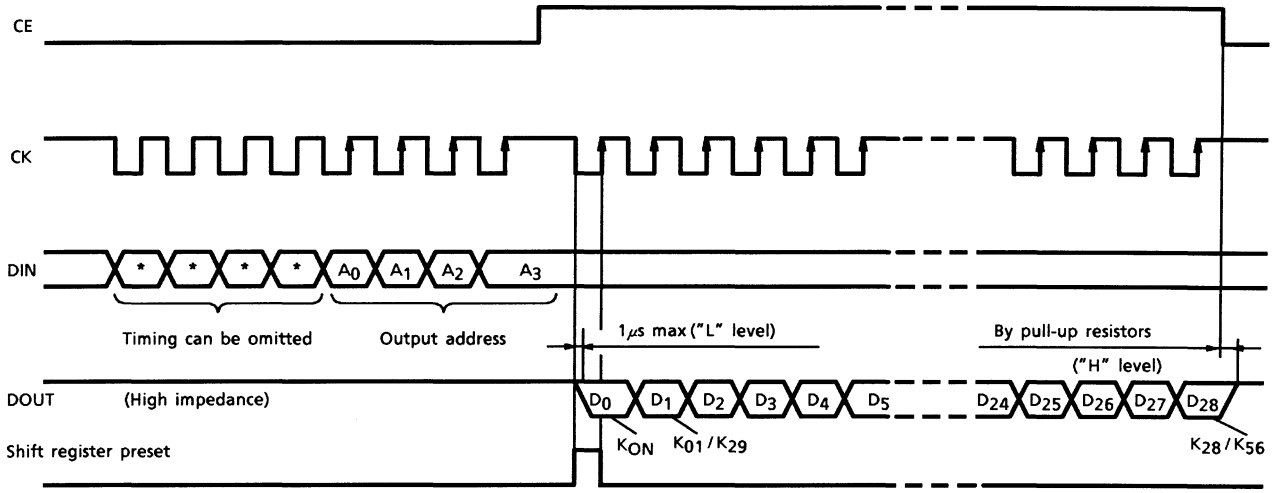
K_0~K_{56} Bits

0	No key input
1	Key input

Note 9: After a reset these data are undefined.

2. Data Output Mode (key data)

(1) The key data are output at the following timing.

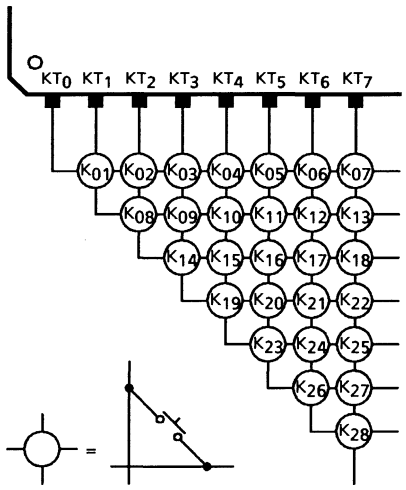


(2) Structure of key matrix

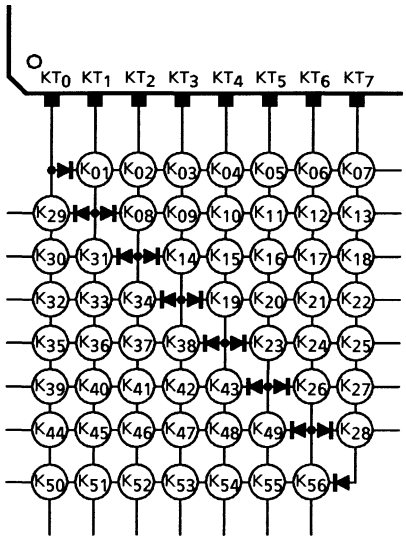
One of two matrices can be selected for the key matrix: a matrix with up to 28 keys without any external components, or a matrix with up to 56 keys with external diodes.

Structure of Key Matrix

(structure 1)



(structure 2)

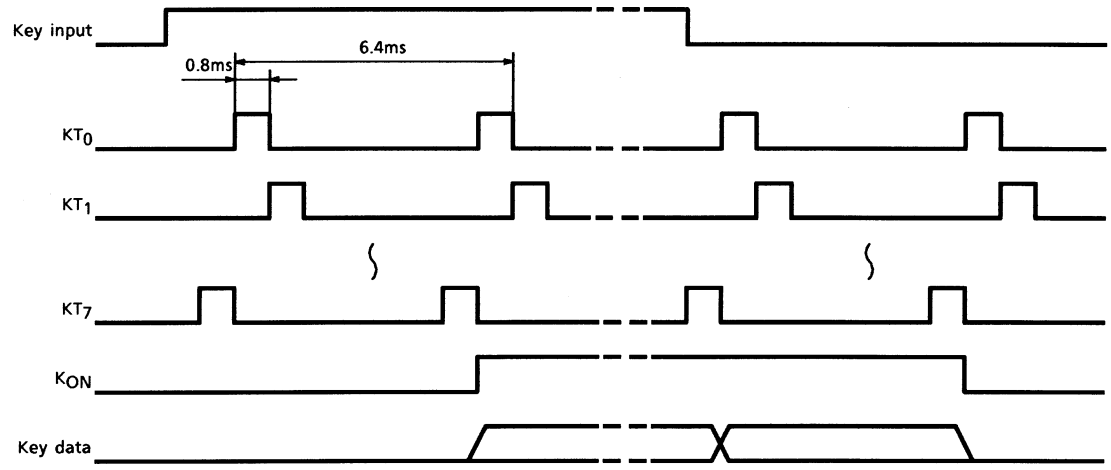


Note 10: When a key is input, K_{ON} is set to 1.

Note 11: Setting the CE pin to 1 then to 0 after address input sets the DOUT pin to output. With DOUT in an output state, the K_{ON} bit can be monitored by halting the timing.

Note 12: If there are any unnecessary key data, the key data output can be stopped by setting the CE pin to 0.

(3) The keys are scanned at the following timing.

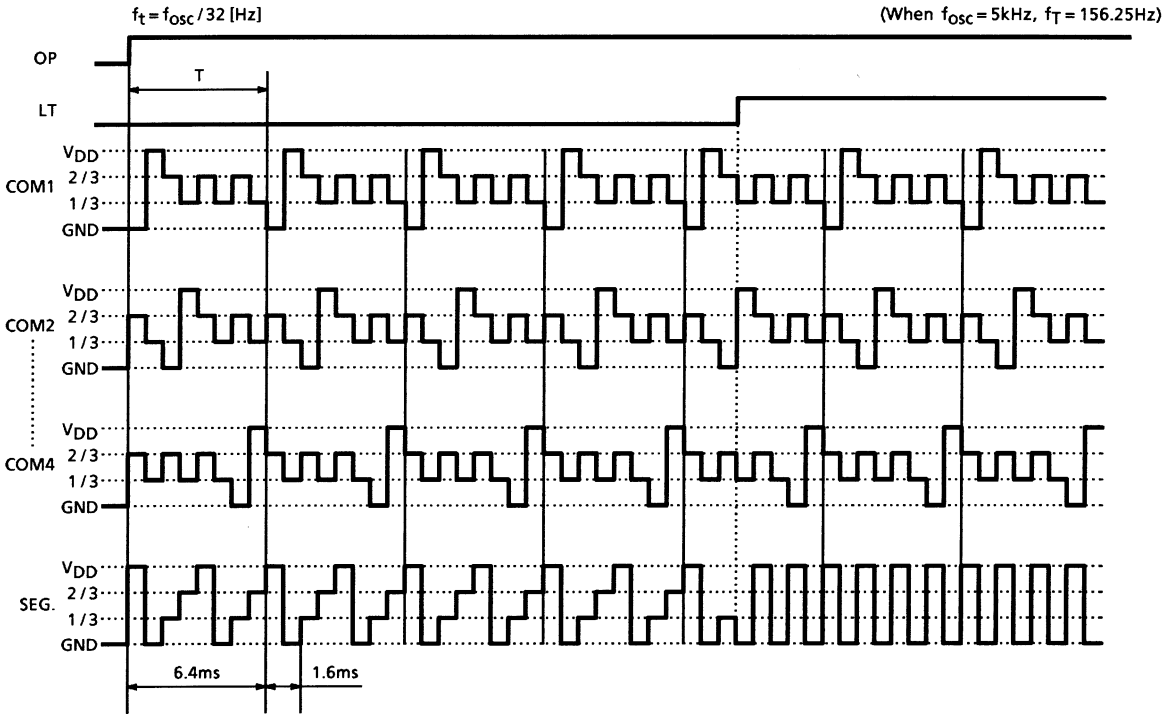


Note 13: When f_{osc} = 5 kHz

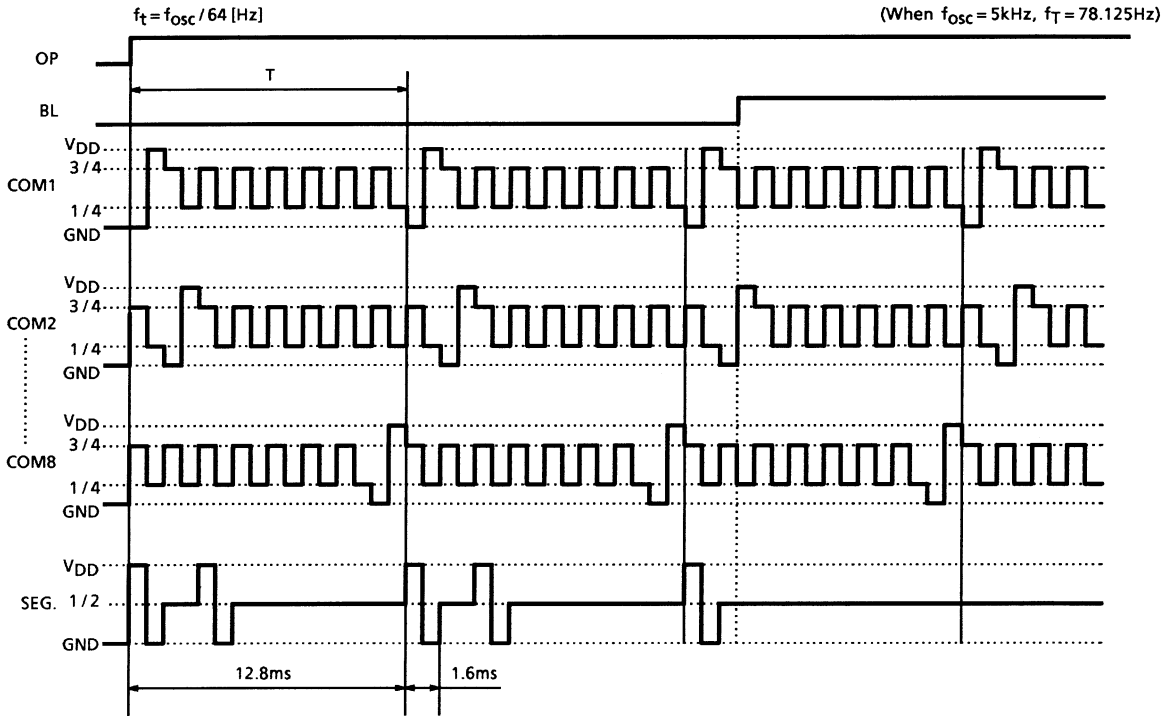
When OP is set to 1, the keys are scanned. The key scan cycle is 32 times the oscillation cycle (6.4 ms @f_{osc} = 5kHz). The key data are also updated at this timing. The actual data become valid and updated one cycle after each key scan cycle.

3. The Output Waveforms of the LCD Driver are as Shown Below.

- 1/4 duty, 1/3 bias (COM1, COM3 system on)



- 1/8 duty, 1/4 bias (COM1, COM3 system on)



Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.3~6.0	V
Input voltage 1	V_{IN1}	−0.3~V_{DD} + 0.3	V
Input voltage 2	V_{IN2}	−0.3~6.0 (Note 14)	V
Power dissipation	P_D	300	mW
Operating temperature	T_{opr}	−40~85	°C
Storage temperature	T_{stg}	−65~150	°C

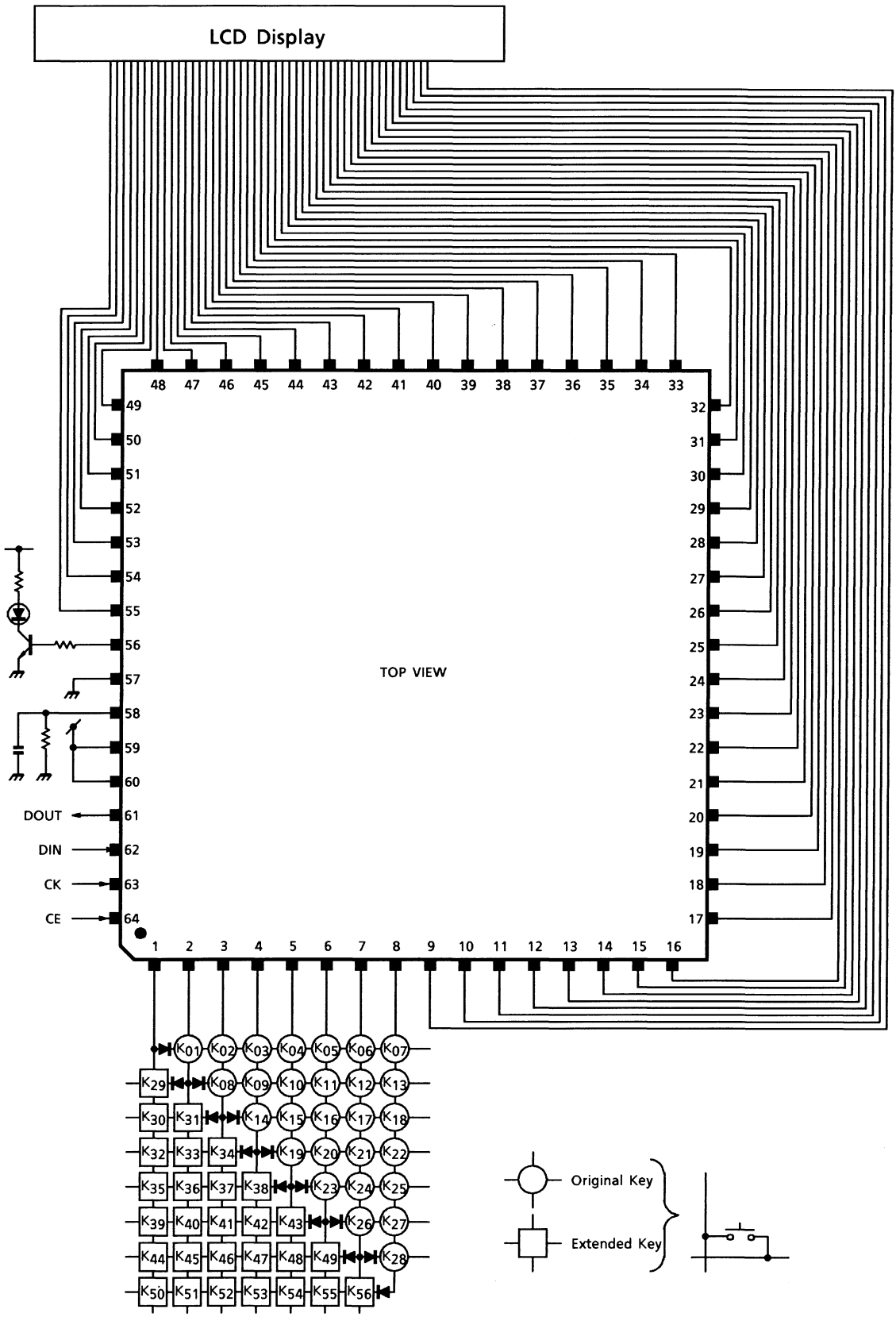
Note 14: DIN, CK, CE pins

Electrical Characteristics (unless otherwise specified, V_{DD} = 2.7 to 5.5 V, Ta = −40 to 85°C)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating supply voltage		V_{DD}	—	—	2.7	5.0	5.5	V
Power-on reset voltage		V_{RST}	—	—	1.5	2.0	2.5	V
Operating supply current		I_{DD1}	—	V_{DD} = 5 V, f_{osc} = 5 kHz, No load 1/3 BIAS, RBIAS = 4 kΩ (typ.)	—	0.7	1.5	mA
			—	V_{DD} = 5 V, f_{osc} = 5 kHz, No load 1/3 BIAS, RBIAS = 2 kΩ (typ.)	—	1.1	2.0	
			—	V_{DD} = 5 V, f_{osc} = 5 kHz, No load 1/4 BIAS, RBIAS = 2 kΩ (typ.)	—	0.9	2.0	
			—	V_{DD} = 5 V, f_{osc} = 5 kHz, No load 1/4 BIAS, RBIAS = 1 kΩ (typ.)	—	1.5	2.5	
Stand-by current		I_{DD2}	—	V_{DD} = 5 V, OP = "0"	—	150	300	μA
Input voltage	"H" level	V_{IH1}	—	KT_0-KT_3	V_{DD} × 0.6	~	V_{DD}	V
		V_{IH2}	—	$\overline{RST}$	V_{DD} × 0.8	~	V_{DD}	
		V_{IH3}	—	DIN, CK, CE	V_{DD} × 0.8	~	5.5	
	"L" level	V_{IL1}	—	K_{T0}-K_{T3}	0	~	V_{DD} × 0.1	
		V_{IL2}	—	$\overline{RST}$, DIN, CK, CE	0	~	V_{DD} × 0.2	
Schmitt voltage		V_{SCH}	—	V_{DD} = 5 V, DIN, CK, CE	—	1.0	—	V
Input leakage current	"H" level	I_{IH}	—	V_{IN} = V_{DD}, $\overline{RST}$, DIN, CK, CE	—	—	±1.0	μA
	"L" level	I_{IL}	—	V_{IN} = 0 V, $\overline{RST}$, DIN, CK, CE	—	—	±1.0	

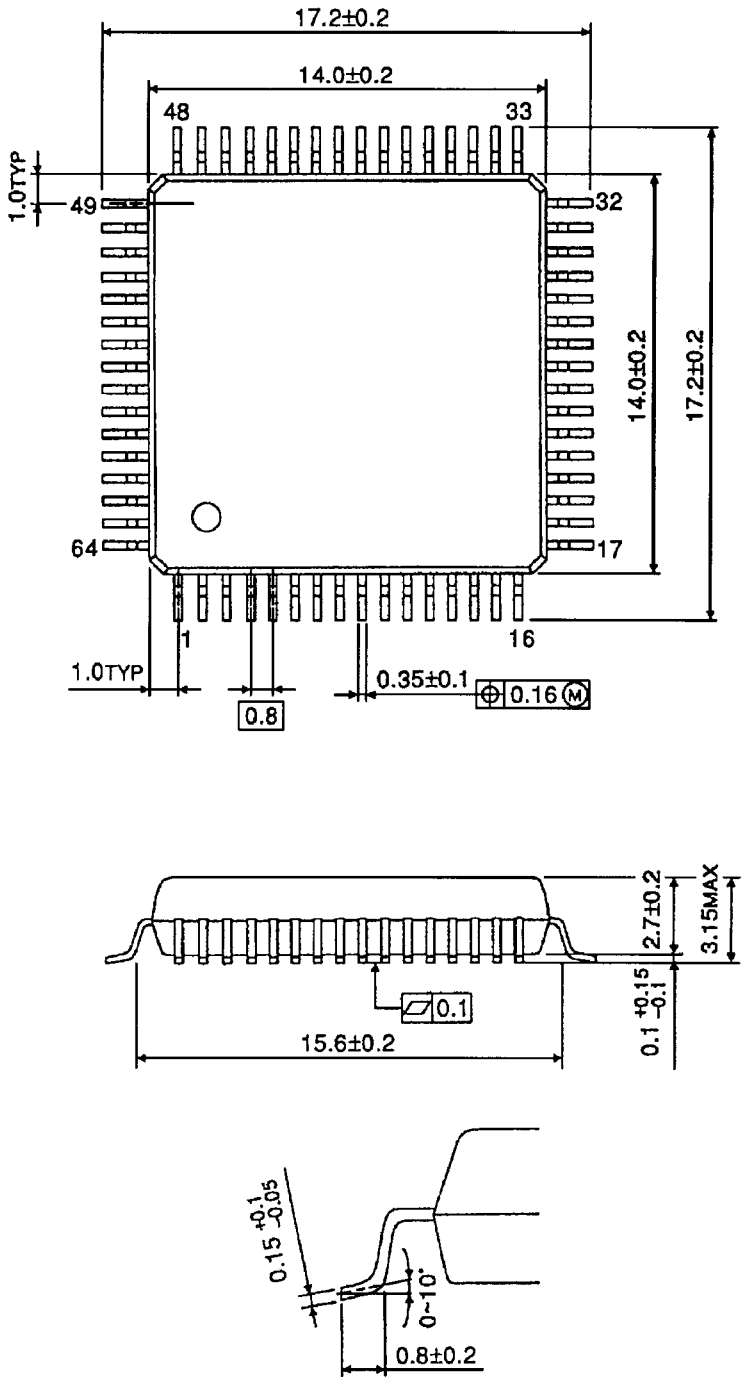
Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output voltage	1/4 level	$V_{1/4}$	—	V_{DD} = 5 V, COM1-COM8	1/4 V_{DD} − 0.3	1/4 V_{DD}	1/4 V_{DD} + 0.3	V
	1/3 level	$V_{1/3}$	—	V_{DD} = 5 V, COM1-COM4, S_0-S_{43}	1/3 V_{DD} − 0.3	1/3 V_{DD}	1/3 V_{DD} + 0.3	
	1/2 level	$V_{1/2}$	—	V_{DD} = 5 V, S_4-S_{43}	1/2 V_{DD} − 0.3	1/2 V_{DD}	1/2 V_{DD} + 0.3	
	2/3 level	$V_{2/3}$	—	V_{DD} = 5 V, COM1-COM4, S_0-S_{43}	2/3 V_{DD} − 0.3	2/3 V_{DD}	2/3 V_{DD} + 0.3	
	3/4 level	$V_{3/4}$	—	V_{DD} = 5 V, COM1-COM8	3/4 V_{DD} − 0.3	3/4 V_{DD}	3/4 V_{DD} + 0.3	
Output current	“H” level	I_{OH}	—	V_{DD} = 5 V, V_{OH} = 4.5 V, KT_0-KT_7, COM1-COM8, S_0-S_{43}, OT_0-OT_3	−0.5	−3.0	—	mA
	“L” level	I_{OL}	—	V_{DD} = 5 V, V_{OL} = 0.5 V, KT_0-KT_7, COM1-COM8, S_0-S_{43}, OT_0-OT_3, DOUT	0.5	3.0	—	
Off leakage current		I_{LO}	—	V_{OUT} = 5.5 V, DOUT	—	—	±1.0	μA
Pull-down resistance		R_{IN}	—	KT_0-KT_7	75	150	300	kΩ
Oscillation frequency		f_{osc}	—	—	—	5	20	kHz

Example for Application Circuit



Package Dimensions

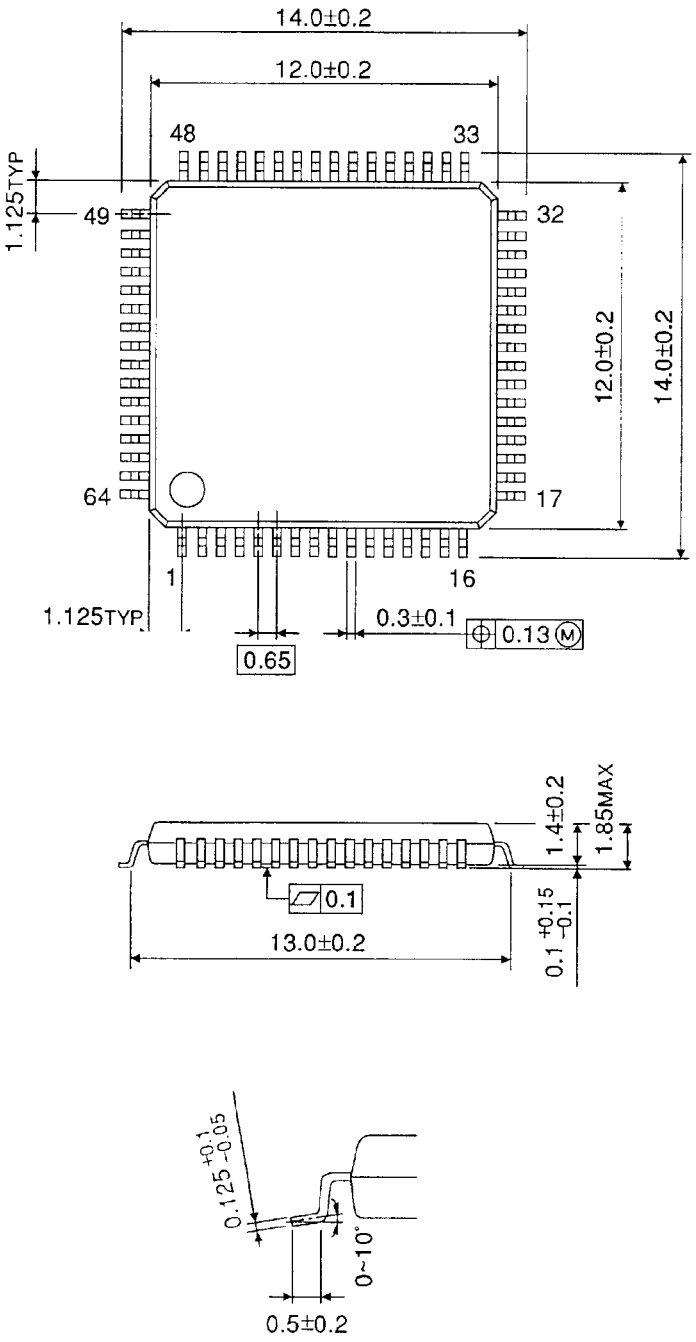
QFP64-P-1414-0.80A Unit : mm



Weight: 1.10 g (typ.)

Package Dimensions

QFP64-P-1212-0.65 Unit : mm



Weight: 0.45 g (typ.)

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