

SN74AVCH32T245
32-BIT DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

SCES589B – AUGUST 2004 – REVISED APRIL 2005

- Member of the Texas Instruments Widebus+™ Family
- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range
- I_{off} Supports Partial-Power-Down Mode Operation
- I/Os Are 4.6-V Tolerant
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 8000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

This 32-bit noninverting bus transceiver uses two separate configurable power-supply rails. The SN74AVCH32T245 is optimized to operate with V_{CCA}/V_{CCB} set at 1.4 V to 3.6 V. It is operational with V_{CCA}/V_{CCB} as low as 1.2 V. The A port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVCH32T245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the outputs so the buses are effectively isolated.

The SN74AVCH32T245 is designed so that the control pins (1DIR, 2DIR, 3DIR, 4DIR, 1 \overline{OE} , 2 \overline{OE} , 3 \overline{OE} , and 4 \overline{OE}) are supplied by V_{CCA} .

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then both ports are in the high-impedance state.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LFBGA – GKE		SN74AVCH32T245KR	
	LFBGA – ZKE (Pb-free)	Tape and reel	74AVCH32T245ZKER	WJ245

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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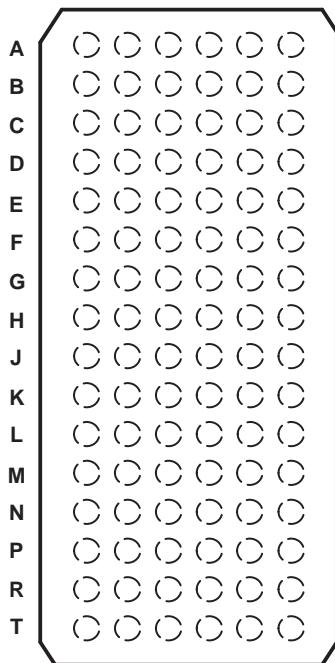
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**GKE OR ZKE PACKAGE
(TOP VIEW)**

1 2 3 4 5 6

**terminal assignments**

	1	2	3	4	5	6
A	1B2	1B1	1DIR	1 \overline{OE}	1A1	1A2
B	1B4	1B3	GND	GND	1A3	1A4
C	1B6	1B5	V _{CCB}	V _{CCA}	1A5	1A6
D	1B8	1B7	GND	GND	1A7	1A8
E	2B2	2B1	GND	GND	2A1	2A2
F	2B4	2B3	V _{CCB}	V _{CCA}	2A3	2A4
G	2B6	2B5	GND	GND	2A5	2A6
H	2B7	2B8	2DIR	2 \overline{OE}	2A8	2A7
J	3B2	3B1	3DIR	3 \overline{OE}	3A1	3A2
K	3B4	3B3	GND	GND	3A3	3A4
L	3B6	3B5	V _{CCB}	V _{CCA}	3A5	3A6
M	3B8	3B7	GND	GND	3A7	3A8
N	4B2	4B1	GND	GND	4A1	4A2
P	4B4	4B3	V _{CCB}	V _{CCA}	4A3	4A4
R	4B6	4B5	GND	GND	4A5	4A6
T	4B7	4B8	4DIR	4 \overline{OE}	4A8	4A7

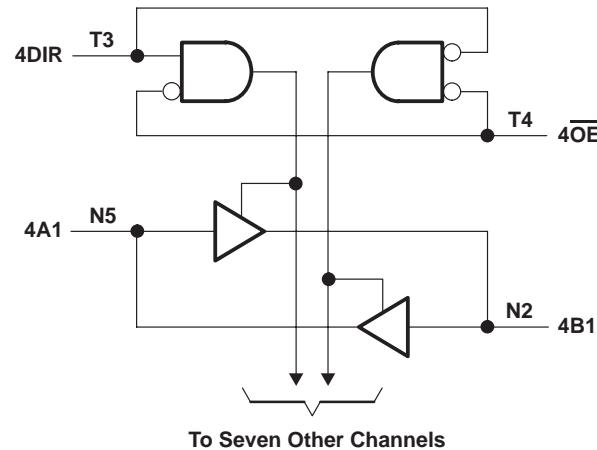
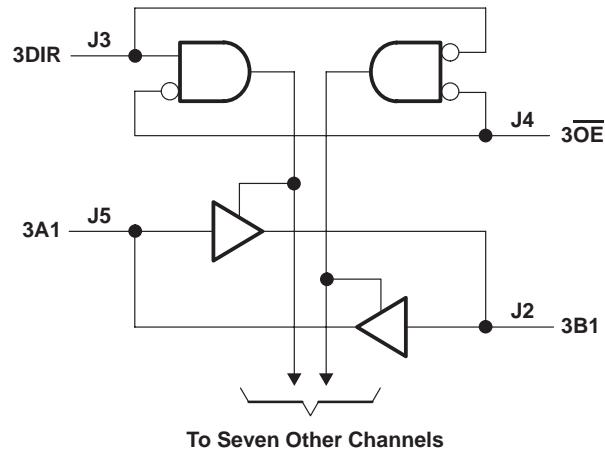
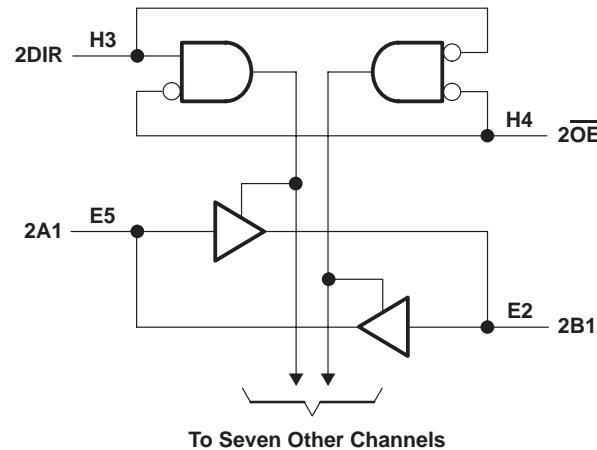
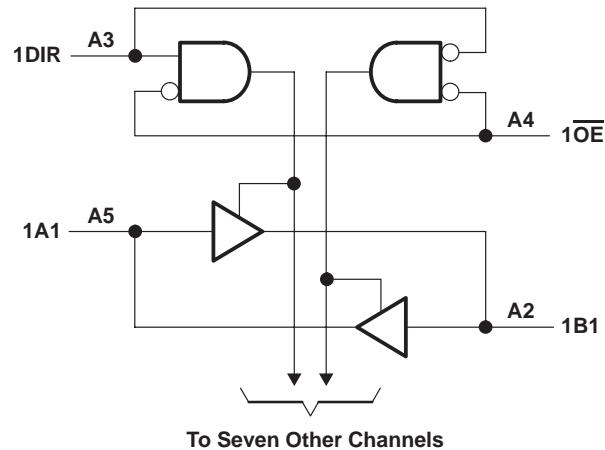
**FUNCTION TABLE
(each 8-bit section)**

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Notes 4 through 8)

		V _{CCI}	V _{CCO}	MIN	MAX	UNIT
V _{CCA}	Supply voltage			1.2	3.6	V
V _{CCB}	Supply voltage			1.2	3.6	V
V _{IH}	High-level input voltage	Data inputs (see Note 7)	1.2 V to 1.95 V		V _{CCI} × 0.65	V
			1.95 V to 2.7 V		1.6	
			2.7 V to 3.6 V		2	
V _{IL}	Low-level input voltage	Data inputs (see Note 7)	1.2 V to 1.95 V		V _{CCI} × 0.35	V
			1.95 V to 2.7 V		0.7	
			2.7 V to 3.6 V		0.8	
V _{IH}	High-level input voltage	DIR (referenced to V _{CCA}) (see Note 8)	1.2 V to 1.95 V		V _{CCA} × 0.65	V
			1.95 V to 2.7 V		1.6	
			2.7 V to 3.6 V		2	
V _{IL}	Low-level input voltage	DIR (referenced to V _{CCA}) (see Note 8)	1.2 V to 1.95 V		V _{CCA} × 0.35	V
			1.95 V to 2.7 V		0.7	
			2.7 V to 3.6 V		0.8	
V _I	Input voltage			0	3.6	V
V _O	Output voltage	Active state		0	V _{CCO}	V
		3-state		0	3.6	
I _{OH}	High-level output current		1.2 V		-3	mA
			1.4 V to 1.6 V		-6	
			1.65 V to 1.95 V		-8	
			2.3 V to 2.7 V		-9	
			3 V to 3.6 V		-12	
I _{OL}	Low-level output current		1.2 V		3	mA
			1.4 V to 1.6 V		6	
			1.65 V to 1.95 V		8	
			2.3 V to 2.7 V		9	
			3 V to 3.6 V		12	
Δt/Δv	Input transition rise or fall rate				5	ns/V
T _A	Operating free-air temperature			-40	85	°C

- NOTES: 4. V_{CCI} is the V_{CC} associated with the data input port.
 5. V_{CCO} is the V_{CC} associated with the output port.
 6. All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
 7. For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V.
 8. For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Notes 9 and 10)

PARAMETER	TEST CONDITIONS	V _{CCA}	V _{CCB}	T _A = 25°C			-40°C TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = -100 µA	V _I = V _{IH}	1.2 V to 3.6 V	1.2 V to 3.6 V			V _{CCO} – 0.2 V		V
	I _{OH} = -3 mA		1.2 V	1.2 V	0.95				
	I _{OH} = -6 mA		1.4 V	1.4 V			1.05		
	I _{OH} = -8 mA		1.65 V	1.65 V			1.2		
	I _{OH} = -9 mA		2.3 V	2.3 V			1.75		
	I _{OH} = -12 mA		3 V	3 V			2.3		
V _{OL}	I _{OL} = 100 µA	V _I = V _{IL}	1.2 V to 3.6 V	1.2 V to 3.6 V			0.2		V
	I _{OL} = 3 mA		1.2 V	1.2 V	0.15				
	I _{OL} = 6 mA		1.4 V	1.4 V			0.35		
	I _{OL} = 8 mA		1.65 V	1.65 V			0.45		
	I _{OL} = 9 mA		2.3 V	2.3 V			0.55		
	I _{OL} = 12 mA		3 V	3 V			0.7		
I _I	Control inputs	V _I = V _{CCA} or GND	1.2 V to 3.6 V	1.2 V to 3.6 V	±0.025	±0.25	±1	µA	
I _{BHL} [†]	V _I = 0.42 V		1.2 V	1.2 V	25				µA
	V _I = 0.49 V		1.4 V	1.4 V			15		
	V _I = 0.58 V		1.65 V	1.65 V			25		
	V _I = 0.7 V		2.3 V	2.3 V			45		
	V _I = 0.8 V		3.3 V	3.3 V			100		
I _{BHH} [‡]	V _I = 0.78 V		1.2 V	1.2 V	-25				µA
	V _I = 0.91 V		1.4 V	1.4 V			-15		
	V _I = 1.07 V		1.65 V	1.65 V			-25		
	V _I = 1.6 V		2.3 V	2.3 V			-45		
	V _I = 2 V		3.3 V	3.3 V			-100		
I _{BHLO} [§]	V _I = 0 to V _{CC}	1.2 V	1.2 V	50					µA
		1.6 V	1.6 V				125		
		1.95 V	1.95 V				200		
		2.7 V	2.7 V				300		
		3.6 V	3.6 V				500		
I _{BHHO} [¶]	V _I = 0 to V _{CC}	1.2 V	1.2 V	-50					µA
		1.6 V	1.6 V				-125		
		1.95 V	1.95 V				-200		
		2.7 V	2.7 V				-300		
		3.6 V	3.6 V				-500		

[†] The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

[‡] The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

[§] An external driver must source at least I_{BHLO} to switch this node from low to high.

[¶] An external driver must sink at least I_{BHHO} to switch this node from high to low.

NOTES: 9. V_{CCO} is the V_{CC} associated with the output port.

10. V_{CCI} is the V_{CC} associated with the input port.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Notes 9 and 10) (continued)

PARAMETER		TEST CONDITIONS		V _{CCA}	V _{CCB}	T _A = 25°C			-40°C TO 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
I _{off}	A port	V _I or V _O = 0 to 3.6 V		0 V	0 to 3.6 V	±0.1	±2.5		±5		μA
	B port			0 to 3.6 V	0 V	±0.1	±2.5		±5		
I _{OZ} [#]	A or B ports	V _O = V _{CCO} or GND, V _I = V _{CCI} or GND	$\overline{OE} = V_{IH}$	3.6 V	3.6 V	±0.5	±2.5		±5		μA
	B port			0 V	3.6 V				±5		
	A port			3.6 V	0 V				±5		
I _{CCA}		V _I = V _{CCI} or GND,	I _O = 0	1.2 V to 3.6 V	1.2 V to 3.6 V				50		μA
				0 V	3.6 V				-10		
				3.6 V	0 V				50		
I _{CCB}		V _I = V _{CCI} or GND,	I _O = 0	1.2 V to 3.6 V	1.2 V to 3.6 V				50		μA
				0 V	3.6 V				50		
				3.6 V	0 V				-10		
I _{CCA} + I _{CCB}		V _I = V _{CCI} or GND,	I _O = 0	1.2 V to 3.6 V	1.2 V to 3.6 V				90		μA
C _i	Control inputs			3.3 V	3.3 V				3.5		pF
C _{io}	A or B ports	V _O = 3.3 V or GND		3.3 V	3.3 V				7		pF

For I/O ports, the parameter I_{OZ} includes the input leakage current.

NOTES: 9. V_{CCO} is the V_{CC} associated with the output port.

10. V_{CCI} is the V_{CC} associated with the input port.

switching characteristics over recommended operating free-air temperature range,
V_{CCA} = 1.2 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.2 V	V _{CCB} = 1.5 V	V _{CCB} = 1.8 V	V _{CCB} = 2.5 V	V _{CCB} = 3.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
t _{PLH}	A	B	4.1	3.3	3	2.8	3.2	ns
			4.1	3.3	3	2.8	3.2	
t _{PHL}	B	A	4.4	4	3.8	3.6	3.5	ns
			4.4	4	3.8	3.6	3.5	
t _{PZH}	\overline{OE}	A	6.4	6.4	6.4	6.4	6.4	ns
			6.4	6.4	6.4	6.4	6.4	
t _{PZL}	\overline{OE}	B	6	4.6	4	3.4	3.2	ns
			6	4.6	4	3.4	3.2	
t _{PHZ}	\overline{OE}	A	6.6	6.6	6.6	6.6	6.8	ns
			6.6	6.6	6.6	6.6	6.8	
t _{PLZ}	\overline{OE}	B	6	4.9	4.9	4.2	5.3	ns
			6	4.9	4.9	4.2	5.3	

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switching characteristics over recommended operating free-air temperature range,
 $V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3.6	0.5	6.2	0.5	5.2	0.5	4.1	0.5	3.7	ns
t_{PHL}			3.6	0.5	6.2	0.5	5.2	0.5	4.1	0.5	3.7	
t_{PLH}	B	A	3.3	0.5	6.2	0.5	5.9	0.5	5.6	0.5	5.5	ns
t_{PHL}			3.3	0.5	6.2	0.5	5.9	0.5	5.6	0.5	5.5	
t_{PZH}	\overline{OE}	A	4.3	1	10.1	1	10.1	1	10.1	1	10.1	ns
t_{PZL}			4.3	1	10.1	1	10.1	1	10.1	1	10.1	
t_{PZH}	\overline{OE}	B	5.6	1	10.1	0.5	8.1	0.5	5.9	0.5	5.2	ns
t_{PZL}			5.6	1	10.1	0.5	8.1	0.5	5.9	0.5	5.2	
t_{PHZ}	\overline{OE}	A	4.5	1.5	9.1	1.5	9.1	1.5	9.1	1.5	9.1	ns
t_{PLZ}			4.5	1.5	9.1	1.5	9.1	1.5	9.1	1.5	9.1	
t_{PHZ}	\overline{OE}	B	5.5	1.5	8.7	1.5	7.5	1	6.5	1	6.3	ns
t_{PLZ}			5.5	1.5	8.7	1.5	7.5	1	6.5	1	6.3	

switching characteristics over recommended operating free-air temperature range,
 $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3.4	0.5	5.9	0.5	4.8	0.5	3.7	0.5	3.3	ns
t_{PHL}			3.4	0.5	5.9	0.5	4.8	0.5	3.7	0.5	3.3	
t_{PLH}	B	A	3	0.5	5.2	0.5	4.8	0.5	4.5	0.5	4.4	ns
t_{PHL}			3	0.5	5.2	0.5	4.8	0.5	4.5	0.5	4.4	
t_{PZH}	\overline{OE}	A	3.4	1	7.8	1	7.8	1	7.8	1	7.8	ns
t_{PZL}			3.4	1	7.8	1	7.8	1	7.8	1	7.8	
t_{PZH}	\overline{OE}	B	5.4	1	9.2	0.5	7.4	0.5	5.3	0.5	4.5	ns
t_{PZL}			5.4	1	9.2	0.5	7.4	0.5	5.3	0.5	4.5	
t_{PHZ}	\overline{OE}	A	4.2	1.5	7.7	1.5	7.7	1.5	7.7	1.5	7.7	ns
t_{PLZ}			4.2	1.5	7.7	1.5	7.7	1.5	7.7	1.5	7.7	
t_{PHZ}	\overline{OE}	B	5.2	1.5	8.4	1.5	7.1	1	5.9	1	5.7	ns
t_{PLZ}			5.2	1.5	8.4	1.5	7.1	1	5.9	1	5.7	

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switching characteristics over recommended operating free-air temperature range,
 $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
tPLH	A	B	3.2	0.5	5.6	0.5	4.5	0.5	3.3	0.5	2.8	ns
tPHL			3.2	0.5	5.6	0.5	4.5	0.5	3.3	0.5	2.8	
tPLH	B	A	2.6	0.5	4.1	0.5	3.7	0.5	3.3	0.5	3.2	ns
tPHL			2.6	0.5	4.1	0.5	3.7	0.5	3.3	0.5	3.2	
tPZH	\overline{OE}	A	2.5	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	ns
tPZL			2.5	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	
tPZH	\overline{OE}	B	5.2	0.5	9.4	0.5	7.3	0.5	5.1	0.5	4.5	ns
tPZL			5.2	0.5	9.4	0.5	7.3	0.5	5.1	0.5	4.5	
tPHZ	\overline{OE}	A	3	1	6.1	1	6.1	1	6.1	1	6.1	ns
tPLZ			3	1	6.1	1	6.1	1	6.1	1	6.1	
tPHZ	\overline{OE}	B	5	1	7.9	1	6.6	1	6.1	1	5.2	ns
tPLZ			5	1	7.9	1	6.6	1	6.1	1	5.2	

switching characteristics over recommended operating free-air temperature range,
 $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
tPLH	A	B	3.2	0.5	5.5	0.5	4.4	0.5	3.2	0.5	2.7	ns
tPHL			3.2	0.5	5.5	0.5	4.4	0.5	3.2	0.5	2.7	
tPLH	B	A	2.8	0.5	3.7	0.5	3.3	0.5	2.8	0.5	2.7	ns
tPHL			2.8	0.5	3.7	0.5	3.3	0.5	2.8	0.5	2.7	
tPZH	\overline{OE}	A	2.2	0.5	4.3	0.5	4.2	0.5	4.1	0.5	4	ns
tPZL			2.2	0.5	4.3	0.5	4.2	0.5	4.1	0.5	4	
tPZH	\overline{OE}	B	5.1	0.5	9.3	0.5	7.2	0.5	4.9	0.5	4	ns
tPZL			5.1	0.5	9.3	0.5	7.2	0.5	4.9	0.5	4	
tPHZ	\overline{OE}	A	3.4	0.5	5	0.5	5	0.5	5	0.5	5	ns
tPLZ			3.4	0.5	5	0.5	5	0.5	5	0.5	5	
tPHZ	\overline{OE}	B	4.9	1	7.7	1	6.5	1	5.2	0.5	5	ns
tPLZ			4.9	1	7.7	1	6.5	1	5.2	0.5	5	

SN74AVCH32T245**32-BIT DUAL-SUPPLY BUS TRANSCEIVER****WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS**

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operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CCA} = V_{CCB} = 1.2\text{ V}$	$V_{CCA} = V_{CCB} = 1.5\text{ V}$	$V_{CCA} = V_{CCB} = 1.8\text{ V}$	$V_{CCA} = V_{CCB} = 2.5\text{ V}$	$V_{CCA} = V_{CCB} = 3.3\text{ V}$	UNIT
				TYP	TYP	TYP	TYP	TYP	
C_{pdA}^\dagger	A to B	Outputs enabled	$C_L = 0$, $f = 10\text{ MHz}$, $t_r = t_f = 1\text{ ns}$	1	1	1	1	2	pF
		Outputs disabled		1	1	1	1	1	
	B to A	Outputs enabled		13	13	14	15	16	
		Outputs disabled		1	1	1	1	1	
	C_{pdB}^\dagger	Outputs enabled		13	13	14	15	16	pF
		Outputs disabled		1	1	1	1	1	
		Outputs enabled		1	1	1	1	2	
		Outputs disabled		1	1	1	1	1	

† Power-dissipation capacitance per transceiver

SN74AVCH32T245
32-BIT DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS
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typical total static power consumption ($I_{CCA} + I_{CCB}$)

Table 1

V_{CCB}	V_{CCA}						UNIT
	0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	<1	<1	<1	<1	<1	
1.2 V	<1	<2	<2	<2	<2	2	
1.5 V	<1	<2	<2	<2	<2	2	
1.8 V	<1	<2	<2	<2	<2	<2	
2.5 V	<1	2	<2	<2	<2	<2	
3.3 V	<1	2	<2	<2	<2	<2	

SN74AVCH32T245
32-BIT DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

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TYPICAL CHARACTERISTICS

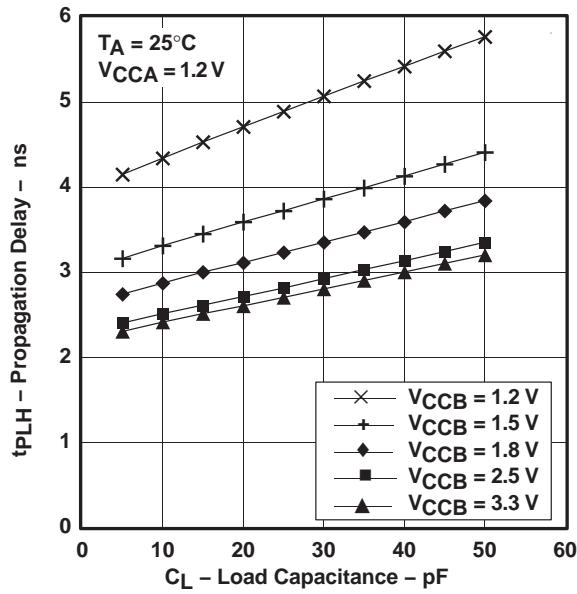


Figure 1

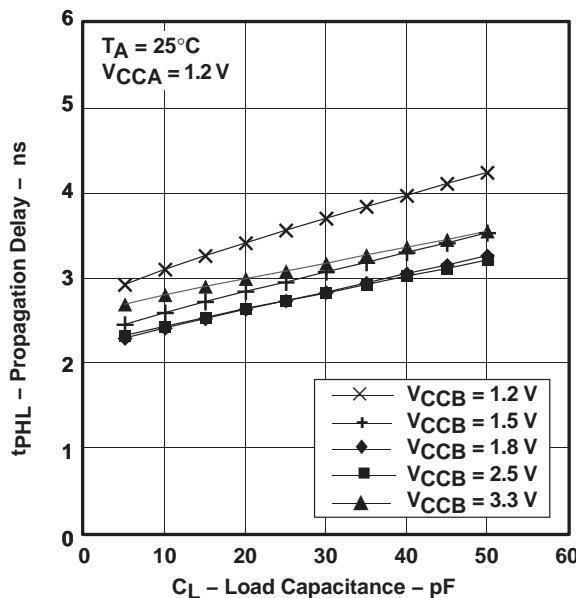


Figure 2

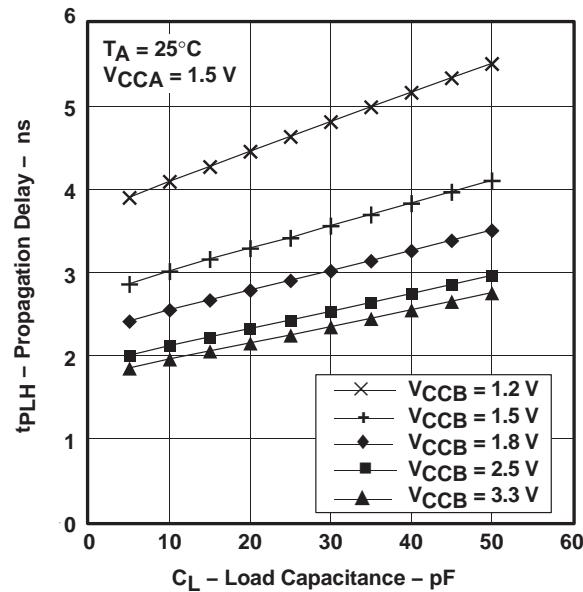


Figure 3

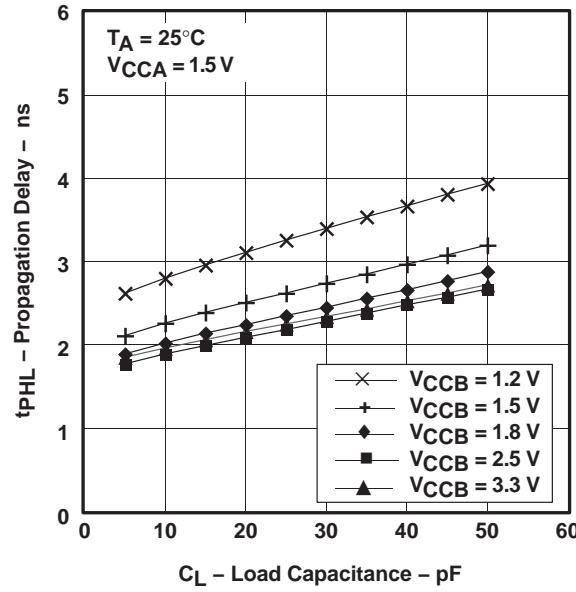


Figure 4

TYPICAL CHARACTERISTICS

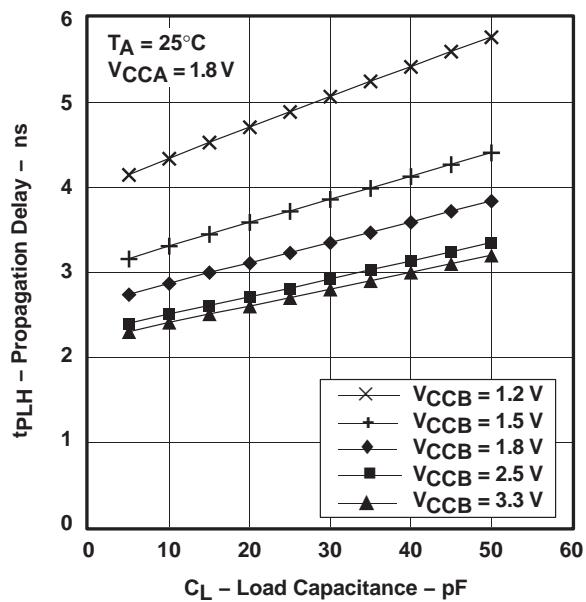


Figure 5

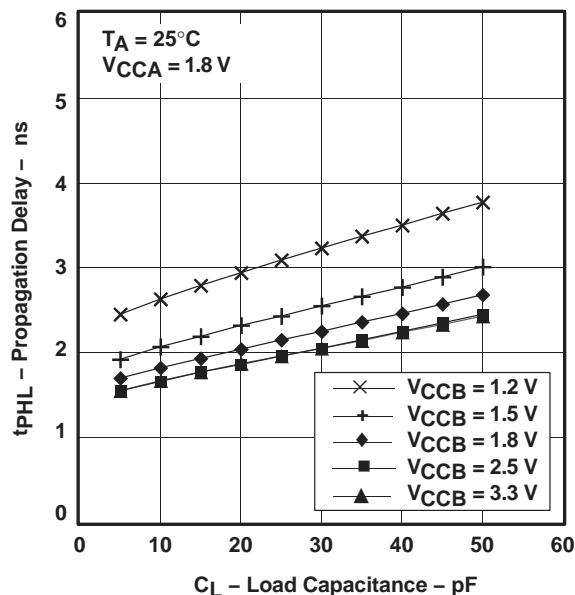


Figure 6

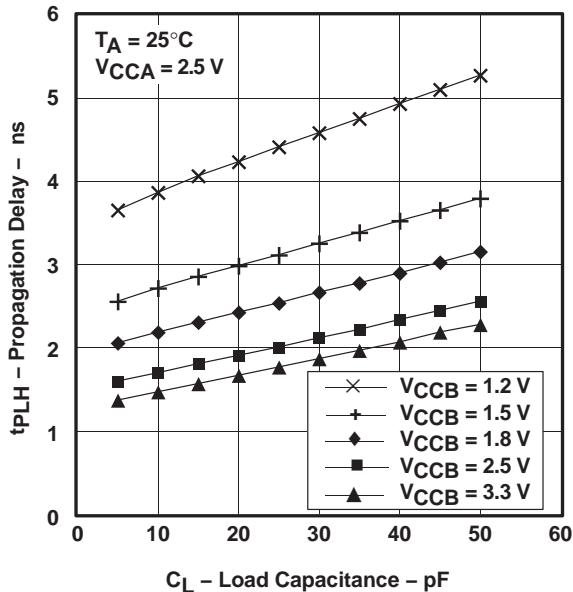


Figure 7

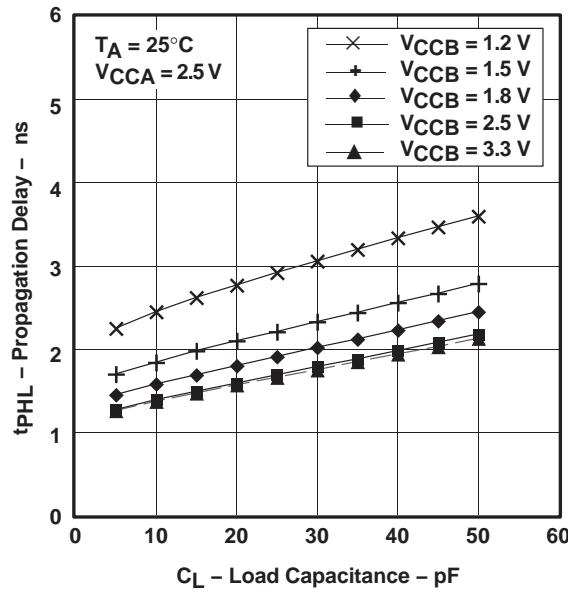


Figure 8

TYPICAL CHARACTERISTICS

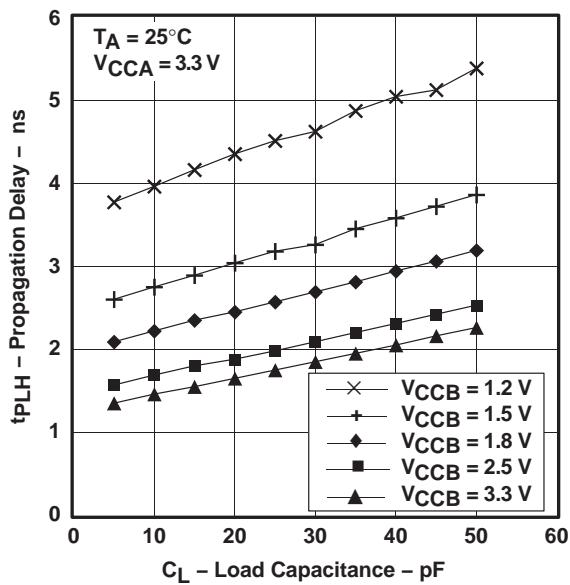


Figure 9

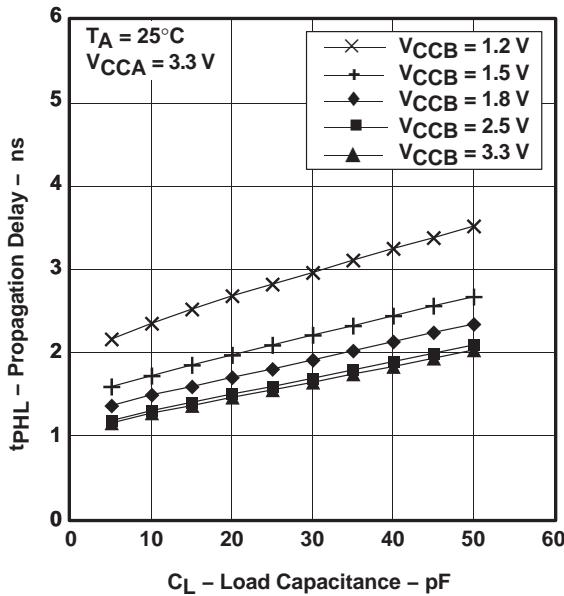
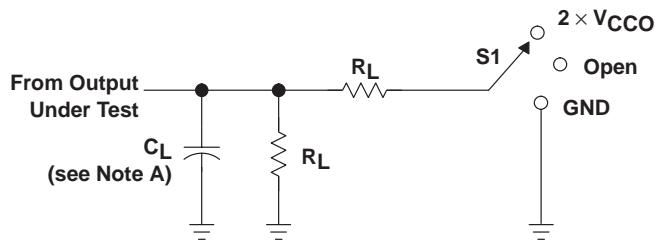


Figure 10

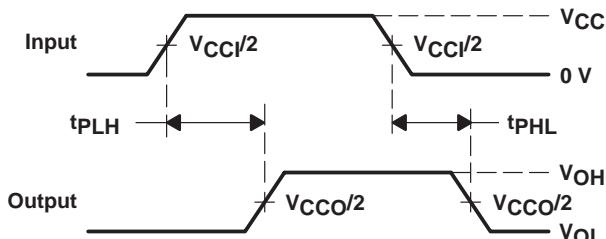
PARAMETER MEASUREMENT INFORMATION



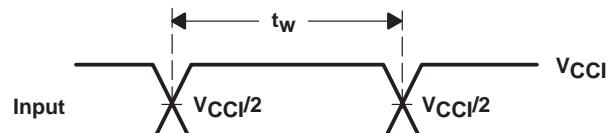
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

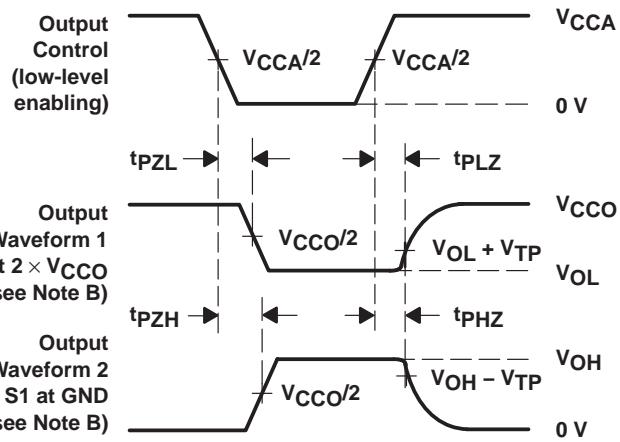
V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 k Ω	0.1 V
$1.5 V \pm 0.1 V$	15 pF	2 k Ω	0.1 V
$1.8 V \pm 0.15 V$	15 pF	2 k Ω	0.15 V
$2.5 V \pm 0.2 V$	15 pF	2 k Ω	0.15 V
$3.3 V \pm 0.3 V$	15 pF	2 k Ω	0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $dv/dt \geq 1$ V/ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. V_{CCI} is the V_{CC} associated with the input port.
 - I. V_{CCO} is the V_{CC} associated with the output port.

Figure 11. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AVCH32T245KR	NRND	LFBGA	GKE	96	1000	TBD	SNPB	Level-2-235C-1 YEAR	-40 to 85	(WJ245 ~ WR245)	
SN74AVCH32T245ZKER	ACTIVE	LFBGA	ZKE	96	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	WR245	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

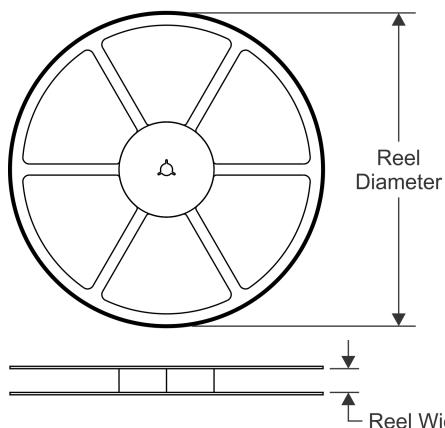
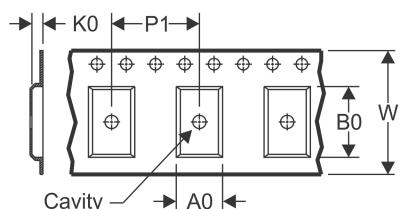
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

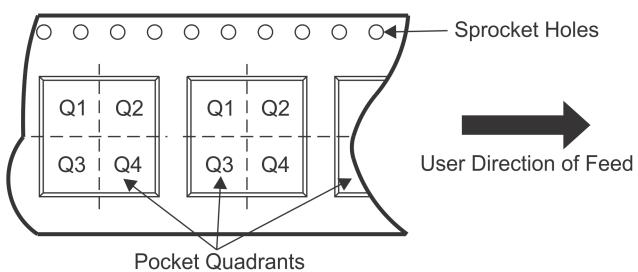
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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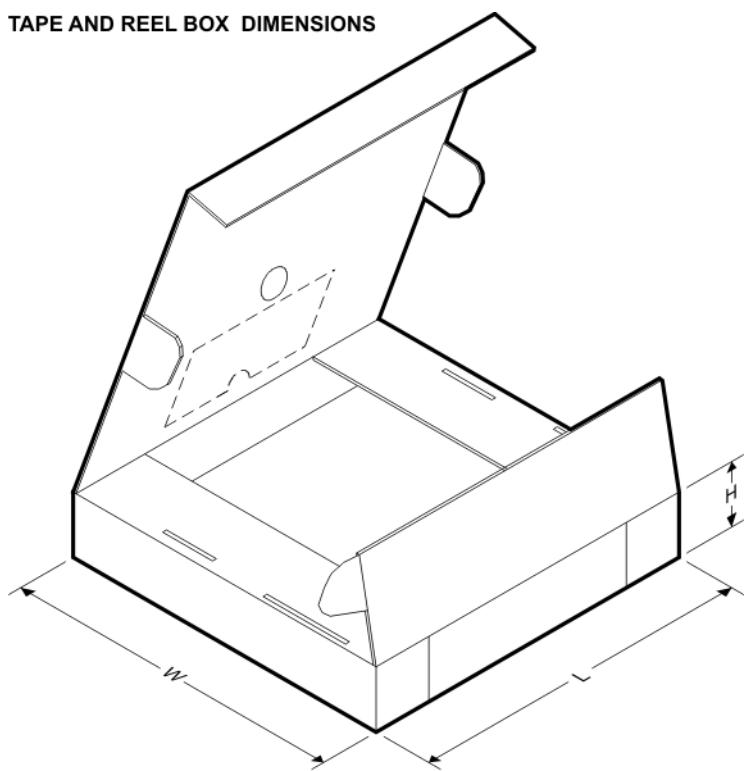
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVCH32T245KR	LFBGA	GKE	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1
SN74AVCH32T245ZKER	LFBGA	ZKE	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1

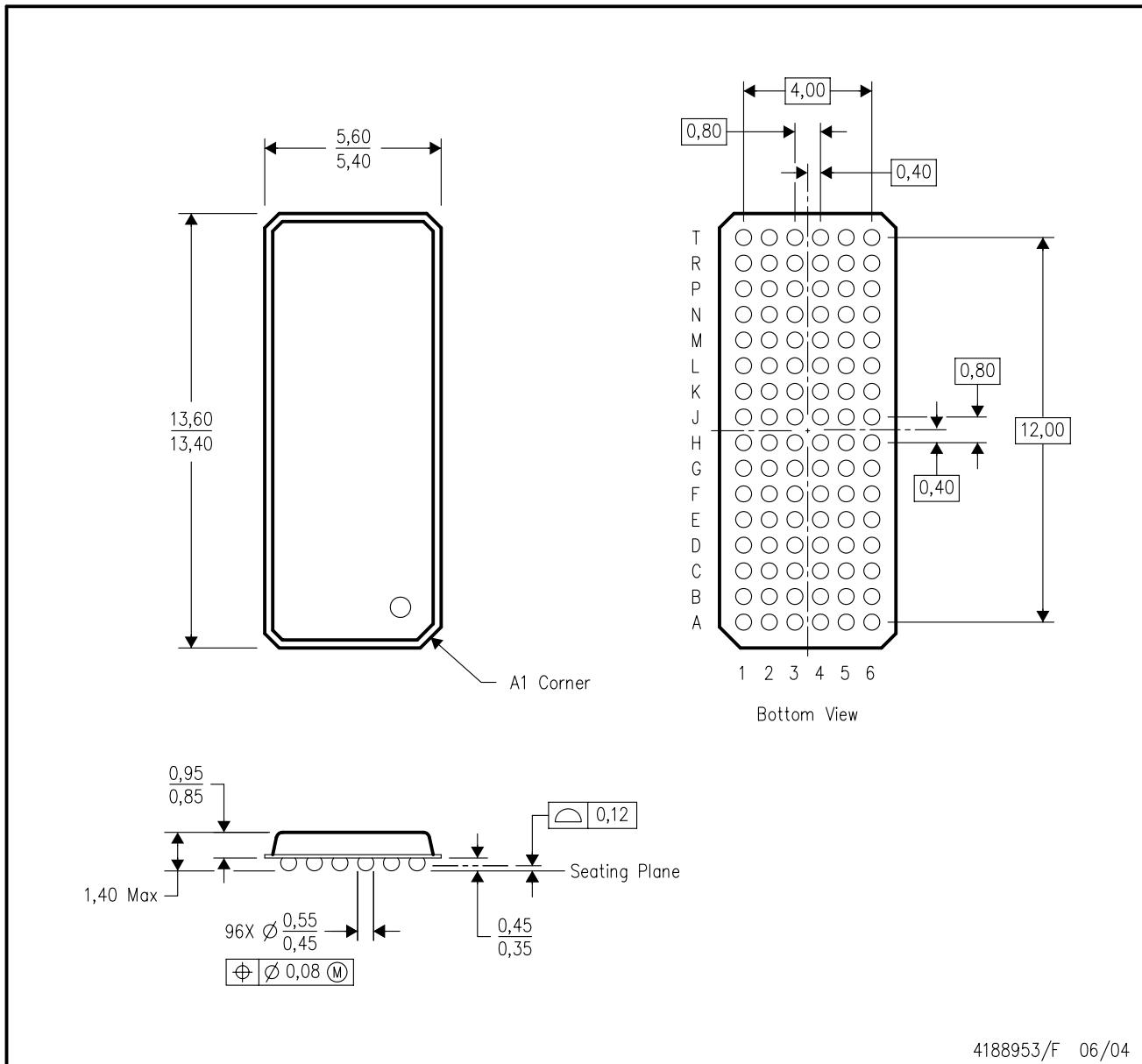
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVCH32T245KR	LFBGA	GKE	96	1000	336.6	336.6	41.3
SN74AVCH32T245ZKER	LFBGA	ZKE	96	1000	336.6	336.6	41.3

GKE (R-PBGA-N96)

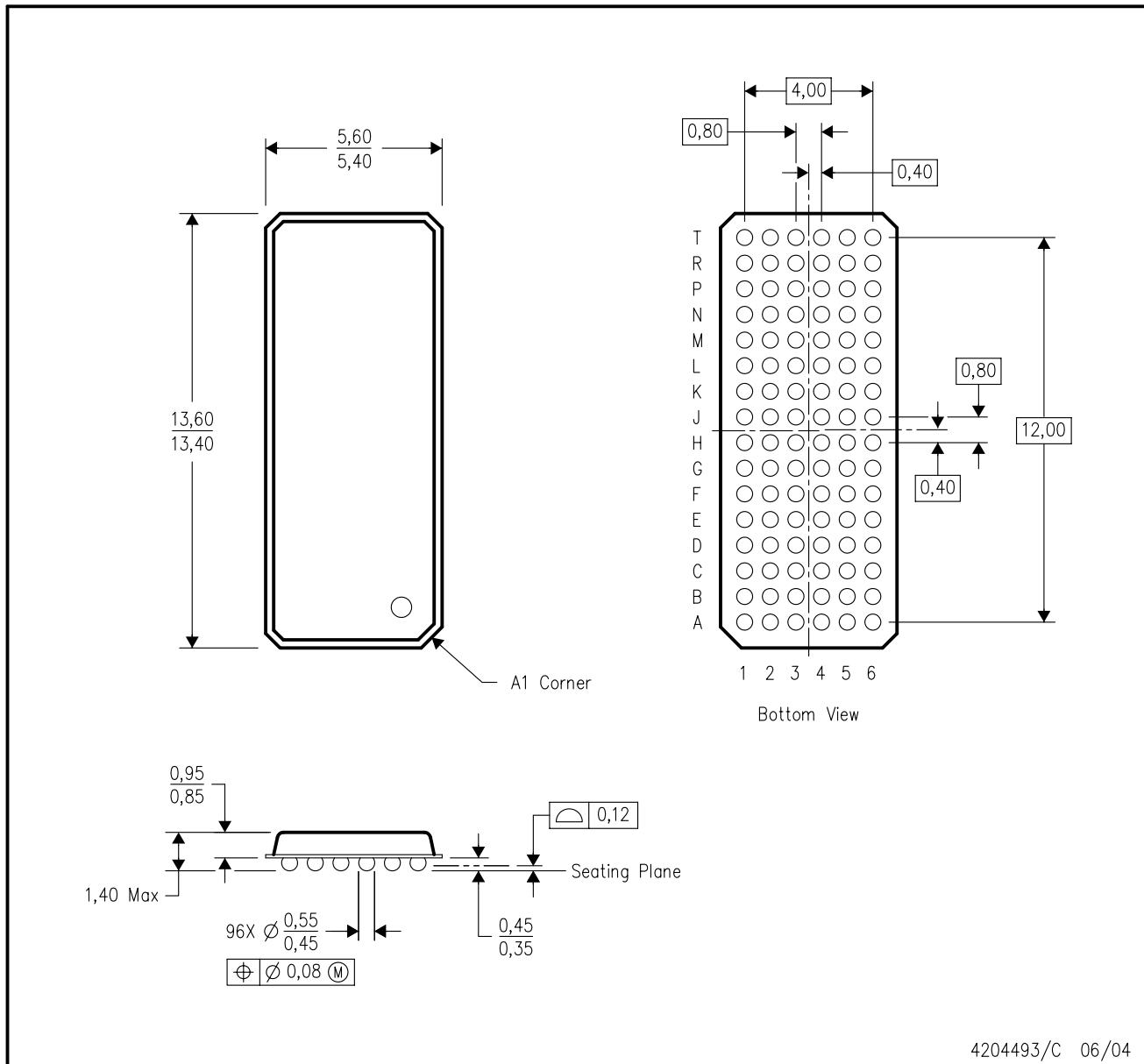
PLASTIC BALL GRID ARRAY



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Falls within JEDEC MO-205 variation CC.
 - This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.

ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Falls within JEDEC MO-205 variation CC.
 - This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).

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