

# **TAS5066-5121K6EVM** **PurePath Digital™ EVM**

**for the TAS5066PAG Six-Channel Digital Audio  
PWM Processor and TAS5121DKD Digital  
Amplifier Power Output Stage**

## *User's Guide*

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During normal operation, some circuit components may have case temperatures greater than xxx°C. The EVM is designed to operate properly with certain components above xxx°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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## Preface

# Read This First

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### ***About This Manual***

This manual describes the operation of the TAS5066-5121K6EVM evaluation module from Texas Instruments.

### ***How to Use This Manual***

This document contains the following chapters:

- Chapter 1 — Overview
- Chapter 2 — System Interfaces
- Chapter 3 — Protection

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This document may contain cautions and warnings.

**This is an example of a caution statement.**

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### **Related Documentation from Texas Instruments**

The following table contains a list of data manuals that have detailed descriptions of the integrated circuits used in the design of the TAS5066–5121K6EVM. The data manuals can be obtained at the URL <http://www.ti.com>.

Part Number	Literature Number
TAS5066PAG	SLES089
TAS5121DKD	SLES086
SN74LV123	SCLS393J
SN74AHC1G08	SCLS314J
SN74LVC1G126	SCES224K
TPS76433	SLVS180B
TPS3801K33	SLVS219B
LM317MKTP	SLVS297K

### **Additional Documentation**

- TAS5066–5121K6EVM Application Report – SLEA032
- PC Configuration Tool for TAS50XX (DAS TCT 50xx – version 3.1 or later)
- General Application Notes

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## Chapter 1

# Overview

The TAS5066–5121K6EVM PurePath Digital™ customer evaluation module demonstrates two integrated circuits TAS5066 and TAS5121 from Texas Instruments (TI).

The TAS5066 is a high-performance 24-bit six-channel digital pulse width modulator (PWM) based Equibit™ technology. The TAS5066 has a wide variety of serial input (I<sup>2</sup>S) options including right justified, left justified, and DSP data formats. It accepts I<sup>2</sup>S data with sample rates up to 192 kHz.

TAS5121 is a high-performance digital amplifier power stage designed to drive a 4-Ohm loudspeaker up to 100 W. It contains integrated gate-drivers, four matched and electrically isolated enhancement-mode N-channel power DMOS transistors and protection / fault-reporting circuitry.

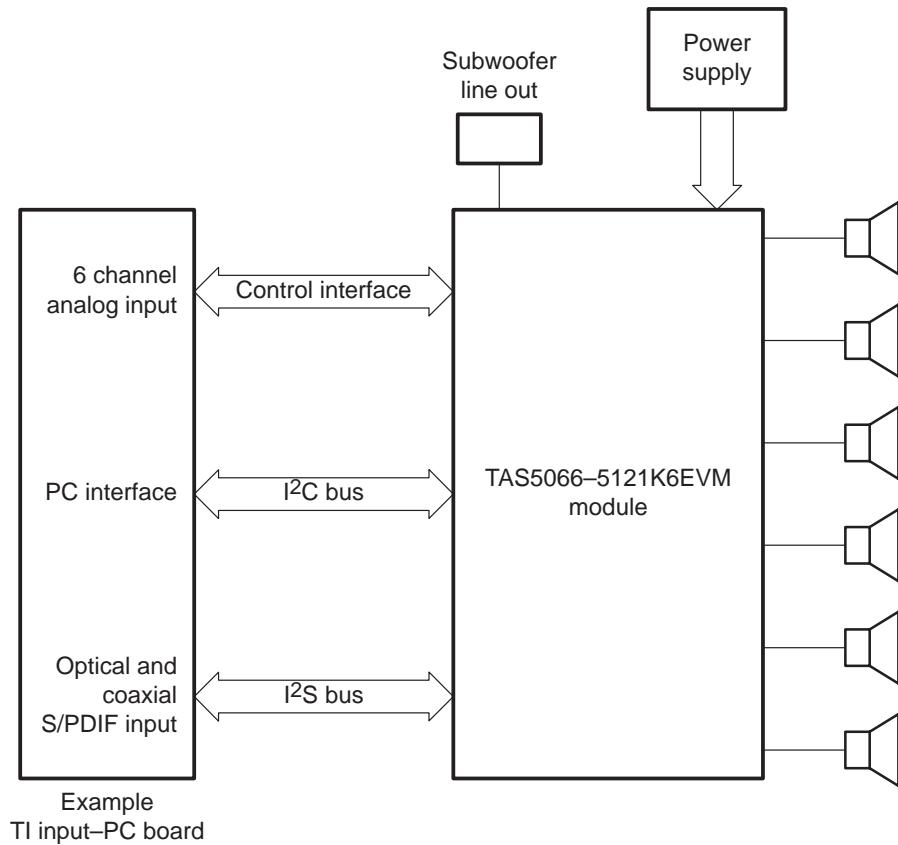
The TAS5066–5121K6EVM, together with a TI input board, is a complete digital audio amplifier system which includes digital input (S/PDIF), analog input, interface to PC, digital volume control, and failure protection. The system was design for home theater applications such as DVD minicomponent systems, home theater in a box (HTIB), DVD receiver, A/V receiver, or TV sets.

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## 1.1 TAS5066-5121K6EVM Features

- 6-channel PurePath Digital™ evaluation module
- Double-sided plated-through PCB layout
- Self-contained protection system (short circuit and thermal)
- Standard I<sup>2</sup>S and I<sup>2</sup>C/control connector for TI input board

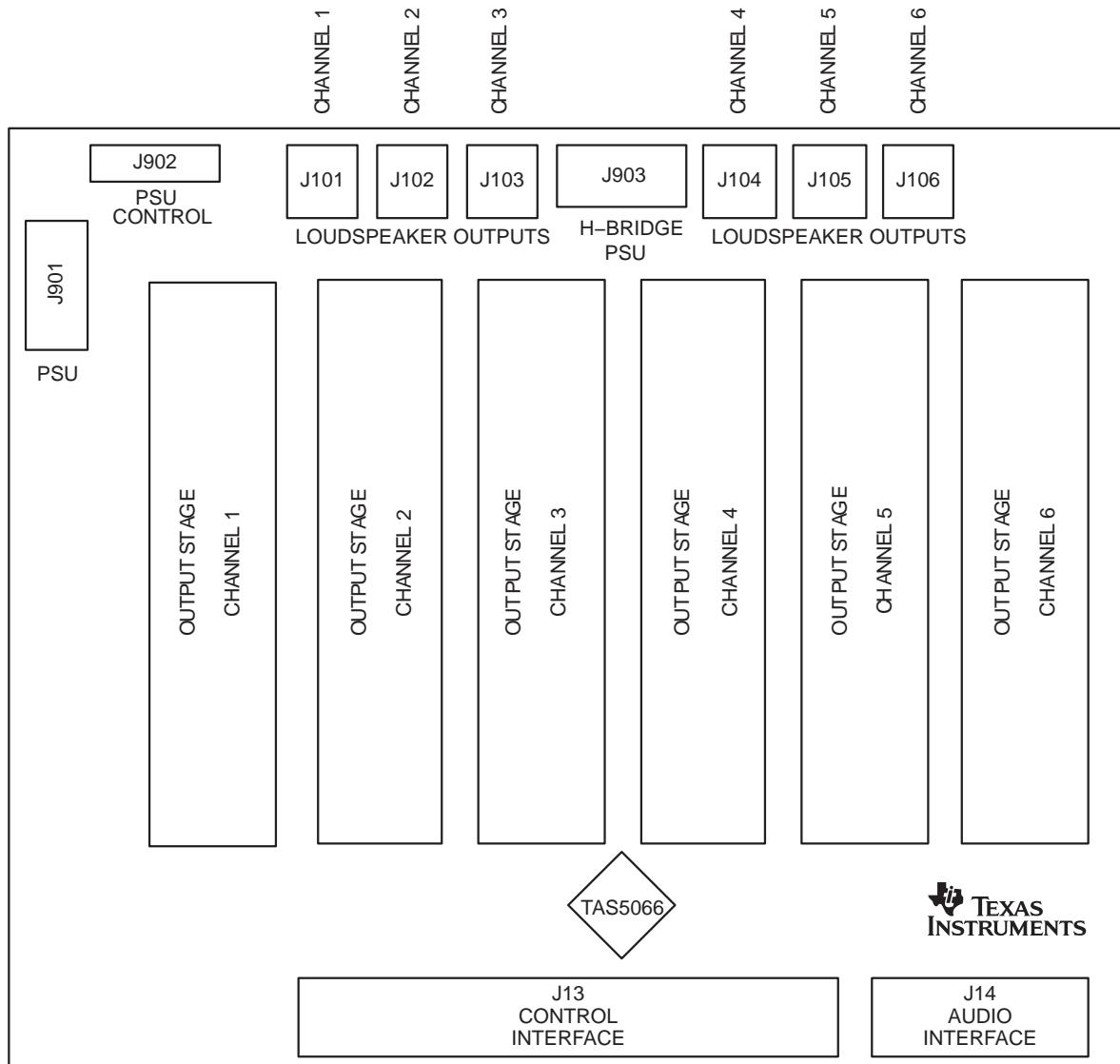
Figure 1-1. Complete PurePath Digital™ System



## 1.2 PCB Key Map

The physical structure for the TAS5066-5121K6EVM is illustrated in the following figure.

Figure 1-2. Physical Structure for the TAS5066-5121K6EVM





## Chapter 2

# System Interfaces

This chapter describes the TAS5066–5121K6EVM board in regards to power supply (PSU) and system interfaces.

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## 2.1 PSU Interface (J901 and J903)

The TAS5066–5121K6EVM module must be powered from external power supplies. High-end audio performance requires a stabilized power supply with low ripple voltage and low output impedance.

**Note:**

The length of power supply cable must be minimized. Increasing length of PSU cable is equal to increasing the distortion for the amplifier at high output levels and low frequencies.

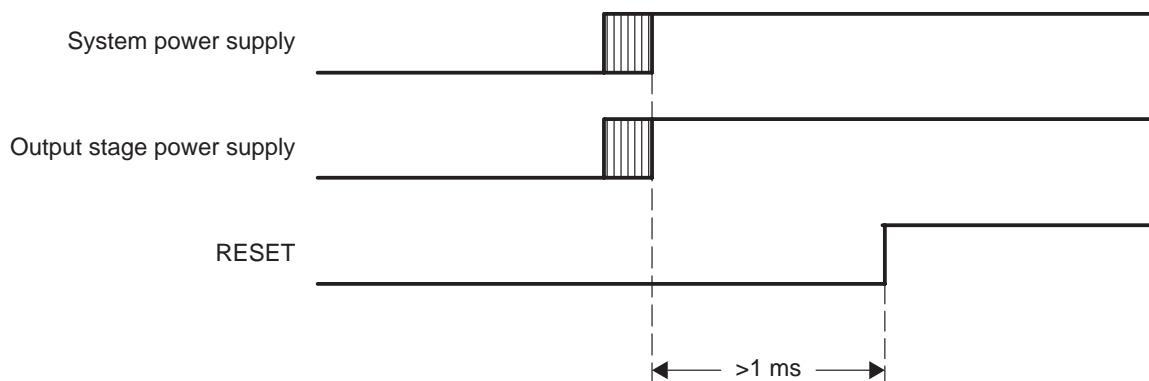
Maximum output stage supply voltage depends of the speaker load resistance. Please check the recommended maximum supply voltage in the TAS5121 datasheet.

*Table 2–1. Recommended Power Supplies*

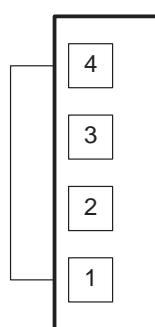
Description	Voltage Limitations (4- $\Omega$ Load)	Current Recommendations
System power supply	15 to 20 V	0.25 A
Output power stage supply	0 to 29.5 V	4.8 A

Figure 2–1 shows the recommended TAS5121 power-up sequence. For proper TAS5121 operation the  $\overline{\text{RESET}}$  signal must be kept low during power-up.  $\overline{\text{RESET}}$  is pulled low during power-up for 200 ms by the on-board reset generator (U903).

*Figure 2–1. Recommended Power-Up Sequence*



*Figure 2–2. J901 and J903 Pin Numbers (PCB Connector Top View)*



*Table 2-2. J901 Pin Description*

Pin Number	Net-Name at Schematics	Description
1	V-HBRIDGE	Output stage power supply
2	–	System power supply
3	GND	Ground
4	GND	Ground

*Table 2-3. J903 Pin Description*

Pin Number	Net-Name at Schematics	Description
1	V-HBRIDGE	Output stage power supply
2	V-HBRIDGE	Output stage power supply
3	GND	Ground
4	GND	Ground

Note: Optional, use to decrease impedance to achieve better performance.

## 2.2 PSU Control Interface (J902)

This interface is used for on-board sensing of output supply voltage.

Figure 2-3. J902 Pin Numbers (PCB Connector Top View)

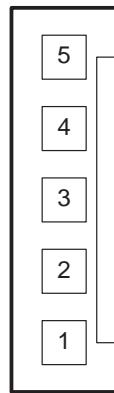


Table 2-4. J902 Pin Description

Pin Number	Net-Name at Schematics	Description
1	NOT USED	–
2	V-HBRIDGE	Sense of output supply voltage
3	GND	Ground
4	RESET	System reset (bi-directional)
5	V-HBRIDGE-CTRL	Power supply output voltage control signal

## 2.3 Loudspeaker Connectors (J100 – J600)

Both positive and negative speaker outputs are floating and may not be connected to ground (e.g., through an oscilloscope).

Figure 2–4. J100 – J600 Pin Numbers (PCB Connector Top View)

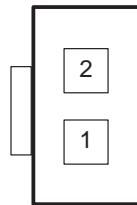


Table 2–5. J100– J600 Pin Description

Pin Number	Net-Name at Schematics	Description
1	OUT-1	Speaker negative output
2	OUT-2	Speaker positive output

## 2.4 Control Interface (J130)

This interface connects the TAS5066-5121K6EVM board to a TI input board.

*Table 2-6. J130 Pin Description*

Pin Number	Net-Name at Schematics	Description
1	GND	Ground
2	V-HBRIDGE-CTRL	Power supply output voltage control signal
3	GND	Ground
4	<u>RESET</u>	System reset (bi-directional). Activate <u>MUTE</u> before <u>RESET</u> for quiet reset.
5	<u>ERR-RCVY</u>	Error recovery or soft reset provides click and pop free reset, without resetting I <sup>2</sup> C volume register settings.
6	<u>MUTE</u>	Ramp volume from any setting to noiseless soft mute. Mute can also be activated by I <sup>2</sup> C.
7	<u>PDN</u>	Power down. TAS5066 enters the power down state when activated.
8, 9	RESERVED	–
10	SDA	I <sup>2</sup> C data clock
11	GND	Ground
12	SCL	I <sup>2</sup> C bit clock
13–16	RESERVED	–
17	GND	Ground
18, 19	RESERVED	–
20	<u>SD1</u>	Shutdown error reporting for all channels. Activated if TAS5121 has high current or high temperature. See Chapter 3, Protection.
21	RESERVED	–
22	<u>TEMP_WARNING</u>	Temperature warning. Activated with low signal if one or more TAS5121 has reached temperature warning level.
23, 24	RESERVED	–
25, 26	GND	Ground
27–30	RESERVED	–
31, 32	GND	Ground
33, 34	+5V	+5-Vdc power supply (output)

## 2.5 Digital Audio Interface (J140)

The digital audio interface contains digital audio signal data (I2S), clocks etc. Please see the TAS5066 data manual for signal timing and details not explained in this document.

Table 2-7. J140 Pin Description

Pin Number	Net-Name at Schematics	Description
1	GND	Ground
2	MCLK	Master clock input. Low jitter system clock for PWM generation and reclocking. Ground connection from source to TAS5066 must be a low impedance connection.
3	GND	Ground
4	SDIN1	I2S data 1, channels 1 and 2
5	SDIN2	I2S data 2, channels 3 and 4
6	SDIN3	I2S data 3, channels 5 and 6
7-9	-	Reserved
10	GND	Ground
11	SCLK	I2S bit clock
12	GND	Ground
13	LRCLK	I2S left-right clock
14	GND	Ground
15	-	Reserved
16	GND	Ground

Table 2-8. Clock Rates

Speed	TAS5066 System Control Register 0 (x02h)	Sample Frequency (F <sub>S</sub> )	LRCLK	SCLK (64xF <sub>S</sub> )	MCLK
Normal speed MCLK = 256xF <sub>S</sub>	D7 = 0 D6 = 0	32 kHz 44.1 kHz 48 kHz	32.0 kHz 44.1 kHz 48.0 kHz	2.0480 MHz 2.8224 MHz 3.0720 MHz	8.1920 MHz 11.2896 MHz 12.2880 MHz
Double speed MCLK = 256xF <sub>S</sub>	D7 = 0 D6 = 1	64 kHz 88 kHz 96 kHz	64.0 kHz 88.2 kHz 96.0 kHz	4.0960 MHz 5.6448 MHz 6.1440 MHz	16.3840 MHz 22.5792 MHz 24.5760 MHz
Quad speed MCLK = 128xF <sub>S</sub>	D7 = 1 D6 = 0	176 kHz 192 kHz	176.4 kHz 192.0 kHz	11.2896 MHz 12.2880 MHz	22.5790 MHz 24.5760 MHz

## 2.6 PWM Timing, Interchannel Delay Registers

For maximum performance, the PWM timing must be optimized for the specific configuration and PCB layout. The default values in TAS5066 is properly not optimal in many designs and therefore the interchannel delays must be programmed by I2C to the TAS5066 at startup and after every system reset.

*Table 2–9. Recommended Interchannel Delay Register Values (based on EVM designs)*

Register Description	Register Address	Value (hex)
Inter–Channel Delay Channel 1	0x0C	0x01
Inter–Channel Delay Channel 2	0x0D	0x49
Inter–Channel Delay Channel 3	0x0E	0x91
Inter–Channel Delay Channel 4	0x0F	0xD9
Inter–Channel Delay Channel 5	0x10	0x21
Inter–Channel Delay Channel 6	0x11	0x69

## Chapter 3

# Protection

This chapter describes the short circuit protection and fault reporting circuitry of the TAS5121 device.

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3.1 Short Circuit Protection and Fault Reporting Circuitry .....	3-2
3.2 Device Fault Reporting .....	3-2

### 3.1 Short Circuit Protection and Fault Reporting Circuitry

TAS5121 is a self-protecting device that provides device fault reporting (including high-temperature protection and short circuit protection). TAS5121 is configured in back-end auto-recovery mode and therefore resets automatically after all errors (M1, M2 and M3 is set low). This means that the device will re-start itself after a error occasion and report shortly through the SHUTDOWN error signals.

### 3.2 Device Fault Reporting

The OTW and SD outputs from TAS5121 indicate fault conditions. Please refer to the TAS5121 data manual for a description of these pins.

*Table 3-1. TAS5121 Error Signal Decoding*

<u>OTW</u>	<u>SD</u>	Device Condition
0	0	High temperature error and/or high current error
0	1	High temperature warning
1	0	Under voltage lockout or high current error
1	1	Normal operation, no errors/warnings

The temperature warning (OTW) signals at the TAS5066–5121K6EVM board are wired-OR to one temperature warning signal (TEMP\_WARNING – pin 22 in control interface connector (J130)). Shutdown signals (SD) are wired-OR into one shutdown signal (SHUTDOWN – pin 20 in control interface connector (J130)). The shutdown signals together with the temperature warning signal will give information on the chip state information as described in the previous table. Device fault reporting outputs are open-drain outputs.