

SIPMOS® Small-Signal-Transistor

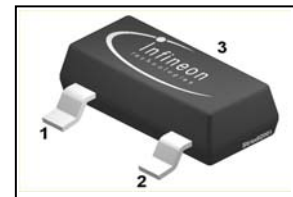
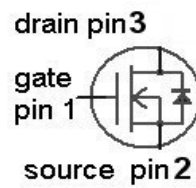
Feature

- n-channel
- enhancement mode
- Logic level
- dv/dt rated
- Pb-free lead plating, RoHS compliant

Product Summary

V_{DS}	600	V
$R_{DS(on),max}$	500	Ω
I_D	0.023	A

PG-SOT23



Type	Package	Ordering Code	Tape and Reel Information	Marking
BSS127	PG-SOT23	Q67045-A5014	E6327: 3000PCS/reel	SI

Maximum ratings, at $T_J=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_A=25\text{ °C}$	0.021	A
		$T_A=70\text{ °C}$	0.017	
Pulsed drain current	$I_{D,pulse}$	$T_A=25\text{ °C}$	0.09	
Reverse diode dv/dt	dv/dt	$I_D=0.09\text{ A}$, $V_{DS}=480\text{ V}$, $di/dt=200\text{ A}/\mu\text{s}$, $T_{j,max}=150\text{ °C}$	6	kV/ μs
Gate source voltage	V_{GS}		± 20	V
ESD sensitivity (HBM) as per MIL-STD 883			Class 1	
Power dissipation	P_{tot}	$T_A=25\text{ °C}$	0.50	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - minimal footprint	R_{thJA}		-	-	250	K/W
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Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=250\text{ }\mu\text{A}$	600	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=0\text{ V}, I_D=8\text{ }\mu\text{A}$	1.4	2.0	2.6	
Drain-source leakage current	$I_{D(off)}$	$V_{DS}=600\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	-	0.1	μA
		$V_{DS}=600\text{ V}, V_{GS}=0\text{ V}, T_j=150\text{ °C}$	-	-	10	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=0.016\text{ A}$	-	330	600	Ω
		$V_{GS}=10\text{ V}, I_D=0.016\text{ A}$	-	310	500	
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=0.01\text{ A}$	0.007	0.015	-	S

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	21	28	pF
Output capacitance	C_{oss}		-	2.4	3	
Reverse transfer capacitance	C_{rss}		-	1.0	1.5	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=300\text{ V},$ $V_{GS}=10\text{ V}, I_D=0.01\text{ A},$ $R_G=6\ \Omega$	-	6.1	19.0	ns
Rise time	t_r		-	9.7	14.5	
Turn-off delay time	$t_{d(off)}$		-	14	21	
Fall time	t_f		-	115	170	

Gate Charge Characteristics

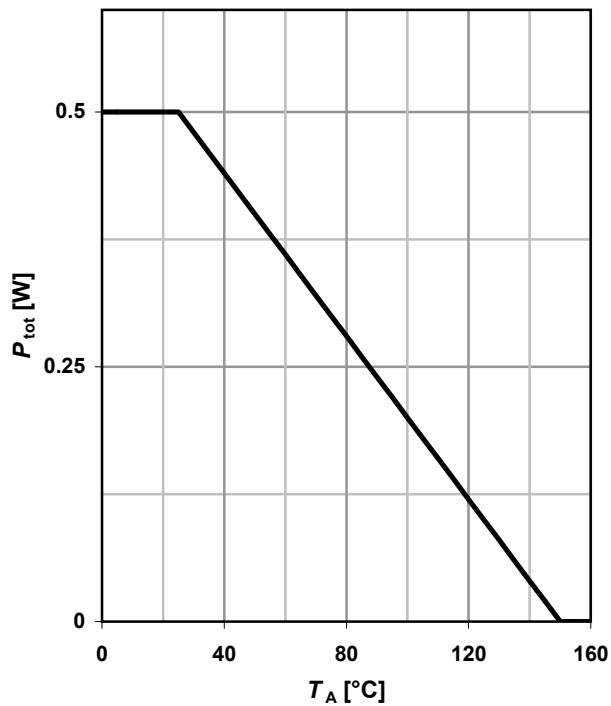
Gate to source charge	Q_{gs}	$V_{DD}=400\text{ V},$ $I_D=0.01\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	0.05	0.08	nC
Gate to drain charge	Q_{gd}		-	1.2	1.8	
Gate charge total	Q_g		-	1.4	2.1	
Gate plateau voltage	$V_{plateau}$		-	3.5	-	V

Reverse Diode

Diode continuous forward current	I_S	$T_A=25\text{ °C}$	-	-	0.016	A
Diode pulse current	$I_{S,pulse}$		-	-	0.09	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=0.016\text{ A},$ $T_J=25\text{ °C}$	-	0.82	1.2	V
Reverse recovery time	t_{rr}	$V_R=300\text{ V},$ $I_F=0.016\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	160	240	ns
Reverse recovery charge	Q_{rr}		-	13.2	19.8	nC

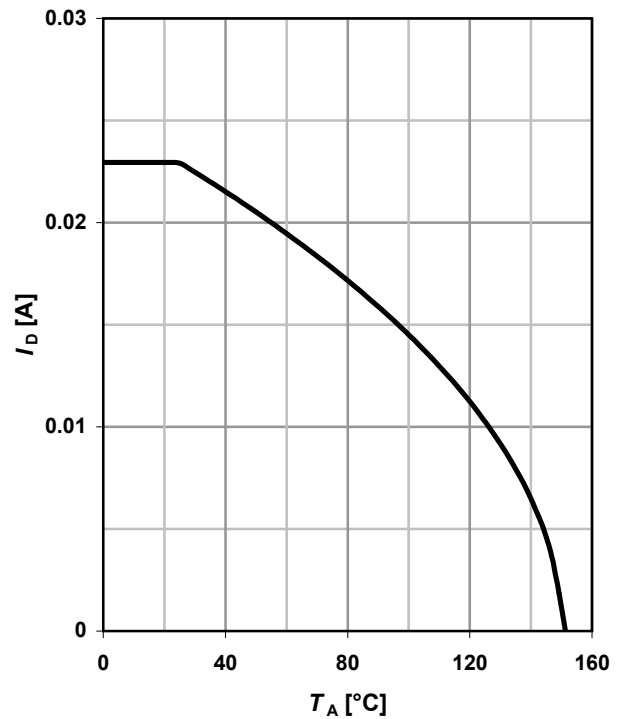
1 Power dissipation

$$P_{\text{tot}} = f(T_A)$$



2 Drain current

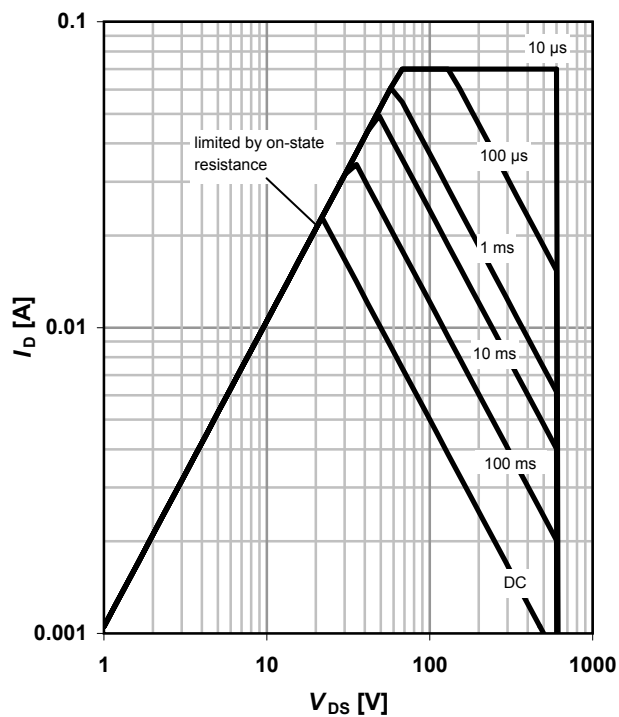
$$I_D = f(T_A); V_{GS} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{DS}); T_A = 25 \text{ °C}; D = 0$$

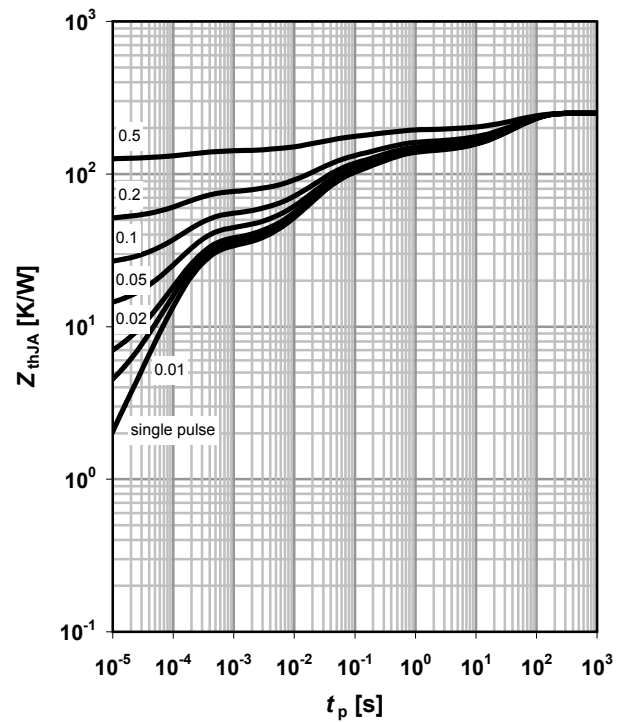
parameter: t_p



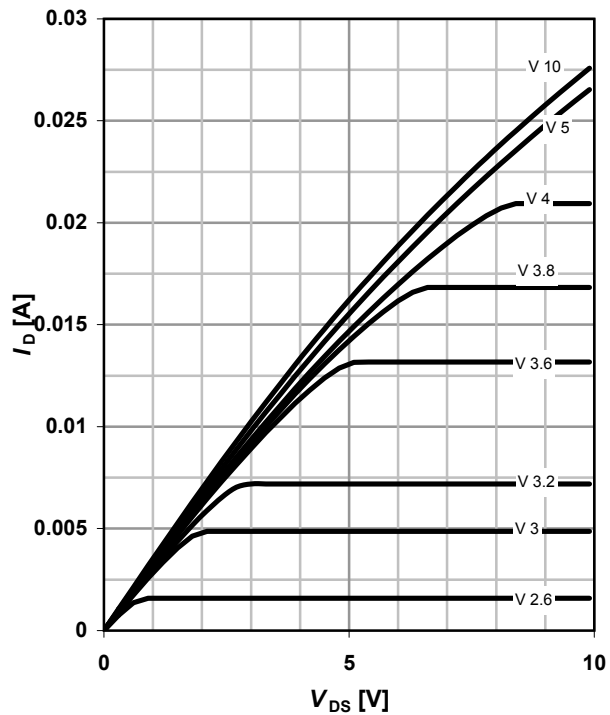
4 Max. transient thermal impedance

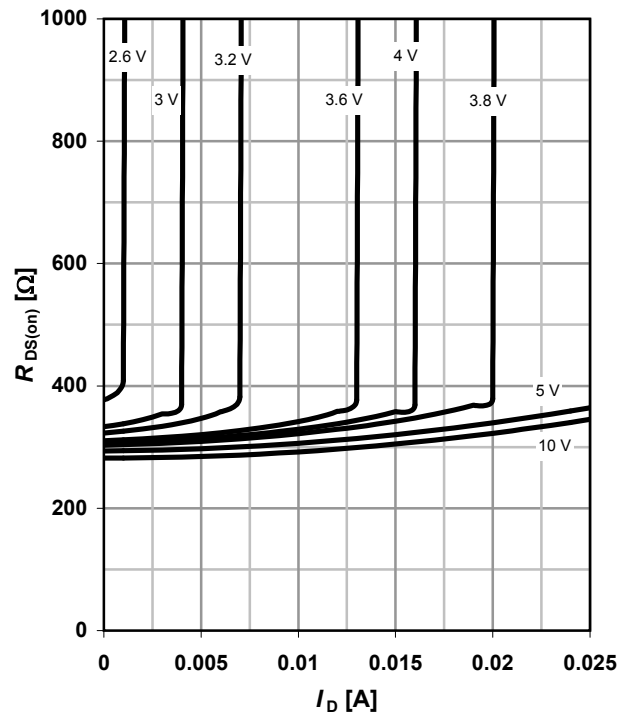
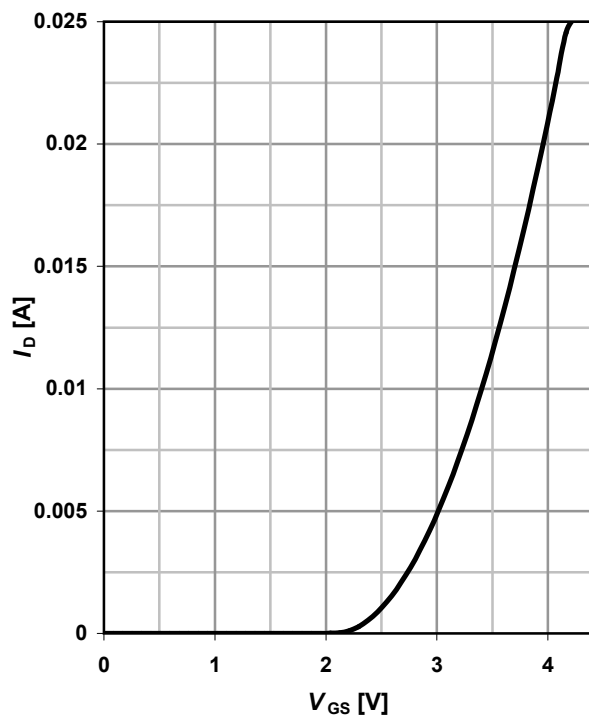
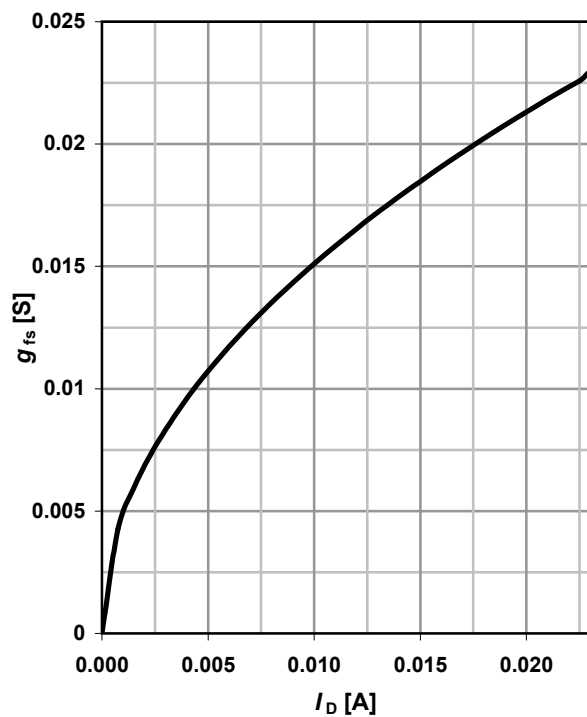
$$Z_{thJA} = f(t_p)$$

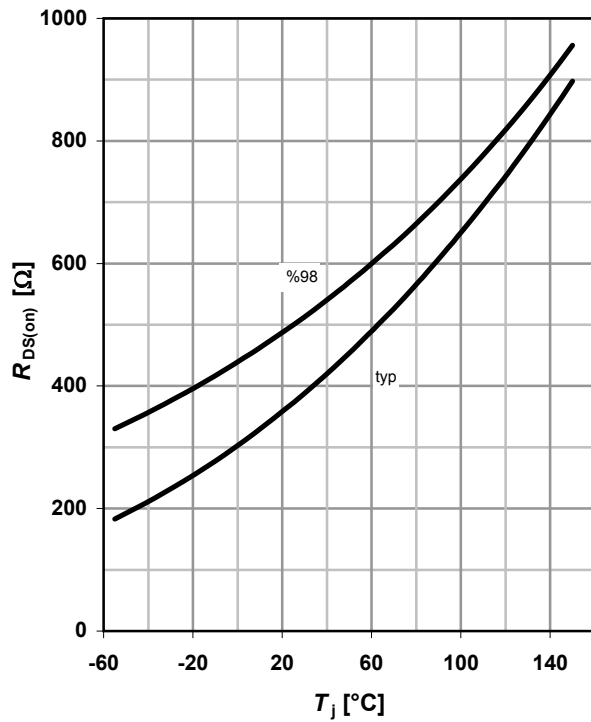
parameter: $D = t_p / T$

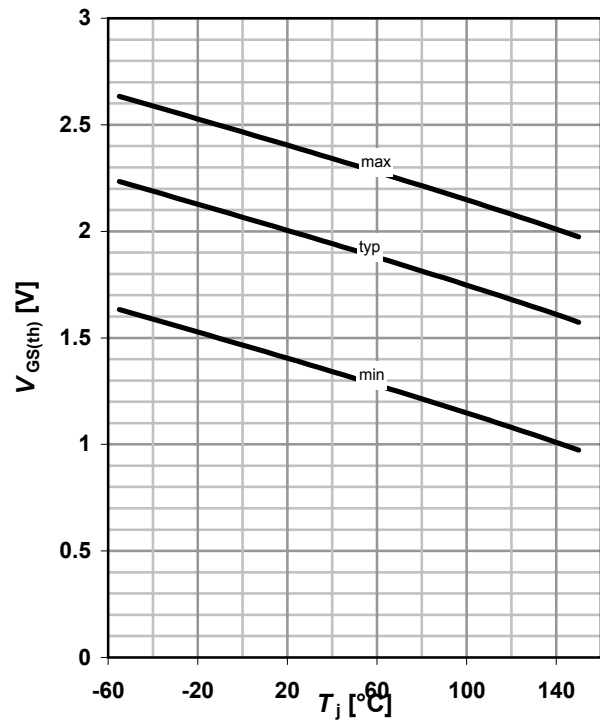
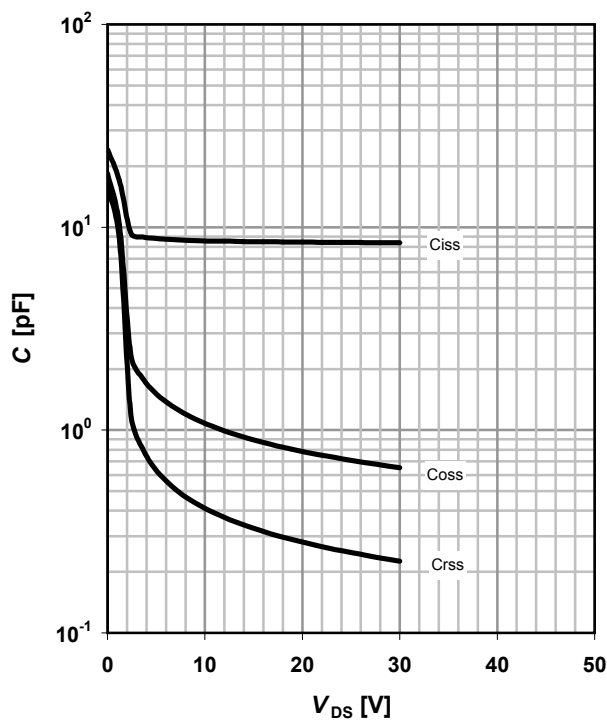


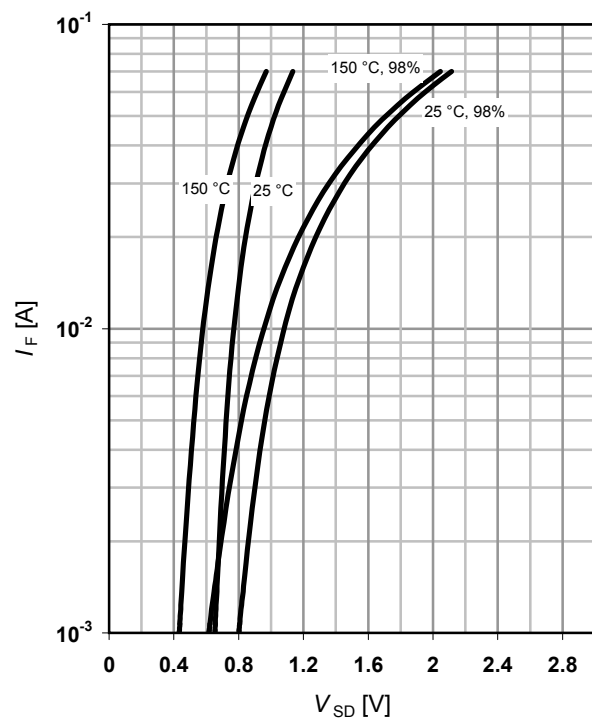
5 Typ. output characteristics
 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}

6 Typ. drain-source on resistance
 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

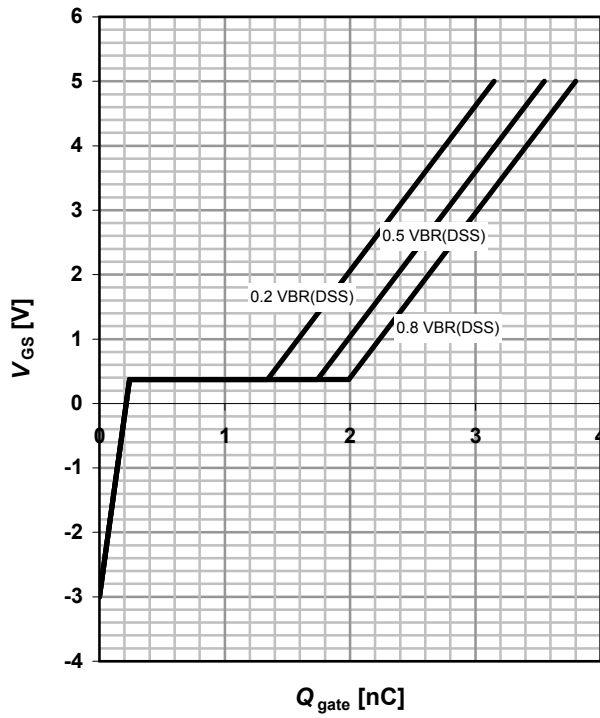
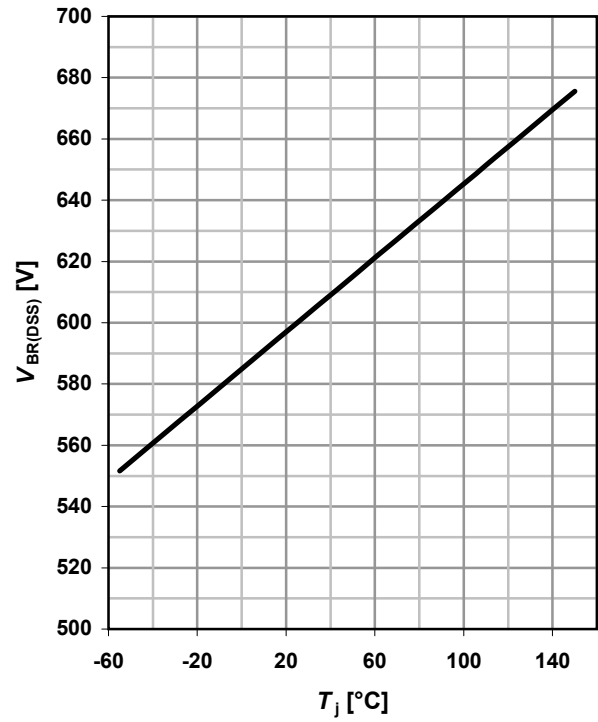
parameter: V_{GS}

7 Typ. transfer characteristics
 $I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

8 Typ. forward transconductance
 $g_{fs} = f(I_D); T_j = 25^\circ\text{C}$


9 Drain-source on-state resistance
 $R_{DS(on)} = f(T_j); I_D = 0.1 \text{ A}; V_{GS} = 10 \text{ V}$

10 Typ. gate threshold voltage
 $V_{GS(th)} = f(T_j); V_{DS} = V_{GS}; I_D = 8 \mu\text{A}$

 parameter: I_D

11 Typ. capacitances
 $C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25^\circ\text{C}$

12 Forward characteristics of reverse diode
 $I_F = f(V_{SD})$

 parameter: T_j


13 Typ. gate charge
 $V_{GS}=f(Q_{gate}); I_D=0.01\text{ A pulsed}$

parameter: V_{DD}

14 Drain-source breakdown voltage
 $V_{BR(DSS)}=f(T_j); I_D=250\text{ }\mu\text{A}$


Technical drawing of a rectangular profile with dimensions and tolerances. The drawing includes a top view and a side view.

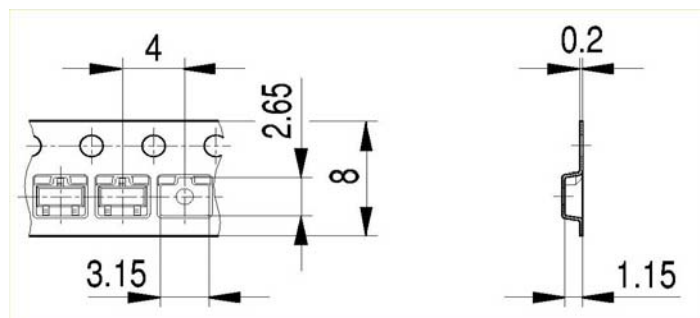
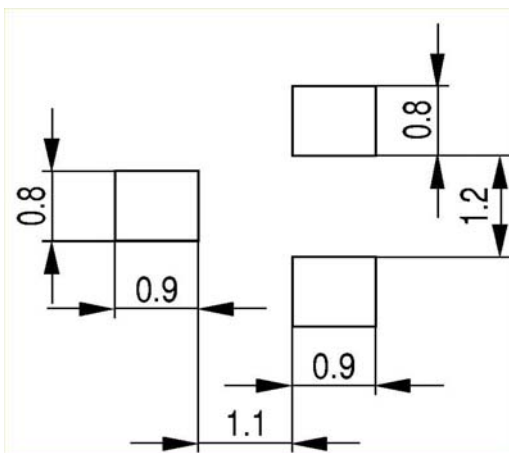
Top View Dimensions:

- Overall width: 2.9 ± 0.1
- Overall height: $0.4^{+0.1}_{-0.05}$
- Internal width: 1.9
- Internal height: 0.95
- Feature 1: 0.25 (M)
- Feature 2: 0.25 (M)
- Feature 3: 0.25 (M)

Side View Dimensions:

- Overall height: 2.6 MAX.
- Internal height: 1.3 ± 0.1
- Feature 1: 0.20 (M)
- Feature 2: 0.20 (M)
- Feature 3: 0.20 (M)
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Packaging:



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