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DDC on Board®

BU-65529 Datasheet

MIL-STD-1553 BC/RT/MT IMB PC/AT® INTERFACE UNIT

FEATURES

- 1/2 Size IBM PC/AT ISA Compatible 16 Bit Interface Card
- 1553B Notice 2 Dual Redundant BC/RT/MT
- Built-In-Test (BIT)
- 8K x 16 Shared RAM
- Software Programmable RT Address, Data Block Allocations, Interrupts, and Illegalization
- Selectable Interrupt Level
- Low Power
- Background Mode Operation
- Free Library Software Available

DESCRIPTION

The BU-65529 provides full, intelligent interfacing between a dual redundant MIL-STD-1553B Data Bus and the IBM PC/AT Bus. Software controls the BU-65529's operation as either a 1553 Bus Controller (BC), Remote Terminal (RT), or Bus Monitor (MT).

The BU-65529 is packaged on a half size IBM PC/AT printed circuit card. The board features DDC's BU-61559D2 Advanced Integrated Mux Hybrid with Enhanced RT Features (AIM-HY'er). As such, it includes dual transceiver and encoder/decoder, complete 1553B protocol, 8K words of shared RAM, and memory management logic for all three modes.

The board includes a set of ten on-board registers. These registers allow selection of the 1553 operating modes and control of memory management, base memory address, 1553 RT address, and interrupt control.

Background Mode Operation prevents inadvertent access to the card during power-on self-test. On-board Interrupt Mask and Interrupt Status Registers support flexible operation for both interrupt and polling applications.

The memory management scheme for RT mode provides an option for separation of broadcast data plus a circular buffer option for individual RT subaddresses to offload the PC host CPU.

Additional features include a wrap-around Built-In-Test, jumper programmable interrupt level, software programmable RT address selection and a free "C" software subroutine library, the BUS-69054. The BU-65529 supports all dual redundant mode codes and message formats. Its full compliance with MIL-STD-1553B makes it an excellent choice for real-time simulation, test, and system integration applications.

DDC® Data Device Corporation

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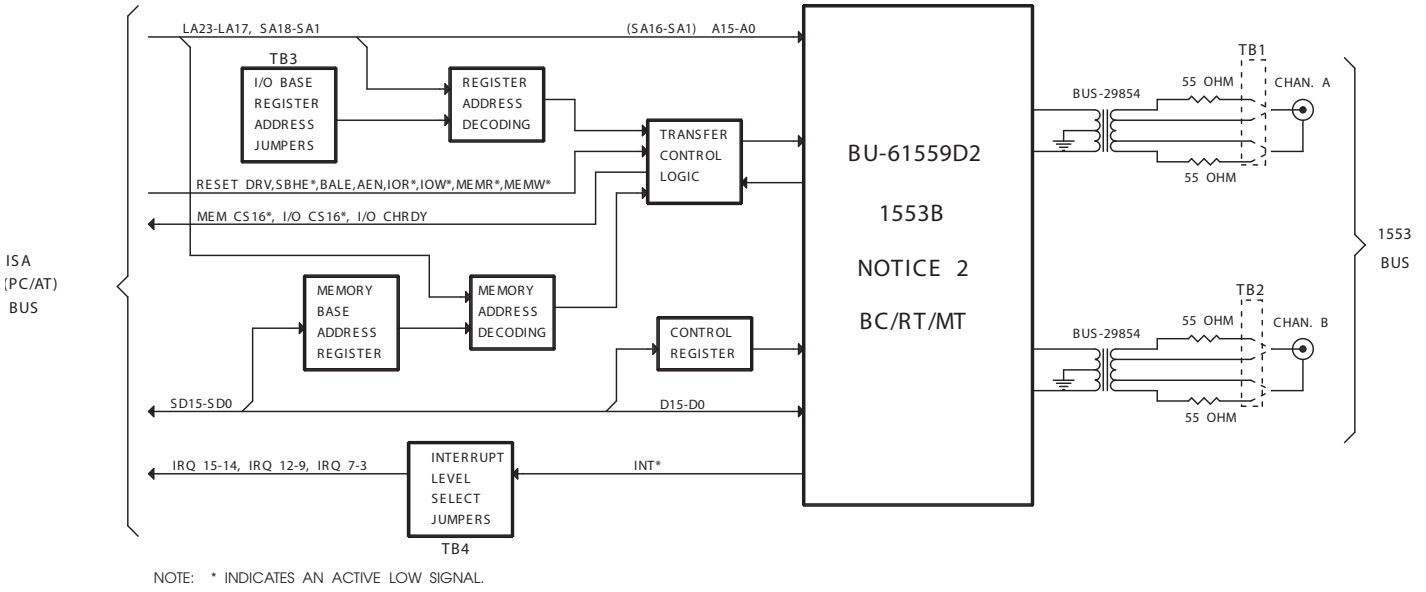

FIGURE 1. BU-65529 BLOCK DIAGRAM

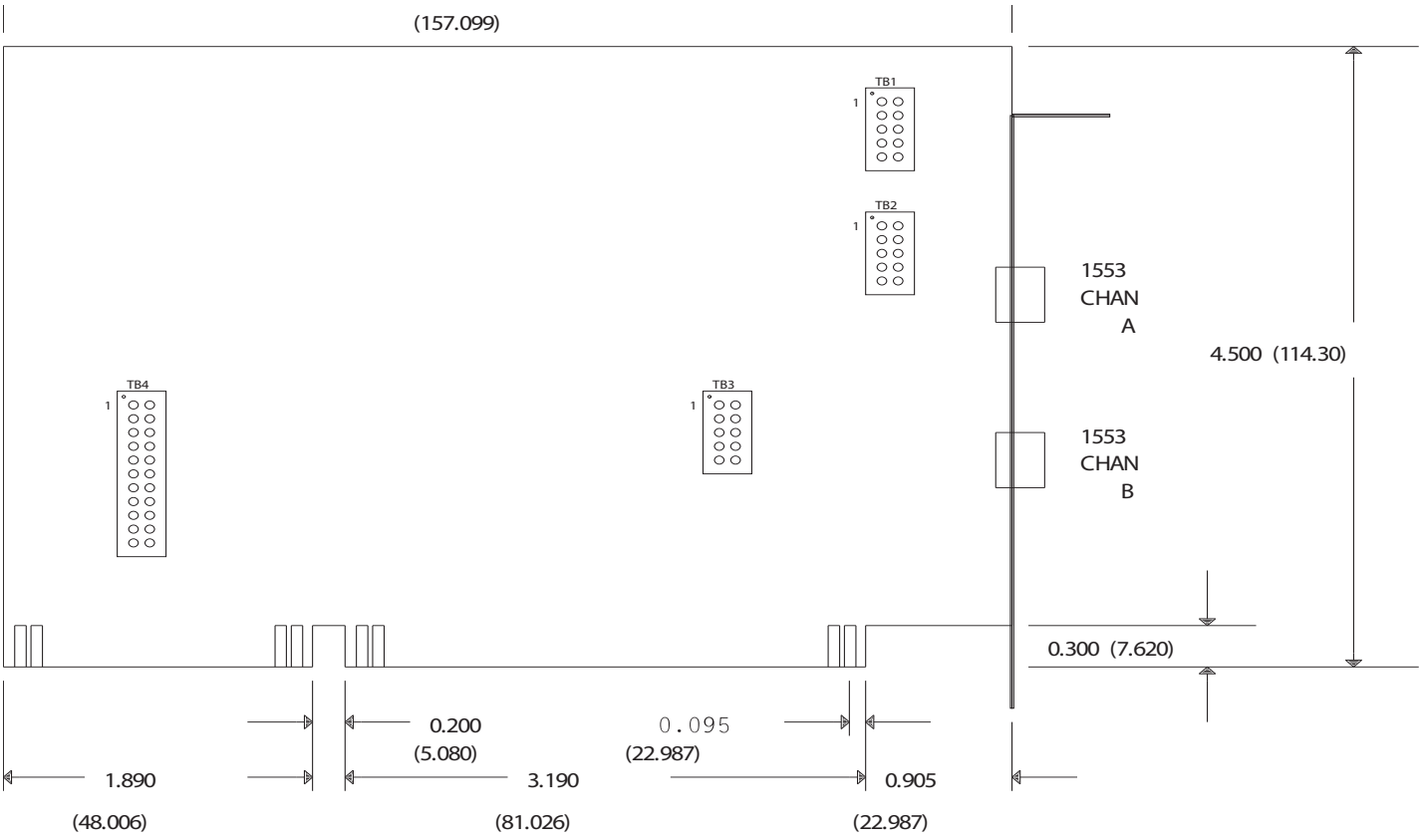

FIGURE 2. MECHANICAL OUTLINE (WITH JUMPER LOCATIONS)

JUMPER CONFIGURATION

TB1: 1553 CHANNEL A. Connection selected by jumpers at TB1
TB2: 1553 CHANNEL B.

PIN NUMBER	COUPLING TYPE
1	DIRECT COUPLED
2	TRANSFORMER COUPLED*
3	CENTER TAP*
4	TRANSFORMER COUPLED
5	DIRECT COUPLED
	Note: * Installed by factory.

TB3: I/O BASE ADDRESS. The BUS-65529 is I/O mapped to the CPU. The user must know the I/O map of the PC that they are using to find an available address. (Adding a jumper sets the selected address bit to a logic "0".)

PIN NUMBER	ADDRESS
1	SA9
2	SA8
3	SA7*
4	SA6
5	SA5
	Note: * Installed by factory (DEFAULT I/O ADDRESS = 0360).

TB4: INTERRUPT LEVEL SELECT. The BUS-65529 allows the user to select the Interrupt Request output from among IRQ levels 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, or 15. To select the desired interrupt request line, connect the pin corre sponding to the desired interrupt level.

PIN NUMBER	HARDWARE INTERRUPT LEVEL
1	IRQ 9 Highest Priority
2	IRQ 10
3	IRQ 11
4	IRQ 12
5	IRQ 14
6	IRQ 15
7	IRQ 3
8	IRQ 4
9	IRQ 5
10	IRQ 6
11	IRQ 7 Lowest Priority

ORDERING INFORMATION

BU-65529

Software:

BUS-69054 Free "C" Library (included)

Notes:
1. The above products contain tin-lead solder.

The information in this data sheet is believed to be accurate; however, no responsibility is assumed by Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith.
Specifications are subject to change without notice.

Please visit our Web site at **www.ddc-web.com** for the latest information.

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