

74F126

Quad buffers; 3-State

Rev. 4 — 23 January 2013

Product data sheet

1. General description

The 74F126 provides four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (nOE). A LOW at nOE causes the outputs to assume a high-impedance OFF-state.

2. Features and benefits

- High impedance NPN base inputs for reduced loading (20 μ A in HIGH and LOW states)

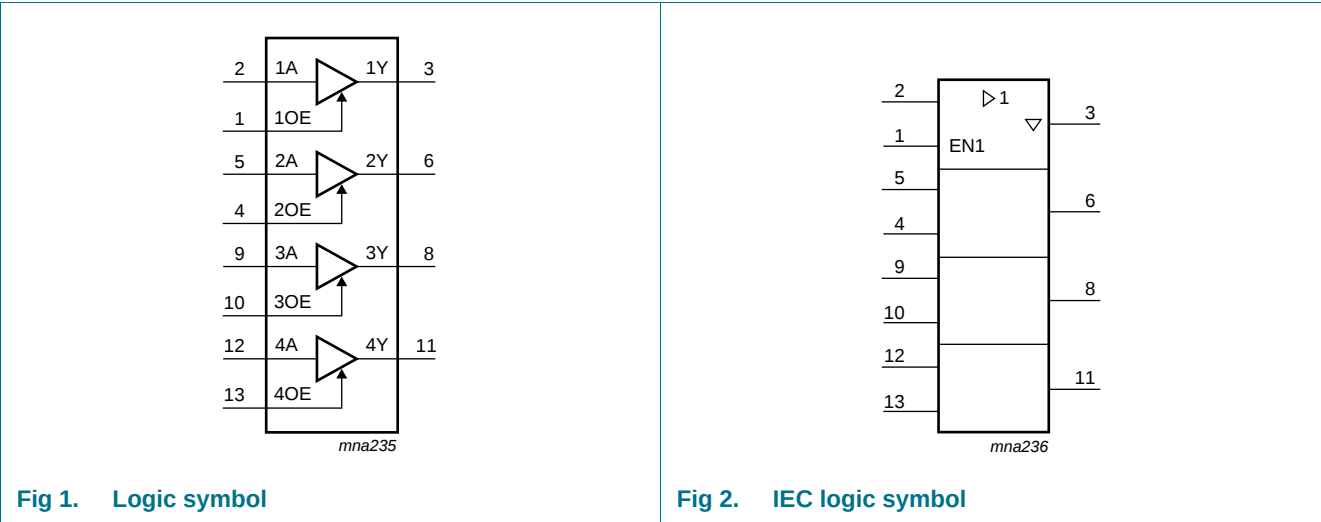
3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
N74F126N	0 °C to +70 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
N74F126D	0 °C to +70 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

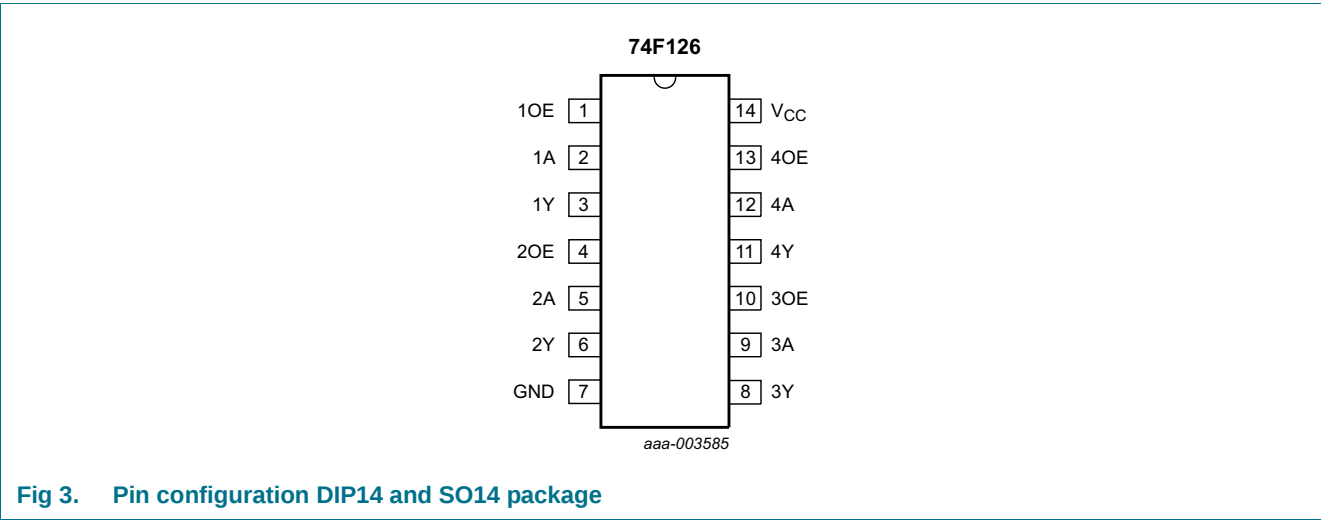


4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description	Unit load HIGH/LOW	Load value ^[1] HIGH/LOW
1OE to 4OE	1, 4, 10, 13	output enable input (active HIGH)	1.0/0.033	20 μ A/20 μ A
1A to 4A	2, 5, 9, 12	data input	1.0/0.033	20 μ A/20 μ A
1Y to 4Y	3, 6, 8, 11	data output	750/106.7	15 mA/64 mA
GND	7	ground (0 V)	-	-
V _{CC}	14	supply voltage	-	-

[1] One FAST Unit Load (UL) is defined as 20 μ A in HIGH state, 0.6 μ A in LOW state.

6. Functional description

Table 3. Function table^[1]

Control	Input	Output
nOE	nA	nY
H	L	L
	H	H
L	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
V _I	input voltage		^[1] -0.5	+7.0	V
V _O	output voltage	output in HIGH-state	^[1] -0.5	V _{CC}	V
I _{IK}	input clamping current	V _I < 0 V	-30	+5	mA
I _O	output current	output in LOW-state	-	128	mA
T _{amb}	ambient temperature	in free air	^[2] 0	70	°C
T _{stg}	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		4.5	5.0	5.5	V
V _{IH}	HIGH-level input voltage		2.0	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.8	V
I _{IK}	input clamping current		-18	-	-	mA
I _{OH}	HIGH-level output current		-15	-	-	mA
I _{OL}	LOW-level output current		-	-	64	mA
T _{amb}	ambient temperature		0		70	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			0 °C to +70 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IK}	input clamping voltage	V _{CC} = 4.5 V; I _{IK} = -18 mA	-1.2	-0.73	-	-1.2	-	V
V _{OH}	HIGH-level output voltage	V _{CC} = 4.5 V; V _{IL} = 0.8 V; V _{IH} = 2.0 V I _{OH} = -3 mA						
		V _{CC} = ±10 %	-	-	-	2.4	-	V
		V _{CC} = ±5 %	-	3.3	-	2.7	-	V
		I _{OH} = -15 mA						
		V _{CC} = ±10 %	-	-	-	2.0	-	V
V _{OL}	LOW-level output voltage	V _{CC} = 4.5 V; V _{IL} = 0.8 V; V _{IH} = 2.0 V I _{OL} = 64 mA						
		V _{CC} = ±10 %	-	-	-	-	0.55	V
		V _{CC} = ±5 %	-	0.42	-	-	0.55	V
I _I	input leakage current	V _{CC} = 0 V; V _I = 7.0 V	-	-	-	-	100	μA
I _{IH}	HIGH-level input current	V _{CC} = 5.5 V; V _I = 2.7 V	-	-	-	-	20	μA
I _{IL}	LOW-level input current	V _{CC} = 5.5 V; V _I = 0.5 V	-	-	-	-20	-	μA
I _{OZ}	OFF-state output current	V _{CC} = 5.5 V						
		V _O = 2.7 V	-	-	-	-	50	μA
		V _O = 0.5 V	-	-	-	-50	-	μA
I _O	output current	V _{CC} = 5.5 V ^[2]	-	-	-	-225	-100	mA
I _{CC}	supply current	V _{CC} = 5.5 V; V _I = GND or V _{CC}						
		outputs HIGH-state	-	20	-	-	30	mA
		outputs LOW-state	-	32	-	-	48	mA
		outputs OFF-state	-	26	-	-	39	mA

[1] All typical values are measured at V_{CC} = 5 V.

[2] No more than one output should be tested at a time, and the duration of the test should not exceed one second.

10. Dynamic characteristics

Table 7. Dynamic characteristics

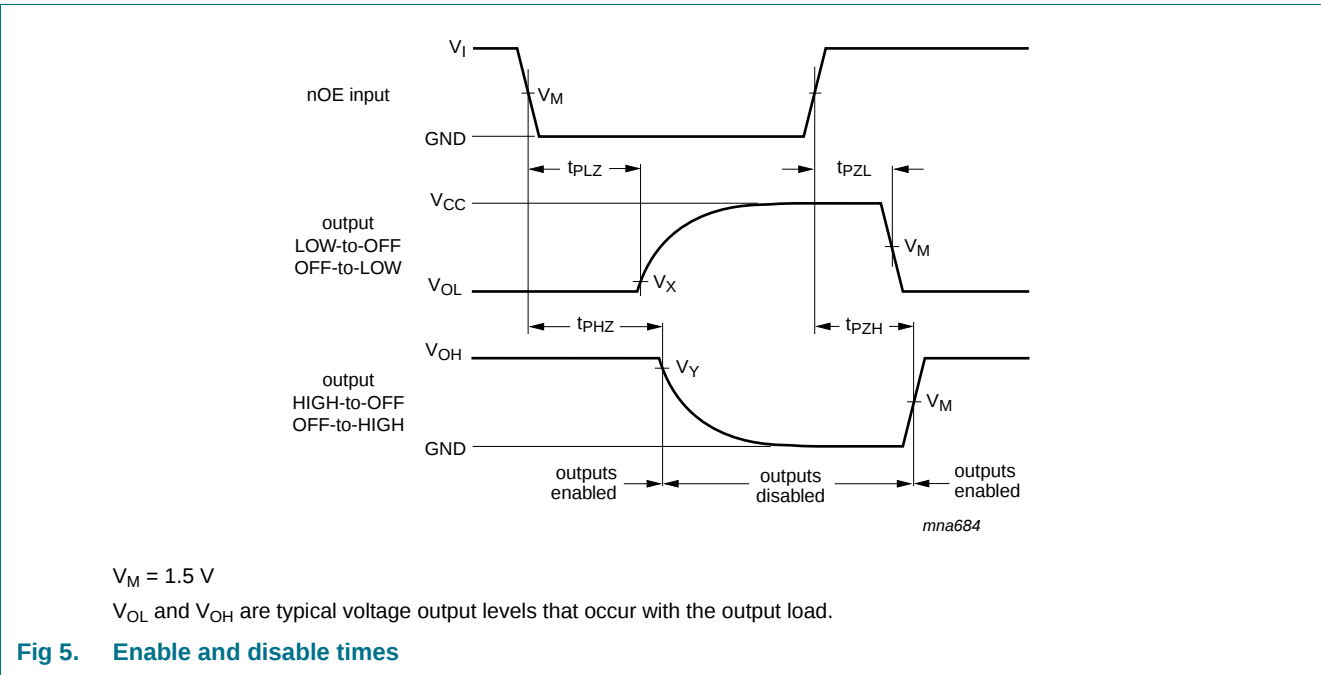
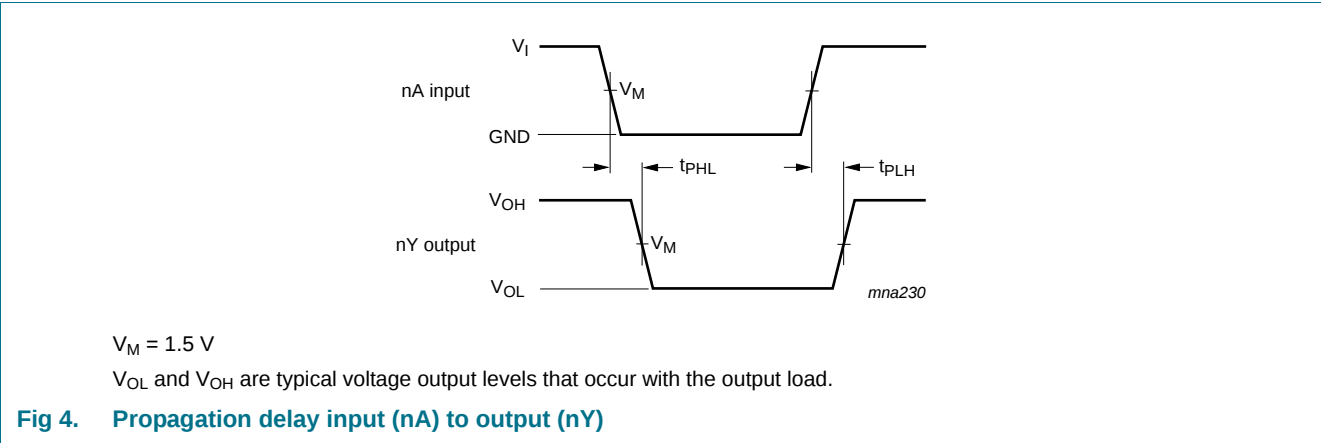
GND = 0 V. Test circuit is shown in [Figure 6](#).

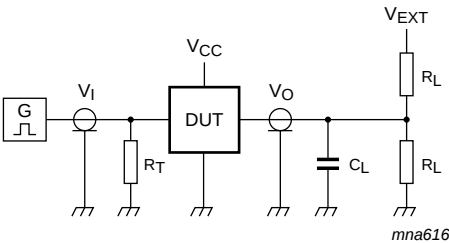
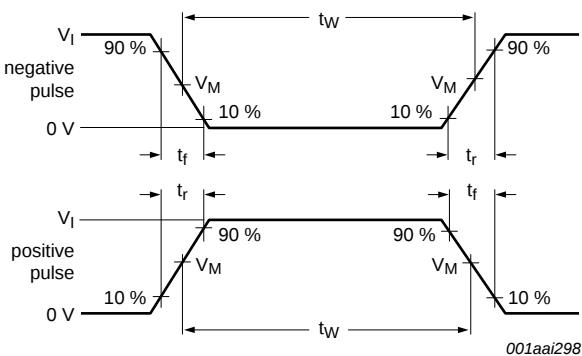
Symbol	Parameter	Conditions	25 °C; V _{CC} = 5.0 V			0 °C to +70 °C; V _{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t _{PLH}	LOW to HIGH propagation delay	nA to nY; see Figure 4	2.0	4.0	6.5	2.0	7.0	ns
t _{PHL}	HIGH to LOW propagation delay	nA to nY; see Figure 4	3.0	5.5	8.0	3.0	8.5	ns
t _{PZH}	OFF-state to HIGH propagation delay	nOE to nY; see Figure 5	4.0	6.0	7.5	3.5	8.5	ns

Table 7. Dynamic characteristics ...continued
GND = 0 V. Test circuit is shown in Figure 6.

Symbol	Parameter	Conditions	25 °C; V _{CC} = 5.0 V			0 °C to +70 °C; V _{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t _{PZL}	OFF-state to LOW propagation delay	nOE to nY; see Figure 5	4.0	6.0	8.0	3.5	8.5	ns
t _{PHZ}	HIGH to OFF-state propagation delay	nOE to nY; see Figure 5	2.0	4.5	6.5	2.0	7.5	ns
t _{PLZ}	LOW to OFF-state propagation delay	nOE to nY; see Figure 5	3.0	5.5	7.5	3.0	8.0	ns

11. Waveforms





a. Input pulse definition

Test data is given in [Table 8](#).

Test circuit definitions:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

b. Test circuit

Fig 6. Load circuitry for switching times

Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

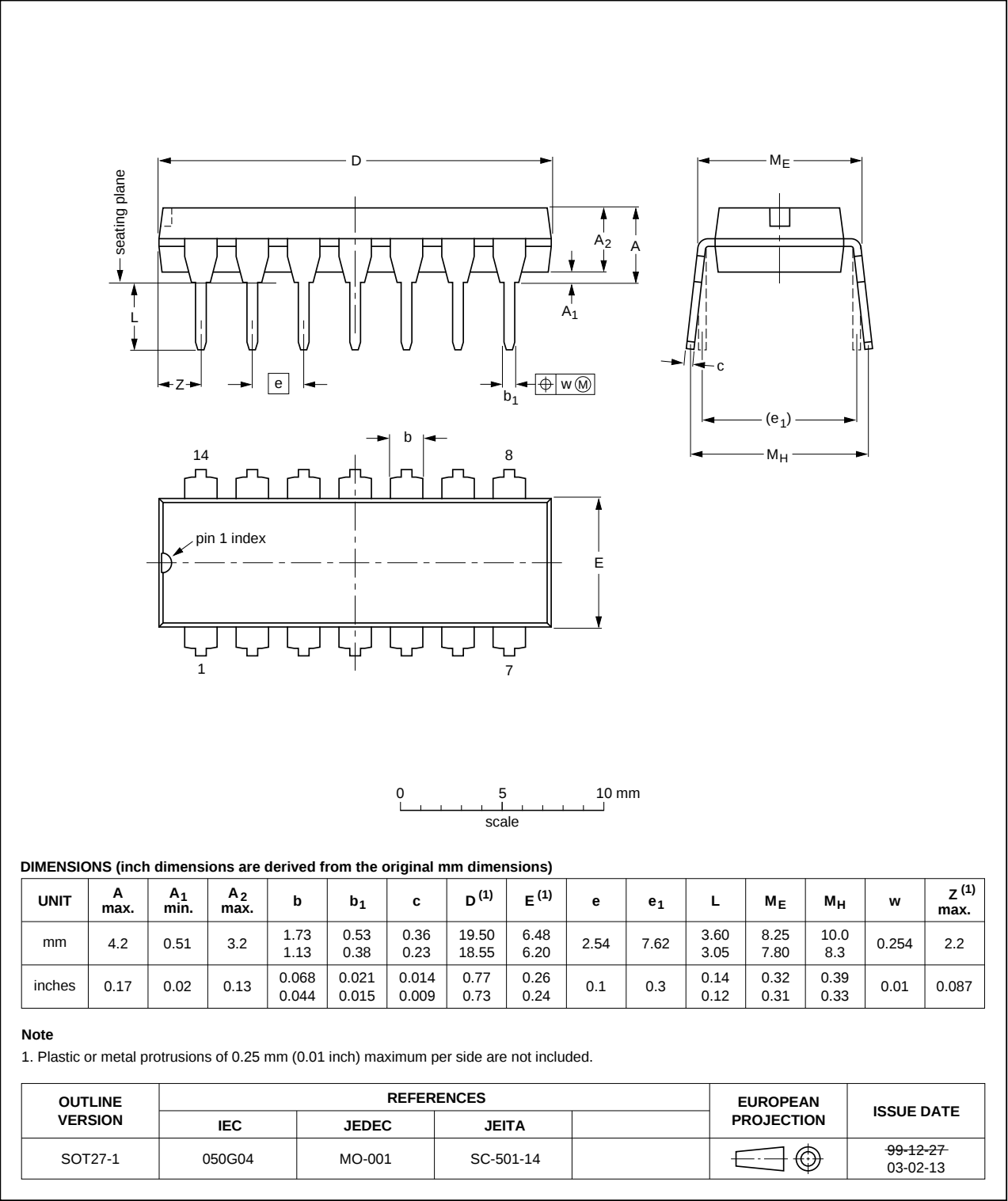


Fig 7. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

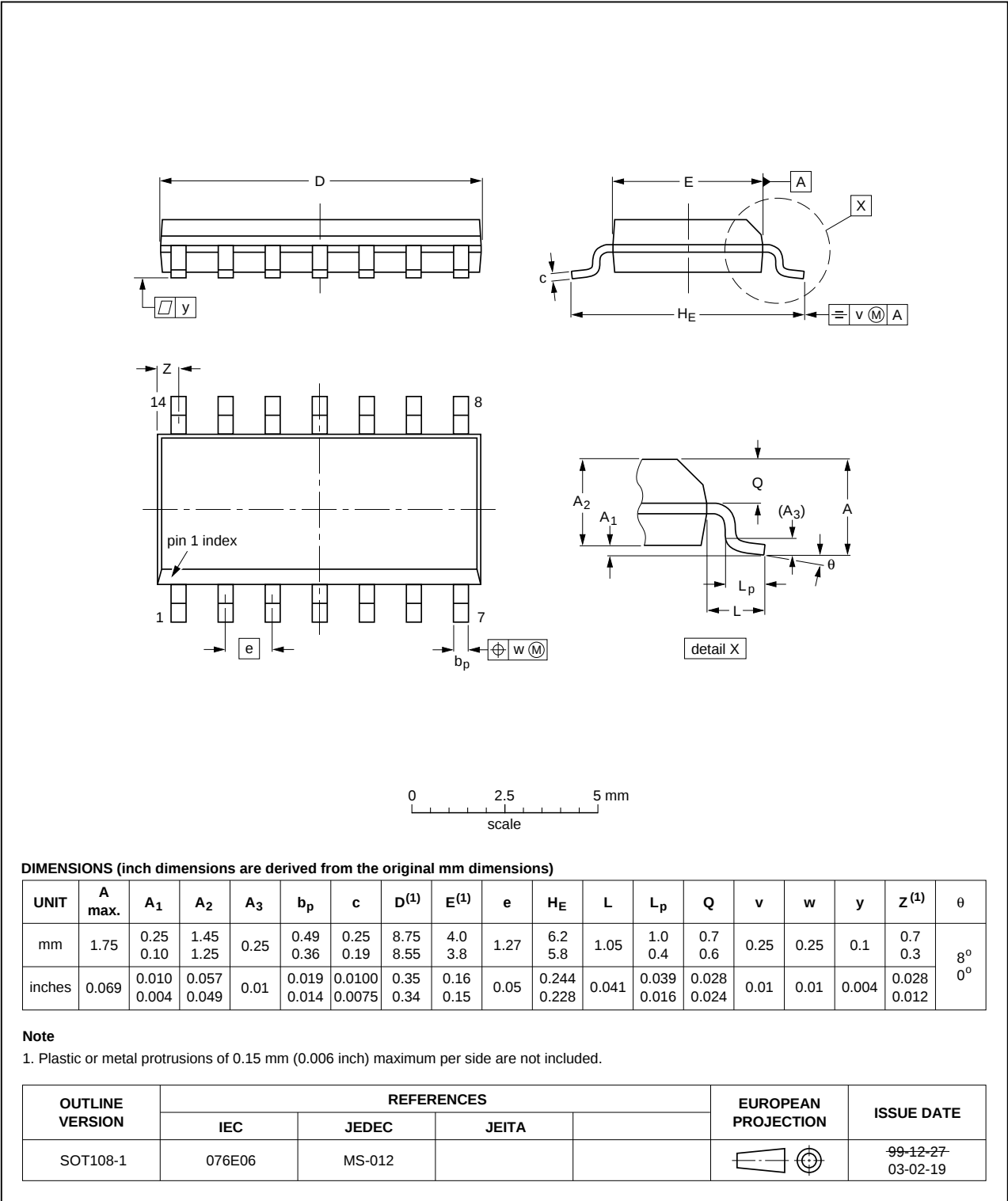


Fig 8. Package outline SOT108-1 (SO14)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
LSTTL	Low-power Schottky Transistor-Transistor Logic
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
CDM	Charge-Device Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74F126 v.4	20130123	Product data sheet	-	74F126 v.3
Modifications:	• Features and benefits: Changed mA into μA (errata).			
74F126 v.3	20130118	Product data sheet	-	74F126 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74F126 v.2	19890328	Product data sheet	-	74F126 v.1

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Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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