Low Capacitance, 4- and 8-Channel ±15 V/12 V *i*CMOS™ Multiplexers

Preliminary Technical Data

ADG1208/ADG1209

FEATURES

2 pF off capacitance
1 pC charge injection
33 V supply range
120 Ω on resistance
Fully specified at ±15 V/12 V
3 V logic compatible inputs
Rail-to-rail operation
Break-before-make switching action
16-lead TSSOP and 4 mm × 4 mm LFCSP packages
Typical power consumption (< 0.03 µW)

APPLICATIONS

Audio and video routing
Automatic test equipment
Data acquisition systems
Battery-powered systems
Sample-and-hold systems
Communication systems

FUNCTIONAL BLOCK DIAGRAMS

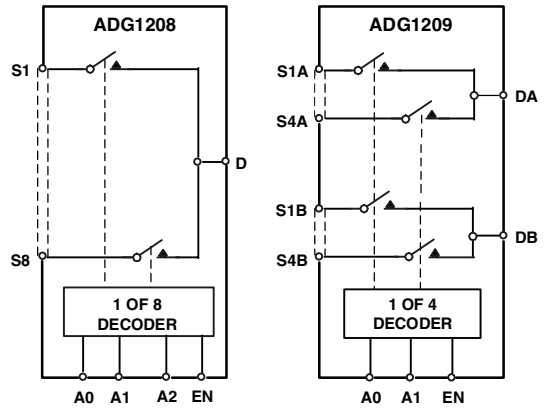

Figure 1.

GENERAL DESCRIPTION

The ADG1208 and ADG1209 are monolithic *i*CMOS analog multiplexers comprising eight single channels and four differential channels, respectively. The ADG1208 switches one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1, and A2. The ADG1209 switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched OFF.

The *i*CMOS (industrial-CMOS) modular manufacturing process combines high-voltage CMOS (complementary metal-oxide semiconductor) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33-V operation in a footprint that no other generation of high-voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages, while providing increased performance, dramatically lower power consumption, and reduced package size.

The ultralow capacitance and charge injection of these multiplexers make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Fast switching speed coupled with high signal bandwidth make the parts suitable for video signal switching. *i*CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery powered instruments.

PRODUCT HIGHLIGHTS

1. 2 pF off capacitance (±15 V supply).
2. 1 pC charge injection.
3. 3 V logic compatible digital input V_{IH} = 2.0 V, V_{IL} = 0.8 V.
4. 16-lead TSSOP and 4 mm ×4 mm LFCSP package.

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REVISION HISTORY

SPECIFICATIONS

DUAL SUPPLY[1]

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	+25°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
R_{ON}	140		Ω typ	V_D = ±10 V, I_S = −10 mA
	160		Ω max	
R_{ON} Flatness	55		Ω typ	V_D = +10 V, −10 V
			Ω max	
ΔR_{ON}	5		Ω typ	V_D = +10 V, −10 V
			Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_D = ±10 V, V_S = −10 V; Test Circuit 2
	±0.5	±5	nA max	±0.5
Drain OFF Leakage I_D (OFF)				V_D = ±10 V; V_S = ±10 V;
ADG1208	±1	±10	nA max	Test Circuit 3
ADG1209	±1	±5	nA max	
Channel ON Leakage I_D, I_S (ON)				V_S = V_D = ±10 V;
ADG1208	±1	±10	nA max	Test Circuit 4
ADG1209	±1	±5	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	±0.005		μA max	V_{IN}= V_{INL} or V_{INH}
		±0.5	μA max	
C_{IN}, Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS[2]				
$t_{TRANSITION}$	80	120	ns typ	R_L = 300 Ω, C_L = 35 pF;
		250	ns max	V_{S1} = ±10 V, V_{S8} = ±10 V; Test Circuit 5
T_{BBM}	10	10	ns typ	R_L = 300 Ω, C_L = 35 pF;
		1	ns min	V_S = 10 V; Test Circuit 6
t_{ON}(EN)	85	125	ns typ	R_L = 300 Ω C_L = 35 pF;
	150	225	ns max	V_S = 5 V; Test Circuit 7
t_{OFF}(EN)	40	65	ns typ	R_L = 300 Ω, C_L = 35 pF;
		150	ns max	V_S = 5 V; Test Circuit 7
Charge Injection	1		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 8
OFF Isolation	75		dB typ	R_L = 1 kΩ, f = 100 kHz; V_{EN} = 0 V; Test Circuit 9
Channel-to-Channel Crosstalk	85		dB typ	RL = 1 kΩ, f = 100 kHz; Test Circuit 10
Total Harmonic Distortion, THD + N	0.002		% typ	R_L = 600 Ω, 5 V rms; f=20 Hz to 20 kHz
−3 dB Bandwidth	700		MHz typ	R_L = 300 Ω, C_L = 5 pF; Test Circuit 10
				Test Circuit 10

Parameter	+25°C	−40°C to +125°C	Unit	Test Conditions/Comments
C_S (OFF)	1.5		pF typ	
C_D (OFF)				
ADG1208	11		pF typ	
ADG1209	6		pF typ	
C_D, C_S(ON)				
ADG1208	15		pF typ	
ADG1209	8		pF typ	
POWER REQUIREMENTS				V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.001		µA typ	Digital inputs= 0 V or V_{DD}
		5	µA max	
I_{DD}	150		µA typ	Digital inputs= 5 V
		300	µA max	
I_{SS}	0.001		µA typ	Digital inputs= 0 V or V_{DD}
		5	µA max	
I_{GND}	0.001		µA typ	Digital inputs= 0 V or V_{DD}
		5	µA max	
I_{GND}	150		µA typ	Digital inputs= 5 V
		300	µA max	

[1] Temperature ranges are as follows: B Version: −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

SINGLE SUPPLY[1]

V_{DD} = 12 V V ± 10%,, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
R_{ON}	300		Ω typ	V_D = 3 V, 10 V, I_S = −1 mA
			Ω max	
R_{ON} Flatness	150		Ω typ	V_D = 3 V, 10 V, I_S = −1 mA
			Ω max	
ΔR_{ON}	5		Ω typ	V_D = 3 V, 10 V, I_S = −1 mA
			Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_D = ±10 V, V_S = −10 V;
				Test Circuit 2
	±0.5	±5	nA max	±0.5
Drain OFF Leakage I_D (OFF)				V_D = ±10 V; V_S = ±10 V;
ADG1208	±1	±10	nA max	Test Circuit 3
ADG1209	±1	±5	nA max	
Channel ON Leakage I_D, I_S (ON)				V_S = V_D = 8 V/0 V;
ADG1208	±1	±10	nA max	Test Circuit 4
ADG1209	±1	±5	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				

Parameter	+25°C	−40°C to +125°C	Unit	Test Conditions/Comments
I_{INL} or I_{INH}		±10	µA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	8		pF typ	f = 1 MHz
DYNAMIC CHARACTERISTICS[2]				
$t_{TRANSITION}$	130		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = 8 V/0 V, V_{S8} = 0 V/8 V; Test Circuit 5
T_{BBM}	10		ns typ	R_L = 300 Ω, C_L = 35 pF;
		1	ns min	V_S = 5 V; Test Circuit 6
t_{ON} (EN)	140		ns typ	R_L = 300 Ω C_L = 35 pF; V_S = 5 V; Test Circuit 7

Parameter	+25°C	−40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS[2]				
t_{OFF} (EN)	60		ns typ	R_L = 300 Ω, C_L = 35 pF; V_S = 5 V; Test Circuit 7
Charge Injection	5		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 8
OFF Isolation	−75		dB typ	R_L = 1 kΩ f = 100 kHz; V_{EN} = 0 V; Test Circuit 9
Channel-to-Channel Crosstalk	85		dB typ	R_L = 1 kΩ, f = 100 kHz; Test Circuit 10
Total Harmonic Distortion, THD + N	0.002		% typ	R_L = 600 Ω, 5 V rms; f=20 Hz to 20 kHz
−3 dB Bandwidth	50		MHz typ	R_L = 300 Ω, C_L = 5 pF; Test Circuit 10
C_S (OFF)	2		pF typ	f = 1 MHz
C_D (OFF)				f = 1 MHz
ADG1208	11		pF typ	
ADG1209	6		pF typ	
C_D, C_S (ON)				f = 1 MHz
ADG1208	15		pF typ	
ADG1209	8		pF typ	
POWER REQUIREMENTS				V_{DD} = 13.2 V
I_{DD}		1	µA typ	Digital inputs= 0 V or V_{DD}
		5	µA max	
I_{DD}	150		µA typ	Digital inputs= 5
		300	µA max	

[1] Temperature ranges are as follows: B Version: −40°C to +125°.
[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	36 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog, Digital Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 20 mA, whichever occurs first
Continuous Current, S or D	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle max)	100 mA
Operating Temperature Range	
Industrial (B Version)	−40° C to +85°C
Automotive (Y Version)	−40° C to +125°C
Storage Temperature Range	−65° C to +150°C
Junction Temperature	150°C
TSSOP Package, Power Dissipation	450 mW
θ_{JA}, Thermal Impedance	150.4°C/W
θ_{JC}, Thermal Impedance	50°C/W
LFCSP, Package, Power Dissipation	450 mW
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] Overvoltages at A, EN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

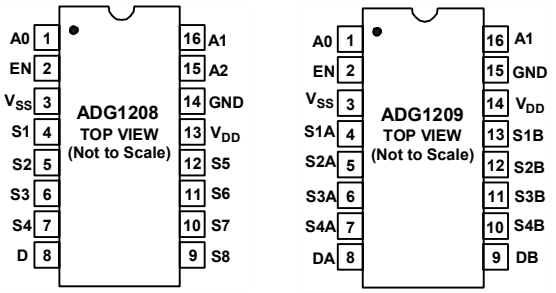

Figure 2. Pin Configurations—TSSOP

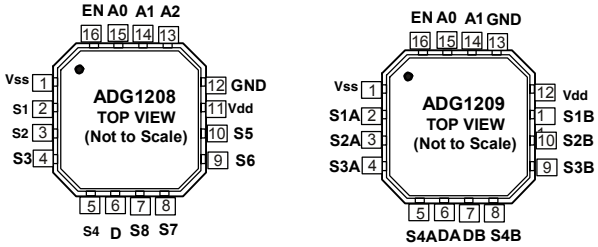

Figure 3. Pin Configurations – 4mm x4mm LFCSP

Table 4. ADG1208 Truth Table

A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Table 5. ADG1209 Truth Table

AI	A0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

TERMINOLOGY

Table 6.

Mnemonic	Description
V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to ground.
GND	Ground (0 V) reference.
R_{ON}	Ohmic resistance between D and S.
ΔR_{ON}	Difference between the R_{ON} of any two channels.
I_S (OFF)	Source leakage current when the switch is off.
I_D (OFF)	Drain leakage current when the switch is off.
I_D, I_S (ON)	Channel leakage current when the switch is on.
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	Channel input capacitance for OFF condition.
C_D (OFF)	Channel output capacitance for OFF condition.
C_D, C_S (ON)	ON switch capacitance.
CI_N	Digital input capacitance.
t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch ON condition.
t_{OFF} (EN)	Delay time between the 50% and 90% points of the digital input and switch OFF condition.
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and the switch ON condition when switching from one address state to another.
t_{OPEN}	OFF time measured between the 80% point of both switches when switching from one address state to another.
V_{INL}	Maximum input voltage for Logic 0.
V_{INH}	Minimum input voltage for Logic 1.
I_{INL} (I_{INH})	Input current of the digital input.
I_{DD}	Positive supply current.
I_{SS}	Negative supply current.
Off Isolation	A measure of unwanted signal coupling through an OFF channel.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Bandwidth	The frequency at which the output is attenuated by 3dBs.
On Response	The frequency response of the “ON” switch.
THD + N	The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

TYPICAL PERFORMANCE CHARACTERISTICS

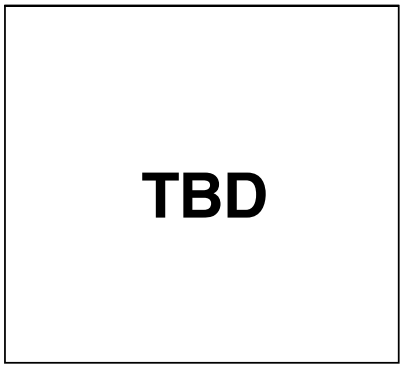

Figure 4. On Resistance as a Function of VD(VS) for Single Supply

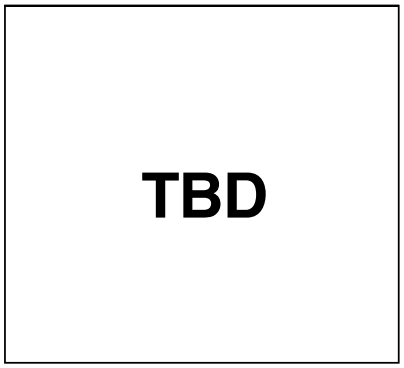

Figure 7. On Resistance as a Function of VD(VS) for Different Temperatures, Single Supply

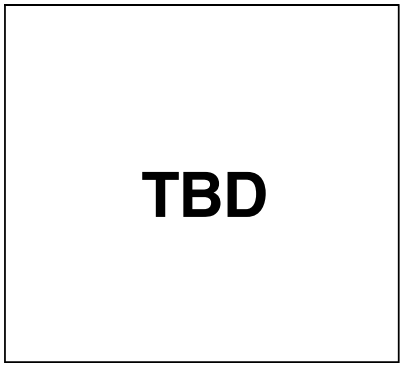

Figure 5. On Resistance as a Function of VD(VS) for Dual Supply

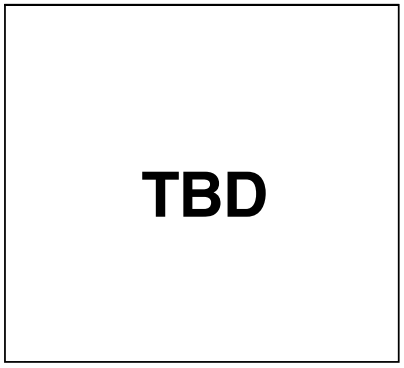

Figure 8. On Resistance as a Function of VD(VS) for Different Temperatures, Dual Supply

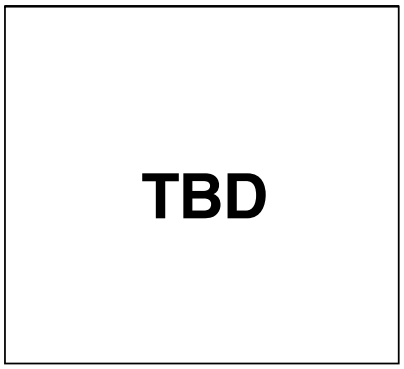

Figure 6. On Resistance as a Function of VD(VS) for Different Temperatures, Single Supply

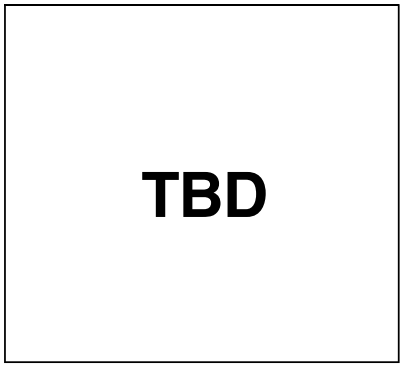

Figure 9. Leakage Currents as a Function of V_D (V_S)

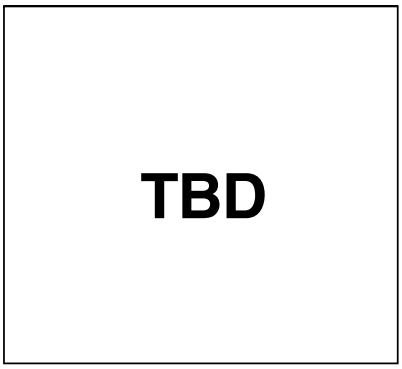

Figure 10. Leakage Currents as a function of Temperature

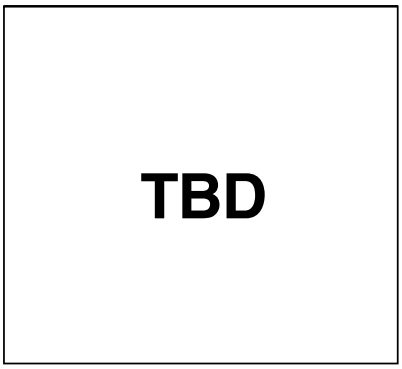

Figure 11. Supply Currents vs. Input Switching Frequency

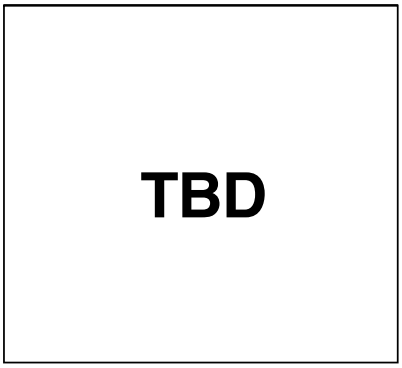

Figure 12. Charge Injection vs. Source Voltage

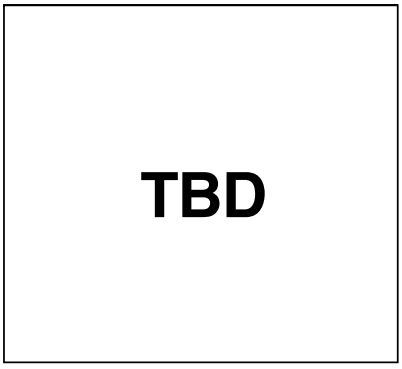

Figure 13. TON/TOFF Times vs. Temperature)

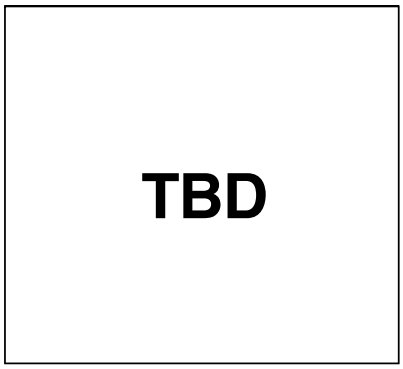

Figure 14. Off Isolation vs. Frequency

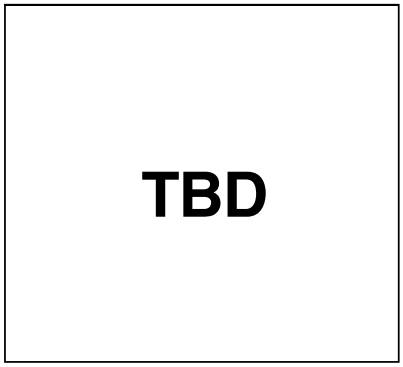

Figure 15. Crosstalk vs. Frequency

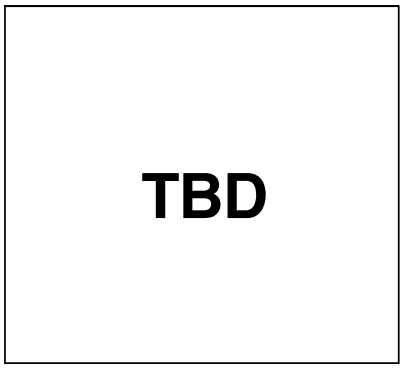

Figure 16. On Response vs. Frequency

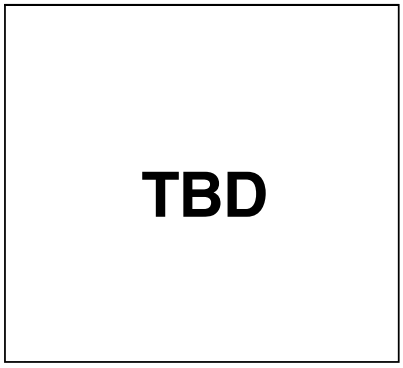

Figure 17. THD + N vs. Frequency

TEST CIRCUITS

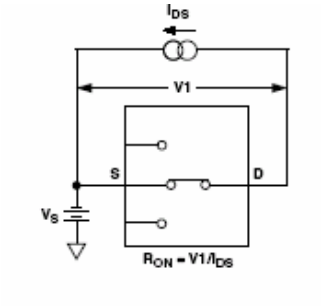

Figure 18. Test Circuit 1. On Resistance

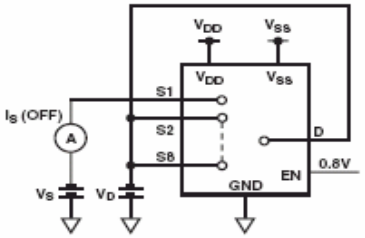

Figure 19. Test Circuit 2. I_S (OFF)

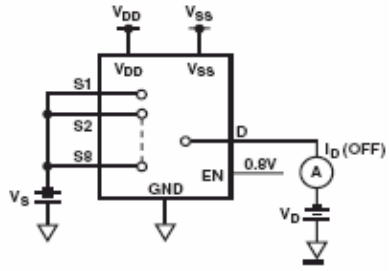

Figure 20. Test Circuit 3. I_D (OFF)

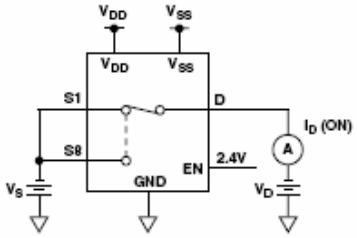

Figure 21. Test Circuit 4. I_D (ON)

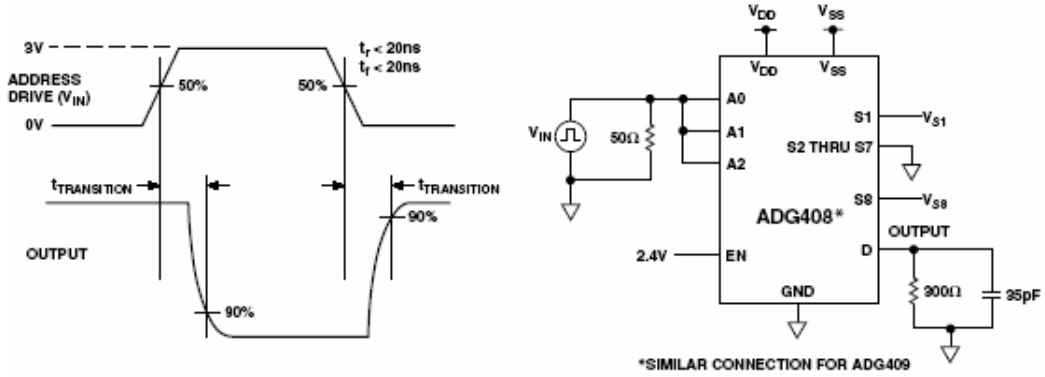

Figure 22. Test Circuit 5. Switching Time of Multiplexer, $t_{TRANSITION}$

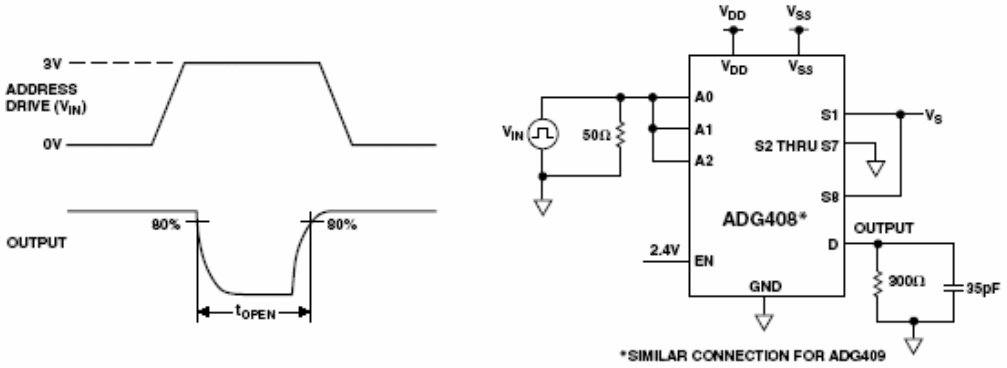

Figure 23. Test Circuit 6. Break-Before-Make Delay, t_{OPEN}

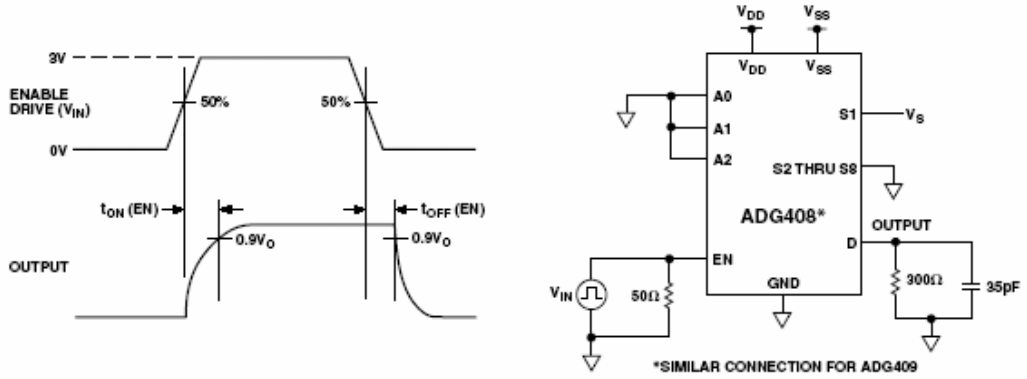

Figure 24. Test Circuit 7. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

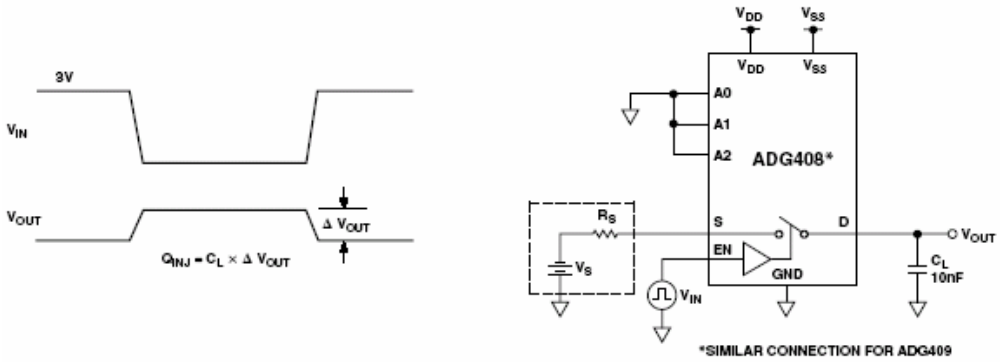

Figure 25. Test Circuit 8. Charge Injection

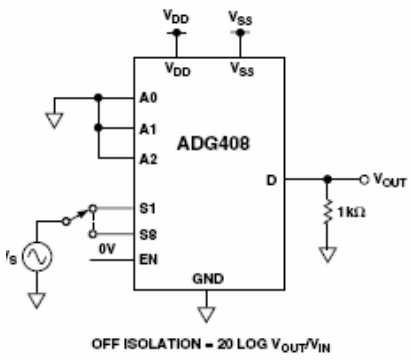

Figure 26. Test Circuit 9. OFF Isolation

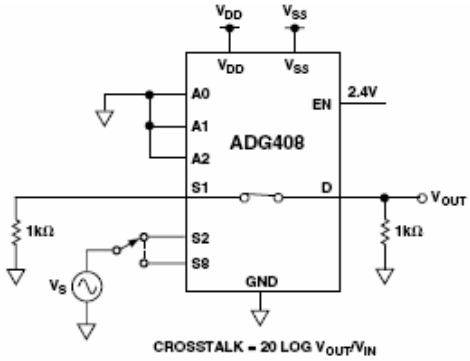

Figure 27. Test Circuit 10. Channel-to-Channel Crosstalk

OUTLINE DIMENSIONS

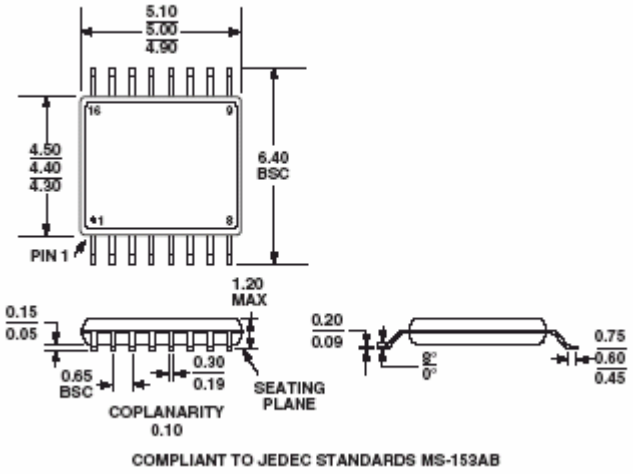

Figure 28. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

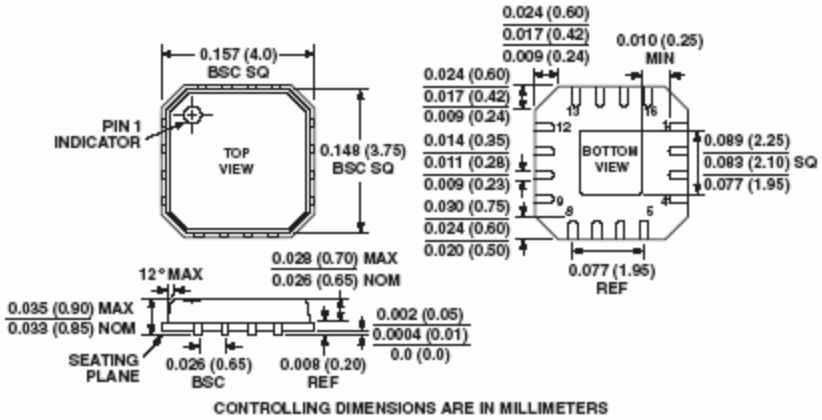

Figure 29. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4mm × 4 mm (CP-16)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Description	Package Option
ADG1208YRU	−40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1209YRU	−40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1209YCP	−40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	CP-16
ADG1209YCP	−40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	CP-16

NOTES

NOTES

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