



3.3V CMOS 18-BIT REGISTERED BUS TRANS- CEIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH16525

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP,
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Normal Range
- $V_{CC} = 2.7\text{V}$ to 3.6V , Extended Range
- $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$
- CMOS power levels ($0.4\mu\text{W}$ typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCH16525:

- High Output Drivers: $\pm 24\text{mA}$
- Suitable for heavy loads

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

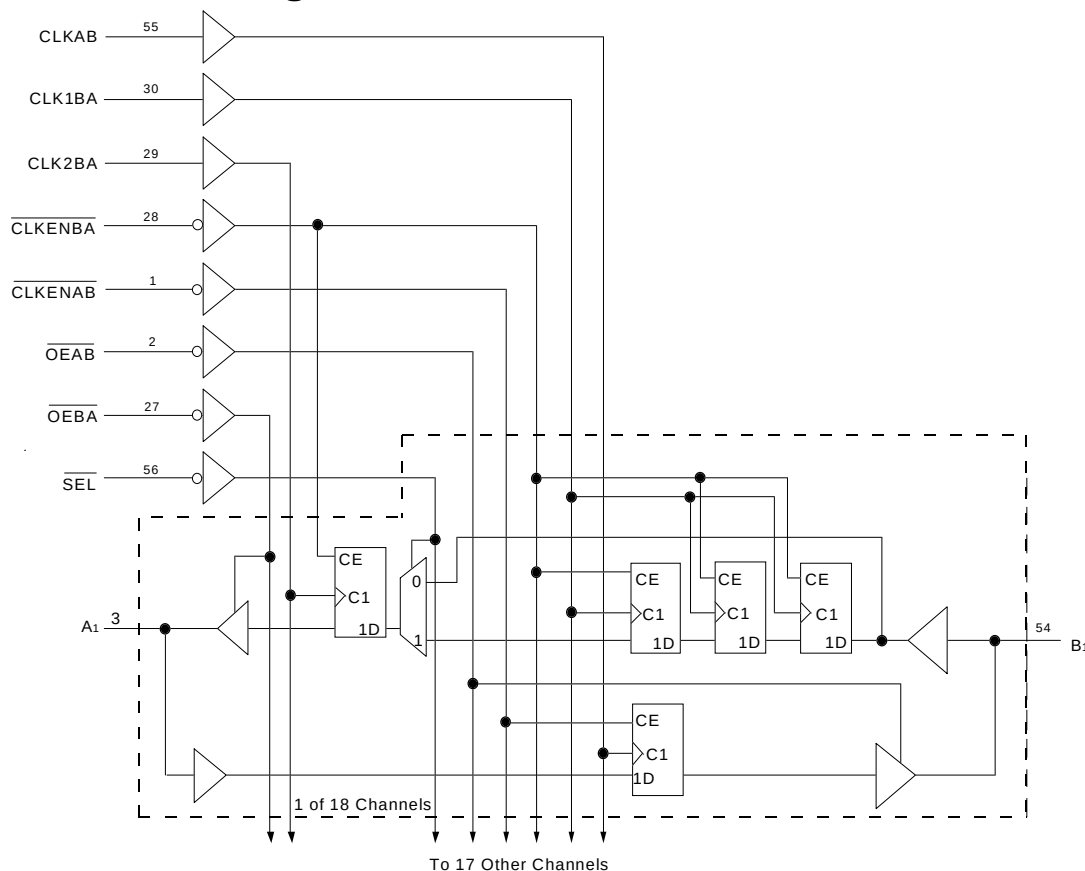
DESCRIPTION:

This 18-bit registered bus transceiver is built using advanced dual metal CMOS technology. Data flow in each direction is controlled by output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$) and clock-enable ($\overline{\text{CLKENAB}}$ and $\overline{\text{CLKENBA}}$) inputs. For the A-to-B data flow, the data flows through a single register. The B-to-A data can flow through a four-stage pipeline register path, or through a single register path, depending on the state of the select ($\overline{\text{SEL}}$) input. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input, provided that the appropriate $\overline{\text{CLKEN}}$ inputs are low. The A-to-B data transfer is synchronized to the CLKAB input, and B-to-A data transfer is synchronized with the CLK1BA and CLK2BA inputs.

The ALVCH16525 has been designed with a $\pm 24\text{mA}$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16525 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

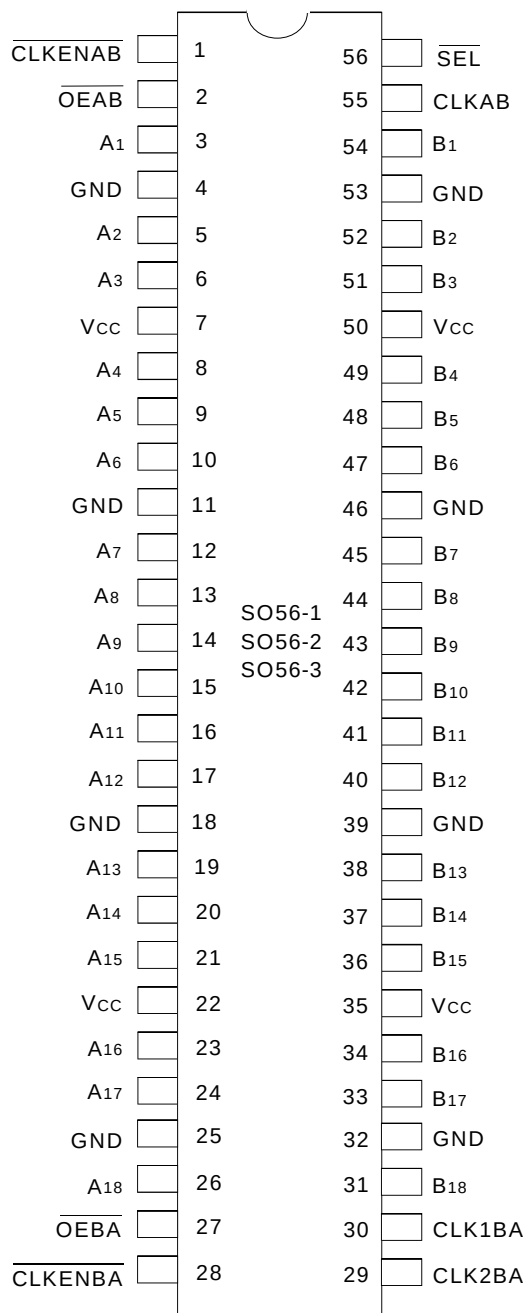
Functional Block Diagram



EXTENDED COMMERCIAL TEMPERATURE RANGE

APRIL 1999

PIN CONFIGURATION



SSOP/TSSOP/TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	– 0.5 to + 4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	– 0.5 to VCC + 0.5	V
TSTG	Storage Temperature	– 65 to + 150	°C
IOUT	DC Output Current	– 50 to + 50	mA
IIK	Continuous Clamp Current, VI < 0 or VI > VCC	± 50	mA
IOK	Continuous Clamp Current, VO < 0	– 50	mA
ICC	Continuous Current through each VCC or GND	± 100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VCC terminals.
- All terminals except VCC.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	5	7	pF
COUT	Output Capacitance	VOUT = 0V	7	9	pF
CIO	I/O Port Capacitance	VIN = 0V	7	9	pF

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NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
CLKAB	Clock Input for the A to B direction
CLK1BA	Clock Input for the B to A pipeline register
CLK2BA	Clock Input for the B to A output register
$\overline{\text{CLKENBA}}$	Clock Enable for the CLK1BA and CLK2BA clocks (Active LOW)
$\overline{\text{CLKENAB}}$	Clock Enable for the CLKAB clock (Active LOW)
$\overline{\text{OEAB}}$	Output Enable for the B port (Active LOW)
$\overline{\text{OEBA}}$	Output Enable for the A port (Active LOW)
$\overline{\text{SEL}}$	Select pin for pipelined/non-pipelined mode in the B-to-A direction (Active LOW)
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs ⁽¹⁾
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs ⁽¹⁾

NOTE:

- These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLES (1)

A-TO-B STORAGE ($\overline{\text{OEAB}} = \text{L}$, $\overline{\text{OEBA}} = \text{H}$)			
Inputs			Output
$\overline{\text{CLKENAB}}$	CLKAB	Ax	Bx
H	X	X	$\text{B}_0^{(2)}$
L	$\uparrow$	L	L
L	$\uparrow$	H	H

B-TO-A STORAGE ($\overline{\text{OEBA}} = \text{L}$, $\overline{\text{OEAB}} = \text{H}$)					
Inputs					Output
$\overline{\text{CLKENBA}}$	CLK2BA	CLK1BA	$\overline{\text{SEL}}$	Bx	Ax
H	X	X	X	X	$\text{A}_0^{(2)}$
L	$\uparrow$	X	H	L	L
L	$\uparrow$	X	H	H	H
L	$\uparrow$	$\uparrow$	L	L	$\text{L}^{(3)}$
L	$\uparrow$	$\uparrow$	L	H	$\text{H}^{(3)}$

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
 $\uparrow$ = LOW-to-HIGH Transition
- Output level before the indicated steady-state input conditions were established.
- Three CLK1BA edges are one CLK2BA needed to propagate data from B to A when $\overline{\text{SEL}}$ is low.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
VIH	Input HIGH Voltage Level	VCC = 2.3V to 2.7V		1.7	—	—	V
		VCC = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	VCC = 2.3V to 2.7V		—	—	0.7	V
		VCC = 2.7V to 3.6V		—	—	0.8	
IiH	Input HIGH Current	VCC = 3.6V	Vi = VCC	—	—	± 5	μA
IiL	Input LOW Current	VCC = 3.6V	Vi = GND	—	—	± 5	
IoZH IoZL	High Impedance Output Current (3-State Output pins)	VCC = 3.6V	Vo = VCC	—	—	± 10	μA
			Vo = GND	—	—	± 10	μA
Vik	Clamp Diode Voltage	VCC = 2.3V, IIN = -18mA		—	-0.7	-1.2	V
VH	Input Hysteresis	VCC = 3.3V		—	100	—	mV
ICCL ICCH ICCZ	Quiescent Power Supply Current	VCC = 3.6V		—	0.1	40	μA
		VIN = GND or VCC					
ΔICC		One input at VCC - 0.6V, other inputs at VCC or GND		—	—	750	

NOTE:

- Typical values are at VCC = 3.3V, +25°C ambient.

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BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
IBHH IBHL	Bus-Hold Input Sustain Current	V _{CC} = 3.0V	V _I = 2.0V	– 75	—	—	μA
			V _I = 0.8V	75	—	—	
IBHH IBHL	Bus-Hold Input Sustain Current	V _{CC} = 2.3V	V _I = 1.7V	– 45	—	—	μA
			V _I = 0.7V	45	—	—	
IBHHO IBHLO	Bus-Hold Input Overdrive Current	V _{CC} = 3.6V	V _I = 0 to 3.6V	—	—	± 500	μA

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NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = – 0.1mA	V _{CC} – 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = – 6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = – 12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3.0V		2.4	—	
		V _{CC} = 3.0V	I _{OH} = – 24mA	2	—	
V _{OL}	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
		V _{CC} = 3.0V	I _{OL} = 24mA	—	0.55	

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NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	$V_{CC} = 2.5V \pm 0.2V$	$V_{CC} = 3.3V \pm 0.3V$	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	$C_L = 0\text{pF}$, $f = 10\text{MHz}$	—	160	pF
CPD	Power Dissipation Capacitance Outputs disabled		—	160	pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}		120	—	125	—	150	—	MHz
t _{PLH} t _{PHL}	Propagation Delay CLKAB to Bx or CLK2BA to Ax	1	4.5	—	4.4	1	4.2	ns
t _{PZH} t _{PZL}	Output Enable Time $\overline{OEAB}$ to Bx or $\overline{OEBA}$ to Ax	1	6.1	—	6.1	1	5.1	ns
t _{PHZ} t _{PLZ}	Output Disable Time $\overline{OEAB}$ to Bx or $\overline{OEBA}$ to Ax	1	6.3	—	5.4	1	4.9	ns
t _{SU}	Setup Time, Ax data before CLKAB $\uparrow$	1.3	—	1.3	—	1.3	—	ns
t _{SU}	Setup Time, Bx data before CLK2BA $\uparrow$	2.1	—	1.8	—	1.7	—	ns
t _{SU}	Setup Time, Bx data before CLK1BA $\uparrow$	1.3	—	1.2	—	1.1	—	ns
t _{SU}	Setup Time, $\overline{SEL}$ before CLK2BA $\uparrow$	3.3	—	3.3	—	3.3	—	ns
t _{SU}	Setup Time, $\overline{CLKENAB}$ before CLKAB $\uparrow$	2.1	—	1.9	—	1.6	—	ns
t _{SU}	Setup Time, $\overline{CLKENBA}$ before CLK1BA $\uparrow$	2.7	—	2.5	—	2.1	—	ns
t _{SU}	Setup Time, $\overline{CLKENBA}$ before CLK2BA $\uparrow$	2.7	—	2.5	—	2.2	—	ns
t _H	Hold Time, Ax data after CLKAB $\uparrow$	0.7	—	0.4	—	0.9	—	ns
t _H	Hold Time, Bx data after CLK2BA $\uparrow$	0.4	—	0	—	0.6	—	ns
t _H	Hold Time, Bx data after CLK1BA $\uparrow$	0.8	—	0.4	—	1	—	ns
t _H	Hold Time, $\overline{SEL}$ after CLK2BA $\uparrow$	0	—	0	—	0.1	—	ns
t _H	Hold Time, $\overline{CLKENAB}$ after CLKAB $\uparrow$	0.1	—	0.3	—	0.3	—	ns
t _H	Hold Time, $\overline{CLKENBA}$ after CLK1BA $\uparrow$	0	—	0	—	0.1	—	ns
t _H	Hold Time, $\overline{CLKENBA}$ after CLK2BA $\uparrow$	0	—	0	—	0	—	ns
t _w	Pulse Duration, CLK HIGH or LOW	3.2	—	3.2	—	3	—	ns
t _{sk(o)}	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:

- See test circuits and waveforms. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.
- Skew between any two outputs of the same package and switching in the same direction.

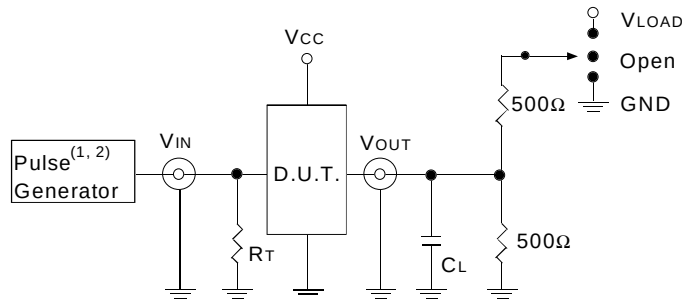
TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	V _{CC} (1)= 3.3V±0.3V	V _{CC} (1)= 2.7V	V _{CC} (2)= 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

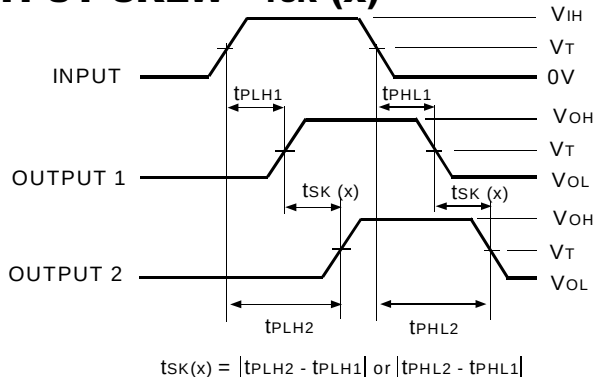
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - t_{SK} (x)

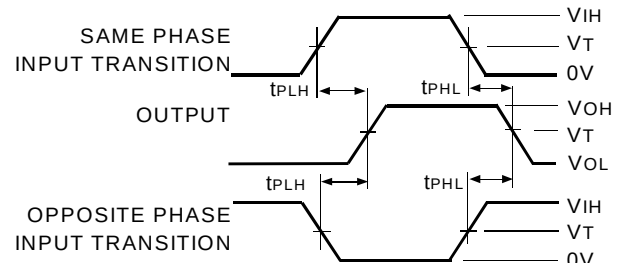


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NOTES:

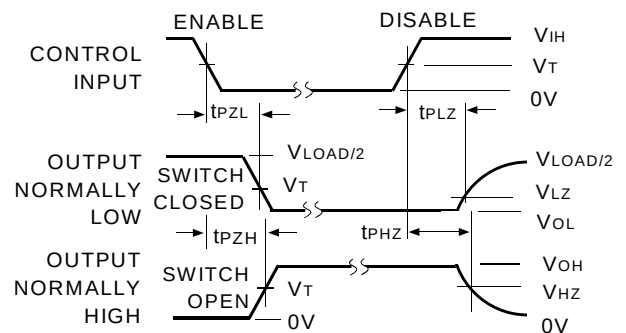
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

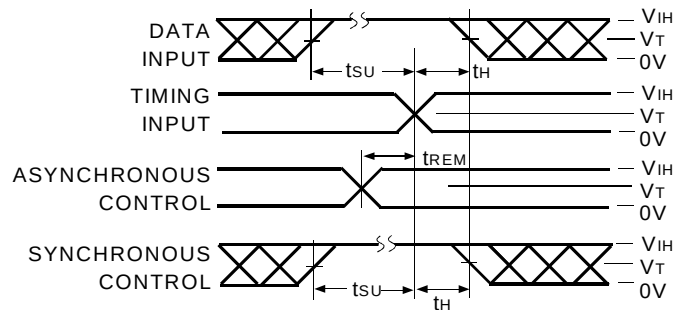


ALVC Link

NOTE:

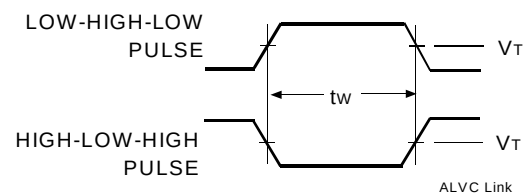
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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PULSE WIDTH



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ORDERING INFORMATION

IDT	XX	ALVC	X	XX	XXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
					525		18-Bit Registered Bus Transceiver with 3-State Outputs
				16			Double-Density with Resistors, $\pm 24\text{mA}$
			H				Bus-Hold
			74				-40°C to $+85^{\circ}\text{C}$



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