STRUCTURE Silicon monolithic integrated circuit

PRODUCT NAME BU97933ACH-3BW

FUNCTION RAM built-in, Dot-matrix 128 x 33 STN LCD control driver

FEATURE
- 4-SPI, 8bit parallel interface (68 series, 80 series)
- Built-in LCD driver power-supply circuit, voltage follower, booster circuit, (Built-in capacitor)
- Built-in bias select circuit (1/5, 1/6)

○ Absolute maximum ratings (VSS1=VSS2=VSS3= 0V)

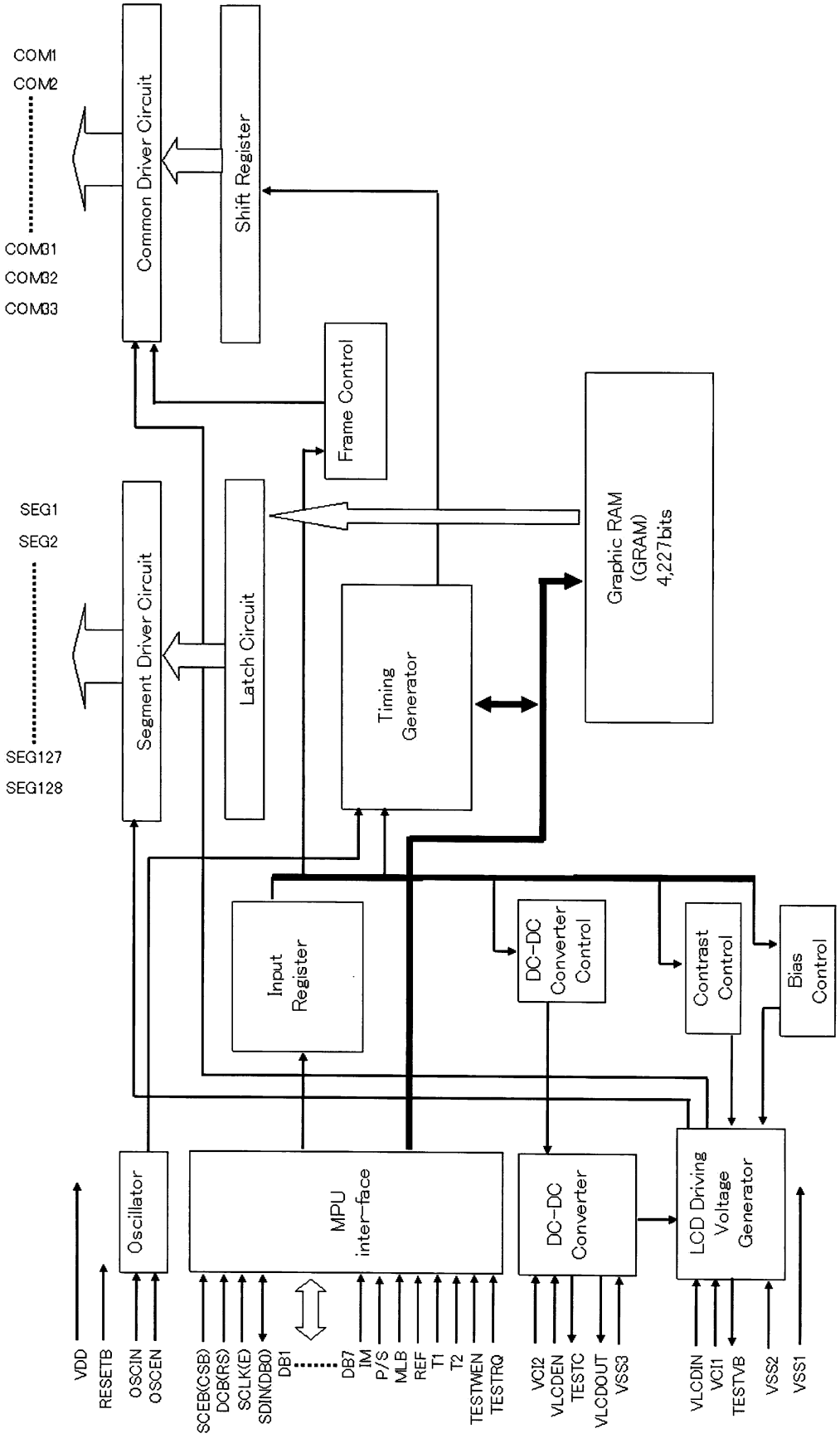
Parameter	Symbol	Rated values	Unit	Remarks
Power supply voltage 1	VDD	-0.5 ~ +4.0	V	
Power supply voltage 2	VCI1,2	-0.5 ~ +4.0	V	
Power supply voltage 3	VLCDIN	-0.5 ~ +11.0	V	
Input voltage range	VIN	-0.5 ~ VDD+0.5	V	
Operational temperature range	Topr	-40 ~ +85	℃	
Storage temperature range	Tstg	-55 ~ +155	℃	

○ Recommend operating conditions (Ta = 25℃, VSS1=VSS2=VSS3= 0V)

Parameter	Symbol	MIN	TYP	MAX	Unit	Remarks
Power supply voltage 1	VDD	1.7	-	3.3	V	
Power supply voltage 2	VCI1, 2	2.4	-	3.3	V	
Power supply voltage 3	VLCDIN	5.5	-	9.0	V	

※ About shape / delivery forms of this product, please refer to "Specification of Chip Shipment"
※ About explanation about panel module design that used this product, please refer to "Panel Layout Design Guide"
※ About detailed function explanation of this product, please refer to "Function Description Guide"
※ About explanation about picture quality adjustment of this product, please refer to "Adjustment manual for the picture quality of LCD Display"

○ Block diagram



○ Electrical characteristics

DC Characteristics

(Ta=25℃,VDD=1.7～3.3V,VCI=2.4～3.3V,VSS1=VSS2=VSS3=0V unless otherwise specified)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
"H" input voltage	VIH	0.7VDD	-	-	V	
"L" input voltage	VIL	-	-	0.3VDD	V	
Input current	IIN	-1	-	1	uA	
On resistance of IC	RON	-	2.0	8.0	kΩ	|Δ Von|=0.5V
LCD Operation Voltage	VLCD	-120	-	+120	mV	VDD=2.8V,VLCDOUT=6.5V
Current consumption	IDD1	-	0.1	5	uA	Standby mode
	IDD2	-	80	-	uA	Normal mode (x3 boost)
	IDD3	-	100	-	uA	Ram write mode (x3 boost)

※) At first the power supply injection of the VLCD (load) is to throw VLCDIN.
As for the injection turn, which doesn't care even about the point with other power supplies.
As for the power supply injection turn at the time of the VLCD internal booster, VDD, VCI1 and 2 which don't care even about the point.
Be sure to take VCI1 and 2≧VDD.

Oscillation Characteristics

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
Internal oscillation frequency	fosc	26	30	34	kHz	Ta=25℃,VDD=2.8V
External clock frequency	fIN	-	15	-	kHz	
External clock duty	tW	-	50	-	%	
Frame frequency *	fFR	65.6	76	85.8	Hz	typ : fosc=30kHz

*: Relations between oscillation frequency (clock frequency) and the frame frequency are shown with the next method.

fFR=fosc/396=2 x fIN/396

RESET Characteristics

(Ta=25℃,VCI=2.4～3.3V,VSS1=VSS2=VSS3=0V unless otherwise specified)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
RESET_B enable pulse width	tRWe	500	-	-	ns	VDD=2.4V～3.3V
RESET_B disable pulse width	tRWn	100	-	-	ns	
RESET_B-Instruction time	tRC	500	-	-	ns	
RESET_B enable pulse width	tRWe	2000	-	-	ns	VDD=1.7V～2.4V
RESET_B disable pulse width	tRWn	500	-	-	ns	
RESET_B-Instruction time	tRC	2000	-	-	ns	

MPU interface Characteristics (4-SPI)

(Ta=25℃,VCI=2.4～3.3V,VSS1=VSS2=VSS3=0V unless otherwise specified)

Parameter	Symbol	Limit			Unit	Conditions
		MIN	TYP	MAX		
Input rise time	tr	-	-	100	ns	VDD=2.4V～3.3V
Input fall time	tf	-	-	100	ns	
SCLK cycle	tCYCS	250	-	-	ns	
"H" SCLK pulse width	tWH	100	-	-	ns	
"L" SCLK pulse width	tWL	100	-	-	ns	
DC_B set-up time	tDCS	100	-	-	ns	
DC_B hold time	tDCH	100	-	-	ns	
SDIN set-up time	tSDINS	100	-	-	ns	
SDIN hold time	tSDINH	100	-	-	ns	
SCEB setup time1	tSCES1	60	-	-	ns	
SCEB setup time2	tSCES2	160	-	-	ns	
SCEB hold time1	tSCEH1	100	-	-	ns	
SCEB hold time2	tSCEH2	100	-	-	ns	
Input rise time	tr	-	-	100	ns	VDD=1.7V～2.4V
Input fall time	tf	-	-	100	ns	
SCLK cycle	tCYCS	300	-	-	ns	
"H" SCLK pulse width	tWH	130	-	-	ns	
"L" SCLK pulse width	tWL	130	-	-	ns	
DC_B set-up time	tDCS	130	-	-	ns	
DC_B hold time	tDCH	130	-	-	ns	
SDIN set-up time	tSDINS	130	-	-	ns	
SDIN hold time	tSDINH	130	-	-	ns	
SCEB setup time1	tSCES1	130	-	-	ns	
SCEB setup time2	tSCES2	260	-	-	ns	
SCEB hold time1	tSCEH1	400	-	-	ns	
SCEB hold time2	tSCEH2	270	-	-	ns	

MPU interface Characteristics (Parallel interface)

(Ta=25℃,VCI=2.4～3.3V,VSS1=VSS2=VSS3=0V unless otherwise specified)

Parameter	Symbol	Limit			Unit	Conditions
		MIN	TYP	MAX		
Address set-up time	tAS	0	-	-	ns	VDD=2.4V～3.3V
Address hold time	tAH	0	-	-	ns	
E pulse width "H"	tWH	120	-	-	ns	
E pulse width "L"	tWL	120	-	-	ns	
E cycle time	tCYC	240	-	-	ns	
Data set-up time	tDS	60	-	-	ns	
Data hold time	tDH	10	-	-	ns	
Address set-up time	tAS	0	-	-	ns	VDD=1.7V～2.4V
Address hold time	tAH	0	-	-	ns	
E pulse width "H"	tWH	500	-	-	ns	
E pulse width "L"	tWL	500	-	-	ns	
E cycle time	tCYC	1000	-	-	ns	
Data set-up time	tDS	80	-	-	ns	
Data hold time	tDH	30	-	-	ns	

○ Cautions on use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operatingconditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) No Connecting input terminals
In terms of extremely high impedance of CMOS gate, to open the input terminals causes unstable state. And unstable state brings the inside gate voltage of p-channel or n-channel transistor into active. As a result, battery current may increase. And unstable state can also causes unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or GND line.

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