1, 2, 4, 6 and 8-Channel Low Capacitance ESD Protection Arrays

Features

- 1, 2, 4, 6 and 8 channels of ESD protection
- Provides ESD protection to IEC61000-4-2 Level 4
  - 8kV contact discharge
  - 15kV air discharge
- Low loading capacitance of 1.0pF typical
- Minimal capacitance change with temperature and voltage
- Channel I/O to GND capacitance difference of 0.02pF typical is ideal for differential signals
- Channel I/O to I/O capacitance 0.8pF typical
- Zener diode protects supply rail and eliminates the need for external by-pass capacitors
- Each I/O pin can withstand over 1000 ESD strikes
- Available in SOT, SOIC and MSOP packages
- Lead-free version available

Applications

- USB2.0 ports at 480Mbps in desktop PCs, notebooks and peripherals
- IEEE1394 Firewire® ports at 400Mbps / 800Mbps
- DVI ports, HDMI ports in notebooks, set top boxes, digital TVs, LCD displays
- Serial ATA ports in desktop PCs and hard disk drives
- PCI Express ports
- General purpose high-speed data line ESD protection

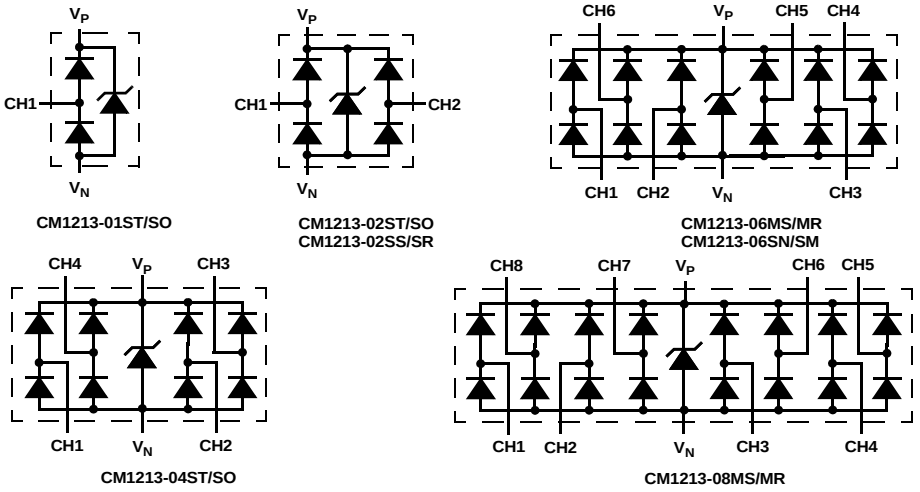
Product Description

The CM1213 family of diode arrays has been designed to provide ESD protection for electronic components or sub-systems requiring minimal capacitive loading. These devices are ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading. Each ESD channel consists of a pair of diodes in series which steer the positive or negative ESD current pulse to either the positive (V_P) or negative (V_N) supply rail. A Zener diode is embedded between V_P and V_N, offering two advantages. First, it protects the V_{CC} rail against ESD strikes, and second, it eliminates the need for a bypass capacitor that would otherwise be needed for absorbing positive ESD strikes to ground. The CM1213 will protect against ESD pulses up to ±8kV per the IEC 61000-4-2 standard and using the MIL-STD-883D (Method 3015) specification for Human Body Model (HBM) ESD, all pins are protected from contact discharges of greater than ±15kV.

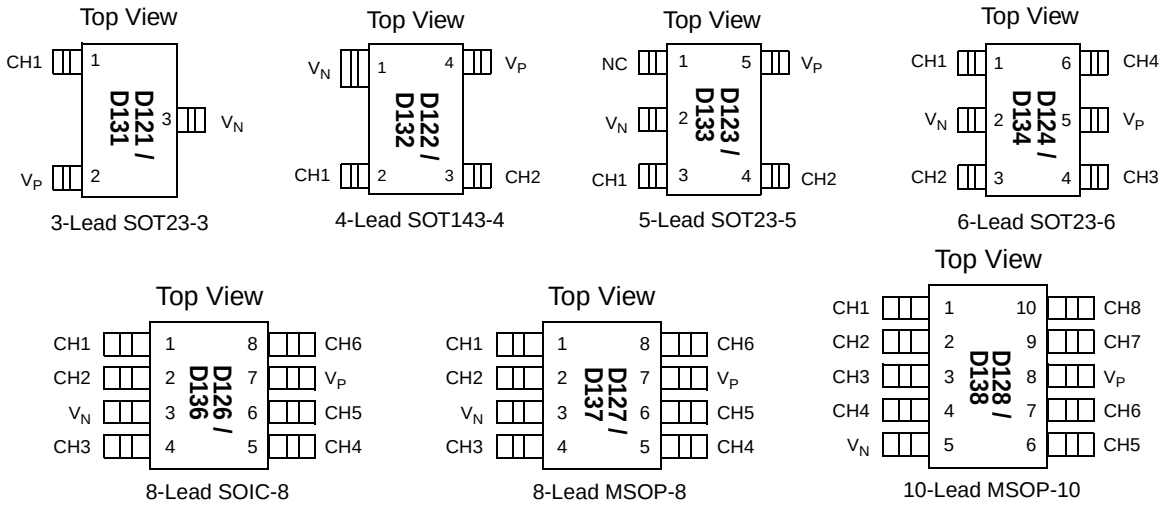
This device is particularly well-suited for protecting systems using high-speed ports such as USB2.0, IEEE1394 (Firewire®, iLink™), Serial ATA, DVI, HDMI and corresponding ports in removable storage, digital camcorders, DVD-RW drives and other applications where extremely low loading capacitance with ESD protection are required in a small package footprint.

The CM1213 family of devices is available with optional lead-free finishing.

Electrical Schematics



PACKAGE / PINOUT DIAGRAMS



Note: These drawings are not to scale.

PIN DESCRIPTIONS

1-CHANNEL, 3-LEAD SOT23-3 PACKAGES

PIN	NAME	TYPE	DESCRIPTION
1	CH1	I/O	ESD Channel
2	V_P	PWR	Positive voltage supply rail
3	V_N	GND	Negative voltage supply rail

2-CHANNEL, 5-LEAD SOT23-5 PACKAGE

PIN	NAME	TYPE	DESCRIPTION
1	NC		No connect
2	V_N	GND	Negative voltage supply rail
3	CH1	I/O	ESD Channel
4	CH2	I/O	ESD Channel
5	V_P	PWR	Positive voltage supply rail

4-CHANNEL, 6-LEAD SOT23-6 PACKAGE

PIN	NAME	TYPE	DESCRIPTION
1	CH1	I/O	ESD Channel
2	V_N	GND	Negative voltage supply rail
3	CH2	I/O	ESD Channel
4	CH3	I/O	ESD Channel
5	V_P	PWR	Positive voltage supply rail
6	CH4	I/O	ESD Channel

2-CHANNEL, 4-LEAD SOT143-4 PACKAGE

PIN	NAME	TYPE	DESCRIPTION
1	V_N	GND	Negative voltage supply rail
2	CH1	I/O	ESD Channel
3	CH2	I/O	ESD Channel
4	V_P	PWR	Positive voltage supply rail

6-CHANNEL, 8-LEAD MSOP-8/SOIC-8 PACKAGE

PIN	NAME	TYPE	DESCRIPTION
1	CH1	I/O	ESD Channel
2	CH2	I/O	ESD Channel
3	V_N	GND	Negative voltage supply rail
4	CH3	I/O	ESD Channel
5	CH4	I/O	ESD Channel
6	CH5	I/O	ESD Channel
7	V_P	PWR	Positive voltage supply rail
8	CH6	I/O	ESD Channel

8-CHANNEL, 10-LEAD MSOP-10 PACKAGE

PIN	NAME	TYPE	DESCRIPTION
1	CH1	I/O	ESD Channel
2	CH2	I/O	ESD Channel
3	CH3	I/O	ESD Channel
4	CH4	I/O	ESD Channel
5	V_N	GND	Negative voltage supply rail
6	CH5	I/O	ESD Channel
7	CH6	I/O	ESD Channel
8	V_P	PWR	Positive voltage supply rail
9	CH7	I/O	ESD Channel
10	CH8	I/O	ESD Channel

Ordering Information

PART NUMBERING INFORMATION						
			Standard Finish		Lead-free Finish	
# of Channels	Leads	Package	Ordering Part Number[1]	Part Marking	Ordering Part Number[1]	Part Marking
1	3	SOT23-3	CM1213-01ST	D121	CM1213-01SO	D131
2	4	SOT143-4	CM1213-02SS	D122	CM1213-02SR	D132
2	5	SOT23-5	CM1213-02ST	D123	CM1213-02SO	D133
4	6	SOT23-6	CM1213-04ST	D124	CM1213-04SO	D134
6	8	SOIC-8	CM1213-06SN	D126	CM1213-06SM	D136
6	8	MSOP-8	CM1213-06MS	D127	CM1213-06MR	D137
8	10	MSOP-10	CM1213-08MS	D128	CM1213-08MR	D138

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	RATING	UNITS
Operating Supply Voltage (V_P - V_N)	6.0	V
Diode Forward DC Current (Note 1)	8	mA
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
DC Voltage at any channel input	(V_N - 0.5) to (V_P + 0.5)	V

Note 1: Only one diode conducting at a time.

STANDARD OPERATING CONDITIONS		
PARAMETER	RATING	UNITS
Operating Temperature Range	-40 to +85	°C
Package Power Rating		
SOT23-3 Package (CM1213-01ST/SO)	225	mW
SOT143-4 Package (CM1213-02SS/SR)	225	mW
SOT23-5 Package (CM1213-02ST/SO)	225	mW
SOT23-6 Package (CM1213-04ST/SO)	225	mW
MSOP-8 Package (CM1213-06MS/MR)	400	mW
SOIC-8 Package (CM1213-06SN/SM)	600	mW
MSOP-10 Package (CM1213-08MS/MR)	400	mW

ELECTRICAL OPERATING CHARACTERISTICS[1]

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_P	Operating Supply Voltage (V_P-V_N)			3.3	5.5	V
I_P	Operating Supply Current	(V_P-V_N)=3.3V			8.0	µA
V_F	Diode Forward Voltage Top Diode Bottom Diode	I_F = 8mA; T_A=25°C	 0.60 0.60	 0.80 0.80	 0.95 0.95	 V V
I_{LEAK}	Channel Leakage Current	T_A=25°C; V_P=5V, V_N=0V		±0.1	±1.0	µA
C_{IN}	Channel Input Capacitance	At 1 MHz, V_P=3.3V, V_N=0V, V_{IN}=1.65V; Note 2 applies		1.0	1.5	pF
ΔC_{IN}	Differential Channel I/O to GND capacitance			0.02		pF
ΔC_{IO}	Channel I/O to I/O capacitance			0.80		pF
V_{ESD}	ESD Protection Peak Discharge Voltage at any channel input, in system a) Contact discharge per IEC 61000-4-2 standard b) Human Body Model, MIL-STD-883, Method 3015	 Notes 2, 4 & 5; T_A=25°C Notes 2, 3 & 5; T_A=25°C	 ±8 ±15			 kV kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	At 8kV ESD HBM; T_A=25°C; Notes 2 & 3		 +9.0 -9.0		 V V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	T_A=25°C; Notes 5 & 6		 1.2 0.6		 Ω Ω

Note 1: All parameters specified at T_A = -40°C to +85°C unless otherwise noted.

Note 2: These parameters guaranteed by design and characterization.

Note 3: Human Body Model per MIL-STD-883, Method 3015, $C_{Discharge}$ = 100pF, $R_{Discharge}$ = 1.5KΩ, V_P = 3.3V, V_N grounded.

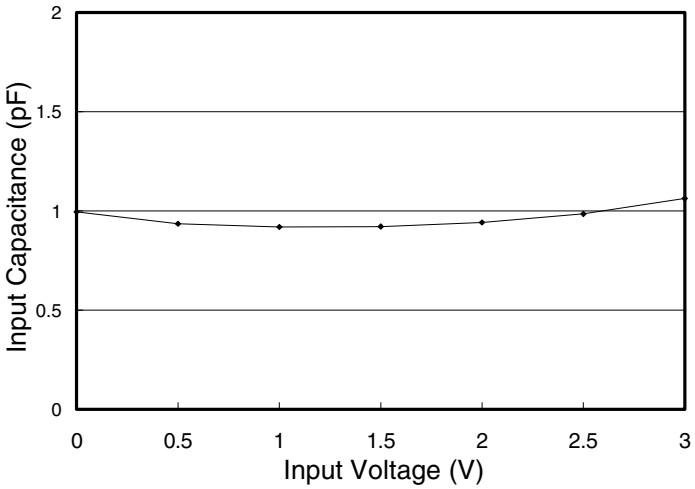
Note 4: Standard IEC 61000-4-2 with $C_{Discharge}$ = 150pF, $R_{Discharge}$ = 330Ω, V_P = 3.3V, V_N grounded.

Note 5: These measurements performed with no external capacitor on V_P.

Note 6: Measured under pulsed conditions, pulse width = 0.7mS, maximum current = 1.5A.

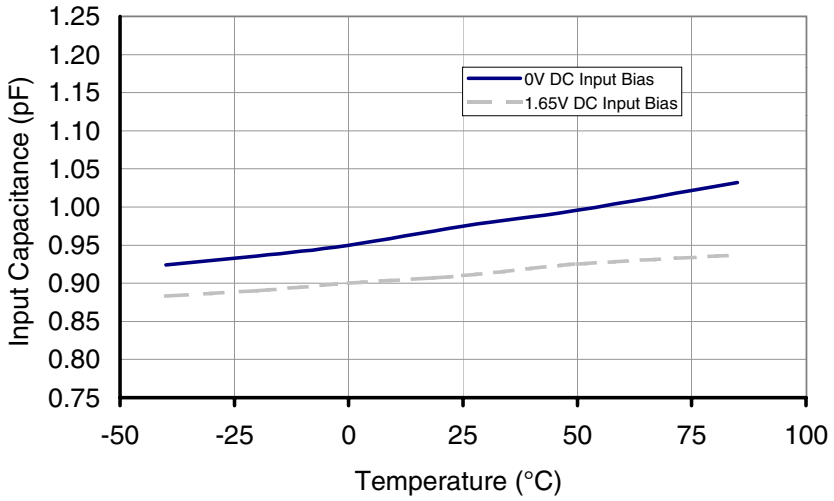
Performance Information

Input Channel Capacitance Performance Curves



Typical Variation of C_{IN} vs. V_{IN}

(f=1MHz, V_P = 3.3V, V_N = 0V, 0.1 µF chip capacitor between V_P and V_N, 25°C)



Typical Variation of C_{IN} vs. Temp

(f=1MHz, V_{IN}=30mV, V_P = 3.3V, V_N = 0V,
0.1 µF chip capacitor between V_P and V_N)

Performance Information (Cont'd)

Typical Filter Performance (nominal conditions unless specified otherwise, 50 Ohm Environment)

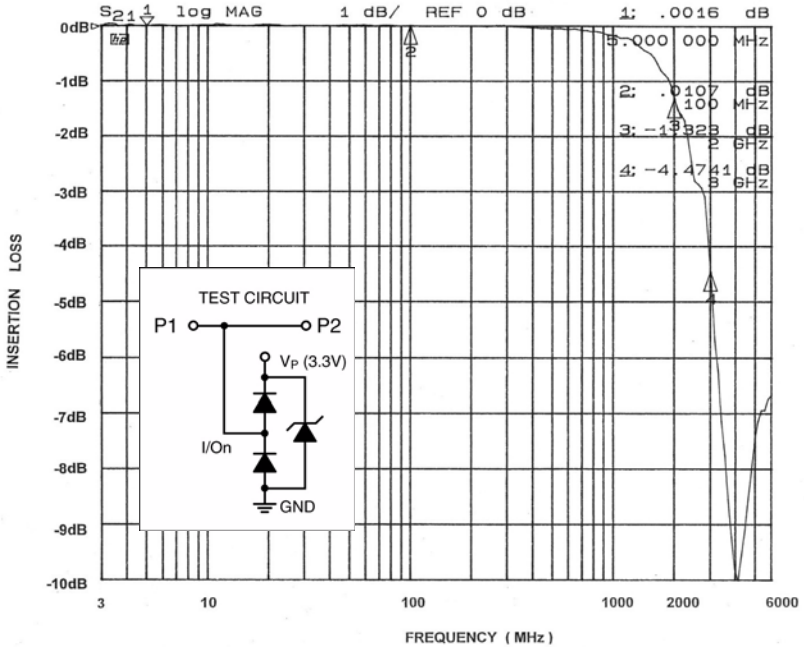


Figure 1. Insertion Loss (S21) VS. Frequency (0V DC Bias, V_P=3.3V)

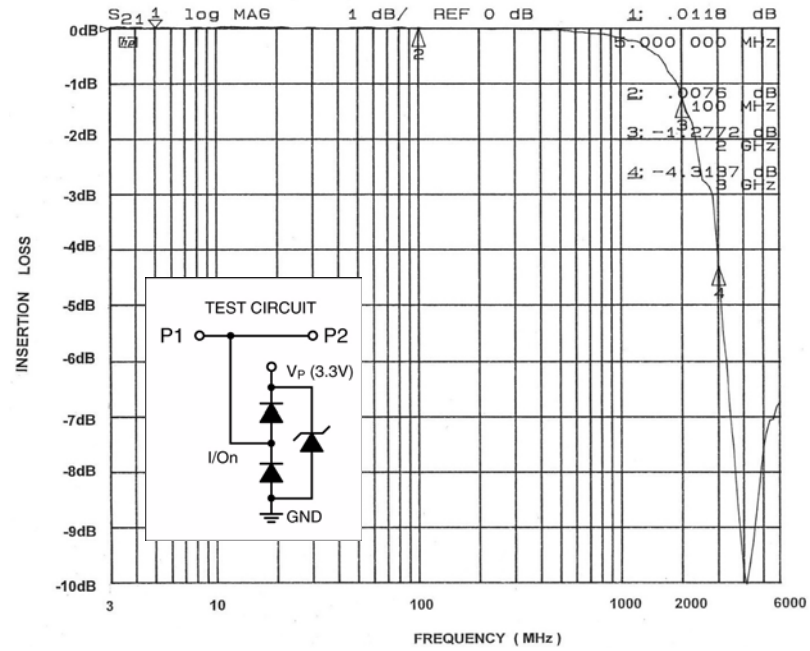


Figure 2. Insertion Loss (S21) VS. Frequency (2.5V DC Bias, V_P=3.3V)

Application Information

Design Considerations

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/ Ground rails as well as the signal trace segment between the signal input (typically a connector) and the ESD protection device. Refer to Figure 3, which illustrates an example of a positive ESD pulse striking an input channel. The parasitic series inductance back to the power supply is represented by L_1 and L_2. The voltage V_{CL} on the line being protected is:

$$V_{CL} = \text{Fwd voltage drop of } D_1 + V_{SUPPLY} + L_1 \times d(I_{ESD}) / dt + L_2 \times d(I_{ESD}) / dt$$

where I_{ESD} is the ESD current pulse, and V_{SUPPLY} is the positive supply voltage.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30 Amps in 1ns. Here $d(I_{ESD})/dt$ can be approximated by $\Delta I_{ESD}/\Delta t$, or $30/(1x10^{-9})$. So just 10nH of series inductance (L_1 and L_2 combined) will lead to a 300V increment in V_{CL}!

Similarly for negative ESD pulses, parasitic series inductance from the V_N pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

The CM1213 has an integrated Zener diode between V_P and V_N. This greatly reduces the effect of supply rail inductance L_2 on V_{CL} by clamping V_P at the breakdown voltage of the Zener diode. However, for the lowest possible V_{CL}, especially when V_P is biased at a voltage significantly below the Zener breakdown voltage, it is recommended that a 0.22µF ceramic chip capacitor be connected between V_P and the ground plane.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the V_P pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

Additional Information

See also California Micro Devices Application Note AP209, “Design Considerations for ESD Protection”, in the Applications section at www.calmicro.com.

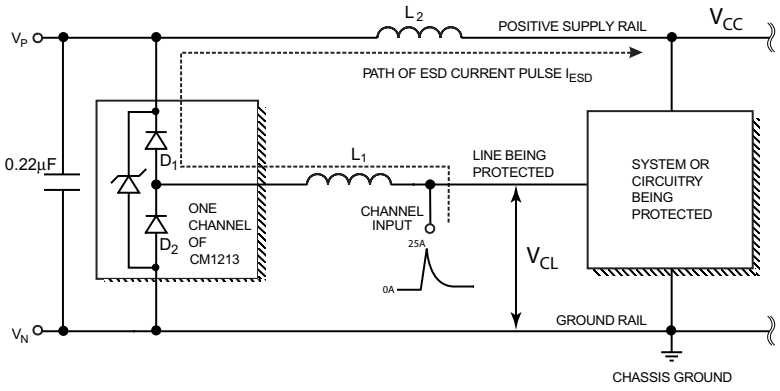


Figure 3. Application of Positive ESD Pulse between Input Channel and Ground

Mechanical Details

The CM1213 is available in SOT23-3, SOT143-4, SOT23-5, SOT23-6, MSOP-8, SOIC-8 and MSOP-10 packages with a lead-free finishing option.The various package drawings are presented below.

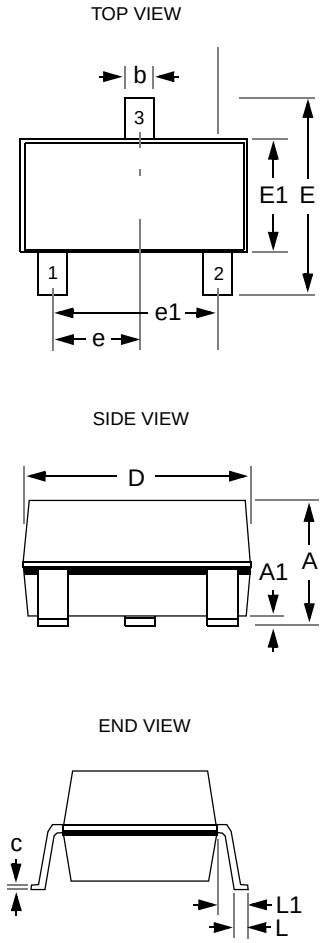
SOT23-3 Mechanical Specifications

Dimensions for CM1213-01ST/SO devices packaged in 3-pin SOT23 packages are presented below.

For complete information on the SOT23-3 package, see the California Micro Devices SOT23 Package Information document.

PACKAGE DIMENSIONS				
Package	SOT23-3 (JEDEC name is TO-236)			
Pins	3			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	0.89	1.12	0.0350	0.0441
A1	0.01	0.10	0.0004	0.0039
b	0.30	0.50	0.0118	0.0197
c	0.08	0.20	0.0031	0.0079
D	2.80	3.04	0.1102	0.1197
E	2.10	2.64	0.0827	0.1039
E1	1.20	1.40	0.0472	0.0551
e	0.95 BSC		0.0374 BSC	
e1	1.90 BSC		0.0748 BSC	
L	0.40	0.60	0.0157	0.0236
L1	0.54 REF		0.0213 REF	
# per tape and reel	3000 pieces			
Controlling dimension: millimeters				

Mechanical Package Diagrams



Package Dimensions for SOT23-3.

Mechanical Details (cont'd)

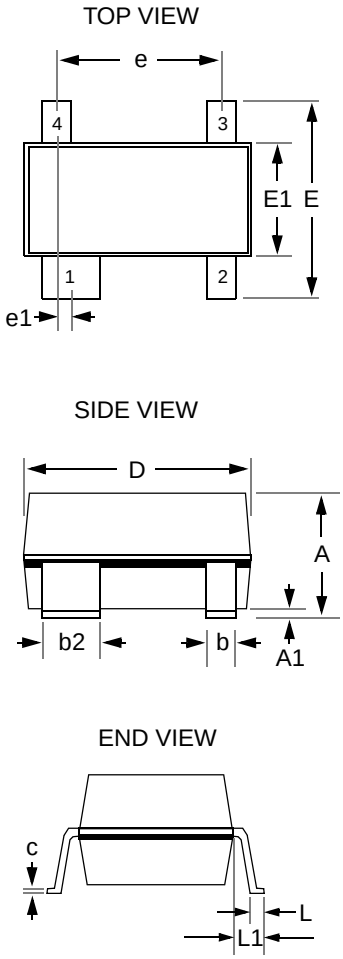
SOT143 Mechanical Specifications

Dimensions for CM1213-02SS/SR devices packaged in 4-pin SOT143 packages are presented below.

For complete information on the SOT143 package, see the California Micro Devices SOT143 Package Information document.

PACKAGE DIMENSIONS				
Package	SOT143			
Pins	4			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	0.80	1.22	0.031	0.048
A1	0.05	0.15	0.002	0.006
b	0.30	0.50	0.012	0.019
b2	0.76	0.89	0.030	0.035
c	0.08	0.20	0.003	0.008
D	2.80	3.04	0.110	0.119
E	2.10	2.64	0.082	0.103
E1	1.20	1.40	0.047	0.055
e	1.92 BSC		0.075 BSC	
e1	0.20 BSC		0.008 BSC	
L	0.4	0.6	0.016	0.024
L1	0.54 REF		0.021 REF	
# per tape and reel	3000 pieces			
Controlling dimension: millimeters				

Mechanical Package Diagrams



Package Dimensions for SOT143.

Mechanical Details (cont'd)

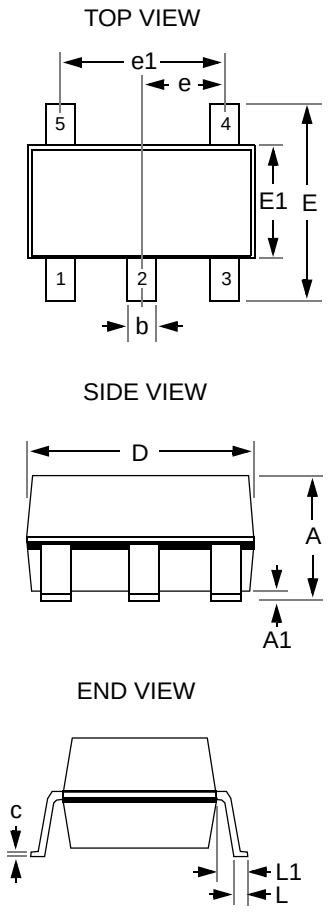
SOT23-5 Mechanical Specifications

Dimensions for CM1213-02ST/SO devices packaged in 5-pin SOT23 packages are presented below.

For complete information on the SOT23-5 package, see the California Micro Devices SOT23 Package Information document.

PACKAGE DIMENSIONS				
Package	SOT23-5 (JEDEC name is MO-178)			
Pins	5			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	--	1.45	--	0.0571
A1	0.00	0.15	0.0000	0.0059
b	0.30	0.50	0.0118	0.0197
c	0.08	0.22	0.0031	0.0087
D	2.75	3.05	0.1083	0.1201
E	2.60	3.00	0.1024	0.1181
E1	1.45	1.75	0.0571	0.0689
e	0.95 BSC		0.0374 BSC	
e1	1.90 BSC		0.0748 BSC	
L	0.30	0.60	0.0118	0.0236
L1	0.60 REF		0.0236 REF	
# per tape and reel	3000 pieces			
Controlling dimension: millimeters				

Mechanical Package Diagrams



Package Dimensions for SOT23-5.

Mechanical Details (cont'd)

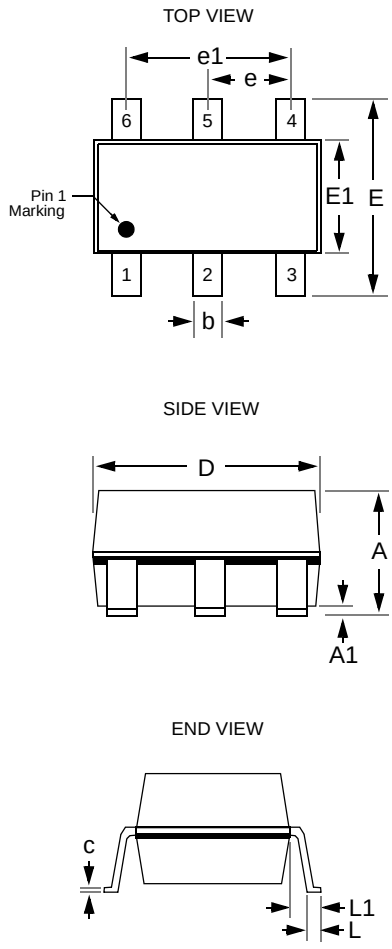
SOT23-6 Mechanical Specifications

CM1213-04ST/SO devices are packaged in 6-pin SOT23 packages. Dimensions are presented below.

For complete information on the SOT23-6 package, see the California Micro Devices SOT23 Package Information document.

PACKAGE DIMENSIONS				
Package	SOT23-6 (JEDEC name is MO-178)			
Pins	6			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	--	1.45	--	0.0571
A1	0.00	0.15	0.0000	0.0059
b	0.30	0.50	0.0118	0.0197
c	0.08	0.22	0.0031	0.0087
D	2.75	3.05	0.1083	0.1201
E	2.60	3.00	0.1024	0.1181
E1	1.45	1.75	0.0571	0.0689
e	0.95 BSC		0.0374 BSC	
e1	1.90 BSC		0.0748 BSC	
L	0.30	0.60	0.0118	0.0236
L1	0.60 REF		0.0236 REF	
# per tape and reel	3000 pieces			
Controlling dimension: millimeters				

Mechanical Package Diagrams



Package Dimensions for SOT23-6.

Mechanical Details

SOIC-8 Mechanical Specifications

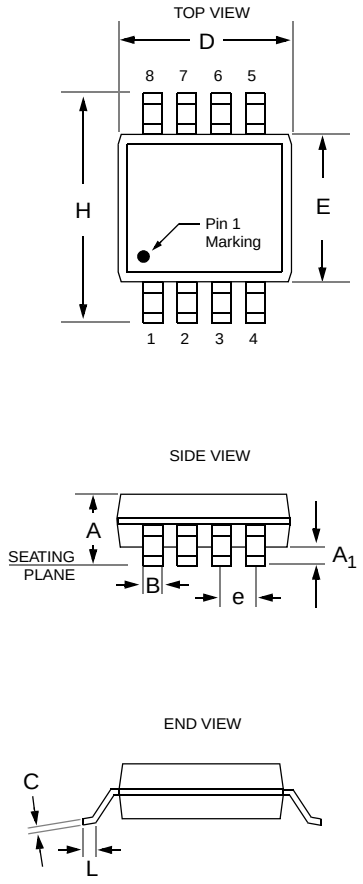
Dimensions for CM1213-06SN/SM devices packaged in 8-pin SOIC packages are presented below.

For complete information on the SOIC-8 package, see the California Micro Devices SOIC Package Information document.

PACKAGE DIMENSIONS				
Package	SOIC			
Pins	8			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.19	0.150	0.165
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
# per tube	100 pieces*			
# per tape and reel	2500 pieces			
Controlling dimension: inches				

* This is an approximate number which may vary.

Mechanical Package Diagrams



Package Dimensions for SOIC-8

Mechanical Details

MSOP-8 Mechanical Specifications:

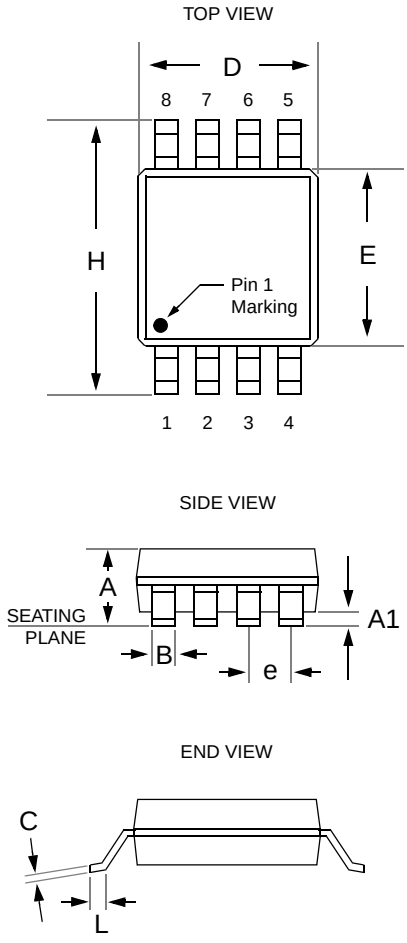
CM1213-06MS/MR devices are packaged in 8-pin MSOP packages. Dimensions are presented below.

For complete information on the MSOP-8 package, see the California Micro Devices MSOP Package Information document.

PACKAGE DIMENSIONS				
Package	MSOP			
Pins	8			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	0.87	1.17	0.034	0.046
A1	0.05	0.25	0.002	0.010
B	0.30 (typ)		0.012 (typ)	
C	0.18		0.007	
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.65 BSC		0.025 BSC	
H	4.78	4.98	0.188	0.196
L	0.52	0.54	0.017	0.025
# per tube	80 pieces*			
# per tape and reel	4000 pieces			
Controlling dimension: inches				

* This is an approximate amount which may vary.

Mechanical Package Diagrams



Package Dimensions for MSOP-8

Mechanical Details (cont'd)

MSOP-10 Mechanical Specifications

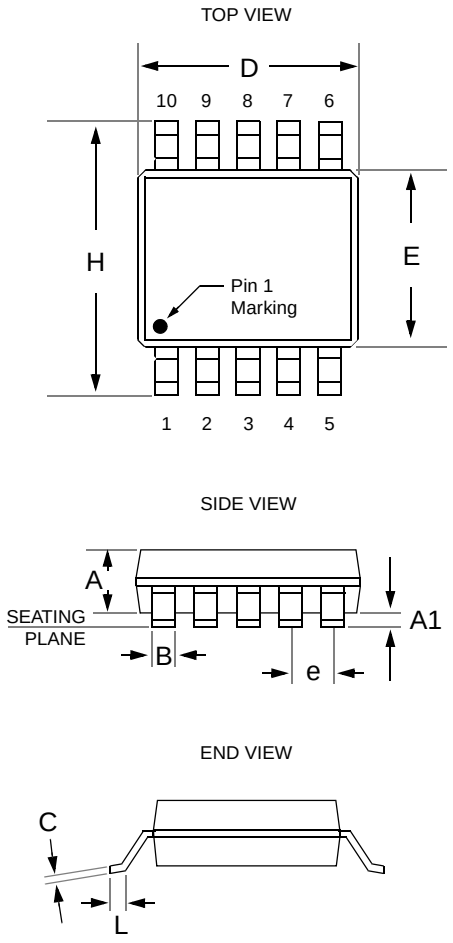
CM1213-08MS/MR devices are packaged in 10-pin MSOP packages. Dimensions are presented below.

For complete information on the MSOP-10 package, see the California Micro Devices MSOP Package Information document.

PACKAGE DIMENSIONS				
Package	MSOP			
Pins	10			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	0.75	0.95	0.028	0.038
A1	0.05	0.15	0.002	0.006
B	0.18	0.40	0.006	0.016
C	0.18		0.007	
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.50 BSC		0.0196 BSC	
H	4.76	5.00	0.187	0.197
L	0.40	0.70	0.0137	0.029
# per tube	80 pieces*			
# per tape and reel	4000			
Controlling dimension: inches				

* This is an approximate number which may vary.

Mechanical Package Diagrams



Package Dimensions for MSOP-10