Preliminary Data Sheet, DS3, July 2003

DuSLIC

Dual Channel Subscriber Line Interface Concept

PEB 3264, Version 1.4

PEB 3265, Version 1.5

PEB 4264/-2, Version 1.1/1.2

PEB 4364, Version 1.1/1.2

PEB 4265/-2, Version 1.1/1.2

PEB 4365, Version 1.2

PEB 4266, Version 1.2

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Edition 2003-07-11

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
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Preliminary Data Sheet

Revision History: 2003-07-11 DS3

Previous Version: DS2

Page	Subjects (major changes since last revision)
Title	Product name corrected to *Dual Channel Subscriber Line Interface Concept*
all	PEB 3265 version changed from 1.2 to 1.5
all	PEB 4264/-2 and PEB 4265/-2: version 1.2 added
all	PEB 4266 version changed from 1.1 to 1.2
all	PEB 3264 version changed from 1.2 to 1.4
all	Bit VRTLIM renamed to VTRLIM
all	Bit VRTLIM-M renamed to VTRLIM-M
all	New SLICs TSLIC-E and TSLIC-S added
all	New SLICOFI-2 (Version 1.5 only) package P-TQFP-64-1 added
all	New package P-VQFN-48-4 for SLIC-S/-S2, SLIC-E/-E2 and SLIC-P added
all	Former chapter 2 "Pin Descriptions" removed. See updated device data sheets.
Page 18	**“Overview” on Page 18**: Chapter reworked, tables for codec and SLIC chips added.
Page 23	**“Features” on Page 23**: ITU-T Recommendation G.712 added
Page 25	**“Logic Symbols” on Page 25**: Logic symbol for SLIC-E/-E2 Version 1.2 added.
Page 32	**“Block Diagram SLICOFI-2/-2S” on Page 32**: block diagrams of SLIC devices removed.
Page 33	**Figure 10 "Signal Paths – DC Feeding" on Page 33**: C_{ITA} (C_{ITB}) renamed to C_{ITACA} (C_{ITACB}).
Page 38	**Table 4 "DC Characteristics" on Page 38**: V_{LIM} changed from 50 V to 72 V.
Page 42	**Figure 19 "Signal Paths – AC Transmission" on Page 42**: C_{ITA} (C_{ITB}) renamed to C_{ITACA} (C_{ITACB}).
Page 50	**“Internal Balanced Ringing via SLICs” on Page 50**: $V_{DROP,RT}$ renamed to $V_{DROP,TR}$, $V_{RT,RMS}$ renamed to $V_{TR,RMS}$, $V_{RT0,RMS}$ renamed to $V_{TR0,RMS}$
Page 61	**Figure 30 "Bellcore On-Hook Caller ID Physical Layer Transmission" on Page 61**: note added.
Page 61	**“Caller ID Buffer Handling of SLICOFI-2” on Page 61**: description for listing item (9) changed
Page 64	**“Non Linear Processor (NLP) in DuSLIC-E/-E2/-P” on Page 64** added.

Page 66	**“MIPS Requirements for EDSP Capabilities” on Page 66** updated with NLP examples.
Page 68	**“Three-party Conferencing in DuSLIC-E/-E2/-P” on Page 68**: sentence about Multi-party Conferencing added
Page 84	**“Hardware and Power On Reset” on Page 84**: reset routine duration changed to 1.5 ms.
Page 85	**Figure 36 "DuSLIC Reset Sequence" on Page 85**: textual description changed.
Page 86	**Table 17**, **“Default DC and AC Values” on Page 86**: L_X and L_R changed.
Page 88	**“Recommended Procedure for Reading the Interrupt Registers” on Page 88** added.
Page 90	**“Power Management and Operating Modes” on Page 90**: Power dissipation values and description updated.
Page 94	**“Integrated Test and Diagnostic Functions (ITDF)” on Page 94**: ITDF is now also available for SLICOFI-2S.
Page 94	**Figure 3.8.1.2 "DuSLIC Line Testing" on Page 94**: description on line testing capability modified.
Page 97	**“Using the Level Metering Integrator” on Page 97**: timing for LM-OK bit added.
Page 99	**Figure 44**, **“Timing LM-OK Bit” on Page 99**: 1 ms delay time for SLICOFI-2 Version 1.5 added.
Page 101	**Table 20 "KINTDC Setting Table" on Page 101**: description about DuSLICOS settings added below.
Page 113	**“Capacitance Measurements” on Page 113**: note on offset calibration added at the end of the chapter.
Page 116	**“Line Capacitance Measurements Ring and Tip to GND” on Page 116**: description of last list item in section "Calculating parameter values" modified, description in table of section "Program Sequence" modified
Page 137	**Chapter 4.2.3**, **Operation with IOM-2 TE Devices (1.536 MHz)** added.
Page 139	**“TIP/RING Interface” on Page 139**: content removed - see device data sheets for detailed information.
Page 144	**“SOP Command” on Page 144**: note on empty register bits added
Page 151	Register **XCR**: Description for bit ASYNCH-R changed
Page 152	Register **INTREG1**, bits HOOK and GNDK: description changes
Page 154	Register **INTREG2**: reset value changed from 20_H to $4F_H$, description for bit RSTAT modified
Page 167	Register **BCR1**, bit SLEEP-EN: note added
Page 170	Register **BCR2**: description added fot bits UTDX-SRC and PDOT-DIS
Page 177	Register **BCR5**, bit DTMF-SRC: description added
Page 179	Register **DSCR**, bit PTG: description added
Page 203	**“COP Command” on Page 203**: note on empty register bits added

Page 205	**Table 35 "CRAM Coefficients" on Page 205**: TTX Slope extended by nibbles 6 and 7
Page 207	**“POP Command” on Page 207**: note on the necessity of immediate programming added
Page 207	**“Sequence for POP Register Programming” on Page 207** added (because added NLP coefficients)
Page 208	**“POP Register Overview” on Page 208**: NLP coefficients added
Page 213	**“POP Register Description” on Page 213**: NLP coefficients added
Page 233	**Table 53 "Range of DeltaPLEC" on Page 233**: "0x80 - no detection" added.
Page 248	Register **CIS/LEC-MODE**: description added for bit UTDX-SUM and note on bit 3 added.
Page 258	**“Recommended NLP Coefficients” on Page 258** added
Page 266	**“SOP Command” on Page 266**: note on empty register bits added
Page 273	Register XCR: Description for bit ASYNCH-R changed
Page 278	Register **LMRES1**: bits added.
Page 278	Register **LMRES2**: bits added.
Page 287	Register **BCR1**: bits added.
Page 295	Register **DSCR**, bit PTG: description added
Page 297	Register **LMCR1**: bits added.
Page 299	Register **LMCR2**: bits added.
Page 301	Register **LMCR3**: bits added.
Page 315	**“COP Command” on Page 315**: note on empty register bits added
Page 318	**Table 73 "CRAM Coefficients" on Page 318**: TTX slope extended by nibbles 6 and 7
Page 325	**“Electrical Characteristics” on Page 325**: SLIC and *SLICOFI-2x* data removed - for detailed information see device data sheets.
Page 326	**Table 76**, **“AC Transmission” on Page 326**: Symbol V_{RT} renamed to V_{TR}
Page 331	AC Transmission Characteristics: Values for Distortion and associated figures changed
Page 342	**“Input/Output Waveform for AC Tests” on Page 342** added.
Page 344	PCM interface timings **“Single-Clocking Mode” on Page 344** and **“Double-Clocking Mode” on Page 346**: FSC hold time (t_{FSC_h}) renamed to FSC hold time 1 (t_{FSC_h1}), FSC hold time 2 (t_{FSC_h2}) added, formula of max. value for TCA/B delay time off (t_{dTCoff}) modified
Page 349	IOM-2 interface timings **“Single-Clocking Mode” on Page 349** and **“Double-Clocking Mode” on Page 351**: FSC hold time (t_{FSC_h}) renamed to FSC hold time 1 (t_{FSC_h1}), FSC hold time 2 (t_{FSC_h2}) added, parameters and timing of pin DU modified Period PCLK (t_{PCLK}) for double clocking: formula for typ. value modified.

Page 353	**Figure 90, “Internal (balanced and unbalanced) Ringing with SLIC-P” on Page 353**: pin TS2/CS changed to TS2/$\overline{CS}$, illustration of connection between pins C3 and IO2A modified, SLIC supply voltages added, arrangement of diodes D1 and D2 modified.
Page 355	**Table 79, “External Components in Application Circuit DuSLIC-E/-E2/-S/-S2/-P” on Page 355**: tolerance of R_{STAB} and R_{PROT} changed to 1%, footnote added.
Page 357	**Figure 92, “External Unbalanced Ringing with SLIC-E/-E2 or SLIC-S/-S2” on Page 357**: pin TS2/CS changed to TS2/$\overline{CS}$, illustration of connection between pins C3 and IO2A modified,SLIC supply voltages added
Page 359	**Figure 94, “External Unb. Ringing (Long Loops) with SLIC-E/-E2 or SLIC-S/-S2” on Page 359**: pin TS2/CS changed to TS2/$\overline{CS}$, illustration of connection between pins C3 and IO2A modified, SLIC supply voltages added
Page 363	**Figure 97, “SLIC-S/-S2, SLIC-E/-E2, SLIC-P (PEB 426x)” on Page 363**: note on SLIC clockwise pin counting added, security warning for all SLIC packages added

Table of Contents

		Page
1	**Overview**	18
1.1	Features	23
1.2	Typical Applications	24
1.3	Logic Symbols	25
2	**Functional Description**	29
2.1	Functional Overview	29
2.1.1	Basic Functions of all DuSLIC Chip Sets	29
2.1.2	Additional Functions of the DuSLIC-E/-E2/-P Chip Sets	30
2.2	Block Diagram SLICOFI-2/-2S	32
2.3	DC Feeding	33
2.3.1	DC Characteristic Feeding Zones	34
2.3.2	Constant Current Zone	35
2.3.3	Resistive Zone	36
2.3.4	Constant Voltage Zone	37
2.3.5	Programmable Voltage and Current Range: DC Characteristics	38
2.3.6	SLIC Power Dissipation	39
2.3.7	Necessary Voltage Reserve	40
2.3.8	Extended Battery Feeding	41
2.4	AC Transmission Characteristics	42
2.4.1	Transmit Path	43
2.4.2	Receive Path	43
2.4.3	Matching	44
2.5	Ringing	45
2.5.1	Ringer Load	45
2.5.2	Ring Trip	45
2.5.3	Ringing Methods	46
2.5.4	DuSLIC Ringing Options	47
2.5.5	Internal Balanced Ringing via SLICs	50
2.5.6	Internal Unbalanced Ringing with SLIC-P	51
2.5.7	External Unbalanced Ringing	52
2.6	Signaling (Supervision)	52
2.7	Metering	54
2.7.1	Metering by 12/16 kHz Sinusoidal Bursts	54
2.7.2	Metering by Polarity Reversal	55
2.7.2.1	Soft Reversal	55
2.8	DuSLIC Enhanced Signal Processing Capabilities	56
2.8.1	DTMF Generation and Detection	57
2.8.2	Caller ID Generation in DuSLIC-E/-E2/-P	59
2.8.2.1	Caller ID Buffer Handling of SLICOFI-2	61
2.8.3	Line Echo Cancellation in DuSLIC-E/-E2/-P	63
2.8.4	Non Linear Processor (NLP) in DuSLIC-E/-E2/-P	64
2.8.5	Universal Tone Detection in DuSLIC-E/-E2/-P	65

Table of Contents **Page**

2.8.6 MIPS Requirements for EDSP Capabilities . . . 66
2.9 Message Waiting Indication in DuSLIC-E/-E2/-P . . . 67
2.10 Three-party Conferencing in DuSLIC-E/-E2/-P . . . 68
2.10.1 Conferencing Modes . . . 69
2.11 16 kHz Mode on PCM Highways . . . 71

3 Operational Description . . . 74
3.1 Overview of all DuSLIC Operating Modes . . . 74
3.2 Operating Modes for the DuSLIC-S/-S2/-SE/-SE2 Chip Set . . . 78
3.3 Operating Modes for the DuSLIC-E/-E2/-ES/-ES2 Chip Set . . . 80
3.4 Operating Modes for the DuSLIC-P Chip Set . . . 82
3.5 Reset Mode and Reset Behavior . . . 84
3.5.1 Hardware and Power On Reset . . . 84
3.5.2 Software Reset . . . 86
3.6 Interrupt Handling . . . 88
3.6.1 Recommended Procedure for Reading the Interrupt Registers . . . 88
3.7 Power Management and Operating Modes . . . 90
3.7.1 *SLICOFI-2x* Power Dissipation . . . 91
3.7.2 SLIC Power Dissipation . . . 91
3.7.2.1 Power Down Modes . . . 91
3.7.2.2 Active Modes . . . 92
3.7.2.3 Ringing Mode . . . 93
3.8 Integrated Test and Diagnostic Functions (ITDF) . . . 94
3.8.1 Introduction . . . 94
3.8.1.1 Conventional Line Testing . . . 94
3.8.1.2 DuSLIC Line Testing . . . 94
3.8.2 Diagnostics . . . 95
3.8.2.1 Line Test Capabilities . . . 95
3.8.2.2 Integrated Signal Sources . . . 95
3.8.2.3 Result Register Data Format . . . 97
3.8.2.4 Using the Level Metering Integrator . . . 97
3.8.2.5 DC Level Metering . . . 100
3.8.2.6 AC Level Meter . . . 105
3.8.2.7 Level Meter Threshold . . . 108
3.8.2.8 Current Offset Error Compensation . . . 110
3.8.2.9 Loop Resistance Measurements . . . 111
3.8.2.10 Line Resistance Tip/GND and Ring/GND . . . 113
3.8.2.11 Capacitance Measurements . . . 113
3.8.2.12 Line Capacitance Measurements Ring and Tip to GND . . . 116
3.8.2.13 Foreign- and Ring Voltage Measurements . . . 116
3.9 Signal Path and Test Loops . . . 119
3.9.1 AC Test Loops . . . 119
3.9.2 DC Test Loops . . . 121

Table of Contents **Page**

4 Interfaces 122
4.1 PCM Interface with a Serial Microcontroller Interface 122
4.1.1 PCM Interface 122
4.1.2 Control of the Active PCM Channels 126
4.1.3 Serial Microcontroller Interface 127
4.2 The IOM-2 Interface 129
4.2.1 IOM-2 Interface Monitor Transfer Protocol 133
4.2.2 *SLICOFI-2x* Identification Command 137
4.2.3 Operation with IOM-2 TE Devices (1.536 MHz) 137
4.3 TIP/RING Interface 139

5 *SLICOFI-2x* Command Structure and Programming 140
5.1 Overview of Commands 143
5.2 SLICOFI-2 Command Structure and Programming 144
5.2.1 SOP Command 144
5.2.1.1 SOP Register Overview 144
5.2.1.2 SOP Register Description 149
5.2.2 COP Command 203
5.2.2.1 CRAM Programming Ranges 206
5.2.3 POP Command 207
5.2.3.1 Sequence for POP Register Programming 207
5.2.3.2 POP Register Overview 208
5.2.3.3 POP Register Description 213
5.2.3.4 Recommended NLP Coefficients 258
5.2.4 IOM-2 Interface Command/Indication Byte 260
5.2.5 Programming Examples of the SLICOFI-2 262
5.2.5.1 Microcontroller Interface 262
5.2.5.2 IOM-2 Interface 263
5.3 SLICOFI-2S Command Structure and Programming 266
5.3.1 SOP Command 266
5.3.1.1 SOP Register Overview 266
5.3.1.2 SOP Register Description 271
5.3.2 COP Command 315
5.3.2.1 CRAM Programming Ranges 319
5.3.3 IOM-2 Interface Command/Indication Byte 320
5.3.4 Programming Examples of the SLICOFI-2S 322
5.3.4.1 Microcontroller Interface 322
5.3.4.2 IOM-2 Interface 323

6 Electrical Characteristics 325
6.1 AC Transmission DuSLIC 325
6.1.1 Frequency Response 334
6.1.2 Gain Tracking (Receive or Transmit) 335

Table of Contents **Page**

6.1.3 Group Delay . . . 336
6.1.4 Out-of-Band Signals at Analog Output (Receive) . . . 336
6.1.5 Out-of-Band Signals at Analog Input (Transmit) . . . 338
6.1.6 Total Distortion Measured with Sine Wave . . . 339
6.2 DC Characteristics . . . 341
6.3 DuSLIC Power Up . . . 342
6.4 DuSLIC Timing Characteristics . . . 342
6.4.1 Input/Output Waveform for AC Tests . . . 342
6.4.2 MCLK/FSC Timing . . . 343
6.4.3 PCM Interface Timing . . . 344
6.4.3.1 Single-Clocking Mode . . . 344
6.4.3.2 Double-Clocking Mode . . . 346
6.4.4 Microcontroller Interface Timing . . . 348
6.4.5 IOM-2 Interface Timing . . . 349
6.4.5.1 Single-Clocking Mode . . . 349
6.4.5.2 Double-Clocking Mode . . . 351

7 Application Circuits . . . 352
7.1 Internal Ringing (Balanced/Unbalanced) . . . 352
7.1.1 Circuit Diagrams Internal Ringing (Balanced & Unbalanced) . . . 353
7.1.2 Bill of Materials . . . 355
7.2 External Unbalanced Ringing with DuSLIC-E/-E2/-S/-S2/-P . . . 356
7.2.1 Circuit Diagrams External Unbalanced Ringing . . . 357
7.3 DuSLIC Layout Recommendations . . . 361

8 Package Outlines . . . 363

9 Terminology . . . 369

10 Index . . . 371

List of Figures

		Page
Figure 1	DuSLIC Chip Set	22
Figure 2	Logic Symbol: SLICOFI-2/-2S	25
Figure 3	Logic Symbol: SLIC-S/SLIC-S2 (V1.1, V1.2), SLIC-E/SLIC-E2 (V1.1)	26
Figure 4	Logic Symbol: SLIC-E/SLIC-E2 (V1.2)	26
Figure 5	Logic Symbol: SLIC-P	27
Figure 6	Logic Symbol: TSLIC-S/TSLIC-E	28
Figure 7	Line Circuit Functions in the DuSLIC-S/-S2	31
Figure 8	Line Circuit Functions in the DuSLIC-E/-E2/-P	31
Figure 9	Block Diagram: SLICOFI-2/-2S (PEB 3265, PEB 3264)	32
Figure 10	Signal Paths – DC Feeding	33
Figure 11	DC Feeding Characteristic	34
Figure 12	Constant Current Zone	35
Figure 13	Resistive Zone	36
Figure 14	Constant Voltage Zone	37
Figure 15	DC Characteristics	38
Figure 16	Power Dissipation	39
Figure 17	TTX Voltage Reserve Schematic	40
Figure 18	DC Feeding Characteristics (ACTH, ACTR)	41
Figure 19	Signal Paths – AC Transmission	42
Figure 20	Signal Flow in Voice Channel (A)	43
Figure 21	Nyquist Diagram	44
Figure 22	Typical Ringer Loads of 1 and 5 REN used in USA	45
Figure 23	External Ringing Zero Crossing Synchronization	49
Figure 24	Balanced Ringing via SLIC-E/-E2, SLIC-S and SLIC-P	50
Figure 25	Unbalanced Ringing Signal	51
Figure 26	Teletax Injection and Metering	54
Figure 27	Soft Reversal (Example for Open Loop)	55
Figure 28	DuSLIC AC Signal Path	56
Figure 29	DuSLIC EDSP Signal Path	56
Figure 30	Bellcore On-Hook Caller ID Physical Layer Transmission	61
Figure 31	Line Echo Cancellation Unit Block Diagram	63
Figure 32	UTD Functional Block Diagram	65
Figure 33	MWI Circuitry with Glow Lamp	67
Figure 34	Timing Diagram	68
Figure 35	Conference Block for One DuSLIC Channel	69
Figure 36	DuSLIC Reset Sequence	85
Figure 37	Reading Interrupt Registers	89
Figure 38	Typical SLIC Power Dissipation	92
Figure 39	DuSLIC Line Testing	94
Figure 40	Level Metering Block Diagram	96
Figure 41	Single Measurement Sequence (AC & DC Level Metering)	97
Figure 42	Continuous Measurement Sequence (DC Level Metering)	98

List of Figures

Page

Figure 43 Continuous Measurement Sequence (AC Level Metering) 98
Figure 44 Timing LM-OK Bit. 99
Figure 45 Example Resistance Measurement 111
Figure 46 Differential Resistance Measurement 112
Figure 47 Capacitance Measurement 114
Figure 48 Foreign Voltage Measurement Principle 117
Figure 49 AC Test Loops DuSLIC-E/-E2/-P/-ES/-ES2. 119
Figure 50 AC Test Loops DuSLIC-S/-S2/-SE/-SE2 120
Figure 51 DC Test Loops DuSLIC 121
Figure 52 General PCM Interface Timing 123
Figure 53 Setting the Slopes in Register PCMC1 125
Figure 54 Serial Microcontroller Interface Write Access 128
Figure 55 Serial Microcontroller Interface Read Access 128
Figure 56 IOM-2 I/F Timing for up to 16 Voice Channels (Per 8 kHz Frame) . . 130
Figure 57 IOM-2 Interface Timing (DCL = 4096 kHz, Per 8 kHz Frame) 131
Figure 58 IOM-2 Interface Timing (DCL = 2048 kHz, Per 8 kHz Frame) 131
Figure 59 IOM-2 Interface Monitor Transfer Protocol 133
Figure 60 State Diagram of the *SLICOFI-2x* Monitor Transmitter 135
Figure 61 State Diagram of the *SLICOFI-2x* Monitor Receiver 136
Figure 62 PCM/mC Mode used for IOM-2 TE Interface at 1.536 MHz. 138
Figure 63 Example for Switching Between Different Ring Offset Voltages 187
Figure 64 Example for UTD Recognition Timing 256
Figure 65 Example for UTD Tone End Detection Timing. 258
Figure 66 Waveform of Programming Example SOP-Write to Channel 0 262
Figure 67 Waveform of Programming Example SOP Read from Channel 0 . . . 263
Figure 68 Example for Switching Between Different Ring Offset Voltages 303
Figure 69 Waveform of Programming Example SOP Write to Channel 0 322
Figure 70 Waveform of Programming Example SOP Read from Channel 0 . . . 322
Figure 71 Signal Definitions Transmit, Receive 325
Figure 72 Overload Compression 333
Figure 73 Frequency Response Transmit 334
Figure 74 Frequency Response Receive. 334
Figure 75 Gain Tracking Receive. 335
Figure 76 Gain Tracking Transmit 335
Figure 77 Group Delay Distortion Receive and Transmit. 336
Figure 78 Out-of-Band Signals at Analog Output (Receive) 337
Figure 79 Out-of-Band Signals at Analog Input (Transmit) 338
Figure 80 Total Distortion Transmit (LX = 0 dBr) 339
Figure 81 Total Distortion Receive (LR = –7 dBr) 339
Figure 82 Total Distortion Receive (LR = 0 dBr) 340
Figure 83 Waveform for AC Tests 342
Figure 84 MCLK/FSC-Timing. 343

List of Figures

Page

Figure 85 PCM Interface Timing – Single-Clocking Mode 344
Figure 86 PCM Interface Timing – Double-Clocking Mode 346
Figure 87 Microcontroller Interface Timing. 348
Figure 88 IOM-2 Interface Timing – Single-Clocking Mode 349
Figure 89 IOM-2 Interface Timing – Double-Clocking Mode 351
Figure 90 Internal (balanced and unbalanced) Ringing with SLIC-P 353
Figure 91 Internal (balanced) Ringing with SLIC-E/-E2 or SLIC-S/-S2 354
Figure 92 External Unbalanced Ringing with SLIC-E/-E2 or SLIC-S/-S2. 357
Figure 93 External Unbalanced Ringing with SLIC-P 358
Figure 94 External Unb. Ringing (Long Loops) with SLIC-E/-E2 or SLIC-S/-S2 359
Figure 95 External Unbalanced Ringing (Long Loops) with SLIC-P 360
Figure 96 DuSLIC Layout Recommendation 362
Figure 97 SLIC-S/-S2, SLIC-E/-E2, SLIC-P (PEB 426x) 363
Figure 98 SLIC-S/-S2, SLIC-E/-E2, SLIC-P (PEB426x). 364
Figure 99 TSLIC-S (PEB 4364) 365
Figure 100 TSLIC-E (PEB 4365) 366
Figure 101 *SLICOFI-2x* (PEB 3265, PEB 3264) 367
Figure 102 *SLICOFI-2x* (PEB 3265, PEB 3264) 368

List of Tables

		Page
Table 1	Codec Feature Overview	19
Table 2	SLIC Feature Overview	19
Table 3	DuSLIC Chip Sets Presented in this Data Sheet	20
Table 4	DC Characteristics	38
Table 5	Ringing Options with SLIC-S, SLIC-E/-E2 and SLIC-P	47
Table 6	Performance Characteristics of the DTMF Decoder Algorithm	58
Table 7	FSK Modulation Characteristics	60
Table 8	MIPS Requirements	66
Table 9	Conferencing Modes: Receive Channels	69
Table 10	Conferencing Modes: Transmit Channels	70
Table 11	Possible Modes in PCM/∝C Interface Mode: Receive Channels	72
Table 12	Possible Modes in PCM/∝C Interface Mode: Transmit Channels	72
Table 13	Overview of all DuSLIC Operating Modes	74
Table 14	DuSLIC-S/-S2/-SE/-SE2 Operating Modes	78
Table 15	DuSLIC-E/-E2/-ES/-ES2 Operating Modes	80
Table 16	DuSLIC-P Operating Modes	82
Table 17	Default DC and AC Values	86
Table 18	Level Metering Result Value Range	97
Table 19	Selecting DC Level Meter Path	100
Table 20	KINTDC Setting Table	101
Table 21	NSamples Setting Table	102
Table 22	Level Meter Results with and without Integrator Function	103
Table 23	Selecting AC Level Meter Path	105
Table 24	KINTAC Setting Table	106
Table 25	KTG Setting Table	108
Table 26	Threshold Setting Table	109
Table 27	Measurement Input Selection	117
Table 28	*SLICOFI-2x* PCM Interface Configuration	124
Table 29	Active PCM Channel Configuration Bits	126
Table 30	IOM-2 Time Slot Assignment	132
Table 31	M2, M1, M0: General Operating Mode	141
Table 32	Valid DTMF Keys (Bit DTMF-KEY4 = 1)	155
Table 33	DTMF Keys	179
Table 34	Typical Usage for the three Ring Offsets	187
Table 35	CRAM Coefficients	205
Table 36	CRAM Programming Ranges	206
Table 37	Range of $T_{POW-LPF}$	215
Table 38	Range of $Twist_{acc}$	216
Table 39	Range of $T_{POW-LPS}$	217
Table 40	Range of PowBN-LEV-X	218
Table 41	Range of PowBN-LEV-R	220
Table 42	Range of TBN-INC	221

List of Tables

		Page
Table 43	Range of TBN-DEC	223
Table 44	Ranges of GDTMF[dB] dependent on “e”	224
Table 45	Example for DTMF-GAIN Calculation	224
Table 46	Range of PowBN-MAX	225
Table 47	Range for DeltaBN-ADJ	226
Table 48	Range of ERLLRE-MIN	227
Table 49	Range of ERLLRE-EST	228
Table 50	Range of SSD-LEV-X	230
Table 51	Range of PowLECR	231
Table 52	Range of SSD-LEV-R	232
Table 53	Range of DeltaPLEC	233
Table 54	Range of DeltaSD-LEV-BN	234
Table 55	Examples for DeltaQ	235
Table 56	Range of DeltaSD-LEV-RE	236
Table 57	Ranges of GLEC-XI[dB] Dependent on “e”	237
Table 58	Example for LEC-GAIN-XI Calculation	237
Table 59	Range of tSD-OT-DT	238
Table 60	Ranges of GLEC-RI[dB] Dependent on “e”	239
Table 61	Example for LEC-GAIN-RI Calculation	239
Table 62	Range of TERL-LIN-LP	240
Table 63	Ranges of GLEC-X0[dB] Dependent on “e”	241
Table 64	Example for LEC-GAIN-X0 Calculation	241
Table 65	Range of TERL-LEC-LP	242
Table 66	Range of DeltaCT-LEV-RE	243
Table 67	Range of LevCIS	245
Table 68	UTD Inband/Outband Attenuation	254
Table 69	Recommended NLP Coefficients	259
Table 70	M2, M1, M0: General Operating Mode	260
Table 71	DTMF Keys	295
Table 72	Typical Usage for the three Ring Offsets	303
Table 73	CRAM Coefficients	318
Table 74	CRAM Programming Ranges	319
Table 75	M2, M1, M0: General Operating Mode	320
Table 76	AC Transmission	326
Table 77	Group Delay Absolute Values: Signal level 0 dBm0	336
Table 78	DC Characteristics	341
Table 79	External Components in Application Circuit DuSLIC-E/-E2/-S/-S2/-P	355

Preface

This Preliminary Data Sheet describes the family of DuSLIC chip sets. Each chip set comprises a dual channel *SLICOFI-2x* codec and two single- or one dual-channel SLICs. For more DuSLIC related documents, please see our webpage at http://www.infineon.com/duslic.

To simplify matters, the following synonyms are used:

SLICOFI-2x: Synonym used for all codec versions SLICOFI-2/-2S

SLIC: Synonym used for all SLIC versions SLIC-S/-S2, TSLIC-S, SLIC-E/-E2,

TSLIC-E and SLIC-P.

Attention: The TSLIC-S (PEB 4364) and TSLIC-E (PEB 4365) chips are dual channel versions of the SLIC-S (PEB 4364) and SLIC-E (PEB 4365) with identical technical specifications for each channel. Therefore whenever SLIC-S or SLIC-E are mentioned in the specification, also TSLIC-S and TSLIC-E can be deployed.

Organization of this Document

- **Chapter 1, Overview**
  A general description of the chip set, the key features, and some typical applications.
- **Chapter 2, Functional Description**
  The main functions of the chip set are presented with functional block diagrams.
- **Chapter 3, Operational Description**
  A brief description of the operating modes, the power management, and the integrated test and diagnostic functions.
- **Chapter 4, Interfaces**
  Connection information including standard IOM-2 and PCM interface timing frames and pins.
- **Chapter 5, SLICOFI-2x Command Structure and Programming**
  A general description of the *SLICOFI-2x* command structure.
- **Chapter 6, Electrical Characteristics**
  Parameters, symbols, and limit values are provided for the chip set.
- **Chapter 7, Application Circuits**
  External components and layout recommendations are identified. Illustrations of balanced ringing, unbalanced ringing, and protection circuits are included.
- **Chapter 8, Package Outlines**
  Illustrations and dimensions of the package outlines.

- **Chapter 9**, **Terminology**
  List of abbreviations and descriptions of symbols.
- **Chapter 10**, **Index**

1 Overview

DuSLIC is a family of communications chip sets. Each chip set comprises one dual-channel *SLICOFI-2x* codec and two single-channel SLICs or one dual-channel TSLIC. It is a highly flexible codec/SLIC solution for an analog line circuit and is easily programmable via software. Users can now serve different markets with a single hardware design that meets all standards worldwide.

The key benefits of the DuSLIC family include:

Integrated DSP Features

- Line echo cancellation (up to 8 ms)
- DTMF
- Caller-ID
- Full V.90 performance

Integrated Ringing

- Balanced ringing up to 85 Vrms
- Unbalanced ringing up to 50 Vrms
- Full support for external ringing

Smallest Footprint

- Only 121 mm² per channel
- Minimum external components

System Features

- Test & diagnostic functions (complete AC & DC)
- Time-slot assignment on two PCM highways

Proven Technology

- A single hardware design meets/exceeds worldwide requirements.
- 15+ years experience.
- Several million lines deployed worldwide.

The DuSLIC family allows any combination of the codec and SLIC chips shown in Table 1 and Table 2.

Table 1 Codec Feature Overview

Features	SLICOFI-2	SLICOFI-2S
Number of Voice Channels	2	2
DTMF Detection	Yes	No
Line Echo Cancellation (up to 8 ms)	Yes	No
Caller-ID Generation	Yes	No
Integrated Test and Diagnostics (Linetesting)	Yes	Yes
Modem (V.90) transmission	Yes	Yes
Modem tone detection	Yes	No
Metering pulses (TTX)	up to 2.5 Vrms	up to 1.2 Vrms
PCM/Serial Controller Interface	Yes	Yes
IOM2 Interface	Yes	Yes
Internal Ring Support	Yes	Yes
External Ringing Support	Yes	Yes
Supply Voltage	3.3 V	3.3 V

Table 2 SLIC Feature Overview

Features	SLIC-S/ TSLIC-S[1)]	SLIC-S2[2)]	SLIC-E/ TSLIC-E[3)]	SLIC-E2[4)]	SLIC-P
Maximum DC Feeding	32 mA	50 mA	32 mA	50 mA	32 mA
Maximum Ringing Voltage (balanced)	45 Vrms	45 Vrms	85 Vrms	85 Vrms	85 Vrms
Maximum Ringing Voltage (unbalanced)	–	–	–	–	50 Vrms
Longitudinal Balance	53 dB	60 dB	53 dB	60 dB	53 dB
Supply Voltages (negative/positive)	2/1	2/1	2/1	2/1	3/0
Supply Voltage	3.3 V... 5 V	3.3 V... 5 V	5.0 V	5.0 V	3.3 V
External Ring Support	Yes	Yes	Yes	Yes	Yes

Table 2 SLIC Feature Overview (cont'd)

Features	SLIC-S/ TSLIC-S[1)]	SLIC-S2[2)]	SLIC-E/ TSLIC-E[3)]	SLIC-E2[4)]	SLIC-P
Technology	90 V	90 V	170 V	170 V	170 V
On-Hook Transmission	Yes	Yes	Yes	Yes	Yes
Current Limitation	105 mA	105 mA	105 mA	105 mA	60/90 mA
Target Application	Low Cost CPE	Linecard (external ringing)	CPE	Linecard	Low Power CPE

1) Same specifications as SLIC-S, but two voice channels

2) Chip marked as PEB 4264 – packaging unit labeled with PEB 4264-2.

3) Same specifications as SLIC-E, but two voice channels

4) Chip marked as PEB 4265 – packaging unit labeled with PEB 4265-2.

To allow the most cost effective and feature optimized design the following table presents the available SLIC and Codec combinations. The choice of different combinations meets world wide design requirements.

Table 3 DuSLIC Chip Sets Presented in this Data Sheet

Chip Set	DuSLIC-S/ -S2	DuSLIC-SE/-SE2	DuSLIC-ES/-ES2	DuSLIC-E/ -E2	DuSLIC-P
Marketing Name	SLICOFI-2S/ SLIC-S/-S2 (TSLIC-S)[1)]	SLICOFI-2S/ SLIC-E/-E2 (TSLIC-E)[2)]	SLICOFI-2/ SLIC-S/-S2 (TSLIC-S)[1)]	SLICOFI-2/ SLIC-E/-E2 (TSLIC-E)[2)]	SLICOFI-2/ SLIC-P
Product ID	PEB 3264/ PEB 4264/-2 (PEB 4364)	PEB 3264/ PEB 4265/-2 (PEB 4365)	PEB 3265/ PEB 4264/-2 (PEB 4364)	PEB 3265/ PEB 4265/-2 (PEB 4365)	PEB 3265/ PEB 4266

1) Single channel SLIC-S or dual channel TSLIC-S package

2) Single channel SLIC-E or dual channel TSLIC-E package

- The DuSLIC chip sets presented in this Data Sheet are differentiated in terms of the DSP features and ringing voltage :
  - DuSLIC-S (Standard)
  - DuSLIC-SE (Standard Codec, Enhanced SLIC)
  - DuSLIC-ES (Enhanced Codec, Standard SLIC)
  - DuSLIC-E (Enhanced)
  - DuSLIC-P (Power Management).

- For both the DuSLIC-S and DuSLIC-E there are also long-haul versions, offering increased longitudinal balance (60 dB) :
  – DuSLIC-E2 (using SLIC-E2)
  – DuSLIC-S2 (using SLIC-S2)

Usage of Codecs and SLICs

The DuSLIC-S and DuSLIC-S2 chip sets use the SLICOFI-2S (PEB 3264) codec offering full basic POTS functionality, including programmable AC and DC characteristics, integrated ringing and Integrated Test & Diagnostic Functions (ITDF) etc.

The DuSLIC-E, DuSLIC-E2, and DuSLIC-P chip sets use the same SLICOFI-2 (PEB 3265) codec with full EDSP (Enhanced Digital Signal Processor) features such as DTMF detection, Caller ID generation, Universal Tone Detection (UTD) and Line Echo Cancellation (LEC).

These codecs (SLICOFI-2 and SLICOFI-2S) are manufactured using an advanced 0.35 µm 3.3 V CMOS process.

The main criteria for choosing the appropriate SLIC device, are the ringing voltage and longitudinal balance.

- SLIC-S and SLIC-S2 offer balanced ringing (up to 45 Vrms)
- SLIC-E and SLIC-E2 offer balanced ringing (up to 85 Vrms)
- SLIC-P offers both balanced (85Vrms) and unbalanced ringing (50 Vrms)
  Note: the above ring voltages are achievable with 20 Vdc offset. Smaller dc offset will increase the maximum achievable ring voltage

The SLIC-S2 and SLIC-E2 are optimized for longhaul applications, and offer a minimum of 60 dB longitudinal balance.
All Infineon SLICs are manufactured in our well-proven 90 V and 170 V Smart Power Technology (SPT) processes.

Dual-channel SLICs : TSLIC-S & TSLIC-E

The TSLIC-S (PEB 4364) and TSLIC-E (PEB 4365) chips are dual channel versions of the SLIC-S (PEB 4264) and SLIC-E (PEB 4265) with identical technical specifications for each channel. Therefore whenever SLIC-S or SLIC-E are mentioned in this and other DuSLIC documentation, also TSLIC-S and TSLIC-E can be deployed.

DuSLIC Architecture

Unlike traditional designs, DuSLIC splits the SLIC function into high-voltage SLIC functions and low-voltage SLIC functions.

The low-voltage functions are handled in the *SLICOFI-2x* device. The partitioning of the functions is shown in **Figure 1**.

For further information see **Chapter 2.1**.

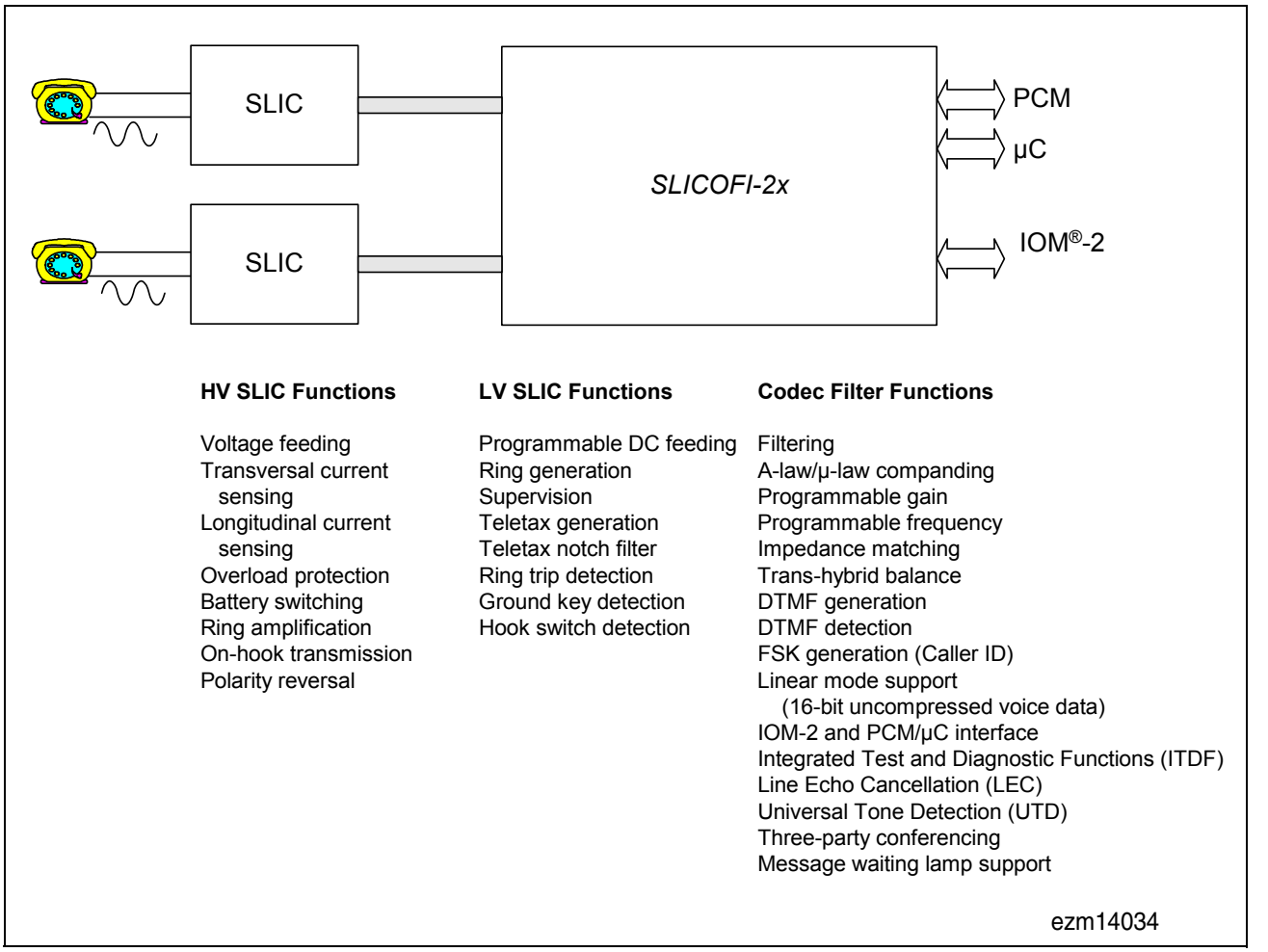


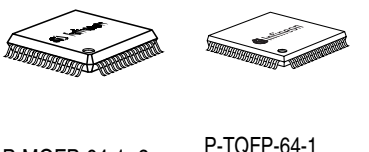
Figure 1 DuSLIC Chip Set

Dual Channel Subscriber Line Interface Concept
DuSLIC

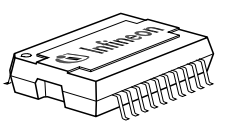
PEB 3264
PEB 3265
PEB 4264/-2
PEB 4364
PEB 4265/-2
PEB 4365
PEB 4266

1.1 Features

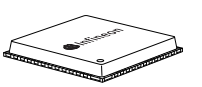
- Fully programmable dual-channel codec
- Programmable AC and DC characteristics
- Integrated Test and Diagnostic Functions (ITDF)
- Programmable integrated ringing : Balanced (85 Vrms) and/or Unbalanced (50 Vrms)
- Programmable Teletax (TTX) generation
- Programmable battery feeding with capability for driving longer loops
- Ground start/loop start signaling supported
- Polarity reversal (hard or soft)
- On-hook transmission
- Integrated DTMF generator
- Integrated DTMF decoder
- Integrated Caller ID generator (FSK or DTMF)
- Universal Tone Detection (UTD) - fax/modem detection
- Integrated Line Echo Cancellation (LEC) up to 8 ms
- Optimized filter structure for modem transmission
- Three-party conferencing (in PCM/µC mode)
- Message waiting lamp support (PBX)
- Power optimized architecture
- Power management capability (integrated battery switches)



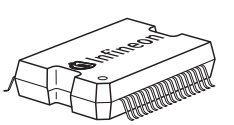
P-MQFP-64-1,-2 P-TQFP-64-1



P-DSO-20-5



P-VQFN-48-4



P-DSO-36-15

Type	Package
PEB 3264	P-MQFP-64-1 or P-TQFP-64-1
PEB 3265	P-MQFP-64-1 or P-TQFP-64-1
PEB 4264/-2	P-DSO-20-5 or P-VQFN-48-4
PEB 4364	P-DSO-36-15
PEB 4265/-2	P-DSO-20-5 or P-VQFN-48-4
PEB 4365	P-DSO-36-15
PEB 4266	P-DSO-20-5 or P-VQFN-48-4

- 8 kHz and 16 kHz PCM Transmission
- IOM-2 or PCM/µC Interface selectable
- G.711 A-law / µ-law companding
- Specifications: ITU-T G.712, Q.552, LSSGR, TR57

1.2 Typical Applications

DuSLIC offers an optimized solution for various applications. The following main applications can be highlighted:

- Access Networks
  - Central Office (CO)
  - Next-Generation Digital Subscriber Line Access Module (NG-DSLAM)
  - Digital Loop Carrier (DLC)
  - Wireless Local Loop (WLL)
  - Fiber in the Loop (FITL)
  - Digital Added Main Line (DAML) / PCM-x
  - Multi-dwelling / Multi-tennant units (MDU / MTU)
- Customer Premises Equipment
  - Private Branch Exchange (PBX)
  - Integrated Access Device (IAD)
  - Voice over Packet (VoDSL, VoIP, VoATM, etc.)
  - ISDN Intelligent Network Termination (iNT)
  - ISDN Terminal Adapter (TA)
  - Cable Modem
  - xDSL NT
  - Router

1.3 Logic Symbols

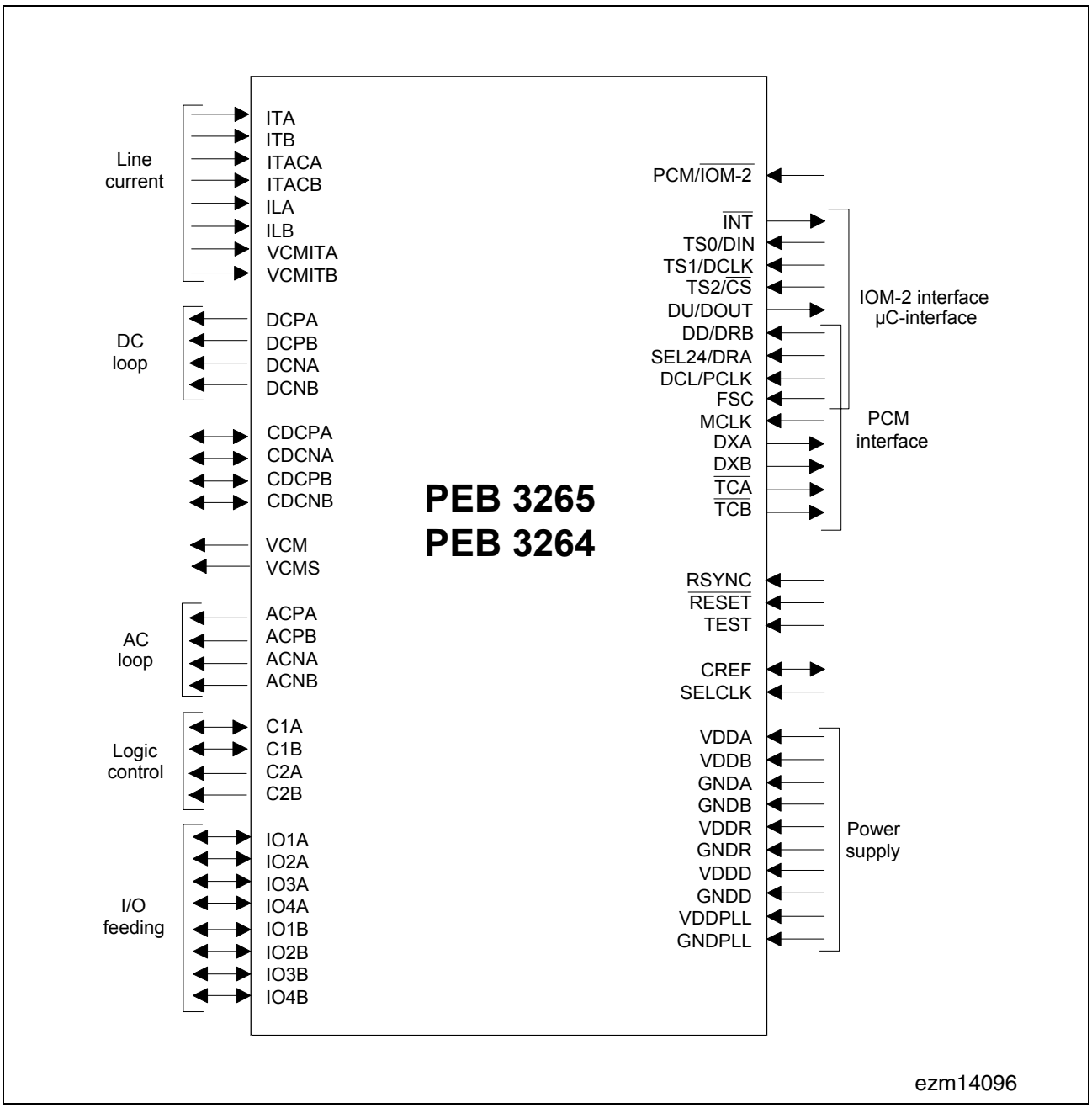


Figure 2 Logic Symbol: SLICOFI-2/-2S

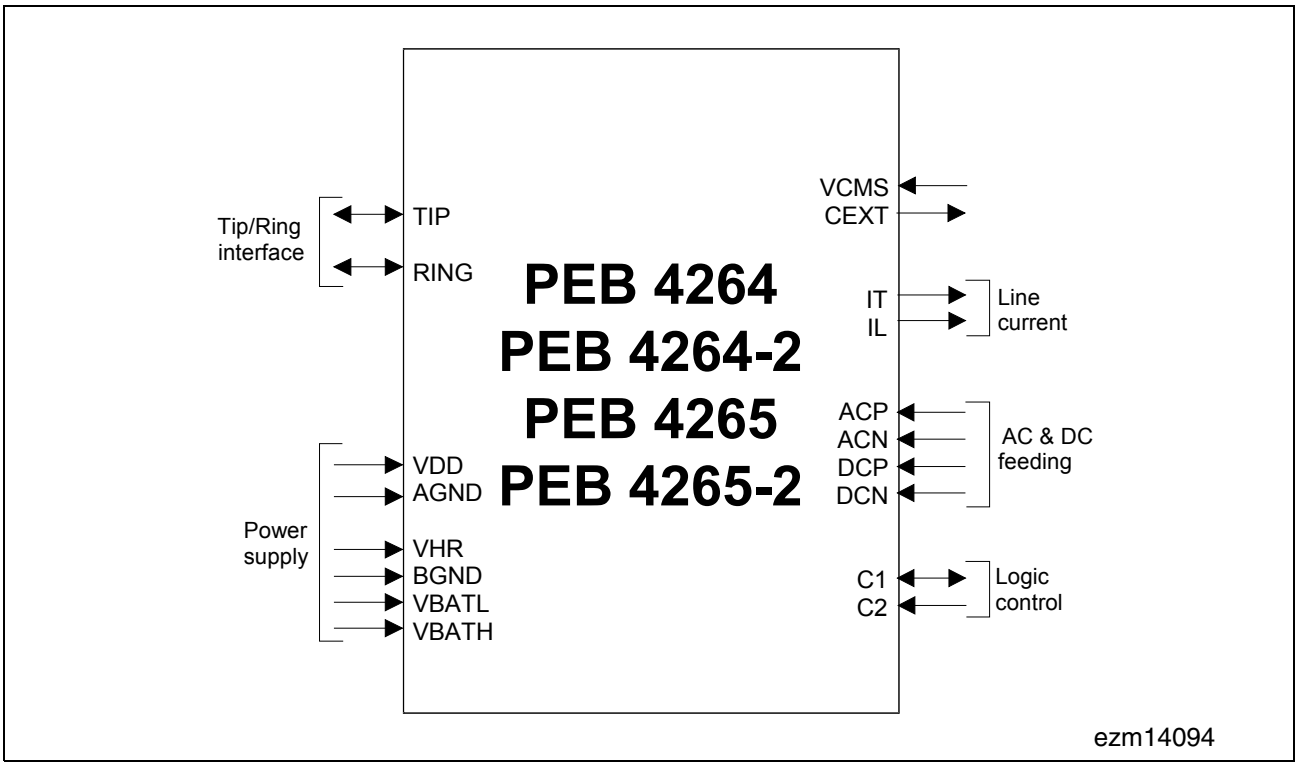


Figure 3 Logic Symbol: SLIC-S/SLIC-S2 (V1.1, V1.2), SLIC-E/SLIC-E2 (V1.1)

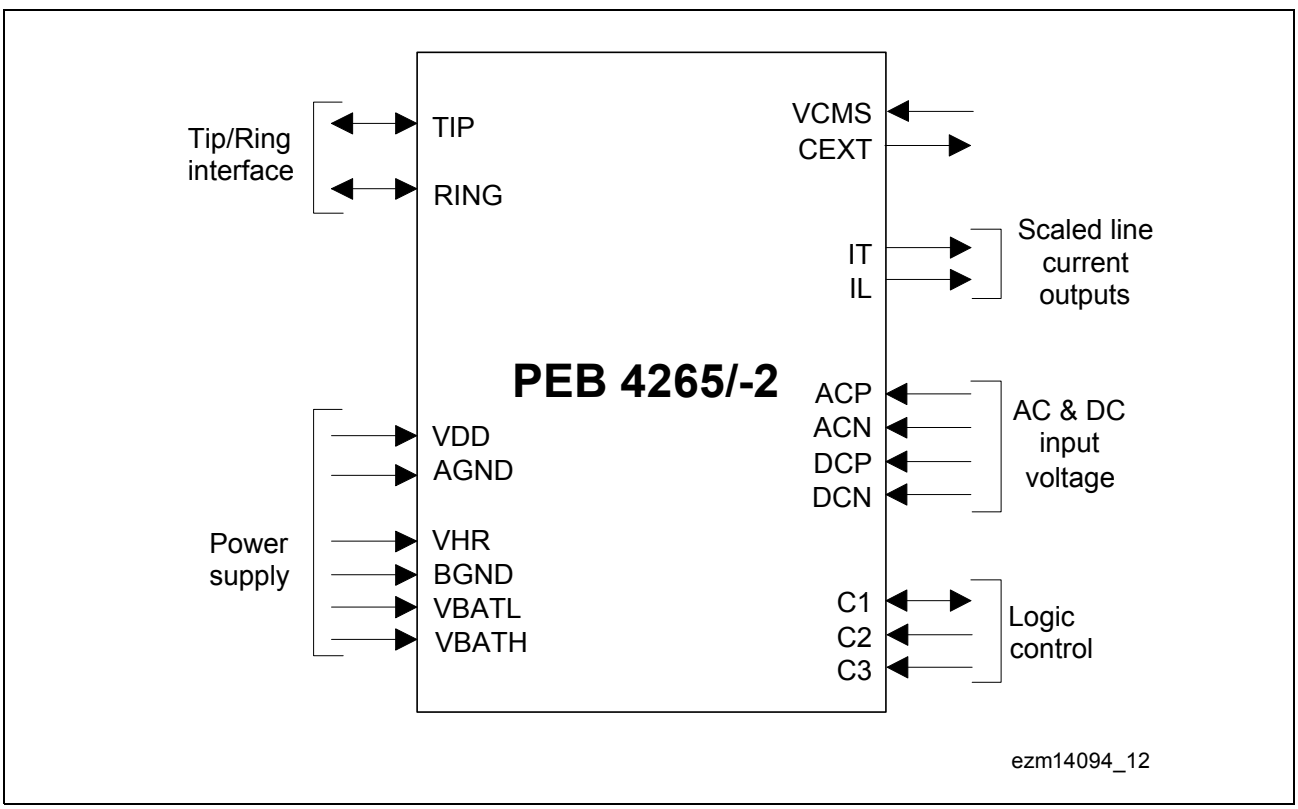


Figure 4 Logic Symbol: SLIC-E/SLIC-E2 (V1.2)

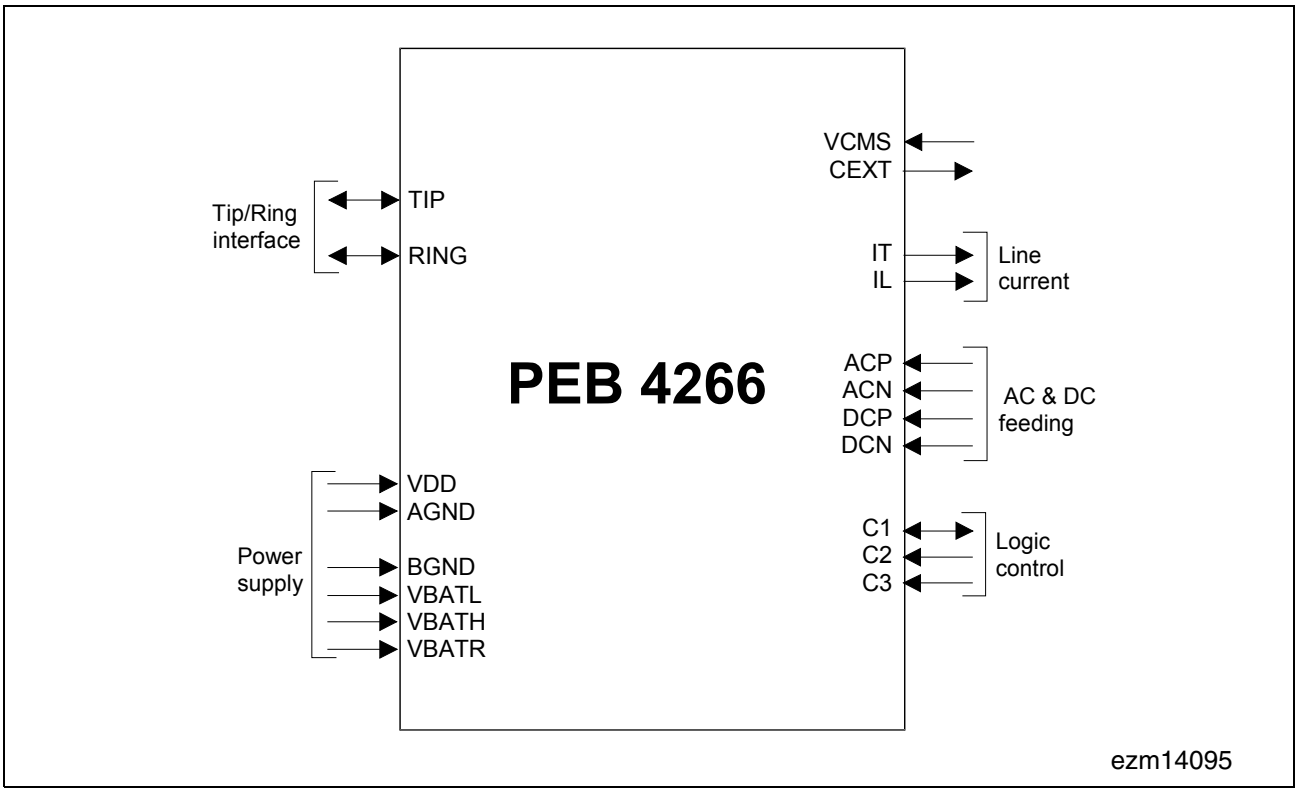


Figure 5 Logic Symbol: SLIC-P

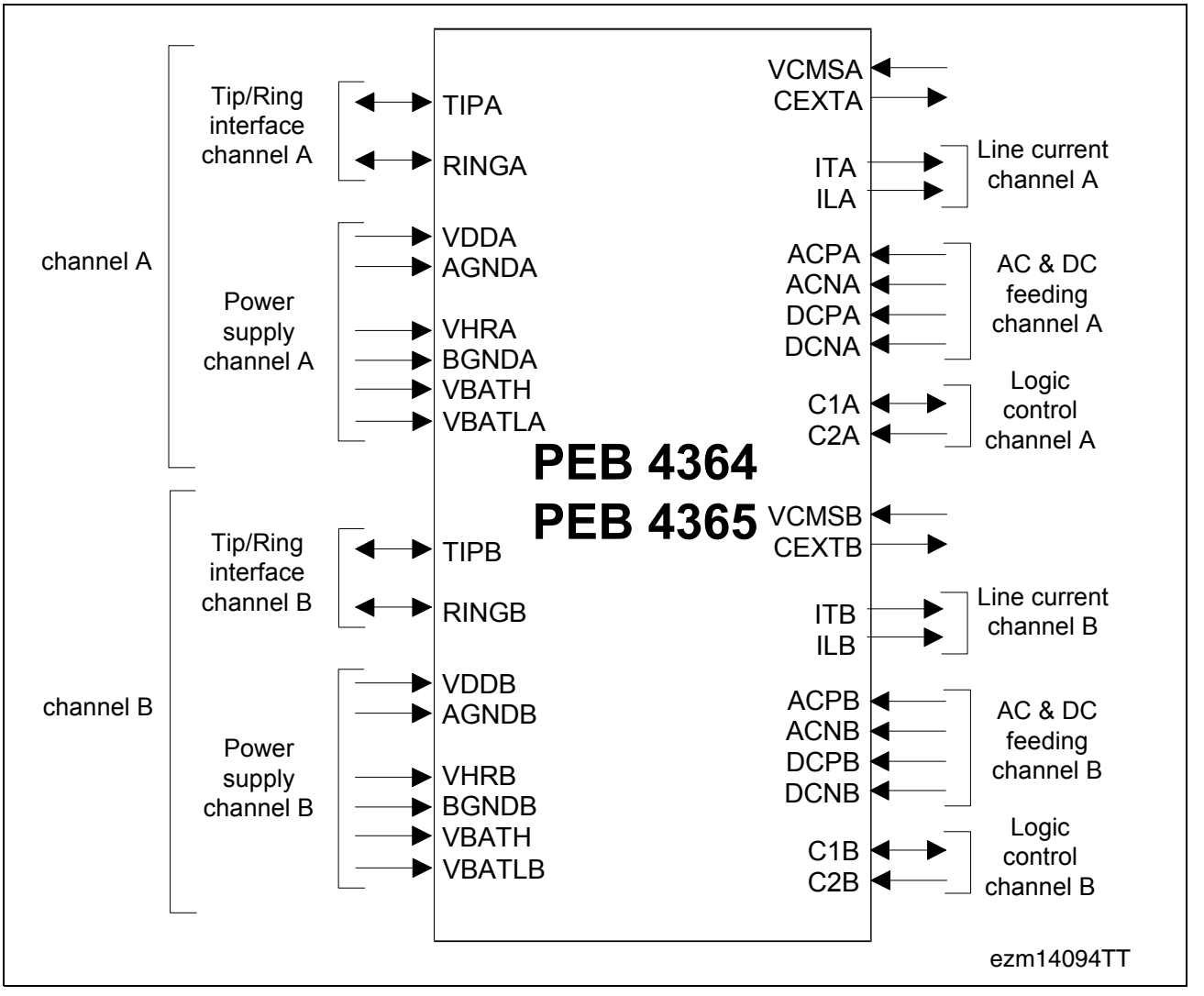


Figure 6 Logic Symbol: TSLIC-S/TSLIC-E

2 Functional Description

2.1 Functional Overview

2.1.1 Basic Functions of all DuSLIC Chip Sets

The functions described in this section are integrated into all DuSLIC chip sets (see **Figure 7** for DuSLIC-S/-S2 and **Figure 8** for DuSLIC-E/-E2/-P).

All BORSCHT functions are integrated:

- Battery feed
- Overvoltage protection
  (implemented by the robust high-voltage SLIC technology and additional circuitry)
- Ringing[1)]
- Signaling (supervision)
- Coding
- Hybrid for 2/4-wire conversion
- Testing

An important feature of the DuSLIC design is the fact that all the SLIC and codec functions are programmable via the IOM-2 or PCM/µC Interface of the dual-channel *SLICOFI-2x* device:

- DC (battery) feed characteristics
- AC impedance matching
- Transmit gain
- Receive gain
- Hybrid balance
- Frequency response in transmit and receive direction
- Ring frequency and amplitude[1)]
- Hook thresholds
- TTX modes[2)]
- DTMF/tone generator

Because signal processing within the *SLICOFI-2x* is completely digital, it is possible to adapt to the requirements listed above by simply updating the coefficients that control DSP processing of all data. This means, for example, that changing impedance matching or hybrid balance requires no hardware modifications. A single hardware design is now capable of meeting the requirements for different markets. The digital nature of the filters and gain stages also assures high reliability, no drifts (over temperature or time), and minimal variations between different lines.

1) For the DuSLIC-S2 chip set, only external ringing is supported

2) Not available with the DuSLIC-S2 chip set

The characteristics for the two voice channels within *SLICOFI-2x* can be programmed independently of each other. The DuSLIC Coefficients Software (DuSLICOS) is provided to automate calculation of coefficients to match different requirements. DuSLICOS also verifies the calculated coefficients.

2.1.2 Additional Functions of the DuSLIC-E/-E2/-P Chip Sets

The following line circuit functions are integrated only in the DuSLIC-E/-E2/-P chip sets (see **Figure 8**):

- Teletax metering

For pulse metering, a 12/16 kHz sinusoidal metering burst must be transmitted. The DuSLIC chip set generates the metering signal internally and has an integrated notch filter.

- DTMF

DuSLIC has an integrated DTMF generator comprising two tone generators and one DTMF decoder. The decoder is able to monitor the transmit or receive path for valid tone pairs and outputs the corresponding digital code for each DTMF tone pair.

- Caller ID Frequency Shift Keying (FSK) Modulator

DuSLIC has an integrated FSK modulator capable of sending Caller ID information. The Caller ID modulator complies with all requirements of ITU-T Recommendation V.23 and Bell 202 (Caller ID can also be done using DTMF generators).

- Line Echo Cancellation (LEC)

DuSLIC contains an adaptive Line Echo Cancellation unit for the cancellation of near end echoes (up to 8 ms cancelable echo delay time).

- Universal Tone Detection (UTD)

DuSLIC has an integrated Universal Tone Detection unit to detect special tones in the receive or transmit path (e.g. fax or modem tones).

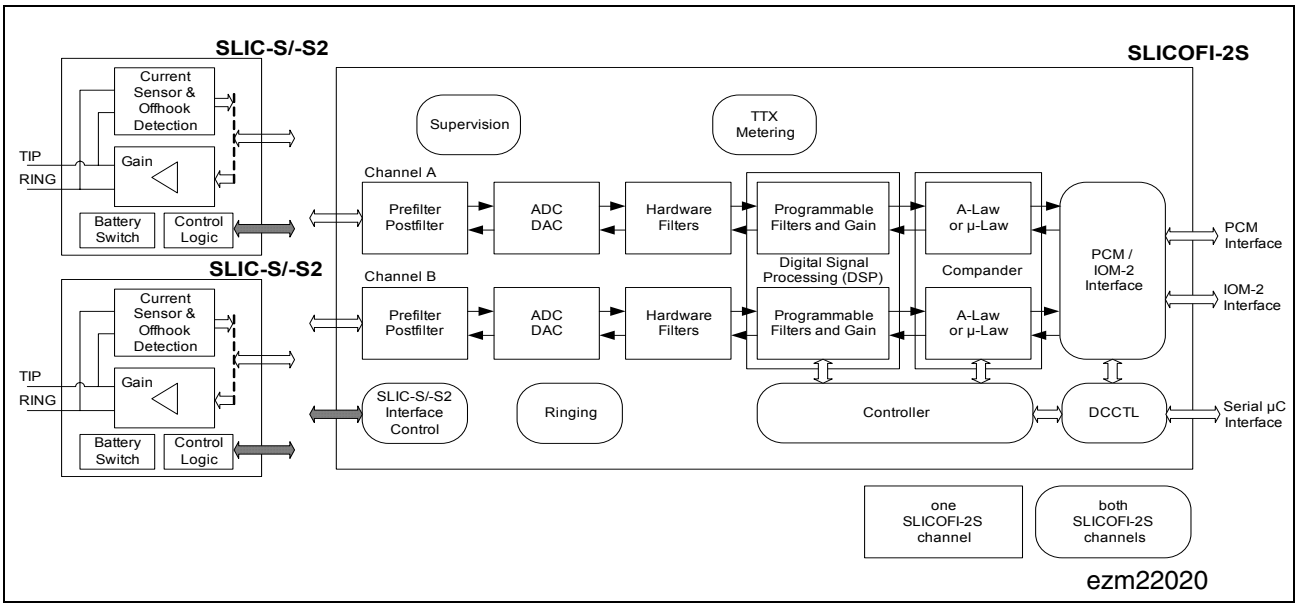


Figure 7 Line Circuit Functions in the DuSLIC-S/-S2

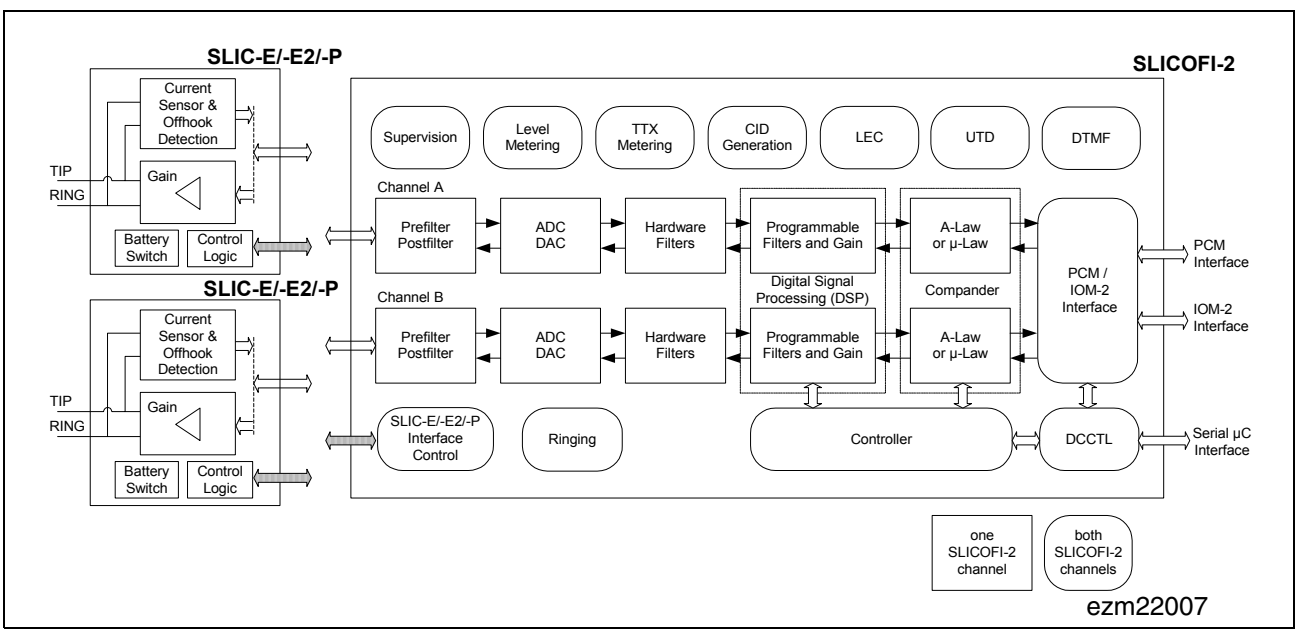


Figure 8 Line Circuit Functions in the DuSLIC-E/-E2/-P

2.2 Block Diagram SLICOFI-2/-2S

Figure 9 shows the internal block structure of all available *SLICOFI-2x* codec versions. The Enhanced Digital Signal Processor (EDSP) providing the add-on functions[1)] is only integrated in the SLICOFI-2 (PEB 3265) device.

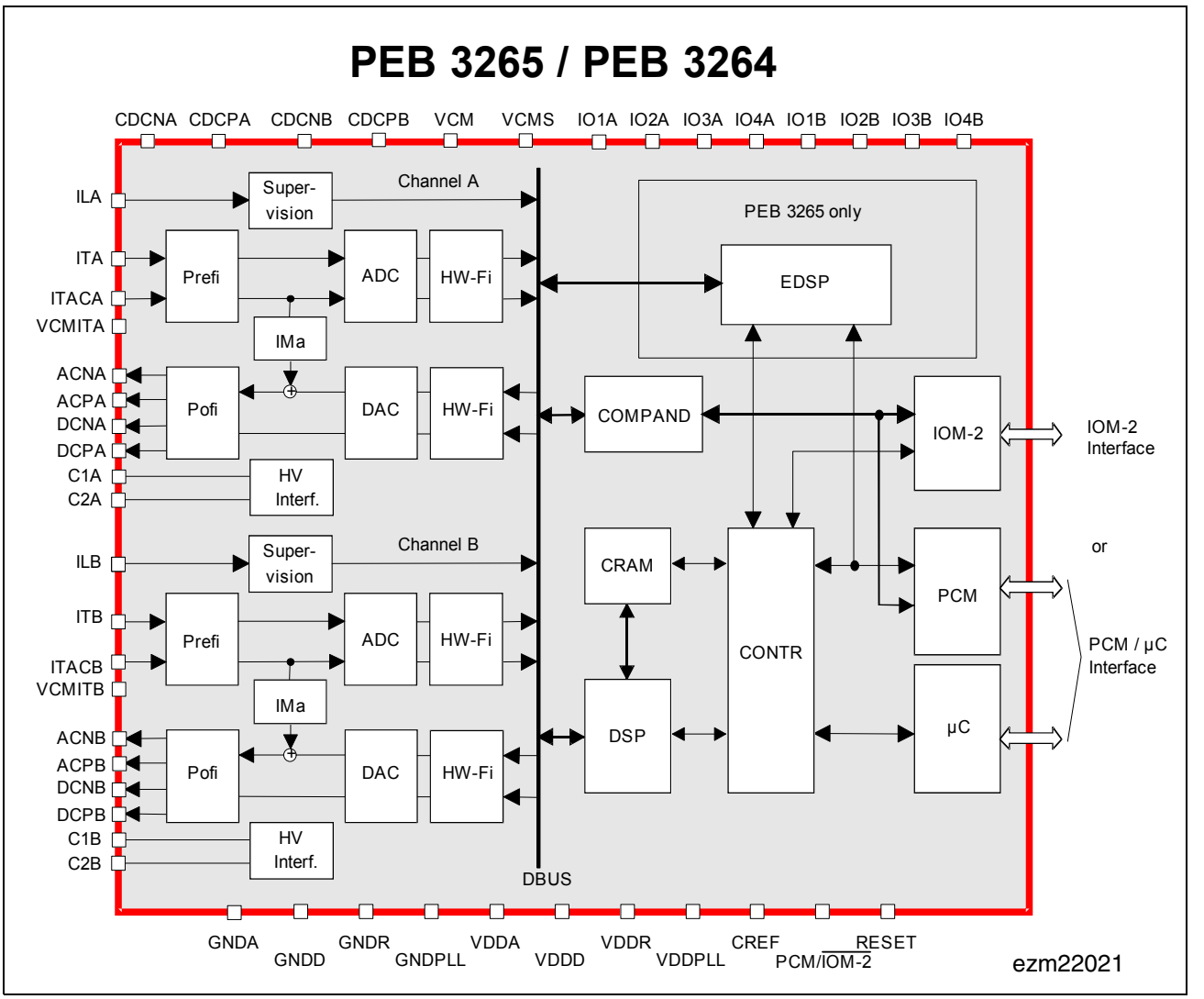


Figure 9 Block Diagram: SLICOFI-2/-2S (PEB 3265, PEB 3264)

1) The add-on functions are DTMF detection, Caller ID generation, Message Waiting lamp support, Three-party Conferencing, Universal Tone Detection (UTD), Line Echo Cancellation (LEC), and Sleep Mode.

2.3 DC Feeding

DC feeding with the DuSLIC is fully programmable as shown in **Table 4** on **Page 38**.

Figure 10 shows the signal paths for DC feeding between the SLIC and the *SLICOFI-2x*:

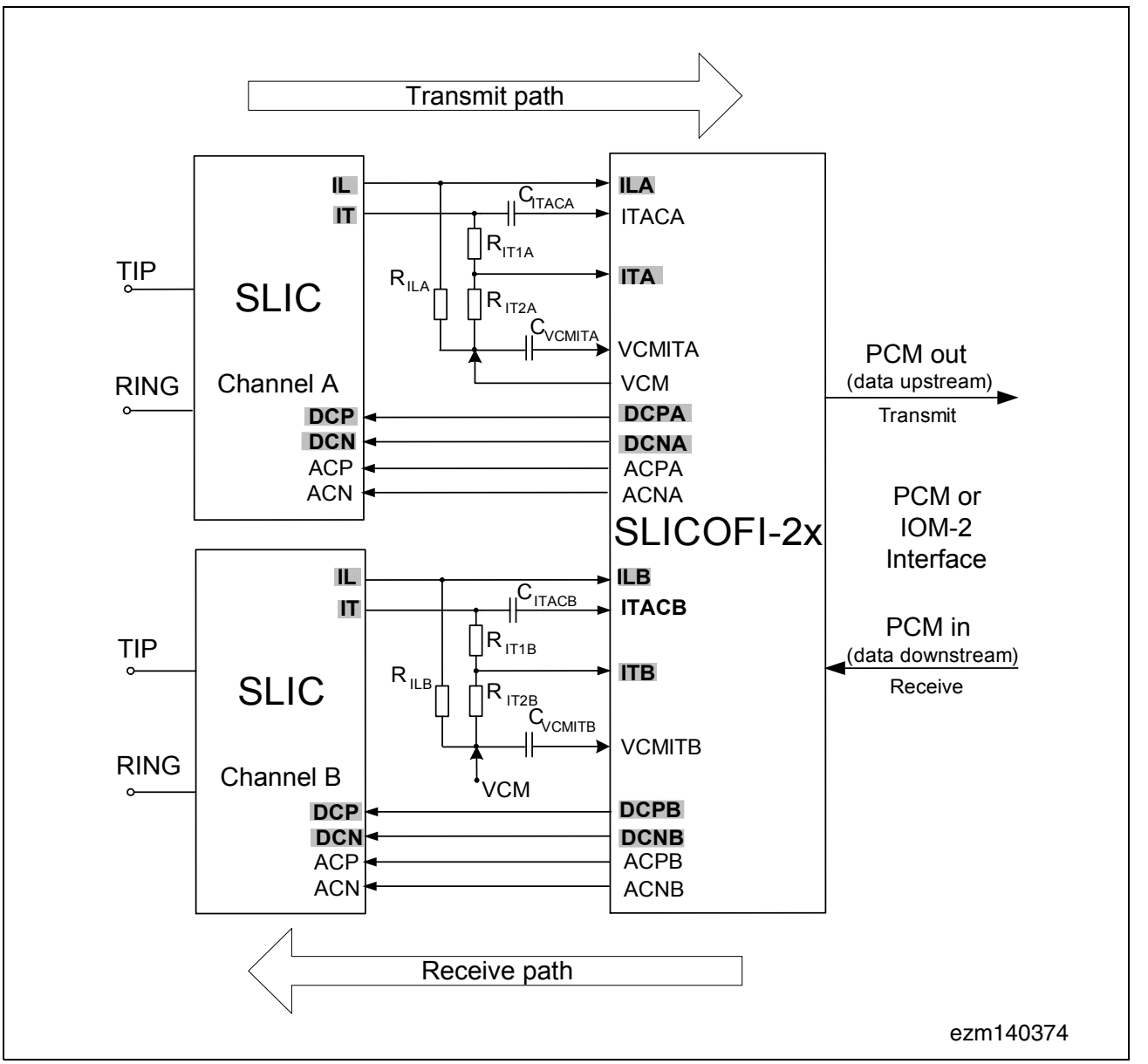


Figure 10 Signal Paths – DC Feeding

2.3.1 DC Characteristic Feeding Zones

The DuSLIC DC feeding characteristic has three different zones: the constant current zone, the resistive zone, and the constant voltage zone. A voltage reserve V_{RES} (see **Chapter 2.3.7**) can be selected to avoid clipping the high level AC signals (such as TTX) and to take into account the voltage drop of the SLIC. The DC feeding characteristic is shown in **Figure 11**.

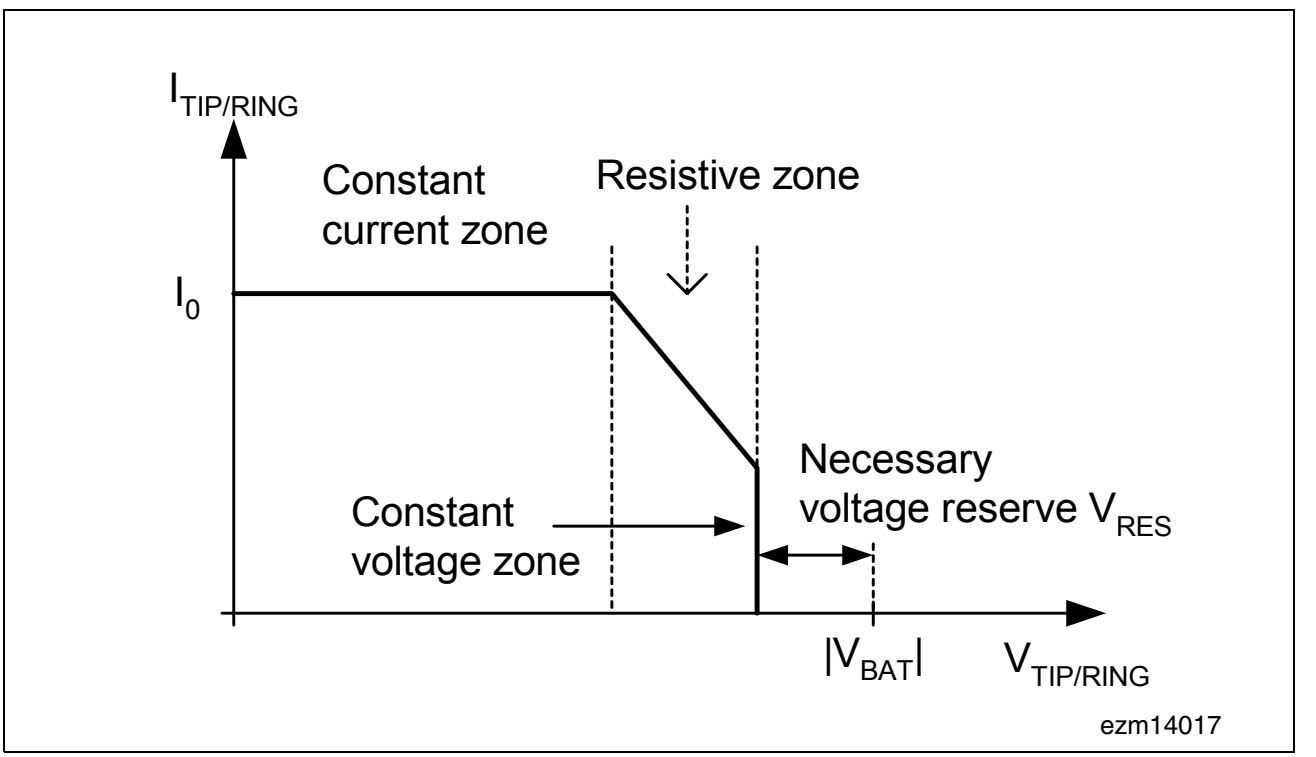


Figure 11 DC Feeding Characteristic

This simplified diagram shows the constant current zone as an ideal current source with an infinite internal resistance, while the constant voltage zone is shown as an ideal voltage source with an internal resistance of 0 Ω. For the specification of the internal resistances, see **Chapter 2.3.5**.

2.3.2 Constant Current Zone

In the off-hook state, the feed current must usually be kept at a constant value independent of load (see **Figure 12**). The SLIC senses the DC current and supplies this information to the *SLICOFI-2x* via the IT pin (input pin for DC control). The *SLICOFI-2x* compares the actual current with the programmed value and adjusts the SLIC drivers as necessary. $I_{TIP/RING}$ in the constant current zone is programmable from 0 to 32 mA or 0 to 50 mA depending on the particular SLIC version in use.

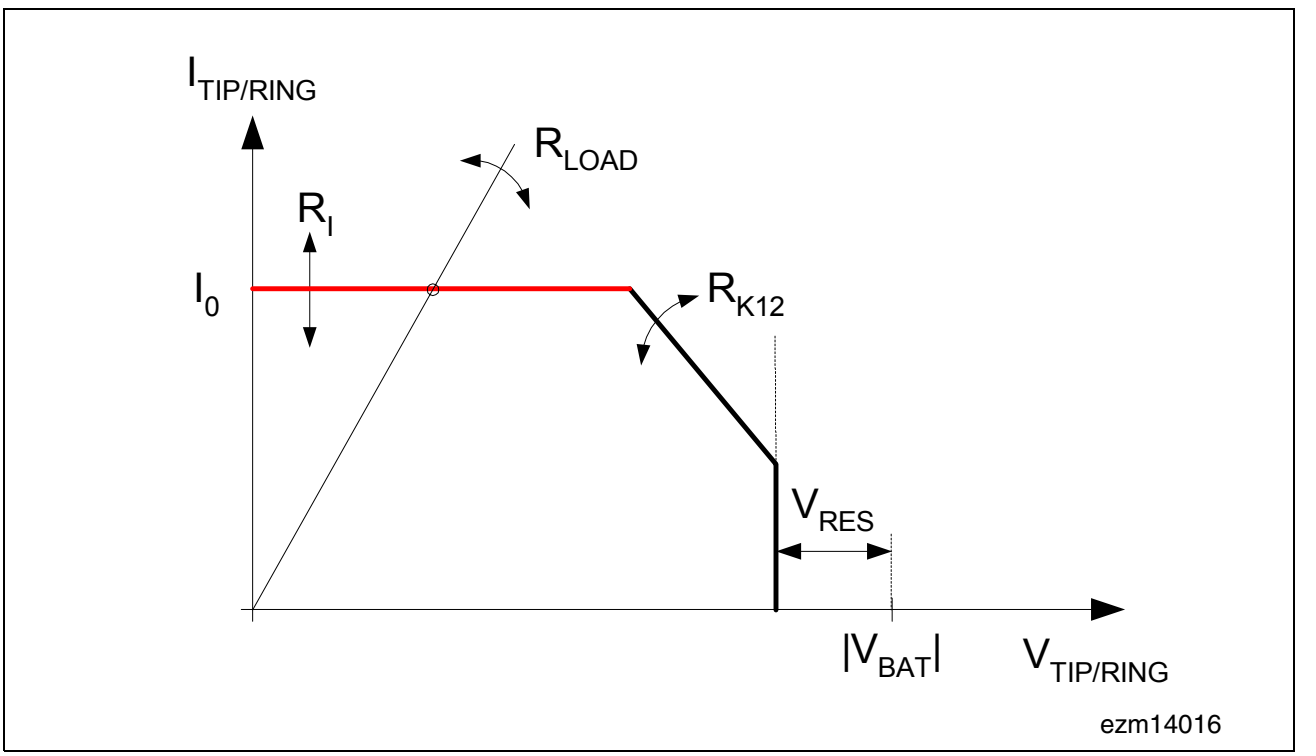


Figure 12 Constant Current Zone

Depending on the load, the operating point is determined by the voltage $V_{TIP/RING}$ between the Tip and Ring pins.

The operating point is calculated from:

$V_{TIP/RING} = R_{LOAD} \times I_{TIP/RING}$

where

$R_{LOAD} = R_{PRE} + R_{LINE} + R_{PHONE,OFF\text{-}HOOK}$

$R_{PRE} = R_{PROT} + R_{STAB}$.

The lower the load resistance R_{LOAD}, the lower the voltage between the Tip and Ring pins. A typical value for the programmable feeding resistance in the constant current zone is about R_I = 10 kΩ (see **Table 4**).

2.3.3 Resistive Zone

The programmable resistive zone R_{K12} of the DuSLIC provides extra flexibility over a wide range of applications. The resistive zone is used for very long lines where the battery is incapable of feeding a constant current into the line.

The operating point in this case crosses from the constant current zone for low and medium impedance loops to the resistive zone for high impedance loops (see **Figure 13**). The resistance of the zone R_{K12} is programmable from R_V to 1000 Ω

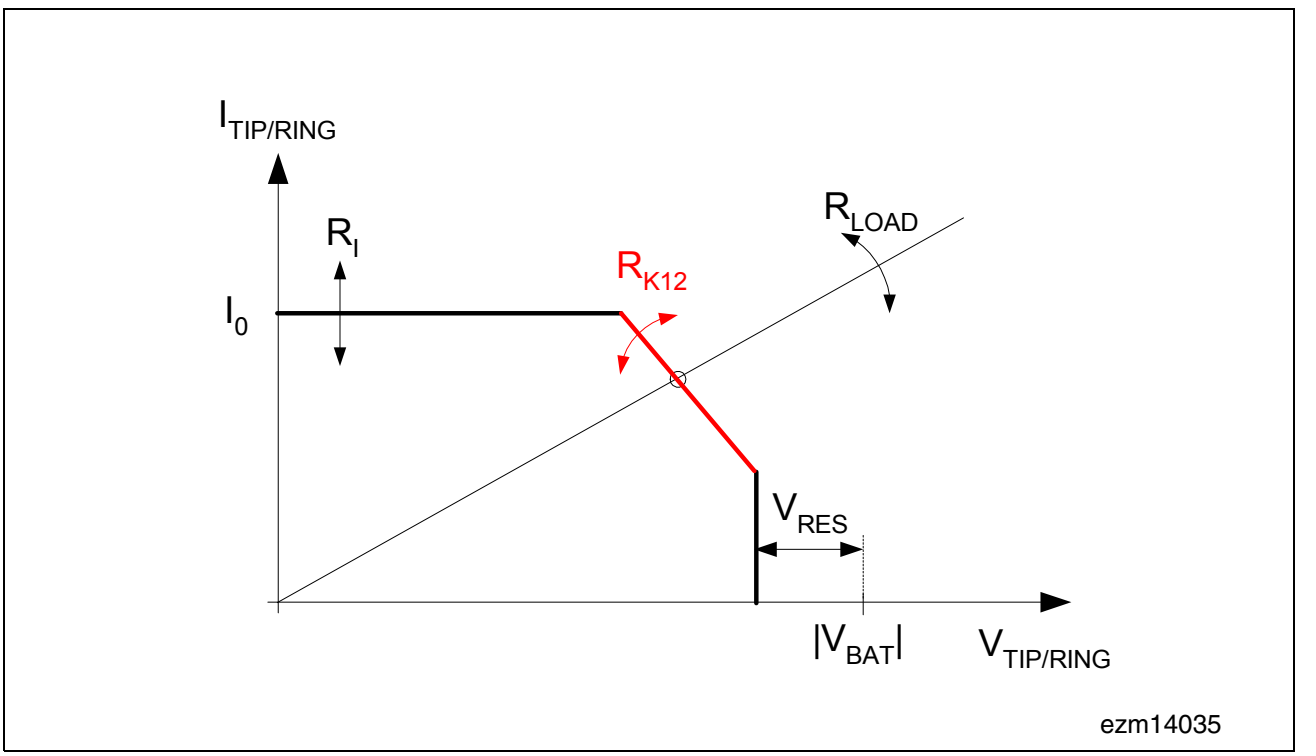


Figure 13 Resistive Zone

2.3.4 Constant Voltage Zone

The constant voltage zone (see **Figure 14**) is used in some applications to supply a constant voltage to the line. In this case, $V_{TIP/RING} = V_{LIM}$ is constant and the current depends on the load between the Tip and Ring pin. V_{LIM} is set by the DuSLICOS software.

In the constant voltage zone, the external resistors $R_{PRE} = R_{PROT} + R_{STAB}$ necessary for stability and protection define the resistance R_V seen at the RING and TIP wires of the application.

The programmable range of the parameters R_I, I_0, I_{K1}, V_{K1}, R_{K12} and V_{LIM} is given in **Table 4**.

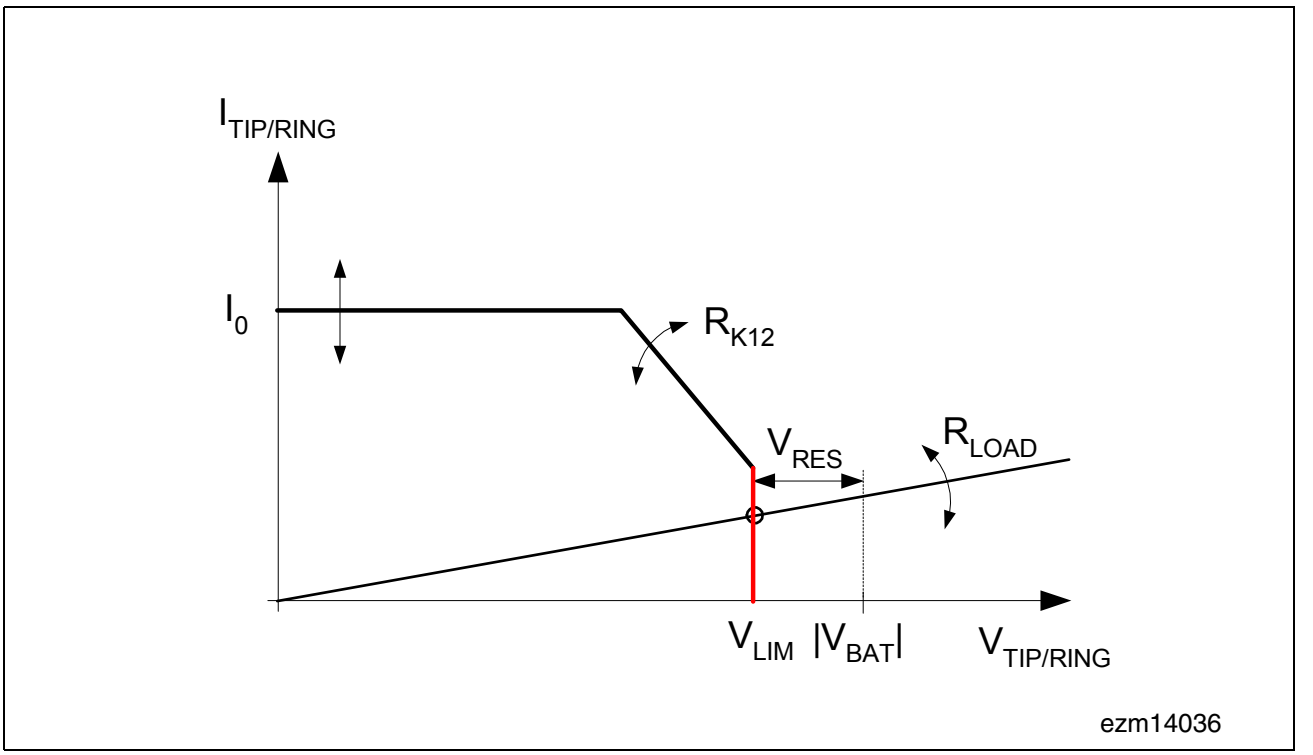


Figure 14 Constant Voltage Zone

2.3.5 Programmable Voltage and Current Range: DC Characteristics

The DC characteristics and all symbols are shown in **Figure 15**.

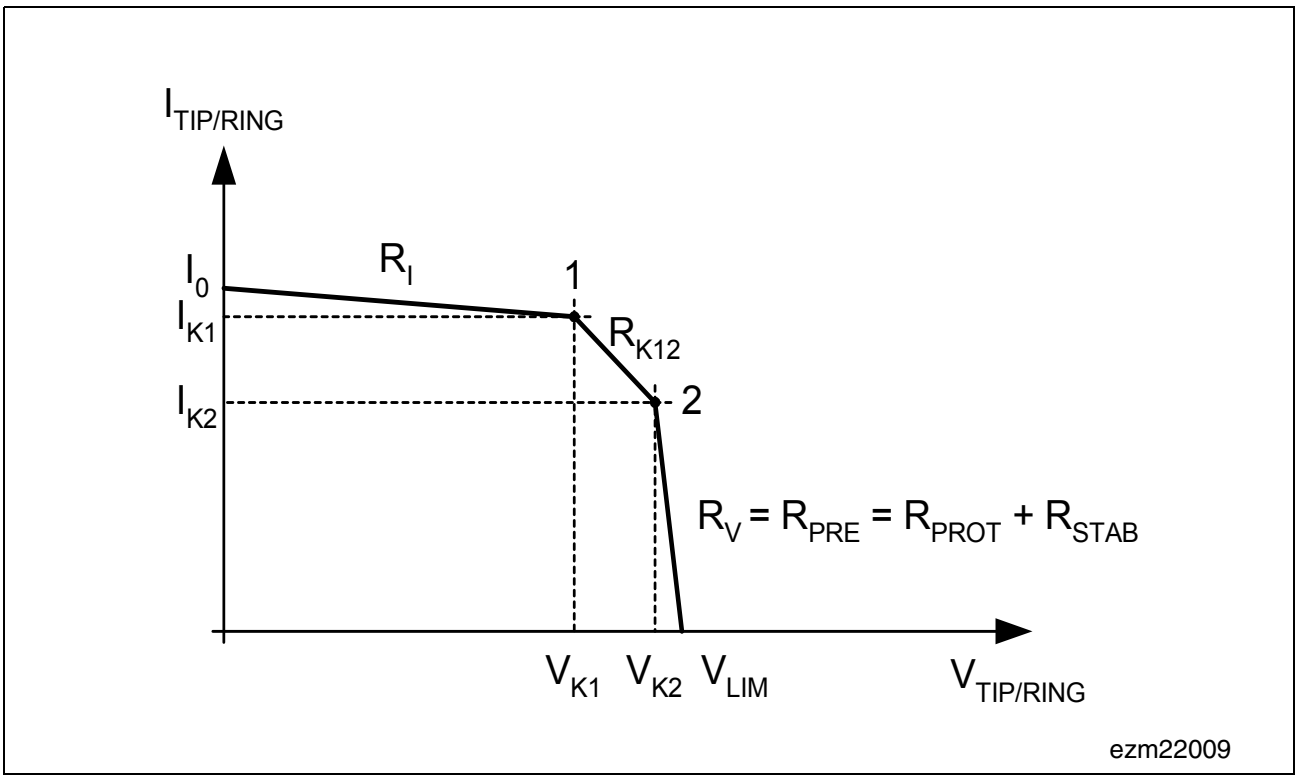


Figure 15 DC Characteristics

Table 4 DC Characteristics

Symbol	Programmable Range	Condition
R_I	1.8 kΩ … 40 kΩ	–
I_0	0 … 32 mA	only for DuSLIC-S, DuSLIC-E, DuSLIC-P
	0 … 50 mA	only for DuSLIC-S2, DuSLIC-E2
I_{K1}	0 … 32 mA	only for DuSLIC-S, DuSLIC-E, DuSLIC-P
	0 … 50 mA	only for DuSLIC-S2, DuSLIC-E2
V_{K1}	0 … 50 V	–
	$V_{K1} < V_{LIM} - I_{K1} \times R_{K12}$	only (V_{K1}, I_{K1})
	$V_{K1} < V_{LIM} - I_{K1} \times R_V$ $V_{K1} > V_{LIM} - I_{K1} \times R_{K12}$	(V_{K1}, I_{K1}) and (V_{K2}, I_{K2})
R_{K12}	R_V … 1000 Ω	–
V_{LIM}	0 … 72 V	–
	$V_{LIM} > V_{K1} + I_{K1} \times R_{K12}$	only (V_{K1}, I_{K1})

2.3.6 SLIC Power Dissipation

The major portion of the power dissipation in the SLIC can be estimated by the power dissipation in the output stages. The power dissipation can be calculated from:

$$P_{SLIC} \approx (V_{BAT} - V_{TIP/RING}) \times I_{TIP/RING}$$

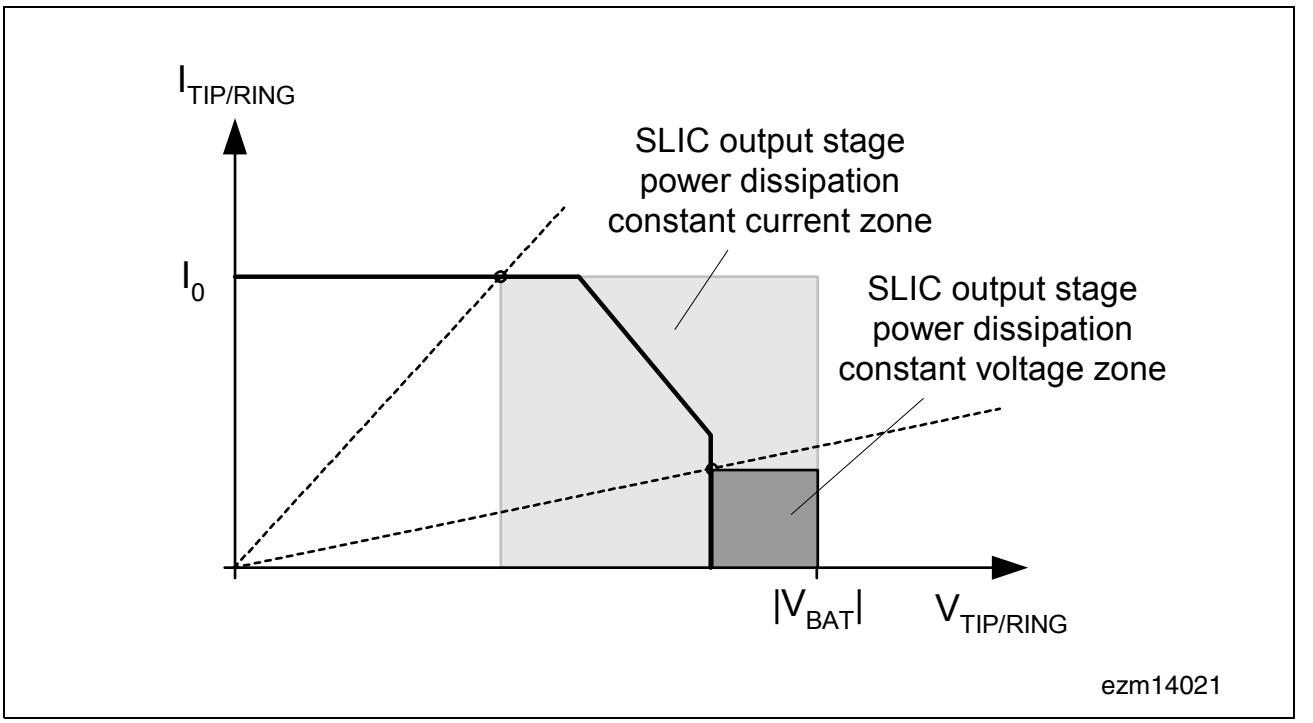


Figure 16 Power Dissipation

For further information, see **Chapter 3.7.2** on **Page 91**.

2.3.7 Necessary Voltage Reserve

To avoid clipping AC speech signals as well as AC metering pulses, a voltage reserve V_{RES} (see **Figure 11**) must be provided.

$V_{RES} = |V_{BAT}| - V_{LIM}$ (see **Page 37**)

$|V_{BAT}|$ is the selected battery voltage, which can be either V_{BATH}, V_{BATL}, or $|V_{HR} - V_{BATH}|$ for the SLIC-S/-S2/-E/-E2, depending on the mode. Similarly, it can be V_{BATH}, V_{BATL}, or V_{BATR} for the SLIC-P, depending on the mode.

V_{RES} consists of:

- Voltage reserve of the SLIC output buffers: this voltage drop depends on the output current through the Tip and Ring pins. For a standard output current of 25 mA, this voltage reserve is a few volts.
- Voltage reserve for AC speech signals: max. signal amplitude (example 2 V)
- Voltage reserve for AC metering pulses: The TTX signal amplitude V_{TTX} depends on local specifications and varies from 0.1 Vrms to several Vrms at a load of 200 Ω. To obtain V_{TTX} = 2 Vrms at a load of 200 Ω and R_{PRE} = 50 Ω ($R_{PRE} = R_{PROT} + R_{STAB}$), 3 Vrms = 4.24 Vpeak are needed at the SLIC output.

Therefore, a V_{RES} value of 10.24 V must be selected (= 4 V (SLIC drop for peak current of DC and speech and TTX) + 2 V (AC speech signals) + 4.24 V (TTX-signal)).

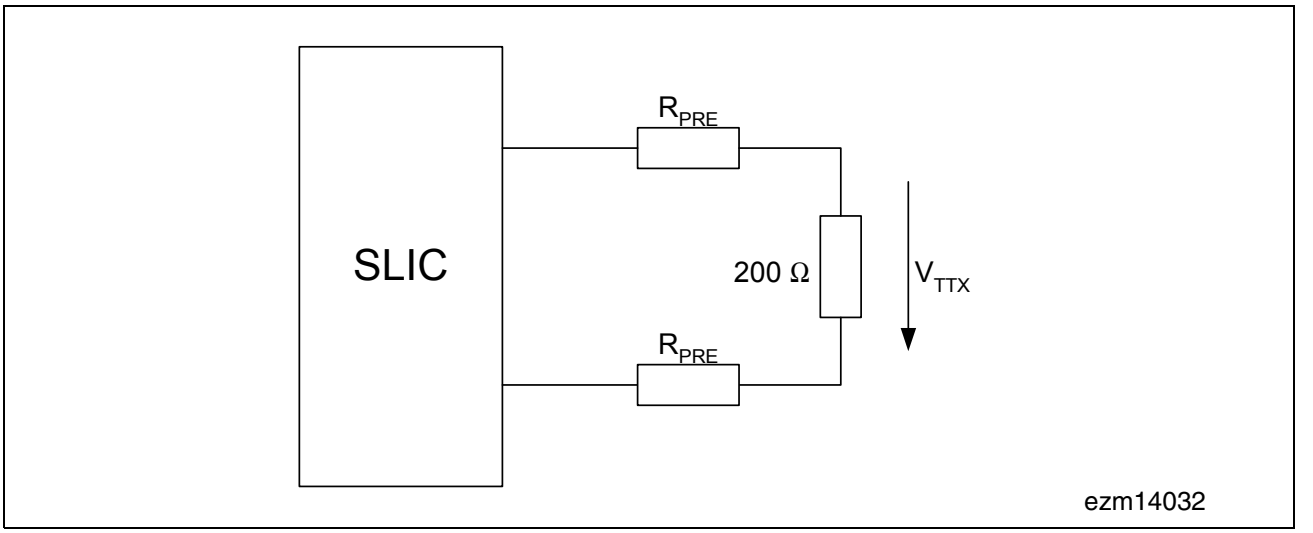


Figure 17 TTX Voltage Reserve Schematic

2.3.8 Extended Battery Feeding

If the battery voltage is not sufficient to supply the minimum required current through the line even in the resistive zone, the auxiliary positive battery voltage can be used to expand the voltage swing between Tip and Ring. With this extended supply voltage – V_{HR} (DuSLIC-S/-S2/E/-E2) or V_{BATR} (DuSLIC-P) – it is possible to supply the constant current for long lines. **Figure 18** shows the DC feeding impedances $R_{MAX,ACTH}$ in ACTH mode and $R_{MAX,ACTR}$ in ACTR mode (for more information about the ACTH and ACTR modes, see **Chapter 3.1**).

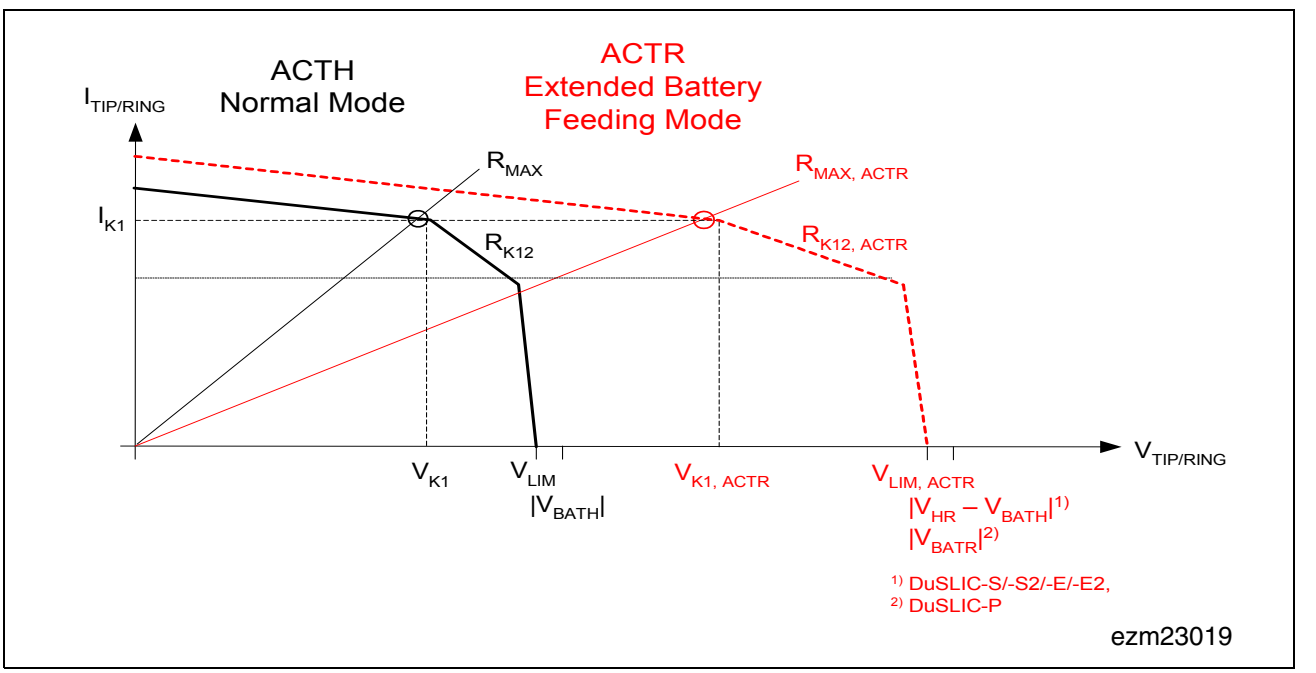


Figure 18 DC Feeding Characteristics (ACTH, ACTR)

The extended feeding characteristic is determined by the feeding characteristic in normal mode (ACTH) and an additional gain factor K_B (DuSLICOS DC Control Parameter 1/4: Additional Gain in active Ring):

$V_{LIM,ACTR} = V_{LIM} \times K_B$

$V_{K1,ACTR} = V_{K1} \times K_B + R_V \times I_{K1} \times (K_B - 1) \approx V_{K1} \times K_B$

$R_{K12,ACTR} = K_B \times (R_{K12} - R_V) + R_V \approx R_{K12} \times K_B$

$R_{I,ACTR} = R_I \times K_B/2$

$I_{K2,ACTR} = I_{K2} \times K_B \times (R_{K12} - R_V)/(K_B \times R_{K12} - R_V)$

$V_{K2,ACTR} = V_{LIM,ACTR} - I_{K2,ACTR} \times R_V$

2.4 AC Transmission Characteristics

SLICOFI-2x uses either an IOM-2 or a PCM digital interface. In receive direction, *SLICOFI-2x* converts PCM data from the network and outputs a differential analog signal (ACP and ACN) to the SLIC that amplifies the signal and applies it to the subscriber line. In transmit direction, the transversal (IT) and longitudinal (IL) currents on the line are sensed by the SLIC and fed to the *SLICOFI-2x*. A capacitor separates the transversal line current into DC (IT) and AC (ITAC) components. Because ITAC is the sensed transversal (also called metallic) current on the line, it includes both the receive and transmit components. *SLICOFI-2x* separates the receive and transmit components digitally, via a transhybrid circuit. **Figure 19** shows the signal paths for AC transmission between the SLICs and *SLICOFI-2x*:

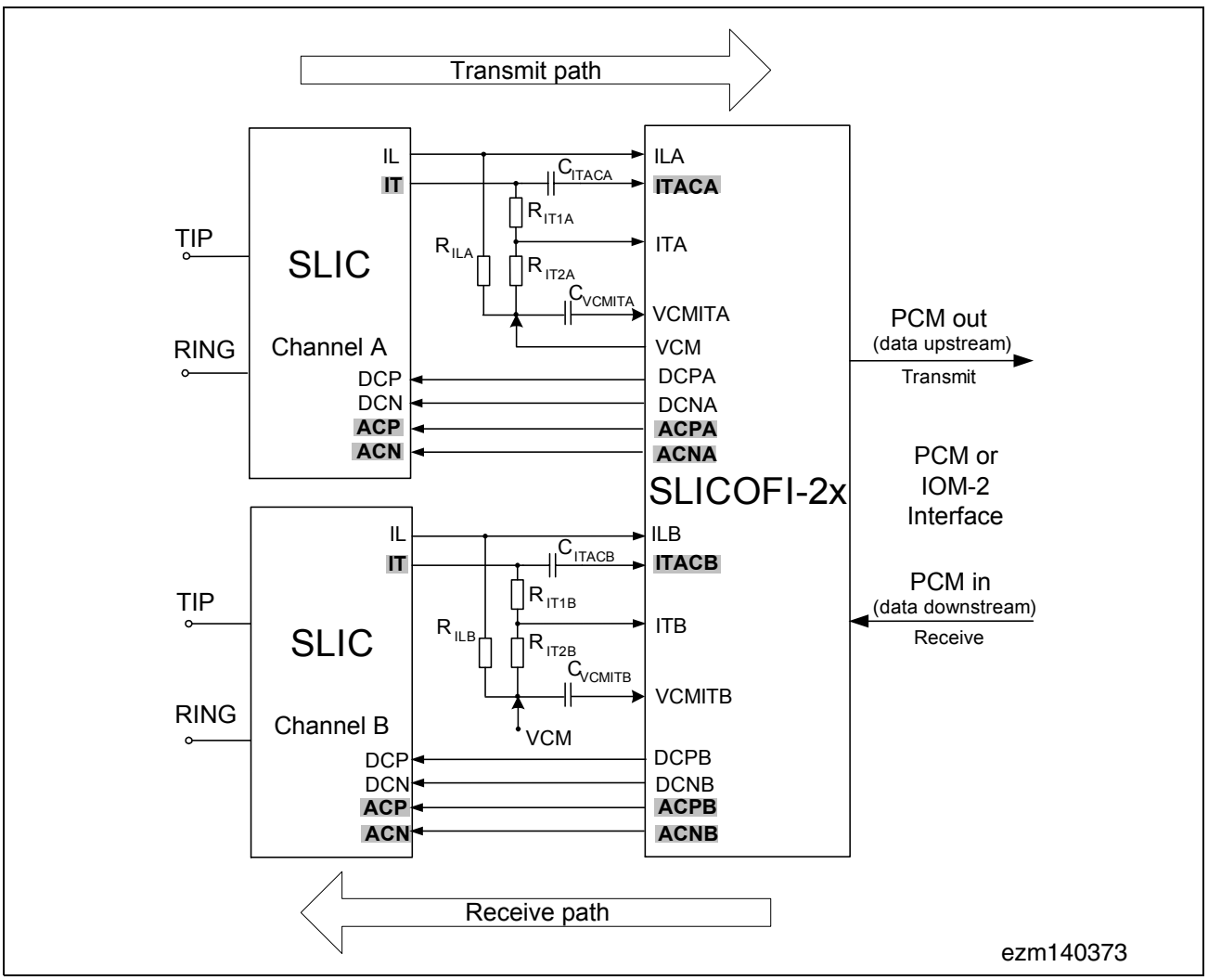


Figure 19 Signal Paths – AC Transmission

The signal flow within the *SLICOFI-2x* for one voice channel is shown in schematic circuitry of **Figure 20**. With the exception of a few analog filter functions, signal processing is performed digitally in the *SLICOFI-2x* codec.

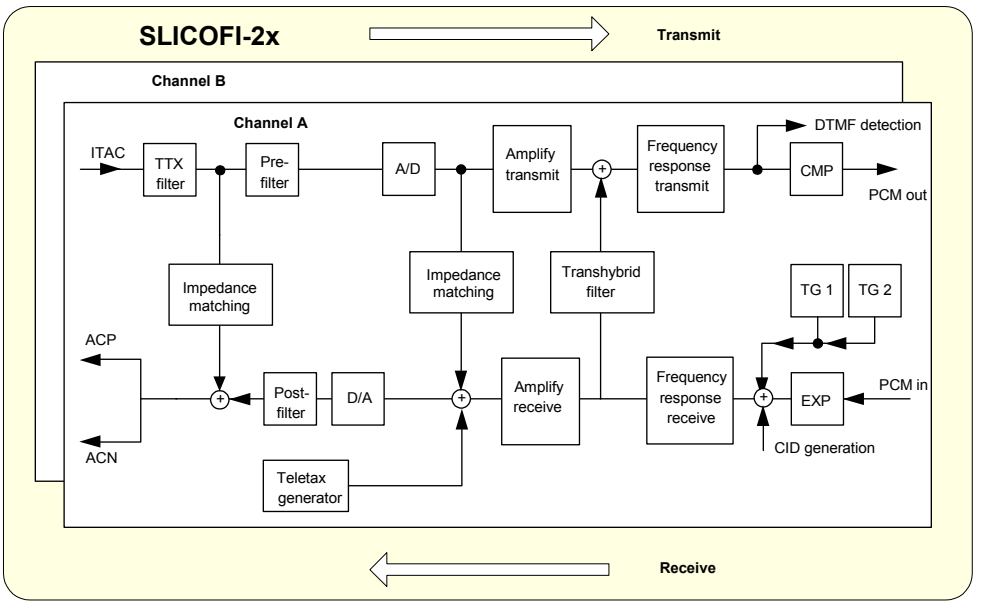


Figure 20 Signal Flow in Voice Channel (A)

2.4.1 Transmit Path

The current sense signal (ITAC) is converted to a voltage by an external resistor. This voltage is first filtered by an anti-aliasing filter (pre-filter) that stops producing noise in the voice band from signals near the A/D sampling frequency. A/D conversion is done by a 1-bit sigma-delta converter. The digital signal is down-sampled further and routed through programmable gain and filter stages. The coefficients for the filter and gain stages can be programmed to meet specific requirements. The processed digital signal goes through a compander (CMP) that converts the voice data into A-Law or µ-Law codes. A time slot assignment unit outputs the voice data to the programmed time slot. *SLICOFI-2x* can also operate in 16-bit linear mode for processing uncompressed voice data. In this case, two time slots are used for one voice channel.

2.4.2 Receive Path

The digital input signal is received via the IOM-2 or PCM Interface. Expansion (EXP), PCM low-pass filtering, frequency response correction, and gain correction are performed by the DSP. The digital data stream is up-sampled and converted to a corresponding analog signal. After smoothing by post-filters in the *SLICOFI-2x*, the AC signal is fed to the SLIC, where it is superimposed on the DC signal. The DC signal has been processed in a separate DC path. A TTX signal, generated digitally within *SLICOFI-2x* can also be added.

2.4.3 Matching

The SLIC outputs the voice signal to the line (receive direction) and also senses the voice signal coming from the subscriber. The AC impedance of the SLIC and the load impedance need to be matched to maximize power transfer and minimize two-wire return loss. The two-wire return loss is a measure of the impedance matching between a transmission line and the AC termination of DuSLIC.

Impedance matching is done digitally within the *SLICOFI-2x* by three integrated impedance matching feedback loops. The loops feed the transmit signal back to the receive signal simulating the programmed impedance through the SLIC. When calculating the feedback filter coefficients, the external resistors between the protection circuit and the SLIC ($R_{PRE} = R_{PROT} + R_{STAB}$, see **Figure 92**, **Page 357**) must be taken into account. The impedance can be programmed to any appropriate real and complex values shown in the Nyquist diagram **Figure 21**. This means that the device can be adapted to requirements anywhere in the world without requiring the hardware changes that are necessary with conventional linecard designs.

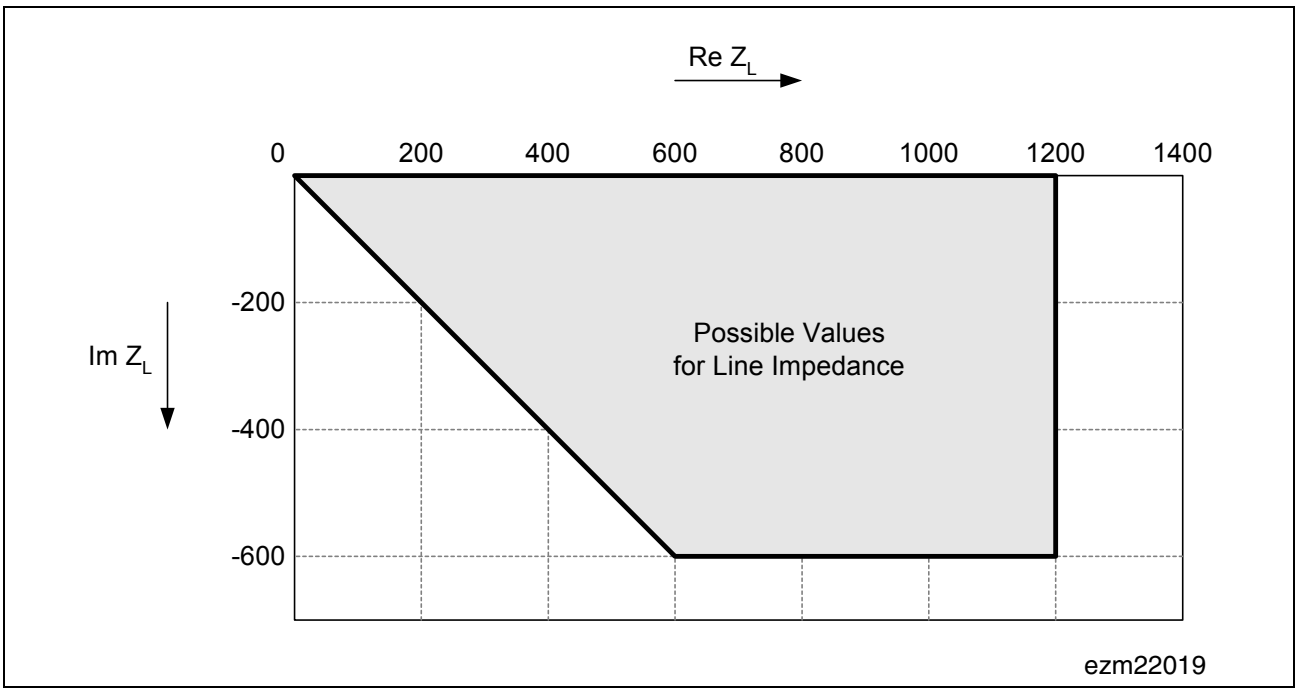


Figure 21 Nyquist Diagram

2.5 Ringing

Because of the 170 V technology used for the SLIC, a ringing voltage of up to 85 Vrms sinusoidal or up to 100 Vrms trapezoidal can be generated on-chip without the need for an external ringing generator (This is with 20 V offset. Higher ring amplitudes are possible if lower DC offset voltage is required.)

The *SLICOFI-2x* generates a sinusoidal ringing signal that causes less noise and cross-talk in neighboring lines than a trapezoidal ringing signal. The ringing frequency is programmable from 3 Hz to 300 Hz.

SLIC-E/-E2, SLIC-S/-S2 and SLIC-P support different ringing methods (see **Chapter 2.5.3**).

2.5.1 Ringer Load

A typical ringer load can be thought of as a resistor in series with a capacitor. Ringer loads are usually described as a Ringer Equivalence Number (REN) value. REN is used to describe the on-hook impedance of the terminal equipment and is actually a dimensionless ratio that reflects a certain load. REN definitions vary from country to country. A commonly used REN is described in FCC Part 68 that defines a single REN as either 5 kΩ, 7 kΩ, or 8 kΩ of AC impedance at 20 Hz. The impedance of an n-multiple REN is equivalent to parallel connection of n single RENs. In this manual, all references to REN assume the 7 kΩ model.

For example, a 1 REN and 5 REN load, typically used in the USA, would be:

Figure 22 Typical Ringer Loads of 1 and 5 REN used in USA

2.5.2 Ring Trip

After the subscriber has gone off-hook, the ringing signal must be removed within a specified time, and power must start feeding to the subscriber's phone. There are two ring trip methods: DC Ring Trip Detection and AC Ring Trip Detection.

DC Ring Trip Detection

Most applications that utilize the DuSLIC chip set use DC ring trip detection. By applying a DC offset together with the ringing signal, a transversal DC loop current starts to flow when the subscriber goes off-hook. This DC current is sensed by the SLIC and in this way is used as an off-hook criterion. The SLIC supplies this information to the *SLICOFI-2x* at the IT pin. The *SLICOFI-2x* continuously integrates the sensed line

current I_{TRANS} over one ringer period. This causes the integration result to represent the DC component of the ring current. If the DC current exceeds the programmed ring trip threshold, *SLICOFI-2x* generates an interrupt. Ring trip is reliably detected and reported within two ring signal periods. The ringing signal is switched off automatically at zero crossing by the *SLICOFI-2x*. The threshold for the ring trip DC current is set internally in the *SLICOFI-2x* and programmed via the digital interface. The DC offset for ring trip detection can be generated by the DuSLIC chip set and the internal ring trip function can be used even if an external ringing generator is used.

AC Ring Trip Detection

For short lines (< 1 kΩ loop length) and for low-power applications, the DC offset can be avoided to reduce the battery voltage for a given ring amplitude. Ring trip detection is done by rectifying the ring current I_{TRANS}, integrating it over one ringer period and comparing it to a programmable AC ring trip threshold. If the ring current exceeds the programmed threshold, the HOOK bit in register INTREG1 is set accordingly.

Most applications that utilize the DuSLIC chip set use the DC ring trip detection, which is more reliable than AC ring trip detection.

2.5.3 Ringing Methods

There are two methods of ringing:

- Balanced ringing (bridged ringing)
- Unbalanced ringing (divided ringing)

Internal balanced ringing generally offers more benefits compared to unbalanced ringing:

- Balanced ringing produces much less longitudinal voltage, which results in a lower amount of noise coupled into adjacent cable pairs (e.g. ADSL lines).
- By using a differential ringing signal, lower supply voltages become possible

The phone itself cannot distinguish between balanced and unbalanced ringing. Where unbalanced ringing is still used, it is often simply an historical leftover. For a comparison between balanced and unbalanced ringing, see also ANSI document T1.401-1993.

Additionally, integrated ringing with the DuSLIC offers the following advantages:

- Internal ringing (no need for external ringing generator and relays)
- Reduction of board space because of much higher integration and fewer external components
- Programmable ringing amplitude, frequency, and ringing DC offset without hardware changes
- Programmable ring trip thresholds
- Switching of the ringing signal at zero-crossing. With relays there is always some residual switching noise, which can cause interference on adjacent cable pairs (e.g. ADSL).

2.5.4 DuSLIC Ringing Options

Application requirements differ with regard to ringing amplitudes, power requirements, loop length, and loads. The DuSLIC options include three different SLICs to ensure the most appropriate ringing methods (see **Table 5**) for these applications:

Table 5 Ringing Options with SLIC-S, SLIC-E/-E2 and SLIC-P

SLIC Version/ Ringing Facility, Battery Voltages	SLIC-S PEB 4264	SLIC-E/-E2 PEB 4265 PEB 4265-2	SLIC-P PEB 4266
Internal max. balanced ringing voltage in Vrms [with 20 V_{DC} used for ring trip detection]			
sinusoidal	45 Vrms	85 Vrms	85 Vrms
trapezoidal	53 Vrms	100 Vrms	100 Vrms
DC voltage for balanced ringing[1]	programmable typ. 0 … 50 V	programmable typ. 0 … 50 V	programmable typ. 0 … 50 V
Internal unbalanced ringing max. voltage in Vrms			
sinusoidal	NO	NO	50 Vrms
trapezoidal	NO	NO	58 Vrms
DC voltage for unbalanced ringing	NO	NO	$V_{BATR}/2$
Required SLIC supply voltages for maximum ringing amplitude (typically)	V_{DD} = 5 V[2], V_{DD} = 3.3 V[3] V_{BATH} = –54 V, V_{HR} = 36 V	V_{DD} = 5 V, V_{BATH} = –70 V, V_{HR} = 80 V	V_{DD} = 5 V or 3.3 V, V_{BATH} = –48 V, V_{BATR} = –150 V
Number of battery voltages for power saving	2 (V_{BATL} & V_{BATH})	2 (V_{BATL} & V_{BATH})	2 (when internal ringing is used) 3 (when external ringing is used)

1) In most applications, 20 V_{DC} are sufficient for reliable ring trip detection. A higher DC voltage will reduce the achievable maximum ringing voltage. For short loops, 10 V_{DC} may be sufficient.

2) 170 V technology

3) 90 V technology

SLIC-S allows balanced ringing up to 45 Vrms and is dedicated to short loop or PBX applications.

For SLIC-S2, only external ringing is provided.

SLIC-E/-E2 allows balanced ringing up to 85 Vrms and can, therefore, be used in systems with higher loop impedance.

The low-power SLIC-P is optimized for power-critical applications (such as intelligent ISDN network termination). Internal ringing can be used up to 85 Vrms balanced or 50 Vrms unbalanced. For lowest power applications where external ringing is preferred, three different battery voltages (V_{BATR}, V_{BATH}, V_{BATL}) can be used to optimize the power consumption of the application.[1)]

SLIC-E/-E2 and SLIC-P differ in supply voltage configuration and the ring voltages at Tip and Ring V_T and V_R. External ringing is supported by both SLICs.

Both internal and external ringing are activated by switching the DuSLIC to ringing mode by setting the CIDD/CIOP[2)] bits M2, M1, M0 to 101 (see **"Overview of all DuSLIC Operating Modes" on Page 74**).

External Ringing Support by DuSLIC

The following settings must be made:

- Enable the use of an external ring signal generator by setting bit REXT-EN in register BCR2 to 1.
- A TTL compatible zero crossing signal must be applied to the RSYNC pin of the *SLICOFI-2x* (see **Figure 23**).
- Activate the ringing mode by setting the CIDD/CIOP bits M2, M1, M0 to 101.
- Set the DuSLIC internal ring frequency to a value according a factor of approximately 0.75 of the external ring frequency.

The ring relay is controlled by the IO1 pin (see **Figure 92**). Due to the high current drive capability of the IO1 output, no additional relay driver is necessary.

The relay is switched either synchronously or asynchronously as follows:

- **Synchronous** to the zero crossing of the external ringing frequency
  (bit ASYNCH-R in register XCR set to 0)

A ring generator delay $T_{RING,DELAY}$ (see DuSLICOS control parameters 2/4) can be programmed to consider the ring relay delay $T_{RING-RELAY,DELAY}$ as shown in **Figure 23**.

- **Asynchronous**
  (bit ASYNCH-R in register XCR set to 1)

The ring relay is switched immediately with the ring command.

1) In this case, V_{BATR} is typically used for the on-hook state, while V_{BATH} and V_{BATL} are used for optimized feeding of different loop lengths in the off-hook state.

2) CIDD = Data Downstream Command/Indication Channel Byte (IOM-2 interface)
CIOP = Command/Indication Operation

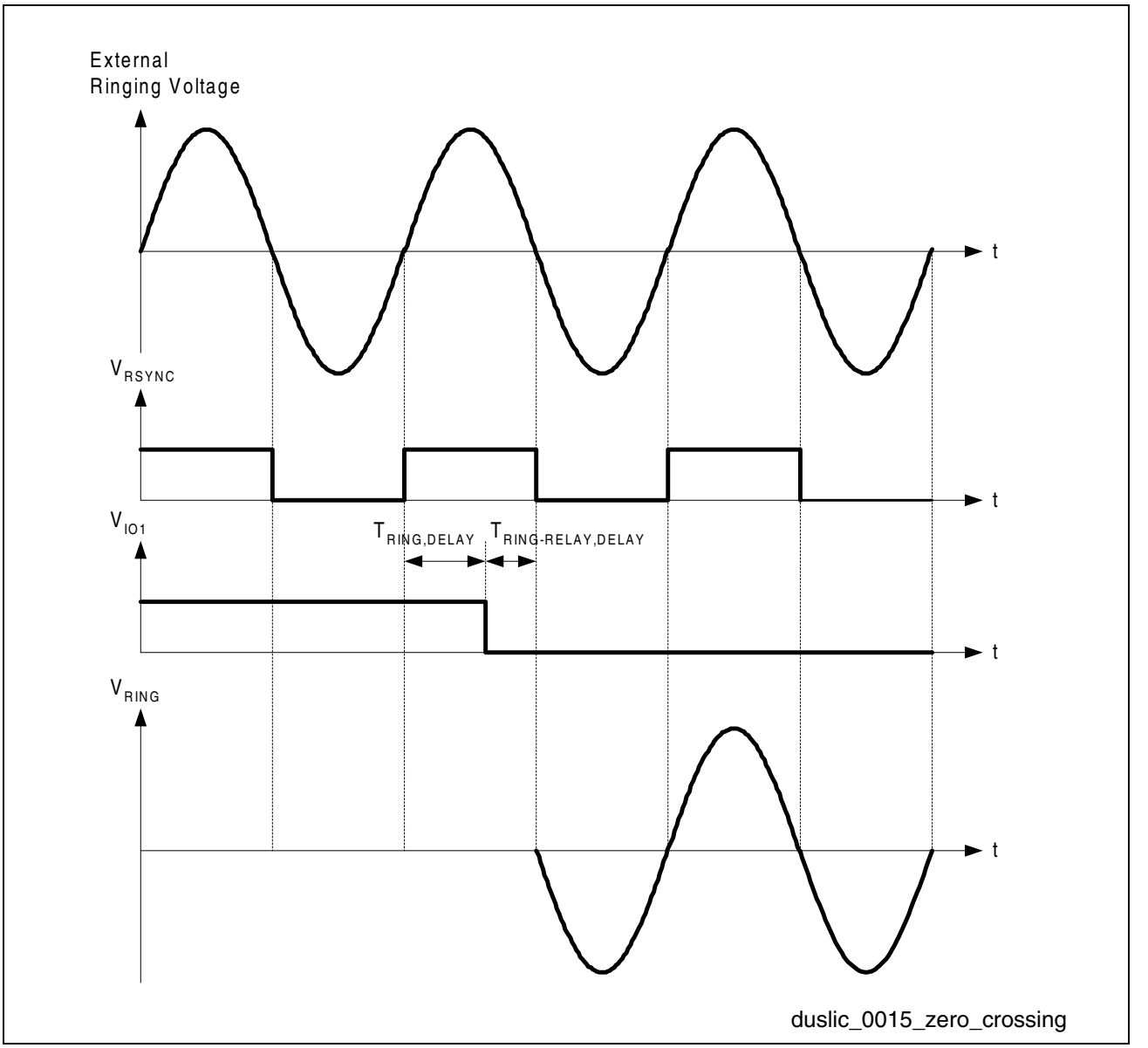


Figure 23 External Ringing Zero Crossing Synchronization

2.5.5 Internal Balanced Ringing via SLICs

SLIC-E/-E2 and SLIC-P support internal balanced ringing up to $V_{RING,RMS}$ = 85 Vrms, while SLIC-S supports balanced ringing up to $V_{RING,RMS}$ = 45 Vrms[1].

The ringing signal is generated digitally within the *SLICOFI-2x*.

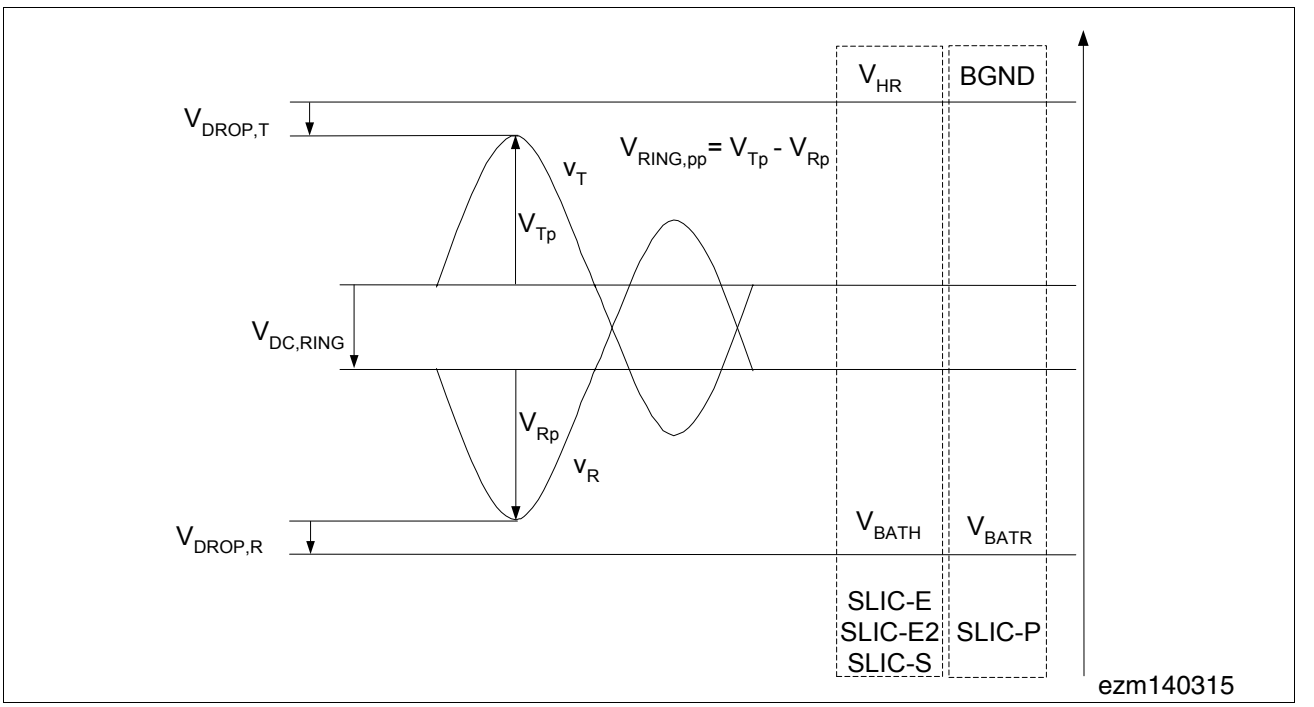


Figure 24 Balanced Ringing via SLIC-E/-E2, SLIC-S and SLIC-P

In ringing mode, the DC feeding regulation loop is not active. A programmable DC ring offset voltage is applied to the line instead. During ring bursts, the ringing DC offset and the ringing signal are summed digitally within *SLICOFI-2x* in accordance with the programmed values. This signal is then converted to an analog signal and is applied to the SLIC. The SLIC amplifies the signal and supplies the line with ringing voltages up to 85 Vrms. In balanced ringing mode, the SLIC uses an additional supply voltage V_{HR} for SLIC-E/-E2/-S and V_{BATR} for SLIC-P. The total supply span is now $V_{HR} - V_{BATH}$ for SLIC-E/-E2/-S and V_{BATR} for SLIC-P.

The maximum ringing voltage that can be achieved is:

for SLIC-E/-E2/-S: $V_{RING,RMS} = (V_{HR} - V_{BATH} - V_{DROP,TR} - V_{DC,RING})/1.41$

for SLIC-P: $V_{RING,RMS} = (-V_{BATR} - V_{DROP,TR} - V_{DC,RING})/1.41$

where: $V_{DROP,TR} = V_{DROP,T} + V_{DROP,R}$

1) In this case $V_{RING,RMS} = V_{TR,RMS} = V_{TR0,RMS}$ because of the low impedance of the SLIC output (< 1 Ω). $V_{TR,RMS}$ is the open-circuit rms voltage measured directly at pins RING and TIP at the SLIC output with ringer load. $V_{TR0,RMS}$ is the rms voltage measured directly at pins RING and TIP at the SLIC output without any ringer load. For calculation of the ringing voltage at the ringer load, see the Application Note *DuSLIC Voltage and Power Dissipation Calculation* and its accompanying MS Excel Sheet for calculation.

Using the DuSLIC chip set, ringing voltages up to 85 Vrms sinusoidal can be applied, and trapezoidal ringing can be programmed as well.
For a detailed application diagram of internal balanced ringing see **Figure 90** on **Page 353**.

2.5.6 Internal Unbalanced Ringing with SLIC-P

The internal unbalanced ringing supported by SLIC-P can be used for ringing voltages up to 50 Vrms. The SLICOFI-2 integrated ringing generator is used and the ringing signal is applied to either the Tip or Ring line. Ringing signal generation is the same as described above for balanced ringing. As only one line is used for ringing, technology limits the ringing amplitude to about half the value of balanced ringing, to a maximum of 50 Vrms.

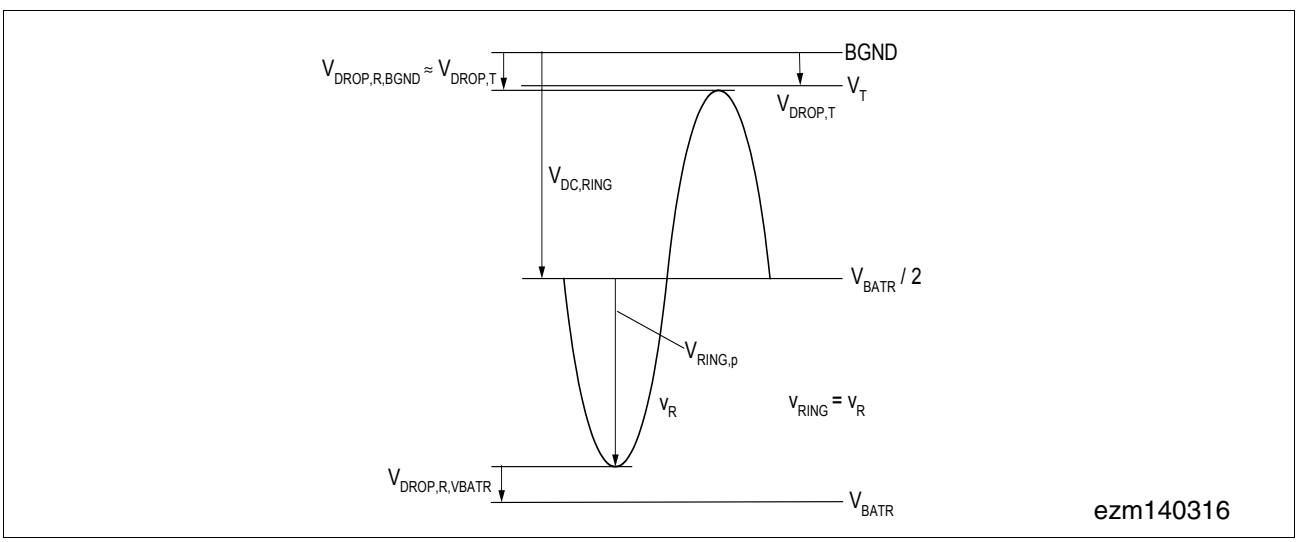


Figure 25 Unbalanced Ringing Signal

Figure 25 shows an example with the Ring line used for ringing and the Tip line fixed at $-V_{DROP,T}$ which is the drop in the output buffer of the Tip line of SLIC-P (typ. < 1 V). The ring line has a fixed DC voltage of $V_{BATR}/2$ used for ring trip detection.

The maximum ringing voltage is:

$V_{RING,RMS} = (-V_{BATR} - V_{DROP,R,VBATR} - V_{DROP,T})/2.82$

When the called subscriber goes off-hook, a DC path is established from the Ring to the Tip line. The DC current is recognized by the SLICOFI-2 because it monitors the IT pin. An interrupt indicates ring trip if the line current exceeds the programmed threshold.

The same hardware can be used for integrated balanced or unbalanced ringing. The balanced and unbalanced modes are configured by software. The maximum achievable amplitudes depend on the values selected for V_{BATR}.

In both balanced and unbalanced ringing modes, SLICOFI-2 automatically applies and removes the ringing signal during zero-crossing. This reduces noise and cross-talk to adjacent lines.

2.5.7 External Unbalanced Ringing

SLICOFI-2x supports external (balanced or unbalanced) ringing for higher ringing voltage requirements with all SLIC versions. In this case, the integrated ring trip functionality of the DuSLIC may be used. For a detailed application diagram of unbalanced ringing, see **Figure 92** (**Page 357**) and **Figure 94** (**Page 359**).

Because high voltages are involved, an external relay should be used to switch the RING line off and to switch the external ringing signal together with a DC voltage to the line. The DC voltage must be applied for the internal ring trip detection mechanism that operates for external ringing in the same way as for internal ringing.

The *SLICOFI-2x* must be set to the external ringing mode by the REXT-EN bit in register BCR2. A synchronization signal of the external ringer is applied to the *SLICOFI-2x* via the RSYNC pin. The external relay is switched on or off synchronously to this signal via the IO1 pin of the *SLICOFI-2x*, according to the actual mode of the DuSLIC. An interrupt is generated if the DC current exceeds the programmed ring trip threshold.

2.6 Signaling (Supervision)

Signaling in the subscriber loop is monitored internally by the DuSLIC chip set.

Supervision is performed by sensing the longitudinal and transversal line currents on the Ring and Tip wires. The scaled values of these currents are generated in the SLIC and are fed to the *SLICOFI-2x* via the IT and IL pins.

Transversal line current: $I_{TRANS} = (I_R + I_T)/2$

Longitudinal line current: $I_{LONG} = (I_R - I_T)/2$

where I_R, I_T are the loop currents on the Ring and Tip wires.

Off-hook Detection

Loop start signaling is the most common type of signaling. The subscriber loop is closed by the hook switch inside the subscriber equipment.

- In Active mode, the resulting transversal loop current is sensed by the internal current sensor in the SLIC. The IT pin of the SLIC indicates the subscriber loop current to the *SLICOFI-2x*. External resistors (R_{IT1}, $R_{IT2,}$ see **Figure 90** on **Page 353**) convert the current information to a voltage on the ITA (or ITB) pin.
  The analog information is first converted to a digital value. It is then filtered and processed further which effectively suppresses line disturbances. If the result exceeds a programmable threshold, an interrupt is generated to indicate off-hook detection.

- In Sleep/Power Down mode (PDRx), a similar mechanism is used. In this mode, the internal current sensor of the SLIC is switched off to minimize power consumption. The loop current is therefore fed and sensed through 5 kΩ resistors integrated within the SLIC. The information is made available on the IT pin and is interpreted by the *SLICOFI-2x*.

– In Sleep mode, the analog information is fed to an analog comparator integrated within the *SLICOFI-2x* that directly indicates off-hook.
– In Power Down mode, the *SLICOFI-2x* converts the analog information to a digital value. It is then filtered and processed further to effectively suppress line disturbances. If the result exceeds a programmable threshold, an interrupt is generated to indicate off-hook detection.

In applications using ground start signaling, DuSLIC can be set to the ground start mode. In this mode, the Tip wire is switched to high impedance mode. Ring ground detection is performed by the internal current sensor in the SLIC and is transferred to the *SLICOFI-2x* via the IT pin.

Ground Key Detection

The scaled longitudinal current information is transferred from the SLIC via the IL pin and the external resistor R_{IL} to *SLICOFI-2x*. This voltage is compared with a fixed threshold value. For the specified R_{IL} (1.6 kΩ, see application circuit **Figure 90**, **Page 353**) this threshold corresponds to 17 mA (positive and negative). After further post-processing, this information generates an interrupt (GNDK bit in the INTREG1 register) and ground key detection is indicated.

The polarity of the longitudinal current is indicated by the GNKP bit in the INTREG1 register. Each change of the GNKP bit generates an interrupt. Both bits (GNDK, GNKP) can be masked in the MASK register.

The post-processing is performed to guarantee ground key detection, even if longitudinal AC currents with frequencies of $16^2/_3$, 50 or 60 Hz are superimposed. The time delay between triggering the ground key function and registering the ground key interrupt will be less than 40 ms in most cases (f = 50 Hz, 60 Hz).

For longitudinal DC signals, the blocking period can be programmed by the Data Upstream Persistence Counter end value (DUP) in register IOCTL3. DC signals with less duration will not be detected. The DUP time is equivalent to the half of the cycle time for the lowest frequency for AC suppression (for values see register IOCTL3 on **Page 166**).

In Power Down mode, the SLIC's internal current sensors are switched off and ground key detection is disabled.

2.7 Metering

One of two different metering methods may be specified:

- Metering by sinusoidal bursts of either 12 kHz or 16 kHz
- Polarity reversal of Tip and Ring.

2.7.1 Metering by 12/16 kHz Sinusoidal Bursts

To satisfy worldwide application requirements, SLICOFI-2/-2S offers integrated metering injection of either 12 or 16 kHz signals with programmable amplitudes. SLICOFI-2/-2S also has an integrated adaptive TTX notch filter and can switch the TTX signal to the line in a smooth way. When switching the signal to the line, the switching noise is less than 1 mV. **Figure 26** shows TTX bursts at certain points of the signal flow within SLICOFI-2/-2S.

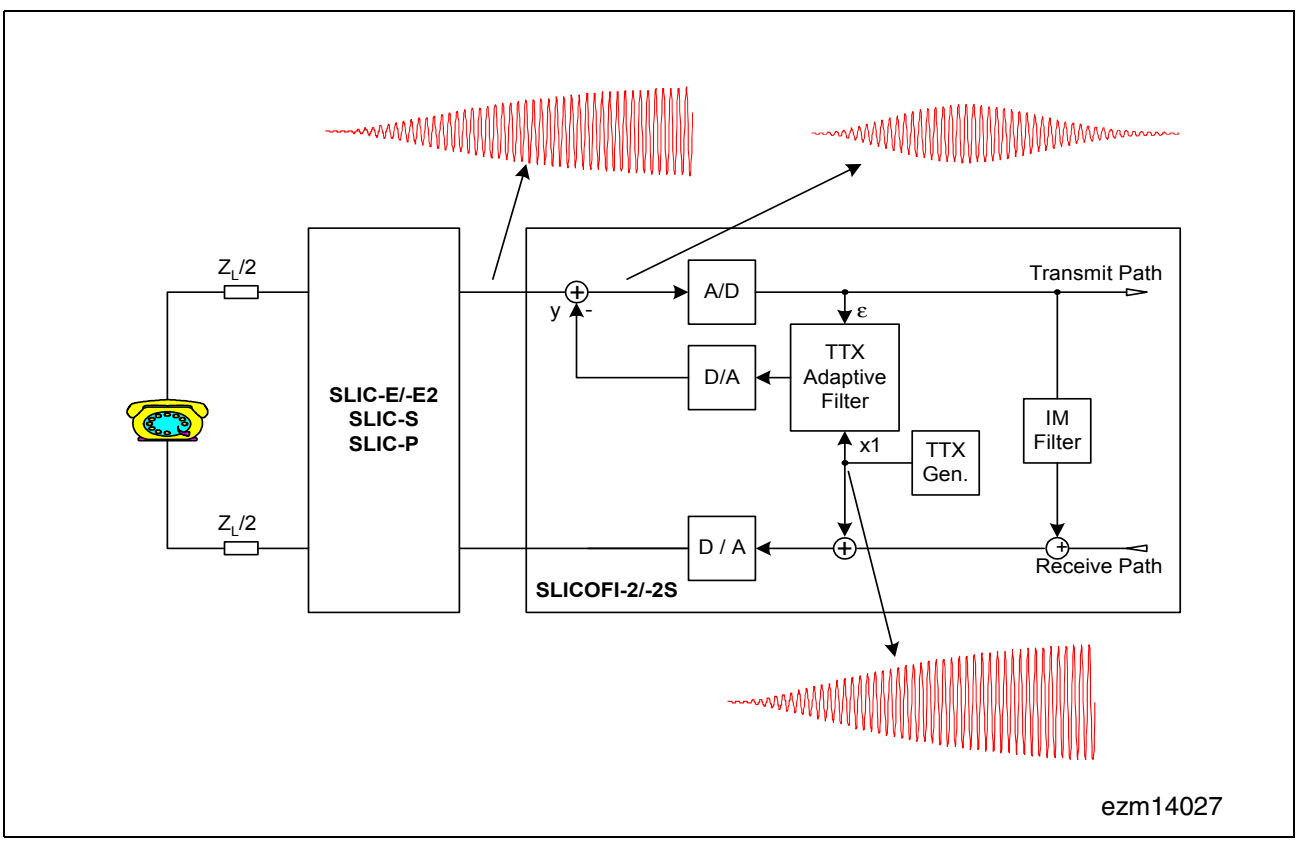


Figure 26 Teletax Injection and Metering

The integrated, adaptive TTX notch filter guarantees an attenuation of > 40 dB. No external components for filtering TTX bursts are required.

2.7.2 Metering by Polarity Reversal

SLICOFI-2/-2S also supports metering by polarity reversal by changing the actual polarity of the voltages on the TIP/RING lines. Polarity reversal is activated by switching the REVPOL bit in register BCR1 to one or by switching to the “Active with Metering” mode by the CIDD or CIOP command (see **“Overview of all DuSLIC Operating Modes” on Page 74**).

2.7.2.1 Soft Reversal

Some applications require a smooth polarity reversal (soft reversal), as shown in **Figure 27**. Soft reversal helps prevent negative effects such as non-required ringing. Soft reversal is deactivated by the SOFT-DIS bit in register BCR2.

SOFT-DIS = 1 Immediate reversal is performed (hard reversal)

SOFT-DIS = 0 Soft reversal is performed. Transition time (time from START to SR-END1, see **Figure 27**) is programmable by CRAM coefficients; default value is 80 ms.

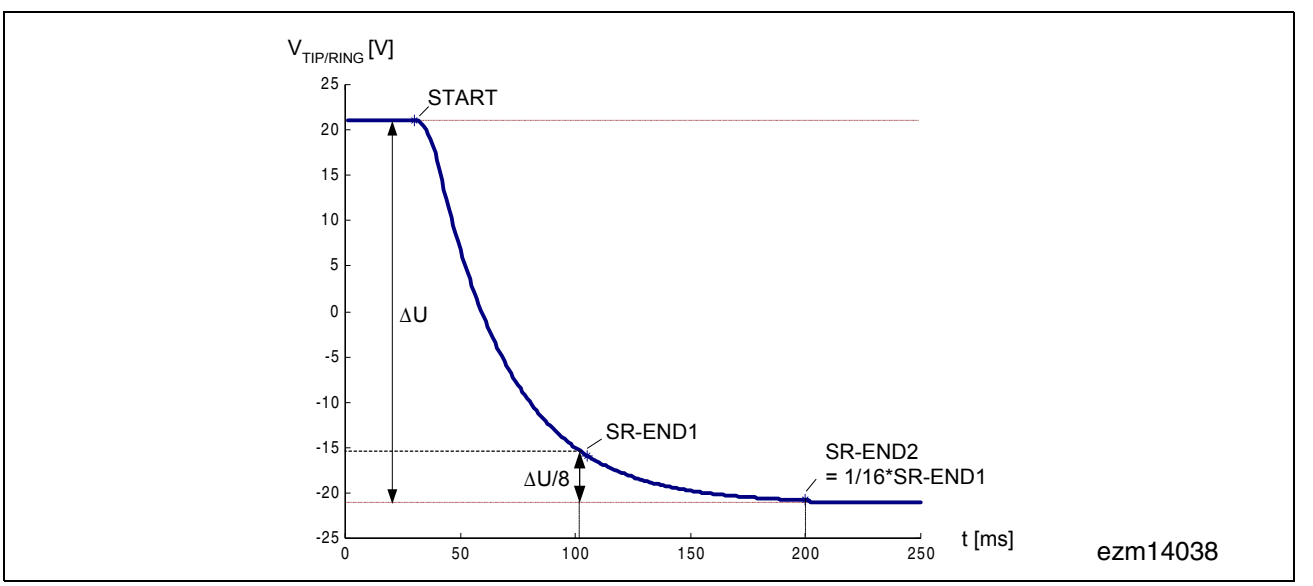


Figure 27 Soft Reversal (Example for Open Loop)

START: The soft ramp starts by setting the REVPOL bit in register BCR1 to 1. The DC characteristic is switched off.
SR-END1: At the soft reversal end one point, the DC characteristic is switched on again. Programmable by the DuSLICOS software, such as ΔU/8.
SR-END2: At the soft reversal end two point, the soft ramp is switched off. Programmable by the DuSLICOS software, such as 1/16 × SR-END1.
From START to SR-END2 the READY bit in register INTREG2 is set to 0 (see register description in **Chapter 5.3.1.2** for further information).

2.8 DuSLIC Enhanced Signal Processing Capabilities

The signal processing capabilities described in this section are implemented by an Enhanced Digital Signal Processor (EDSP), with the exception of DTMF generation. Each function can be individually enabled or disabled for each DuSLIC channel. Therefore, power consumption can be reduced according to the needs of the application. For the MIPS requirements of the different EDSP algorithms see **Chapter 2.8.6**.

Figure 28 shows the AC signal path for DuSLIC with the ADCs and DACs, impedance matching loop, trans-hybrid filter, gain stages, and the connection to the EDSP.

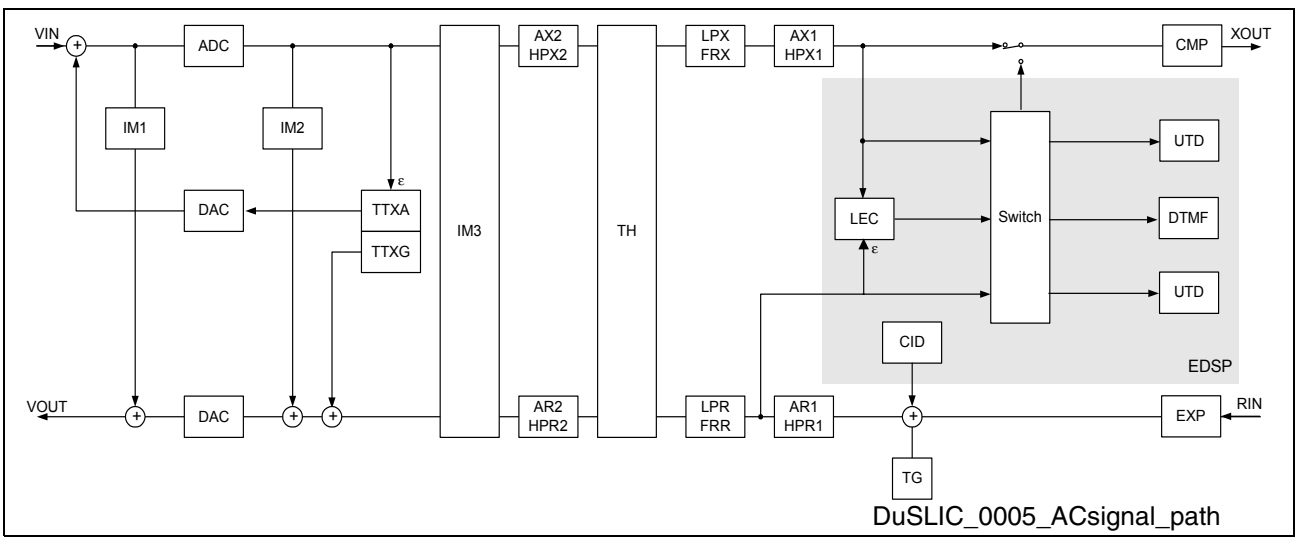


Figure 28 DuSLIC AC Signal Path

Figure 29 shows a close-up on the EDSP signal path shown in **Figure 28** identifying signal names and SOP commands.

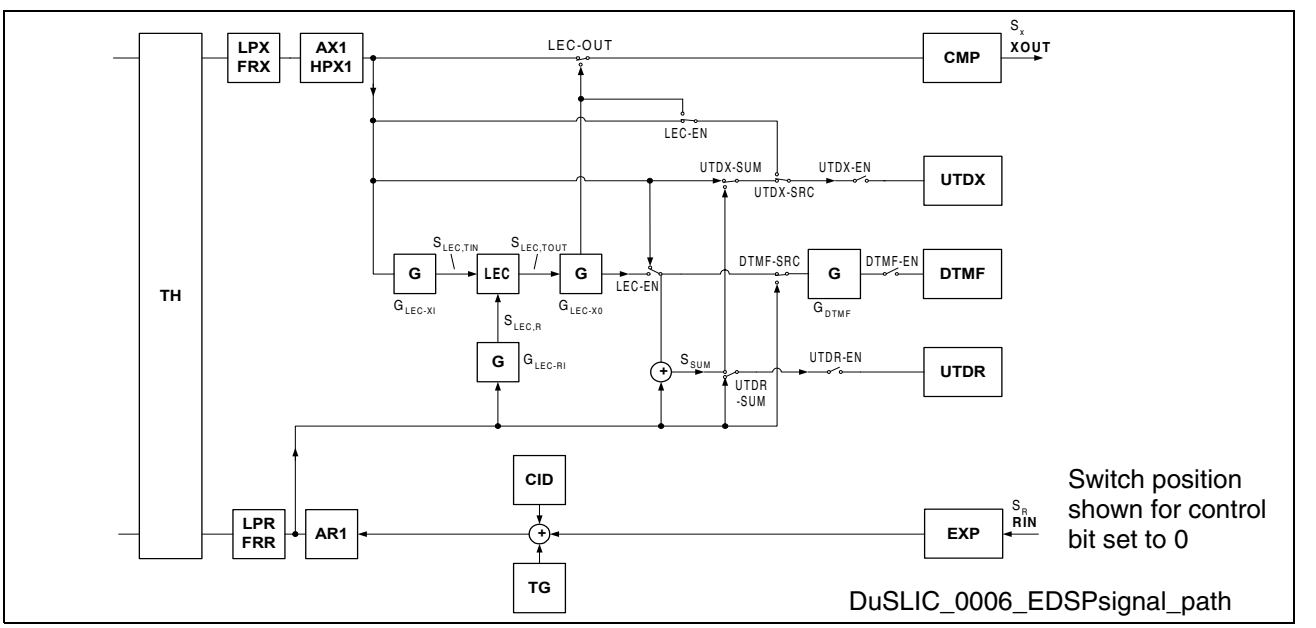


Figure 29 DuSLIC EDSP Signal Path

The enhanced Signal Processing capabilities are available only for the DuSLIC-E/-E2/-P versions, with an exception of DTMF generation.

The DTMF generation is available for all DuSLIC versions.

The functions of the EDSP are configured and controlled by POP register settings (see **Chapter 5.2.3**).

2.8.1 DTMF Generation and Detection

Dual Tone Multi-Frequency (DTMF) is a signaling scheme using voice frequency tones to signal dialing information. A DTMF signal is the sum of two tones, one from a low group (697–941 Hz) and one from a high group (1209–1633 Hz), with each group containing four individual tones. This scheme allows sixteen unique combinations. Ten of these codes represent the numbers from zero through nine on the telephone keypad, the remaining six codes (*, #, A, B, C, D) are reserved for special signaling. The buttons are arranged in a matrix, with the rows determining the low group tones, and the columns determining the high group tone for each button.

In all *SLICOFI-2x* codec versions, the sixteen standard DTMF tone pairs can be generated independently in each channel via two integrated tone generators. Alternatively, the frequency and amplitude of the tone generators can be programmed individually via the digital interface. Each tone generator can be switched on and off. The generated DTMF tone signals meet the frequency variation tolerances specified in the ITU-T Q.23 recommendation.

Both Channels A and B of SLICOFI-2[1)] have a powerful built-in DTMF decoder that will meet most national requirements. The receiver algorithm performance meets the quality criteria for central office/exchange applications. It complies with the requirements of ITU-T Q.24, Bellcore GR-30-CORE (TR-NWT-000506), and Deutsche Telekom network (BAPT 223 ZV 5, Approval Specification of the Federal Office for Post and Telecommunications, Germany), among others.

Note: DTMF Detection is only available for DuSLIC-E/-E2/-P

The performance of the algorithm can be adapted according to the needs of the application via the digital interface (detection level, twist, bandwidth, and center frequency of the notch filter).

Table 6 shows the performance characteristics of the DTMF decoder algorithm:

Table 6 Performance Characteristics of the DTMF Decoder Algorithm

No.	Characteristic	Value	Notes
1	Valid input signal detection level	–48 to 0 dBm0	Programmable
2	Input signal rejection level	–5 dB of valid signal detection level	–
3	Positive twist accept	< 8 dB	Programmable
4	Negative twist accept	< 8 dB	Programmable
5	Frequency deviation accept	< ±(1.5% + 4 Hz) and < ±1.8%	Related to center frequency
6	Frequency deviation reject	> ±3%	Related to center frequency
7	DTMF noise tolerance (could be the same as 14)	–12 dB	dB referenced to lowest amplitude tone
8	Minimum tone accept duration	40 ms	–
9	Maximum tone reject duration	25 ms	–
10	Signaling velocity	≥ 93 ms/digit	–
11	Minimum inter-digit pause duration	40 ms	–
12	Maximum tone drop-out duration	20 ms	–
13	Interference rejection 30 Hz to 480 Hz for valid DTMF recognition	Level in frequency range 30 Hz … 480 Hz ≤ level of DTMF frequency +22 dB	dB referenced to lowest amplitude tone
14	Gaussian noise influence Signal level –22 dBm0, SNR = 23 dB	Error rate better than 1 in 10000	–
15	Pulse noise influence Impulse noise tape 201 according to Bellcore TR-TSY-000762	Error rate better than 14 in 10000	measured with DTMF level –22 dBm0 Impulse Noise –10 dBm0 and –12 dBm0

In the event of pauses < 20 ms:

- If the pause is followed by a tone pair with the same frequencies as before, this is interpreted as drop-out.
- If the pause is followed by a tone pair with different frequencies and if all other conditions are valid, this is interpreted as two different numbers.

DTMF decoders can be switched on or off individually to reduce power consumption. In normal operation, the decoder monitors the Tip and Ring wires via the ITAC pins (transmit path). Alternatively, the decoder can also be switched in the receive path. On detection of a valid DTMF tone pair, SLICOFI-2 generates an interrupt via the appropriate INT pin and indicates a change of status. The DTMF code information is provided by a register that is read via the digital interface.

The DTMF decoder also has excellent speech-rejection capabilities and complies with Bellcore TR-TSY-000763. The algorithm has been fully tested with the speech sample sequences in the Series-1 Digit Simulation Test Tapes for DTMF decoders from Bellcore. The characteristics of DTMF detection can be controlled by POP registers 30h to 39_H.

2.8.2 Caller ID Generation in DuSLIC-E/-E2/-P

A generator to send calling line identification (Caller ID, CID) is integrated in the DuSLIC-E/-E2/-P chip set. Caller ID is a generic name for the service provided by telephone utilities that supply information such as the telephone number or the name of the calling party to the called subscriber at the start of a call. In call waiting, the Caller ID service supplies information about a second incoming caller to a subscriber already busy with a phone call.

In typical Caller ID systems, the coded calling number information is sent from the central exchange to the called phone. This information can be shown on a display on the subscriber telephone set. In this case, the Caller ID information is usually displayed before the subscriber decides to answer the incoming call. If the line is connected to a computer, caller information can be used to search in databases and additional services can be offered.

There are two methods used for sending CID information depending on the application and country-specific requirements:

- Caller ID generation using DTMF signaling (see **Chapter 2.8.1**)
- Caller ID generation using FSK

DuSLIC-E/-E2/-P contains DTMF generation units and FSK generation units that can be used for both channels simultaneously.

The characteristics of the Caller ID generation circuitry can be controlled by POP registers 00_H, 43_H to $4A_H$.

DuSLIC-E/-E2/-P FSK Generation

Different countries use different standards to send Caller ID information.
The DuSLIC-E/-E2/-P chip set is compatible with the widely used Bellcore GR-30-CORE, British Telecom (BT) SIN227, SIN242, and the UK Cable Communications Association (CCA) specification TW/P&E/312 standards. Continuous phase binary Frequency Shift Keying (FSK) modulation is used for coding that is compatible with BELL 202 (see **Table 7**) and ITU-T V.23, the most common standards. The SLICOFI-2 can be easily adapted to these requirements by programming via the microcontroller interface. Coefficient sets are provided for the most common standards.

Table 7 FSK Modulation Characteristics

Characteristic	ITU-T V.23	Bell 202
Mark (Logic 1)	1300 ± 3 Hz	1200 ± 3 Hz
Space (Logic 0)	2100 ± 3 Hz	2200 ± 3 Hz
Modulation	FSK	
Transmission rate	1200 ± 6 baud	
Data format	Serial binary asynchronous	

The Caller ID data of the calling party can be transferred via the microcontroller interface into a SLICOFI-2 buffer register. The SLICOFI-2 will start sending the FSK signal when the CIS-EN bit is set and the CID-data buffer is filled up to CIS-BRS plus 1 byte. The data transfer into the buffer register is handled by a SLICOFI-2 interrupt signal. Caller data is transferred from the buffer via the interface pins to the SLIC-E/-E2/-P and is fed to the Tip and Ring wires. The Caller ID data bytes from the CID-data buffer are sent with the Least Significant Bit (LSB) first.

DuSLIC-E/-E2/-P offers two different levels of framing:

- A basic low-level framing mode

  All the data necessary to implement the FSK data stream—including channel seizure, mark sequence, and framing for the data packet or checksum—must be configured by firmware. SLICOFI-2 transmits the data stream in the same order in which the data is written to the buffer register.

- A high-level framing mode

  The number of channel seizure and mark bits can be programmed and are automatically sent by the DuSLIC-E/-E2/-P. Only the data packet information must be written into the CID buffer. Start and stop bits are automatically inserted by the SLICOFI-2.

The example below shows the signaling of a CID on-hook data transmission in accordance with Bellcore specifications. The Caller ID information applied on Tip and Ring is sent during the period between the first and second ring burst.

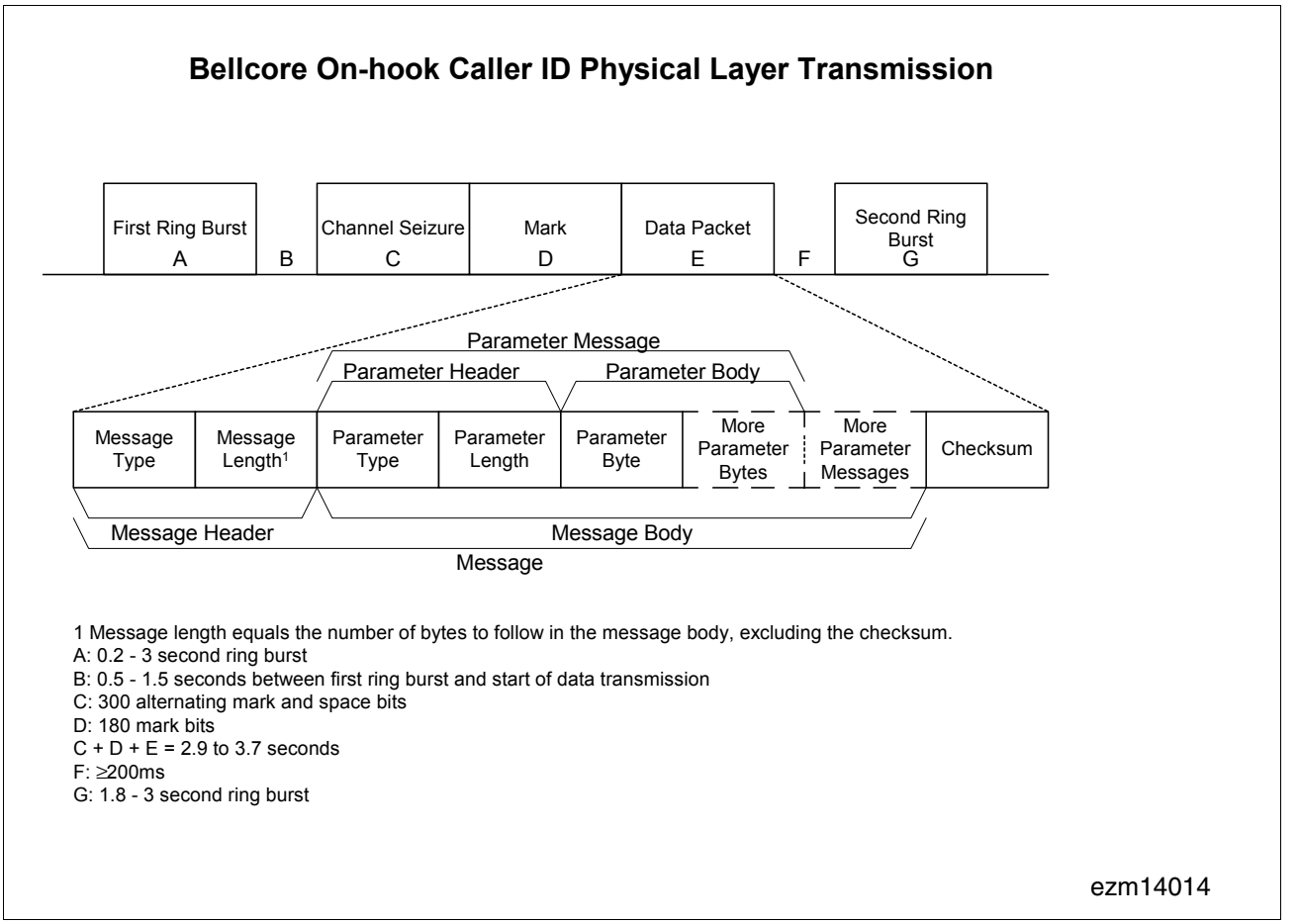


Figure 30 Bellcore On-Hook Caller ID Physical Layer Transmission

Note: As a CID transmission is an on-hook transmission the DuSLIC has to be programmed to Actice Mode.

2.8.2.1 Caller ID Buffer Handling of SLICOFI-2

This section describes the handling of the Caller ID buffer and the corresponding handshake bits in the interrupt registers.

Programming Sequence

In order to send Caller ID information over the telephone line, the following sequence should be programmed between the first and the second ring burst. The initialization part of the coefficients in the POP registers 43h to 4Ah must be done prior to that sequence.

1. Enable the extended feature DSP in register XCR (EDSP-EN = 1)
2. Enable the Caller ID sender feature in register BCR5 (CIS-EN = 1)
3. Wait for an interrupt.
4. Read out all 4 interrupt registers to serve the interrupt and check the CIS-REQ bit.

5. If this bit is set, write at least BRS + 2 bytes (see POP register CIS-BRS) of Caller ID data but not more than 48 bytes to the Caller ID sender buffer register CIS-DAT.
6. Wait for the next interrupt and check again the CIS-REQ bit.
7. If this bit is set, send the next data to the Caller ID-data buffer but not more than (48 – BRS) bytes. CIS-REQ bit gets reset to 0, if the data buffer is filled again above the Caller ID sender buffer request size (BRS).
8. Repeat steps 6 and 7 as long as there is data to be sent.
9. Immediately after sending the last Caller ID data bit to the Caller ID sender buffer, set the bit CIS-AUTO to 1 and subsequently, after a time delay of at least 500 µs, the bit CIS-EN to 0. After processing the last bit, the Caller ID sender will stop automatically and reset the CIS-ACT bit in register INTREG4 to 0. No more CIS interrupts will be generated until the Caller ID sender is enabled again (interrupt bits: CIS-BOF, CIS-BUF and CIS-REQ).

The end of the CID transmission can also be controlled by not setting CIS-AUTO and leaving CIS-EN at 1. If the Caller ID buffer becomes empty, an interrupt is generated to indicate buffer underflow (CIS-BUF). If CIS-BUF is set, reset CIS-EN to 0 with at least 1 ms delay, in order to allow to send the last bit of Caller ID data.

In case of errors in the handling of the CID data buffer, CIS-BUF (buffer underflow) and CIS-BOF (buffer overflow) indicate these errors. CID transmission should be stopped in any of these cases as unpredictable results may occur.

Note: CID data will be sent out with the LSB first

If CIS-FRM is set to 1: seizure and mark bits are generated automatically (according to the settings of CIS-SEIZ-H/L and CIS-MARK-H/L) as well as start and stop bits for every byte.

2.8.3 Line Echo Cancellation in DuSLIC-E/-E2/-P

The DuSLIC-E/-E2/-P contains an adaptive Line Echo Cancellation (LEC) unit for the cancellation of near end echoes. With the adaptive balancing of the LEC unit, the Transhybrid Loss can be improved up to a value of approximately 50 dB. The maximum echo cancellation time selectable is 8 ms. The line echo cancellation unit is especially useful in combination with the DTMF detection unit. In critical situations the performance of the DTMF detection can be improved.

If a line echo cancellation length (LEC Length) of 8 ms is used, please take care about the MIPS requirements described in **Chapter 2.8.6**.

The DuSLIC-E/-E2/-P line echo canceller is compatible with applicable ITU-T G.165 and G.168 standards. An echo cancellation delay time of up to 8 ms can be programmed.

The LEC unit basically consists of an Finite Impulse Response (FIR) filter, a shadow FIR filter, and a coefficient adaptation mechanism between these two filters as shown in **Figure 31**.

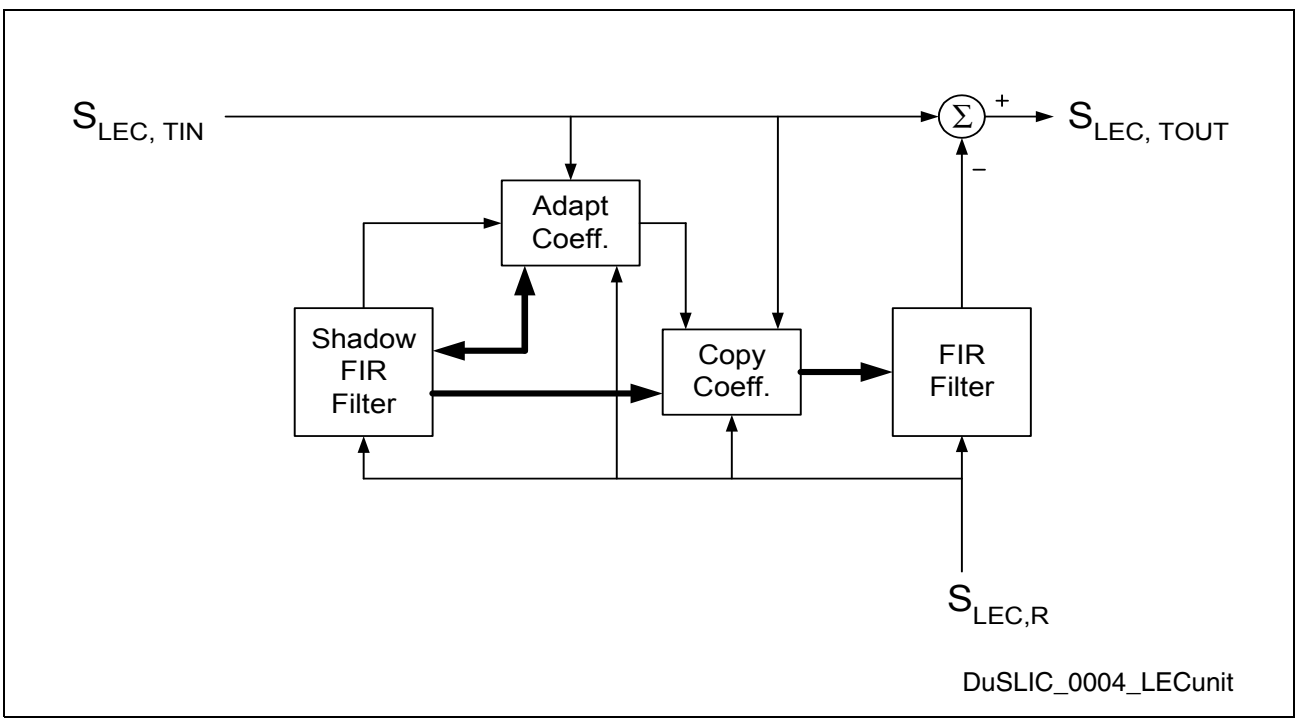


Figure 31 Line Echo Cancellation Unit Block Diagram

The adaptation process is controlled by the three parameters Pow_{LECR} (Power Detection Level Receive), $DeltaP_{LEC}$ (Delta Power) and DeltaQ (Delta Quality) (**"POP Command" on Page 207**). Adaptation takes place only if both of the following conditions hold:

1. $S_{LEC,R} > Pow_{LECR}$
2. $S_{LEC,R} - S_{LEC,TIN} > DeltaP_{LEC}$

With the first condition, adaptation to small signals can be avoided. The second condition avoids adaptation during double talk. The parameter $DeltaP_{LEC}$ represents the echo loss

provided by external circuitry. If the adaptation of the shadow filter is performed better than the adaptation of the actual filter by a value of more than DeltaQ, then the shadow filter coefficients will be copied to the actual filter. At the start of an adaptation process, the coefficients of the LEC unit can be reset to default initial values or can be set to the old coefficient values. The coefficients may also be frozen.

2.8.4 Non Linear Processor (NLP) in DuSLIC-E/-E2/-P

In SLICOFI-2 Version 1.5 a Non Linear Processor (NLP) in addition or as an option to the existing Line Echo Canceller (LEC) is implemented. Please note that the NLP is not available with SLICOFI-2 Version 1.5.

The principle of the NLP is based on a limitation of the input signal. This means, that all samples which are below a limit (in the case of a negative sample above the negative limit), can pass the NLP without any modification. All samples which are above the limit (in the case of a negative sample below the negative limit), will be set to this limit (or negative limit). The value for the limit is the estimated background noise. The advantage of the limitation is, that the background noise can pass the NLP unchanged. Therefore the far end talker can not hear the NLP.

The decision when the NLP should be activated, is based on the estimated residual echo after the LEC. If the signal after the LEC is higher than the estimated residual echo, the NLP is bypassed.
When both the transmit and receive speech detectors are detecting speech (double talk), the NLP is also bypassed. An *overhang* counter ensures, that the end of the speech signal can pass the NLP unchanged. If end of speech is detected, the overhang counter starts counting from a predefined start value down to zero. This time ensures that silent parts at the end of the speech are not ignored.

Important coefficients:

– BN-LEV-X, BN-LEV-R, BN-MAX and BN-ADJ for the background noise estimation
– RE-EST-ERLL for the NLP behavior in the simple mode
– SD-LEV-R, SD-LEV-X and SD-LEV-RE for the speech detection
– CT-LEV-RE for early double talk and near end speech detection

For all other coefficients the default values (see **Table 5.2.3.4**) should be chosen.

LEC and NLP implementation

The NLP is integrated in the LEC unit. That means when the LEC and NLP are active, the output signal of the LEC is influenced by the NLP.

If the DTMF receiver and/or the Universal Tone Detection (UTD) unit are active, the input signal for both is the LEC and the NLP output signal[1)]. Usually this is no problem, as the

1) For the UTD this is only valid when the sum signal of receive and transmit is fed to the UTD (see **Figure 29**).

NLP bypasses local DTMF signals, but it would be a good strategy to only enable the NLP after the call has been completely established (far end talker connected).

2.8.5 Universal Tone Detection in DuSLIC-E/-E2/-P

Each channel of the DuSLIC-E/-E2/-P has two Universal Tone Detection (UTD) units that can be used to detect special tones in the receive and transmit paths, especially fax or modem tones (for example, see the modem startup sequence described in the ITU-T V.8 recommendation). This allows the use of modem-optimized filter for V.34 and V.90 connections. If the DuSLIC-E/-E2/-P UTD detects that a modem connection is about to be established, the optimized filter coefficients for the modem connection can be downloaded before the modem connection is set up. With this mechanism implemented in the DuSLIC-E/-E2/-P chip set, the optimum modem transmission rate can always be achieved.

Figure 32 shows the functional block diagram of the UTD unit:

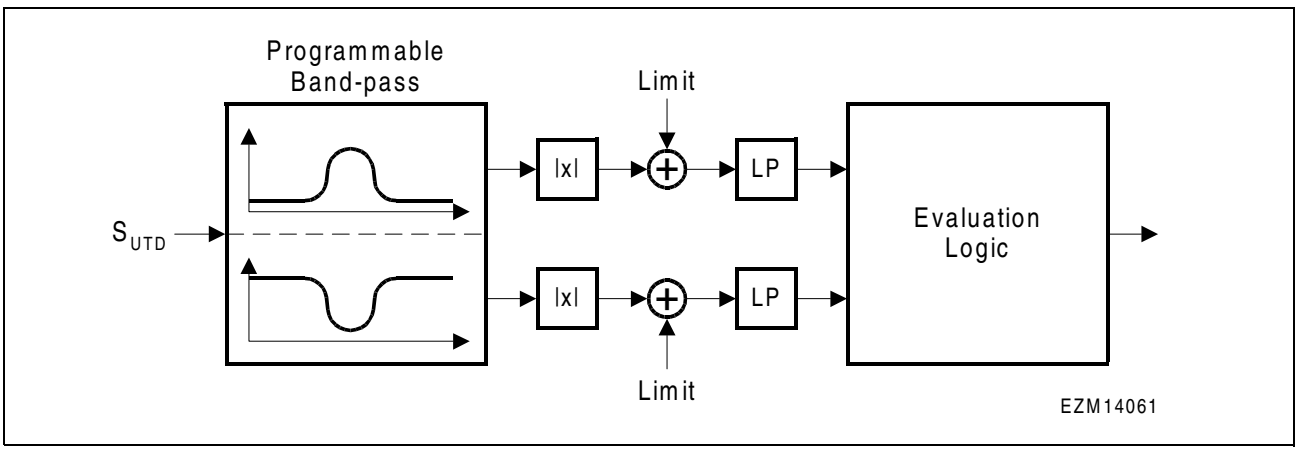


Figure 32 UTD Functional Block Diagram

Initially, the input signal is filtered by a programmable band-pass filter (center frequency f_C and bandwidth f_{BW}). Both the in-band signal (upper path) and the out-of-band signal (lower path) are determined, and the absolute value is calculated. Both signals are furthermore filtered by a limiter and a low-pass filter. All signal samples (absolute values) below a programmable limit Lev_N (noise level) are set to zero and all other signal samples are diminished by Lev_N. The purpose of this limiter is to increase noise robustness. After the limiter stages, both signals are filtered by a fixed low-pass filter. The evaluation logic block determines whether a tone interval or silence interval is detected and whether an interrupt is generated for the receive or transmit path.

The UTDR-OK or UTDX-OK bit (register INTREG3 on Page 155) will be set if both of the following conditions hold for a time span of at least RTime[1)] without breaks longer than RBRKTime:

1. The in-band signal exceeds a programmable level Lev_S.
2. The difference of the in-band and the out-of-band signal levels exceeds $Delta_{UTD}$.

The UTDR-OK or UTDX-OK bit will be reset if at least one of these conditions is violated for a time span of at least ETime during which the violation continues for at least EBRKTime. ETime and EBRKTime help reduce the effects of sporadic dropouts.

If the bandwidth parameter is programmed to a negative value, the UTD unit can be used for the detection of silence intervals in the entire frequency range. The DuSLIC-E/-E2/-P UTD unit is compatible with the ITU-T G.164 recommendation. The UTD is resistant to a modulation with 15 Hz sinusoidal signals and a phase reversal, but is not able to detect the 15 Hz modulation and the phase reversal.

2.8.6 MIPS Requirements for EDSP Capabilities

Table 8 shows the MIPS requirements for each algorithm using the EDSP:

Table 8 MIPS Requirements

Algorithm	Used MIPS	Conditions
Caller ID Sender (CIS)	$1.736*n_{CIS}$	$n_{CIS} = 0...2$
Universal Tone Detection (UTD)	$1.208*n_{UTD}$	$n_{UTD} = 0...4$, transmit and receive for two channels
DTMF Receiver	$6.296*n_{DTMF}$	$n_{DTMF} = 0...2$
Line Echo Canceller (LEC)	$(3.536 + 0.032*LEN)*n_{LEC}$	$n_{LEC} = 0...2$ (for LEN see register LEC-LEN on Page 229)
Non Linear Processor (NLP)[1)]	$2.448*n_{NLP}$	$n_{NLP} = 0...2$
Operating System	1.432	–

1) SLICOFI-2 Version 1.5 only

Attention: The maximum capability of the EDSP is 32 MIPS. The user has to make sure that the sum of all enabled algorithms does not exceed 32 MIPS in any case!

1) for RTime, RBRKTime, ETime and EBRKTime see Chapter 5.2.3.3.

Example:

- All algorithms for all channels enabled and LEC Length = 8 ms (LEN = 64):
  →33.32 MIPS total computing load exceeding the 32 MIPS limit!
- All algorithms for all channels enabled and LEC Length = 4 ms (LEN = 32):
  →31.272 MIPS total computing load within the 32 MIPS limit.
- 4 x UTD, 2 x DTMF Receiver and 2 x LEC (8 ms) enabled:
  →29.85 MIPS total computing load within the 32 MIPS limit.

Example for SLICOFI-2 Version 1.5 (with NLP):

- All algorithms for all channels enabled and LEC Length = 4 ms (LEN = 32):
  →36.344 MIPS total computing load exceeding the 32 MIPS limit!
- 2 x DTMF Receiver, 2 x LEC (8 ms) and 2 x NLP enabled:
  →30.1 MIPS total computing load within the 32 MIPS limit.

2.9 Message Waiting Indication in DuSLIC-E/-E2/-P

Message Waiting Indication (MWI) is usually performed using a glow lamp at the subscriber phone. Current does not flow through a glow lamp until the voltage reaches a threshold value above approximately 80 V. At this threshold, the neon gas in the lamp will start to glow. When the voltage is reduced, the current falls under a certain threshold and the lamp glow is extinguished. DuSLIC has high-voltage SLIC technology (170 V) that is able to activate the glow lamp without any external components.

The hardware circuitry is shown in **Figure 33**. The figure shows a typical telephone circuit with the hook switch in the on-hook mode, together with the impedances for the on-hook (Z_R) and off-hook (Z_L) modes.

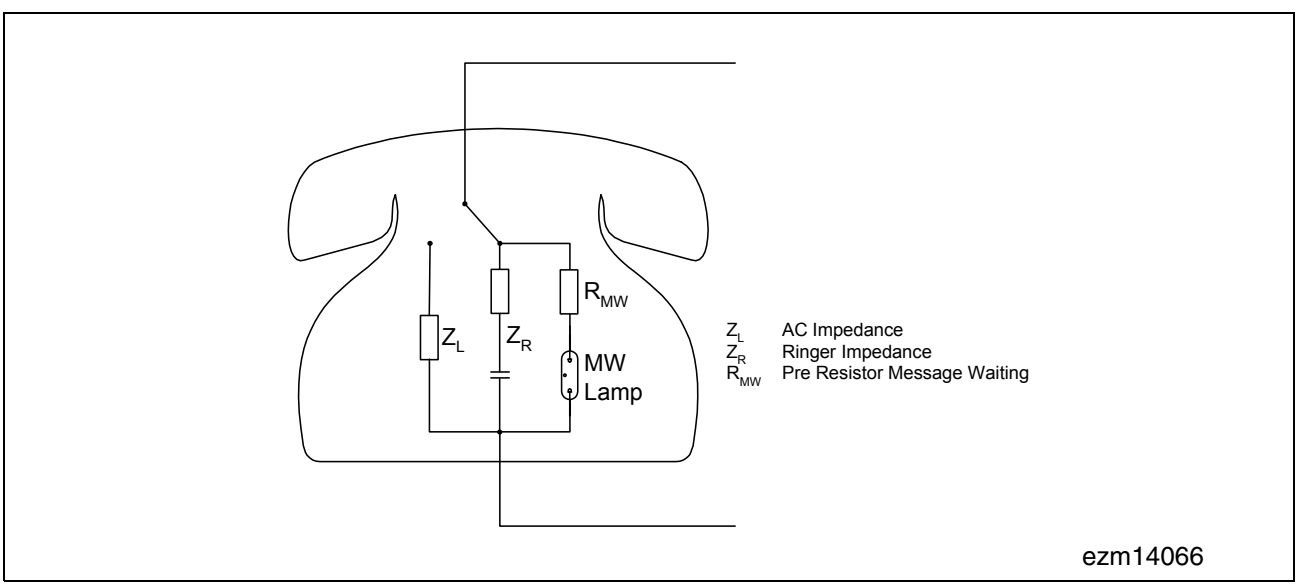


Figure 33 MWI Circuitry with Glow Lamp

The glow lamp circuit also requires a resistor (R_{MW}) and a lamp (MW Lamp) built into the phone. When activated, the lamp must be able to either blink or remain on constantly.

In non-DuSLIC-E/-E2/-P solutions, the telephone ringer may respond briefly if the signal slope is too steep; behavior that is not desirable. The integrated ramp generator of the DuSLIC-E/-E2/-P can be programmed to increase the voltage slowly, to ensure that the lamp is activated and not the ringer.

To activate the Message Waiting function of DuSLIC-E/-E2/-P, the following steps should be performed:

1. Activating Ring Pause mode by setting the M0-M2 bits
2. Select Ring Offset RO2 by setting the bits in register LMCR3
3. Enable the ramp generator by setting bit RAMP-EN in register LMCR2
4. Switch between the Ring Offsets RO3 and RO2 in register LMCR3 to flash the lamp on and off (see **Figure 34**).

The values for RO2 and RO3 must first be programmed in the CRAM to the appropriate values so that the lamp will flash on and off.

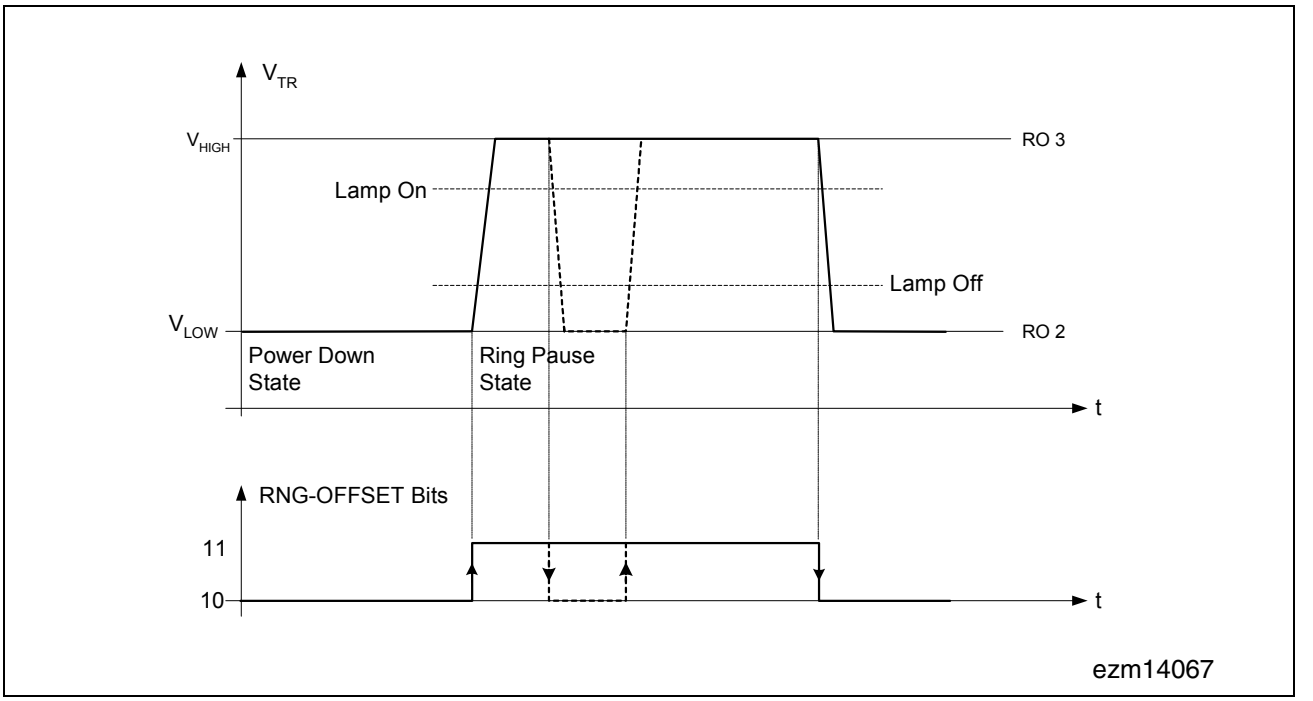


Figure 34 Timing Diagram

2.10 Three-party Conferencing in DuSLIC-E/-E2/-P

Each DuSLIC-E/-E2/-P channel has a three-party conferencing facility implemented which consist of four PCM registers, adders and gain stages in the microprogram and the corresponding control registers (see **Figure 35**). Cascading DuSLIC-E/-E2/-P channels allows Multi-party Conferencing as well.

This facility is available in PCM/µC mode only. The PCM control registers PCMR1 through PCMR4 and PCMX1 through PCMX4 control the time slot assignment and PCM highway selection, while the bits PCMX-EN, CONF-EN, and CONFX-EN in the BCR3 register control the behavior of the conferencing facility and the PCM line drivers (see **Figure 35**). A programmable gain stage G is able to adjust the gain of the conferencing voice data (B, C, D, S) in a range from –6 dB to +3 dB to prevent an overload of the sum signals.

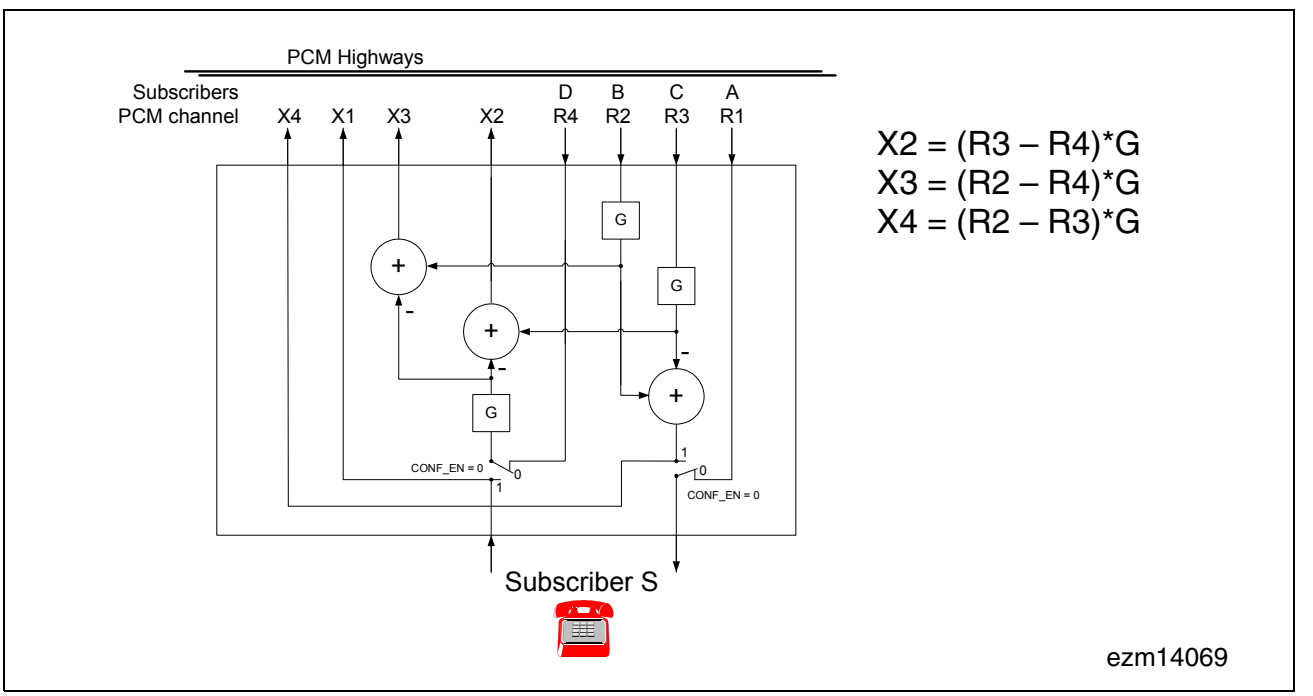


Figure 35 Conference Block for One DuSLIC Channel

Note: G … Gain Stage (Gain Factor) set in CRAM coefficients,
X1 - X4 … PCM transmit channels,
R1 - R4 … PCM receive channels,
A, B, C, D, S … examples for voice data on PCM channels X1–X4, R1–R4.

2.10.1 Conferencing Modes

Table 9 Conferencing Modes: Receive Channels

	Configuration Registers			Receive Channels				Subscr.
Mode	PCMX-EN	CONF-EN	CONFX-EN	R1	R2	R3	R4	S
PCM Off	0	0	0	–	–	–	–	off
PCM Active	1	0	0	A	–	–	–	A

Table 9 Conferencing Modes: Receive Channels (cont'd)

	Configuration Registers			Receive Channels				Subscr.
Mode	PCMX-EN	CONF-EN	CONFX-EN	R1	R2	R3	R4	S
External Conference	0	0	1	–	B	C	D	off
External Conference + PCM Active	1	0	1	A	B	C	D	A
Internal Conference	0	1	0	–	B	C	–	G(B+C)

Table 10 Conferencing Modes: Transmit Channels

	Configuration Registers			Transmit Channels				Subscr.
Mode	PCMX-EN	CONF-EN	CONFX-EN	X1	X2	X3	X4	S
PCM Off	0	0	0	off	off	off	off	off
PCM Active	1	0	0	S	off	off	off	A
External Conference	0	0	1	off	G(C+D)	G(B+D)	G(B+C)	off
External Conference + PCM Active	1	0	1	S	G(C+D)	G(B+D)	G(B+C)	A
Internal Conference	0	1	0	off	G(C+S)	G(B+S)	off	G(B+C)

(see also **"Control of the Active PCM Channels" on Page 126**)

PCM Off

After a reset, or in power down mode, there is no communication via the PCM highways. Also, when selecting new time slots, it is recommended to switch off the PCM line drivers by setting the control bits to zero.

PCM Active

This is the normal operating mode without conferencing. Only the channels R1 and X1 are in use, and voice data are transferred from subscriber A to analog subscriber S and vice versa.

External Conference

In this mode, the SLICOFI-2 acts as a server for a three-party conference of subscribers B, C, and D that may be controlled by any device connected to the PCM highways. The SLICOFI-2 channel itself can remain in power down mode to reduce power consumption.

External Conference + PCM Active

As in External Conference mode, any external three-party conference is supported. At the same time, an internal phone call is active using the channels R1 and X1.

Internal Conference

If the analog subscriber S is one of the conference partners, the internal conference mode will be selected. The partners (B, C) do not need any conference facility as the SLICOFI-2 performs all required functions for them as well.

2.11 16 kHz Mode on PCM Highways

In addition to the standard 8 kHz transmission PCM interface modes, there are also two 16 kHz modes for high-speed data transmission performance.

Table 11 and **Table 12** show the configuration of PCM channels for the different PCM interface modes (see **“Control of the Active PCM Channels” on Page 126**).

Table 11 Possible Modes in PCM/µC Interface Mode: Receive Channels

Mode	Configuration Bits		Receive PCM Channels				
	PCM16K	LIN	R1	R1L[1)]	R2	R3	R4
PCM	0	0	A	[2)]	B	C	D
LIN	0	1	A-HB	A-LB	B	C	D
PCM16	1	0	DS1	–	–	DS2	–
LIN16	1	1	DS1-HB	–	DS1-LB	DS2-HB	DS2-LB

1) Time slot R1 + 1

2) Empty cells in the table indicate unused data in the PCM receive channels and switched-off line drivers in the PCM transmit channels

Table 12 Possible Modes in PCM/µC Interface Mode: Transmit Channels

Mode	Configuration Bits		Transmit PCM Channels				
	PCM16K	LIN	X1	X1L[1)]	X2	X3	X4
PCM	0	0	S	–	depends on conference mode		
LIN	0	1	S-HB	S-LB	depends on conference mode		
PCM16	1	0	DS1	–	–	DS2	–
LIN16	1	1	DS1-HB	–	DS1-LB	DS2-HB	DS2-LB

1) Time slot X1 + 1

The configuration bits PCM16K and LIN (in the BCR3 register) are used to select the following PCM interface modes:

PCM Mode

Normal mode used for voice transmission via channels R1 and X1 (receive and transmit). The PCM input channels R2, R3 and R4 are always available for use in different conference configurations. The status of the PCM output channels depends on the conference mode configuration.

LIN Mode

Similar to the PCM mode, but for 16 bit linear data at 8 kHz sample rate via the PCM channels R1, R1L (receive) and channels X1, X1L (transmit). Data are sent MSB first, two’s complement.

PCM16 Mode

Mode for higher data transmission rate of PCM encoded data using a 16 kHz sample rate (only in PCM/µC Interface mode with the PCMX-EN bit in the BCR3 register set to one). In this mode, the channels R1, R3 (X1, X3) are used to receive (transmit) two samples of data (DS1, DS2) in each 8 kHz frame.

LIN16 Mode

Like the PCM16 mode for 16 kHz sample rate, but for linear data. Channels R1 to R4 (X1 to X4) are used for receiving (transmitting) the high and low bytes of the two linear data samples DS1 and DS2.

3 Operational Description

3.1 Overview of all DuSLIC Operating Modes

Table 13 Overview of all DuSLIC Operating Modes

***SLICOFI-2x* Mode**	**SLIC Type**			**CIDD/CIOP** [1]			**Additional Bits used** [2]
	SLIC-S/ SLIC-S2	**SLIC-E/ SLIC-E2**	**SLIC-P**	**M2**	**M1**	**M0**	
Sleep (SL)	–	PDRH	PDRH	1	1	1	SLEEP-EN = 1
			PDRR	1	1	1	SLEEP-EN = 1, ACTR = 1
Power Down Resistive (PDR)	PDRH	PDRH	PDRH	1	1	1	SLEEP-EN = 0
			PDRR	1	1	1	SLEEP-EN = 0, ACTR = 1
Power Down High Impedance (PDH)	PDH	PDH	PDH	0	0	0	–
Active High (ACTH)	ACTH	ACTH	ACTH	0	1	0	–
Active Low (ACTL)	ACTL	ACTL	ACTL	0	1	0	ACTL = 1
Active Ring (ACTR)	ACTR	ACTR	ACTR	0	1	0	ACTR = 1
Ringing (Ring)	ACTR [3]	ACTR	ACTR	1	0	1	–
	–	–	ROT	1	0	1	HIT = 1
	–	–	ROR	1	0	1	HIR = 1
Active with HIT [4]	HIT	HIT		0	1	0	HIT = 1
			HIT	0	1	0	HIT = 1, ACTR = 0
Active with HIR [5]	HIR	HIR		0	1	0	HIR = 0
			HIR	0	1	0	HIR = 0, ACTR = 0
Active with Ring to Ground			ROT	0	1	0	HIT = 1, ACTR = 1
Active with Tip to Ground			ROR	0	1	0	HIR = 1, ACTR = 1
High Impedance on Ring and Tip (HIRT)	–	HIRT	HIRT	0	1	0	HIR = 1, HIT = 1

Table 13 Overview of all DuSLIC Operating Modes (cont'd)

SLICOFI-2x Mode	SLIC Type			CIDD/CIOP [1]			Additional Bits used[2]
	SLIC-S/ SLIC-S2	SLIC-E/ SLIC-E2	SLIC-P	M2	M1	M0	
Active with Metering	ACTx[3] [6]	ACTx[4]	ACTx[4]	1	1	0	TTX-DIS to select Reverse Polarity or TTX Metering
Ground Start	HIT	HIT	 HIT	1 1	0 0	0 0	– ACTR = 0
Ring Pause	ACTR[3]	ACTR	ACTR ROR ROT	0	0	1	 HIR = 1 HIT = 1

1) CIDD = Data Downstream Command/Indication Channel Byte (IOM-2 Interface)
CIOP = Command/Indication Operation
For further information, see **"SLICOFI-2x Command Structure and Programming" on Page 140**.

2) If not otherwise stated in the table, the bits ACTL, ACTR, HIT, HIR must be set to 0.

3) Only for SLIC-S

4) HIT = High Impedance on Tip

5) HIR = High Impedance on Ring

6) ACTx means ACTH, ACTL or ACTR.

Sleep (SL) – only available with DuSLIC-E/-E2/-P/-ES/-ES2

The SLICOFI-2 is able to go into Sleep mode with minimal power dissipation. In this mode, off-hook detection is performed without any checks on spikes or glitches. The Sleep mode can be used for either channel, but for the most effective power savings, both channels should be set to this mode. Note that this requires the following:

- If both channels are set to the Sleep mode, only non-noisy lines should be used due to the lack of persistence checking. Wake up takes about 1.25 ms, as the on-chip PLL is also switched off. Therefore, it is also possible to switch off all external clocks. In this mode, no programming or other functionality is available. The off-hook event is indicated either by (1) setting the interrupt pin to Low level, if the PCM/µC Interface mode is selected, or (2) pulling down the DU pin, if IOM-2 Interface is used.
- If only one channel is set to Sleep mode, persistence checking and off-hook indication are performed as in any other mode, but the off-hook level is fixed to 2 mA at the subscriber line. No special wake up is needed if only one channel is in Sleep mode. A simple mode change ends the Sleep mode.
- A sleeping SLICOFI-2 wakes up if the $\overline{CS}$ pin is drawn to low level when the PCM/µC Interface is used or if the MX bit is set to 0 when the IOM-2 Interface is used. Note

that no programming is possible until the SLICOFI-2 wakes up. In IOM-2 mode, the identification request can be used as a wake up signal as this command is independent of the internal clock. In the PCM/µC mode, it is recommended that $\overline{CS}$ be set to 0 for only one clock cycle.

- After a wake up from Sleep mode, the SLICOFI-2 enters the PDRH or PDRR mode. To re-enter Sleep mode, it is necessary to first perform a mode change to any Active mode on at least one channel.

Power Down Resistive (PDRH for SLIC-E/-E2/-S/-S2 and PDRH, PDRR for SLIC-P)

The Power Down Resistive mode is the standard mode for none-active lines. Off-hook is detected by a current value fed to the DSP, is compared with a programmable threshold, and is filtered by a data upstream persistence checker. The power management SLIC-P can be switched to a Power Down Resistive High (PDRH) mode or to a Power Down Resistive Ring (PDRR) mode.

High Impedance on Ring and Tip (HIRT)

The line drivers in the SLIC-E/-E2/-P are shut down and no resistors are switched to the line. Off-hook detection is not possible. In HIRT mode, the SLICOFI-2 is able to measure the input offset of the current sensors.

Power Down High Impedance (PDH)

In Power Down High Impedance mode, the SLIC is totally powered down. No off-hook sensing can be performed. This mode can be used for emergency shutdown of a line.

Active High (ACTH)

A regular call can be performed, voice and metering pulses can be transferred via the telephone line, and the DC loop is operational in the Active High mode using V_{BATH}.

Active Low (ACTL)

The Active Low mode is similar to the Active High mode. The only difference is that the SLIC uses a lower battery voltage, V_{BATL} (bit ACTL = 1).

Active Ring (ACTR)

The Active Ring mode for the SLIC-E/-E2 is different from the Active Ring mode for the SLIC-P. The SLIC-E/-E2 uses the additional positive voltage V_{HR} for extended feeding, whereas the SLIC-P switches to the negative battery voltage V_{BATR}.

Ringing

If the *SLICOFI-2x* is switched to Ringing mode, the SLIC is switched to ACTR mode.

With the SLIC-P connected to the SLICOFI-2, the Ring on Ring (ROR) mode allows unbalanced internal ringing on the Ring wire. The Tip wire is set to battery ground. The Ring signal will be superimposed by $V_{BATR}/2$.

The Ring on Tip (ROT) mode is equivalent to the ROR mode.

Active with HIT

This is a testing mode where the Tip wire is set to a high impedance mode. It is used for special line testing. It is only available in an Active mode of the *SLICOFI-2x* to enable all necessary test features.

Active with HIR

HIR is similar to HIT but with the Ring wire set to high impedance.

Active with Metering

Any available Active mode can be used for metering, with either Reverse Polarity or with TTX Signals.

Ground Start

The Tip wire is set to high impedance in Ground Start mode. Any current drawn on the Ring wire leads to a signal on IT, indicating off-hook.

Ring Pause

The Ring burst is switched off in Ring Pause, but the SLIC remains in the specified mode and the off-hook recognition behaves the same as in Ringing mode (Ring Trip).

3.2 Operating Modes for the DuSLIC-S/-S2/-SE/-SE2 Chip Set

Table 14 DuSLIC-S/-S2/-SE/-SE2 Operating Modes

SLICOFI-2S /SLICOFI-2S2 Mode	SLIC-S/S2 /SLIC-E/E2 Mode	SLIC-S/-S2 /SLICE/E2 Internal Supply Voltages (+/–) [V_{HI}/V_{BI}]	System Functionality	Active Circuits	Tip/Ring Output Voltage
PDH	PDH	Open/V_{BATH}	None	None	High Impedance
Power Down Resistive	PDRH	Open/V_{BATH}	Off-hook detect as in Active mode (DSP)	Off-hook, DC transmit path	V_{BGND}/V_{BATH} (via 5 kΩ)
–	PDRHL[1)]	Open/V_{BATH}	Off-hook detect as in Active mode (DSP)	Off-hook, DC transmit path	V_{BGND}/V_{BATH} (via 5 kΩ)
Active Low (ACTL)	ACTL	V_{BGND}/V_{BATL}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: (V_{BATL} + V_{AC} + V_{DC})/2 Ring: (V_{BATL} –V_{AC} – V_{DC})/2
Active High (ACTH)	ACTH	V_{BGND}/V_{BATH}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: (V_{BATH} + V_{AC} + V_{DC})/2 Ring: (V_{BATH} –V_{AC} – V_{DC})/2
Active Ring (ACTR)	ACTR	V_{HR}/V_{BATH}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: (+ V_{BATH} + V_{HR} + V_{AC} + V_{DC})/2 Ring: (+ V_{BATH} + V_{HR} – V_{AC} – V_{DC})/2

Table 14 DuSLIC-S/-S2/-SE/-SE2 Operating Modes (cont'd)

SLICOFI-2S /SLICOFI-2S2 Mode	SLIC-S/S2 /SLIC-E/E2 Mode	SLIC-S/-S2 /SLICE/E2 Internal Supply Voltages (+/–) [V_{HI}/V_{BI}]	System Functionality	Active Circuits	Tip/Ring Output Voltage
Ringing (Ring)	ACTR	V_{HR}/V_{BATH}	Balanced ring signal feed (including DC offset)	Buffer, Sensor, DC loop, Ring generator	Tip: $(V_{BATH} + V_{HR} + V_{DC})/2$ Ring: $(V_{BATH} + V_{HR} - V_{DC})/2$
Ring Pause	ACTR	V_{HR}/V_{BATH}	DC offset feed	Buffer, Sensor, DC loop, Ramp generator	Tip: $(V_{BATH} + V_{HR} + V_{DC})/2$ Ring: $(V_{BATH} + V_{HR} - V_{DC})/2$
HIRT	HIRT	V_{HR}/V_{BATH}	For example: sensor offset calibration	Sensor, DC transmit path	High Impedance
Active with HIR	HIR	V_{HR}/V_{BATH}	For example: line test (Tip)	Tip Buffer, Sensor, DC + AC loop	Tip: $(V_{BATH} + V_{HR} + V_{AC} + V_{DC})/2$ Ring: High impedance
Active with HIT	HIT	V_{HR}/V_{BATH}	For example: line test (Ring)	Ring Buffer, Sensor, DC + AC loop	Ring: $(V_{BATH} + V_{HR} - V_{AC} - V_{DC})/2$ Tip: High impedance

1) Load external C for switching from PDRH to ACTH in on-hook mode.

V_{AC} … Tip/Ring AC Voltage

V_{DC} … Tip/Ring DC Voltage

3.3 Operating Modes for the DuSLIC-E/-E2/-ES/-ES2 Chip Set

Table 15 DuSLIC-E/-E2/-ES/-ES2 Operating Modes

SLICOFI-2 Mode	SLIC-E/E2 /SLIC-S/S2 Mode	SLIC-E/-E2 /SLIC-S/S2 Internal Supply Voltages (+/–) [V_{HI}/V_{BI}]	System Functionality	Active Circuits	Tip/Ring Output Voltage
PDH	PDH	Open/V_{BATH}	None	None	High Impedance
Sleep	PDRH	Open/V_{BATH}	Off-hook detect via off-hook comparator	Off-hook, Analog comparator	V_{BGND}/V_{BATH} (via 5 kΩ)
Power Down Resistive	PDRH	Open/V_{BATH}	Off-hook detect as in Active mode (DSP)	Off-hook, DC transmit path	V_{BGND}/V_{BATH} (via 5 kΩ)
–	PDRHL[1)]	Open/V_{BATH}	Off-hook detect as in Active mode (DSP)	Off-hook, DC transmit path	V_{BGND}/V_{BATH} (via 5 kΩ)
Active Low (ACTL)	ACTL	V_{BGND}/V_{BATL}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: (V_{BATL} + V_{AC} + V_{DC})/2 Ring: (V_{BATL} –V_{AC} – V_{DC})/2
Active High (ACTH)	ACTH	V_{BGND}/V_{BATH}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: (V_{BATH} + V_{AC} + V_{DC})/2 Ring: (V_{BATH} –V_{AC} – V_{DC})/2
Active Ring (ACTR)	ACTR	V_{HR}/V_{BATH}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: (+ V_{BATH} + V_{HR} + V_{AC} + V_{DC})/2 Ring: (+ V_{BATH} + V_{HR} – V_{AC} – V_{DC})/2

Table 15 DuSLIC-E/-E2/-ES/-ES2 Operating Modes (cont'd)

SLICOFI-2 Mode	SLIC-E/E2 /SLIC-S/S2 Mode	SLIC-E/-E2 /SLIC-S/S2 Internal Supply Voltages (+/–) [V_{HI}/V_{BI}]	System Functionality	Active Circuits	Tip/Ring Output Voltage
Ringing (Ring)	ACTR	V_{HR}/V_{BATH}	Balanced Ring signal feed (including DC offset)	Buffer, Sensor, DC loop, Ring generator	Tip: (V_{BATH} + V_{HR} + V_{DC})/2 Ring: (V_{BATH} + V_{HR} – V_{DC})/2
Ring Pause	ACTR	V_{HR}/V_{BATH}	DC offset feed	Buffer, Sensor, DC loop, Ramp generator	Tip: (V_{BATH} + V_{HR} + V_{DC})/2 Ring: (V_{BATH} + V_{HR} – V_{DC})/2
HIRT	HIRT	V_{HR}/V_{BATH}	For example: sensor offset calibration	Sensor, DC transmit path	High Impedance
Active with HIR	HIR	V_{HR}/V_{BATH}	For example: line test (Tip)	Tip-Buffer, Sensor, DC + AC loop	Tip: (V_{BATH} + V_{HR} + V_{AC} + V_{DC})/2 Ring: High impedance
Active with HIT	HIT	V_{HR}/V_{BATH}	For example: line test (Ring)	Ring-Buffer, Sensor, DC + AC loop	Ring: (V_{BATH} + V_{HR} – V_{AC} –V_{DC})/2 Tip: High impedance

1) Load external C for switching from PDRH to ACTH in on-hook mode

V_{AC} … Tip/Ring AC Voltage

V_{DC} … Tip/Ring DC Voltage

3.4 Operating Modes for the DuSLIC-P Chip Set

Table 16 DuSLIC-P Operating Modes

SLICOFI-2 Mode	SLIC-P Mode	SLIC-P Internal Supply Voltages [V_{BI}]	System Functionality	Active Circuits	Tip/Ring Output Voltage
PDH	PDH	V_{BATR}	None	None	High impedance
Sleep	PDRH	V_{BATH}	Off-hook detect via off-hook comparator	Off-hook, Analog comparator	V_{BGND}/V_{BATH} (via 5 kΩ)
Sleep	PDRR	V_{BATR}	Off-hook detect via off-hook comparator	Off-hook, Analog comparator	V_{BGND}/V_{BATR} (via 5 kΩ)
Power Down Resistive	PDRH	V_{BATH}	Off-hook detect as in Active mode (DSP)	Off-hook, DC transmit path	V_{BGND}/V_{BATH} (via 5 kΩ)
–	PDRHL[1)]	V_{BATH}	Off-hook detect as in Active mode (DSP)	Off-hook, DC transmit path	V_{BGND}/V_{BATH} (via 5 kΩ)
–	PDRR	V_{BATR}	Off-hook detect as in Active mode (DSP)	Off-hook, Analog comparator	V_{BGND}/V_{BATR} (via 5 kΩ)
–	PDRRL[2)]	V_{BATR}	Off-hook detect as in Active mode (DSP)	Off-hook, DC transmit path	V_{BGND}/V_{BATR} (via 5 kΩ)
Active Low (ACTL)	ACTL	V_{BATL}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: $(V_{BATL} + V_{AC} + V_{DC})/2$ Ring: $(V_{BATL} - V_{AC} - V_{DC})/2$
Active High (ACTH)	ACTH	V_{BATH}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: $(V_{BATH} + V_{AC} + V_{DC})/2$ Ring: $(V_{BATH} - V_{AC} - V_{DC})/2$

Table 16 DuSLIC-P Operating Modes (cont'd)

SLICOFI-2 Mode	SLIC-P Mode	SLIC-P Internal Supply Voltages [V_{BI}]	System Functionality	Active Circuits	Tip/Ring Output Voltage
Active Ring (ACTR)	ACTR	V_{BATR}	Voice and/or TTX transmission	Buffer, Sensor, DC + AC loop, TTX generator (optional)	Tip: (V_{BATR} + V_{AC} + V_{DC})/2 Ring: (V_{BATR} – V_{AC} – V_{DC})/2
Ringing (Ring)	ACTR	V_{BATR}	Balanced ring signal feed (including DC offset)	Buffer, Sensor, DC loop, ring generator	Tip: (V_{BATR} + V_{DC})/2 Ring: (V_{BATR} –V_{DC})/2
Ringing (Ring)	ROR	V_{BATR}	Ring signal on ring, Tip on BGND	Buffer, Sensor, DC loop, ring generator	Ring: (V_{BATR} –V_{DC})/2 Tip: 0 V
Ringing (Ring)	ROT	V_{BATR}	Ring signal on ring, Tip on BGND	Buffer, Sensor, DC loop, ring generator	Tip: (V_{BATR} + V_{DC})/2 Ring: 0 V
Ring Pause	ACTR, ROR, ROT	V_{BATR}	DC offset feed	Buffer, Sensor, DC loop, ramp generator	Tip: (V_{BATR} + V_{DC})/2 Ring: (V_{BATR} –V_{DC})/2
HIRT	HIRT	V_{BATR}	For example: sensor offset calibration	Sensor, DC transmit path	High impedance
Active with HIR	HIR	V_{BATR}	For example: line test (Tip)	Tip-Buffer, Sensor, DC + AC loop	Tip: (V_{BATR} + V_{AC} + V_{DC})/2 Ring: High impedance
Active with HIT	HIT	V_{BATR}	For example: line test (Ring)	Ring-Buffer, Sensor, DC + AC loop	Ring: (V_{BATR} –V_{AC} – V_{DC})/2 Tip: High impedance

1) Load external C for switching from PDRH to ACTH in On-Hook mode

2) Load external C for switching from PDRR to ACTR in On-Hook mode

3.5 Reset Mode and Reset Behavior

3.5.1 Hardware and Power On Reset

A reset of the DuSLIC is initiated by a power-on reset or by a hardware reset. Hardware reset requires setting the signal at $\overline{\text{RESET}}$ input pin to low level for at least 4 µs. The reset input pin has a spike rejection that will safely suppress spikes with a duration of less than 1 µs.

Note: Maximum spike rejection time is $t_{rej,\ max}$. Minimum spike rejection time is $t_{rej,min}$.

The *SLICOFI-2x* is reset by taking the $\overline{\text{RESET}}$ line to low (see **Figure 36**). During this time:

- all I/O pins are deactivated
- all outputs are inactive (e.g. DXA/DXB)
- internal PLL is stopped
- internal clocks are deactivated
- the chip enters the power down high impedance mode (PDH) when the Reset is 1 (otherwise the chip is in a kind of Reset Mode that does not exactly equal the power down high impedance mode as the VCM voltage for the SLIC is missing)

With the high going reset signal, the following actions take place:

- Clock detection
- PLL synchronization
- Reset routine runs
- when the reset routine has finished the chip is in power down impedance mode (PDH)

The internal reset routine will then initialize the entire chip to default condition as described in the SOP default register setting (see **Chapter 5**). To run through the internal reset routine, it is necessary that all external clocks are supplied. The clocks are determined by the mode:

- µC/PCM mode: FSC, MCLK, PCLK
- IOM-2 mode: FSC and DCL.

Note: Without valid and stable external clock signals, the DuSLIC will not complete the reset sequence properly.

The internal reset routine requires 12 frames (12 × 125 µs = 1.5 ms) to be finished (including PLL start up and clock synchronization) and requires setting the default values given in **Table 17**. The first register access to the *SLICOFI-2x* may be performed after the internal reset routine is finished.

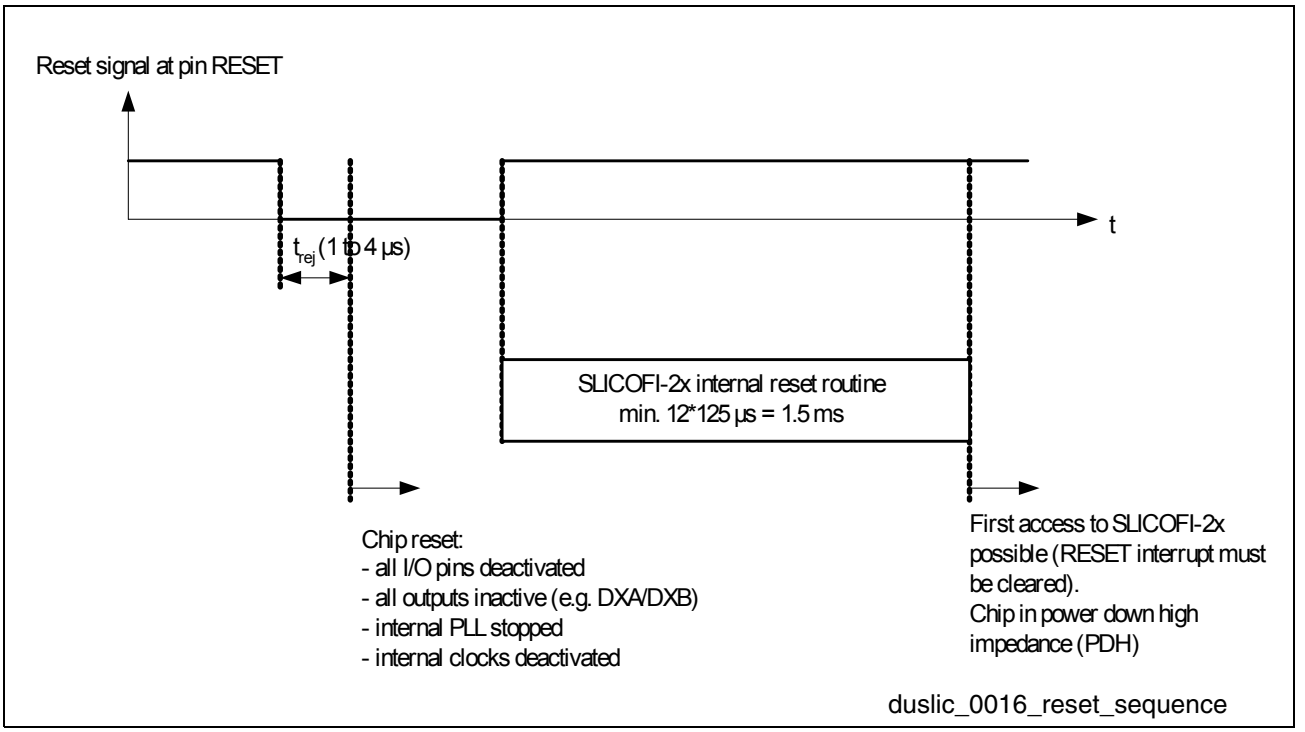


Figure 36 DuSLIC Reset Sequence

3.5.2 Software Reset

When performing a software reset, the DuSLIC runs the reset routine and sets the default settings of the configuration registers. The software reset can be performed individually for each channel.

Table 17 Default DC and AC Values

DC			
I_{K1}	20	mA	Limit for Constant Current
V_{K1}	34	V	Voltage of limit between Constant Current and Resistive Zone
K_B	1	–	Additional gain with extended battery feeding
R_I	10	kΩ	Output Resistance in constant current zone
R_{K12}	100	Ω	Programmable resistance in resistive zone
f_{RING}	25.4	Hz	Ring frequency
A_{RING}	62	Vrms	Ring amplitude at Tip/Ring wire
RO1	23	V	Ring offset voltage RO1
RO2	0	V	Ring offset voltage RO2
RO3	50	V	Ring offset voltage RO3
f_{RINGLP}	75	Hz	Corner frequency of Ring low-pass filter
Off-hookPD	2	mA	Current threshold for Off-hook Detection in Power Down mode
Off-hookAct	8	mA	Off-hook Detection in Active with 2 mA hysteresis
Off-hookRing	5	mA	DC-Current threshold for Off-hook Detection in Ringing mode
Off-hookMW	5	mA	DC-Current threshold for Off-hook Detection in Message Waiting
Off-hookAC	22	mArms	Current threshold for AC Ring Trip detection
LineSup	5	mA	Current threshold Line-Supervision for ground start
Tip/Ring	30	V	Voltage threshold at Tip/Ring wire for VTRLIM bit
DC-Lowpass	1.2/20	Hz	DC low-pass set to 1.2 and 20 Hz respectively
ConstRamp	300	V/s	Slope of the ramp generator
$delay_{RING}$	0	ms	Delay of Ring burst
SRend1	1/128	–	Soft-reversal threshold 1 (referred to the input of the ramp generator)

Table 17 Default DC and AC Values (cont'd)

SRend2	1/512	–	Soft-reversal threshold 2 (referred to the input of the ramp generator)
DUP	10	ms	Data Upstream Persistence Counter is set to 10 ms
DUP-IO	16.5	ms	Data Upstream Persistence Counter for I/O pins, VTRLIM and ICON bits (register INTREG1) is set to 16.5 ms
SR-Time	80	ms	Time for soft-reversal
AC			
IM-Filter	900	Ω	Approximately 900 Ω real input impedance
TH-Filter	TH_{GER}	–	Approximately complex german impedance for balanced network
L_X	0	dBr	Relative level in transmit
L_R	–7	dBr	Relative level in receive
ATTX	2.5	Vrms	Teletax generator amplitude at the resistance of 200 Ω
f_{TTX}	16	kHz	Teletax generator frequency
TG1	940	Hz	Tone generator 1 (–12 dBm)
TG2	1633	Hz	Tone generator 2 (–10 dBm)
AC-LM-BP	1004	Hz	AC level meter band pass

3.6 Interrupt Handling

Attention: Even if interrupts are not used in the system application, the user has to clear the reset interrupt after each power-up reset.

SLICOFI-2x provides extensive interrupt data for the host system. Interrupt handling is performed by the on-chip microprogram that handles the interrupts in a fixed 2 kHz (500 µs) frame. Therefore, some delays up to 500 µs can occur in the reactions of *SLICOFI-2x*, depending on when the host reads the interrupt registers.

Independent of the selected interface mode (PCM/µC or IOM-2), the general behavior of the interrupt is as follows:

- Any change in one of the four interrupt registers (at some bits, only transitions from 0 to 1) leads to an interrupt. The interrupt channel bit INT-CH in INTREG1 is set to 1 and all interrupt registers of one DuSLIC channel are locked at the end of the interrupt procedure (500 µs period). Therefore, all changes within one 2 kHz frame are stored in the interrupt registers. The lock remains until the interrupt channel bit is cleared (Release Interrupt by reading all four interrupt registers INTREG1 to INTREG4 with one command).
- In IOM-2 Interface mode, the interrupt channel bits are fed to the CIDU channel (see IOM-CIDU). In PCM mode, the INT pin is set to active (low).
- The interrupt is released (INT-CH bit reset to 0) by **reading all four interrupt registers by one command**. Reading the interrupt registers one-by-one using a series of commands does not release the interrupt even if all four registers are read.
- A hardware or power-on reset of the chip clears all pending interrupts and resets the INT line to inactive (PCM/µC mode) or resets the INT-CH bit in CIDU (IOM-2 mode). The behavior after a software reset of both channels is similar, the interrupt signal switches to non-active within 500 µs. A software reset of one DuSLIC channel deactivates the interrupt signal if there is no active interrupt on the other DuSLIC channel.
  If the reset line is deactivated, a reset interrupt is generated for each channel (bit RSTAT in register INTREG2).

3.6.1 Recommended Procedure for Reading the Interrupt Registers

When using SLICOFI-2, the following procedure has to be applied:
In case of an interrupt it is recommended to identify the interrupting channels first, before reading all four interrupt registers (see **Figure 37**):

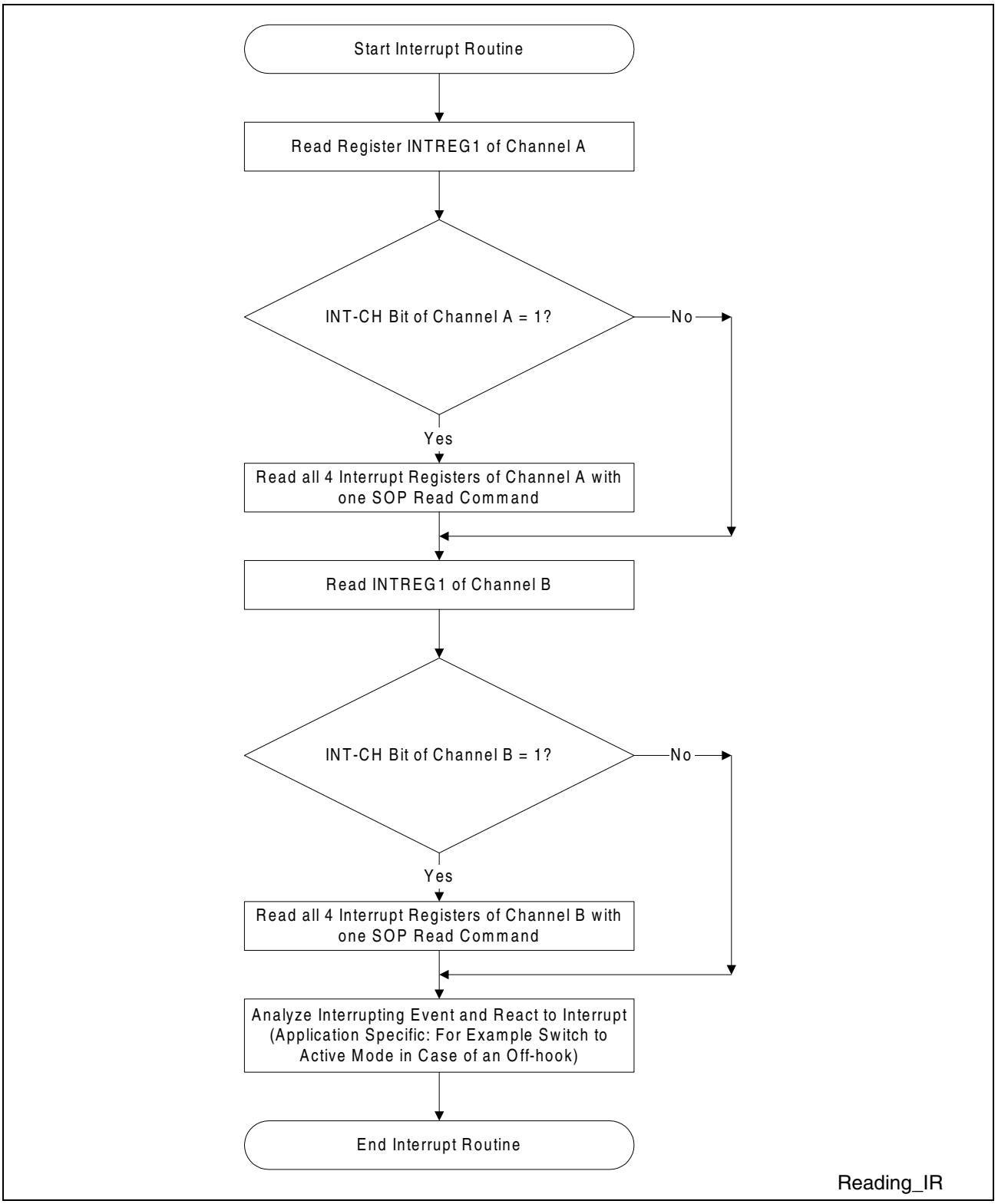


Figure 37 Reading Interrupt Registers

3.7 Power Management and Operating Modes

In many applications the power dissipated on the linecard is a critical parameter. In large systems it is the mean power value (taking into account traffic statistics and line length distribution) that determines cooling requirements. On the other hand, particularly in remotely fed systems, the maximum power per line must be kept below a given limit.

Generally, system power dissipation is determined primarily by the high-voltage part. The most effective power-saving method thus is to optimize both SLIC functionality and supply voltage. This is primarily achieved by using different operating modes.
The three main modes (Power Down, Active and Ringing) correspond to the main system states: on-hook, signal transmission (voice, DTMF and/or TTX) and ring signal feed.

Power Down

Off-hook detection is the only function available. It is achieved by internally connecting 5 kΩ resistors from Tip to BGND and from Ring to V_{BAT}. A simple sensing circuit supervises the DC current through these resistors (zero in on-hook and non-zero in off-hook state). This scaled transversal line current is transferred to the IT pin and compared with a programmable current threshold in the *SLICOFI-2x*. Only the DC loop in the *SLICOFI-2x* is active.

Sleep Mode

In Sleep mode both AC and DC loops are inactive. Off-hook detection, however, is still possible using an analog comparator. For lowest power consumption the clocks fed to the MCLK and PCLK pins also must be shut off.

To change the DuSLIC to another state, it must be woken up according to the procedure described in **Chapter 3.1**.

Active

Both AC and DC loops are operative. The SLIC provides low-impedance voltage feed to the line. An integrated supply voltage switch allows to choose between two (SLIC-S/E) or even three (SLIC-P) different battery voltages, depending on loop length.

Ringing

For internal ringing applications, the total supply range can be extended to 150 V to allow ring signals up to 85 Vrms. Whereas SLIC-S/E uses a positive supply VHR, the most negative battery voltage VBATR is intended for ringing with SLIC-P. The voltage capability is sufficient to drive very long lines at any ringer load and to reliably detect Ring trip. For an overview of all DuSLIC operating modes, see **Table 14** for PEB 4264/-2, **Table 15** for PEB 4265/-2 and **Table 16** for PEB 4266.

3.7.1 *SLICOFI-2x* Power Dissipation

For optimized power consumption, unused EDSP functions must be switched off. Typical power dissipation values for different operating modes of the *SLICOFI-2x* can be found in the device data sheets.

3.7.2 SLIC Power Dissipation

The SLIC's power dissipation can be divided into two parts, the first arising from internal bias currents, the second being caused by any current fed to the line:

$P = P_Q + P_O$

with

$$P_Q = V_{DD} * I_{DD} + |V_{BATL}| * I_{BATL} + |V_{BATH}| * I_{BATH} + |V_{BATR}| * I_{BATR} + V_{HR} * I_{HR} \quad [1]$$

$$P_O = (1.05 * V_{BATx} - V_{TR}) * I_{TR} = 1.05 * V_{BATx} * I_{TR} - R_{Loop} * I_{TR}^2 \quad [2]$$

Note: V_{BATx} is the relevant output stage supply voltage, whereas V_{TR}, I_{TR} and R_{Loop} denote line voltage, current and total line resistance, resp..

For any operating mode, the quiescent power dissipation P_Q (power at zero line current) thus is determined by the internal supply currents as specified in the respective SLIC data sheets (I_{BATR} = 0 for SLIC-E/S, I_{HR} = 0 for SLIC-P). Significant design effort has been spent to keep them low.

Nevertheless, in typical active operations, the power component P_O caused by the line current dominates. This power is dissipated in the output stages (to some small extent also in the current sensor) and is approximately proportional to the difference of respective supply voltage V_{BATx} and line voltage V_{TR}. Obviously, the best way for power reduction is to keep the supply voltage as low as possible.

3.7.2.1 Power Down Modes

In all Power Down modes, the internal bias currents are extremely small and no current is fed to the line. Even with active off-hook detection, the resulting power dissipation of 5 mW is negligible. It is worth pointing out, that in large systems, due to the high percentage of inactive lines, this is the dominant factor for achieving a very low mean power value.

3.7.2.2 Active Modes

In all active modes, the total power dissipation usually is dominated by the line current part P_O (eq. 2); the quiescent power typically is below 150 mW.

For any line with total resistance R_{Loop}, the battery supply V_{BATx} has to fulfill the condition

$V_{BATx} > I_{TR,DC} * R_{Loop} + V_{AC,pk} + V_{Drop}$

$V_{AC,pk}$ peak value of AC signal

V_{Drop} sum of voltage drops in SLIC output stage (typ. 2 V @ 20 mA)

Ideally, the supply voltage would be optimized individually for any line. This, however, is only possible at the expense of high effort, as it would require an highly efficient DC/DC converter per line. On the other hand, a single fixed VBAT is determined by the longest loop (largest R_{Loop}) to be served, and from eq. [2] would lead to very high power at short lines.

A very efficient way to reduce short-loop power dissipation now is to use a second, lower battery supply voltage (V_{BATL}) whenever line resistance is small enough. This method is supported on all SLICs by the integration of a battery switch (SLIC-P even allows the use of 3 battery voltages). The efficiency is demonstrated in **Figure 38** comparing typical total active power dissipation values for a 20 mA line current as a function of loop resistance for single -48 V (dotted) and double -48/-24 V (solid) battery voltages, resp..

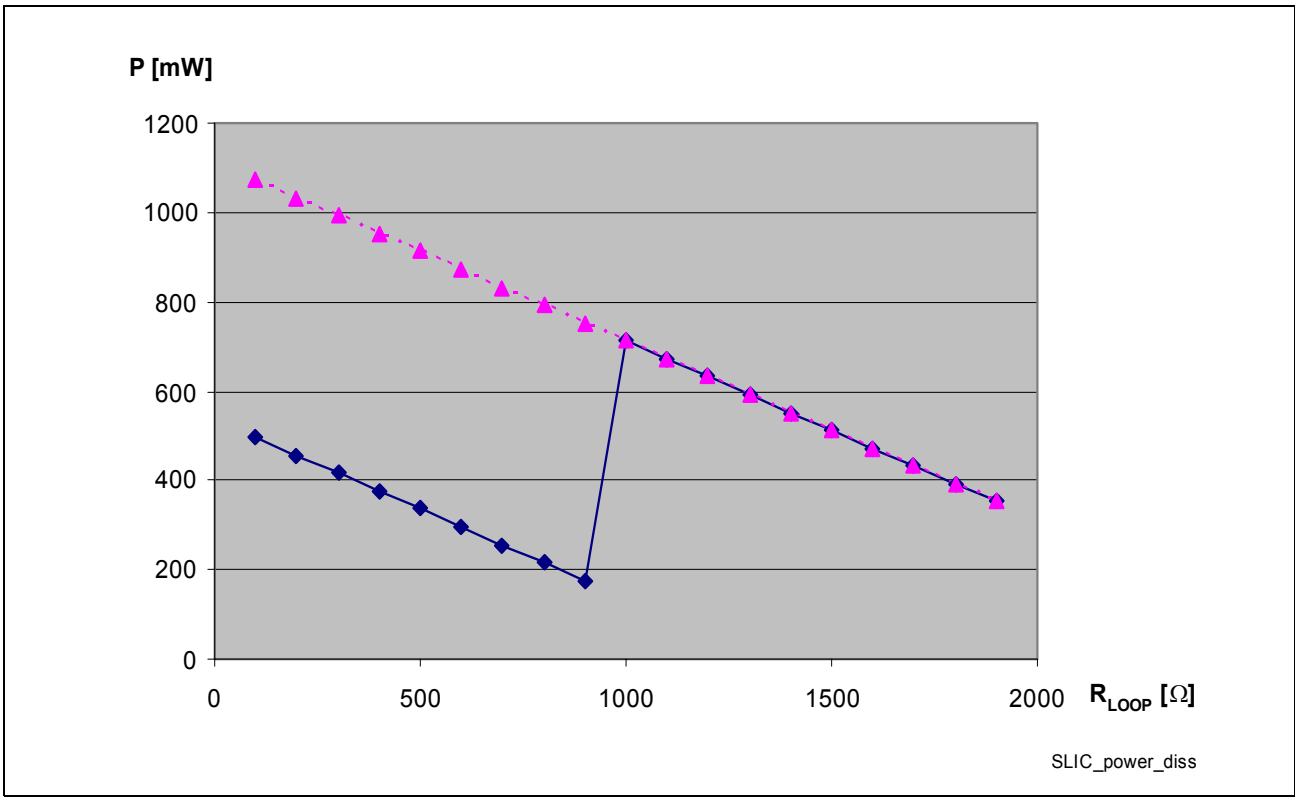


Figure 38 Typical SLIC Power Dissipation

3.7.2.3 Ringing Mode

Basically the considerations above are also valid in Ringing Mode. The only difference results from the fact, that in Ringing a large sinusoidal signal is applied to a complex RC load (compared with DC drive of an ohmic load in active modes). Eq. [2] is still valid, but obviously P_O now is time dependent due to the time dependence of both ringing voltage VTR and the resulting loop current.

If the total load impedance (loop resistance plus ringer load) is denoted as

$Z_L = |Z_L| * e^{j\phi} = R_{Loop} + R_{Ring} + 1 / j\omega C_{Ring}$

calculation of the average ring power yields

$P_O = (4 * V_{BATx} - \pi * V_{Ring,pk} * \cos \phi) * V_{Ring,pk} / (2 * \pi * Z_L)$

Here V_{BATx} again denotes the total battery supply voltage. The minimum value can be derived from the condition

$V_{BATx} > V_{Ring,pk} + V_{Ring,DC} + V_{Drop} = V_{Ring,rms} *$ crest factor $+ V_{Ring,DC} + V_{Drop}$

The crest factor is the ratio of peak and rms value (here 1.41, as sinusoidal ringing is assumed).

$V_{Ring,DC}$ superimposed DC voltage for Ring trip detection (10 to 20 V)

V_{Drop} sum of voltage drops in SLIC output stage (typ. 2 V @ 20 mA)

$V_{Ring,pk / rms}$ peak / effective ring voltage at Tip/Ring pins

As the resulting V_{BATx} for ringing typically is significantly larger than in active transmission modes, the total supply range is increased by either using an additional positive supply V_{HR} (so $V_{BATx} = V_{HR} - V_{BATH}$ for SLIC-S/E) or providing a third battery voltage V_{BATR} ($V_{BATx} = V_{BATR}$ for SLIC-P).

Again, to minimize power dissipation, V_{BATx} has to be kept as low as possible. In ringing, however, the voltage at the ringer rather than at the TIP/RING pins is decisive. Due to voltage division between ringer and line, the worst case for V_{BATx} is represented by maximum ringer load (minimum ringer impedance, e.g 5 US REN) at maximum loop length.

The above calculation is valid for power dissipation during the ring burst. The power values cover a broad range from typically 1 W to 3 W, mainly depending on the ringer load. The mean ring power then can be calculated by averaging over the burst / pause cycle. So for a typical ringing cadence (1 second on and 4 seconds off) power is given by

$P_{average} = k * P_{Ring} + (1 - k) * P_{RingPause}$

with k = 0.20

3.8 Integrated Test and Diagnostic Functions (ITDF)

3.8.1 Introduction

Subscriber loops are affected by a variety of failures that must be monitored. Monitoring the loop requires access to the subscriber loop and requires test equipment in place that is capable of performing certain specific measurements. The tests involve measurement of resistance, capacitance, leakage, and any interfering currents and voltages.

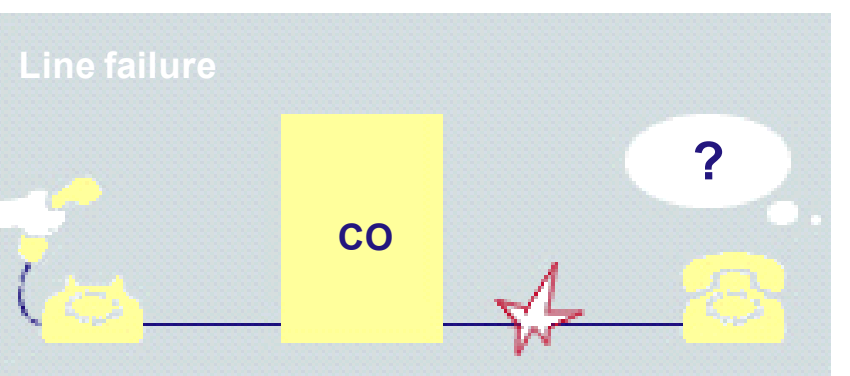
3.8.1.1 Conventional Line Testing

Conventional linecards in Central Office (CO) applications usually need two test relays per channel to access the subscriber loop with the appropriate test equipment. One relay (test-out) connects the actual test unit to the local loop. All required line tests can be accomplished that way. The second relay (test-in) separates the local loop from the SLIC and connects a termination impedance to it. Hence, sending a tone signal allows the entire loop to be checked, including the *SLICOFI-2x* and SLIC.

3.8.1.2 DuSLIC Line Testing

The DuSLIC chip set uses its Integrated Test and Diagnostic Functions (ITDF) to perform all tests necessary for monitoring the local loop without an external test unit and test relays. The fact that measurements can be accomplished much faster than with conventional test capabilities makes an even more compelling argument for the use of the DuSLIC chip set. With the DuSLIC, line tests on both channels can be performed concurrently, which also has a tremendous impact on the test time. All in all, the DuSLIC increases the quality of service and reduces the costs in various applications.

	Line Testing
DuSLIC-S	Yes
DuSLIC-S2	Yes
DuSLIC-E	Yes
DuSLIC-E2	Yes
DuSLIC-P	Yes



duslic_0025_linetesting

Figure 39 DuSLIC Line Testing

3.8.2 Diagnostics

DuSLIC incorporates signal generators and test features implemented to accomplish a variety of diagnostic functions. The *SLICOFI-2x* device generates all test signals, processes the information that comes back from the SLIC, and provides the data to a higher level master device, such as a microprocessor. All the tests can be initiated by the microprocessor and the results can be read back very easily.

3.8.2.1 Line Test Capabilities

The line test comprises the following functions:

- Loop resistance
- Leakage current Tip/Ring
- Leakage current Tip/GND
- Leakage current Ring/GND
- Ringer capacitance
- Line capacitance Tip/Ring
- Line capacitance Tip/GND
- Line capacitance Ring/GND
- Foreign voltage measurement Tip/GND
- Foreign voltage measurement Ring/GND
- Foreign voltage measurement Tip/Ring
- Measurement of ringing voltage
- Measurement of line feed current
- Measurement of supply voltage V_{DD} of the *SLICOFI-2x*
- Measurement of transversal- and longitudinal current

Two main transfer paths (level metering) are implemented to accomplish all the different line measurement functions (refer to **Figure 40**).

3.8.2.2 Integrated Signal Sources

The signal sources available on the DuSLIC chip set are:

- Constant DC voltage (three programmable ringing DC offset voltages)
  Refer to the CRAM coefficient set and register LMCR3 (bits RNG-OFFSET[1:0]) on **Page 185** for more information.
- 2 independent tone generators TG1 and TG2:
  Refer to the CRAM coefficient set and register DSCR (bits PTG, TG2-EN, TG1-EN) on **Page 179** for more information.
- TTX metering signal generator (12/16 kHz)
  Refer to the CRAM coefficient set and register BCR2 (bits TTX-DIS, TTX-12k) on **Page 170** for more information.
- Ramp generator (used for capacitance measurements)
  Refer to the CRAM coefficient set and register LMCR2 (bit RAMP-EN) on **Page 183**.

- Ring generator (5 Hz - 300 Hz)
  Refer to the CRAM coefficient **Table 35 "CRAM Coefficients" on Page 205**.

Figure 40 shows the entire level metering block for AC and DC:

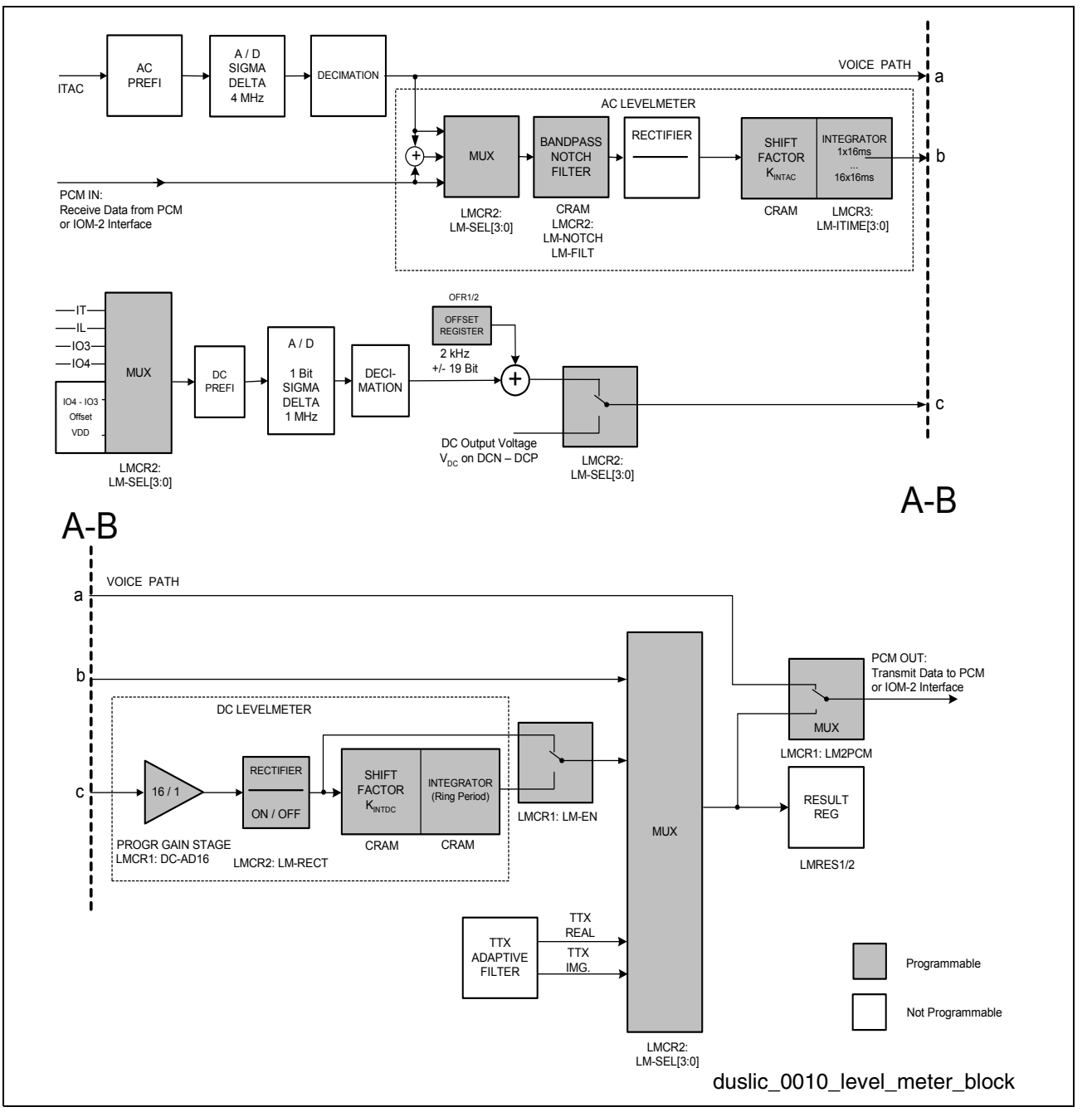


Figure 40 Level Metering Block Diagram

3.8.2.3 Result Register Data Format

The result of any measurement can be read via the result registers LMRES1/2. This gives a 16-bit value, with LMRES1 being the high and LMRES2 being the low byte. The result is coded in 16-bit two´s complement:

Table 18 Level Metering Result Value Range

Negative Value Range		Positive Value Range	
–Full Scale			**+Full Scale**
0x8000	0xFFFF	0	0x7FFF
–32768	–1	0	+32767

3.8.2.4 Using the Level Metering Integrator

Both AC and DC level metering allows use of a programmable integrator. The integrator may be configured for a single measurement or to run continuously. See **Figure 41** through **Figure 43**.

Single Measurement Sequence (AC & DC Level Metering)

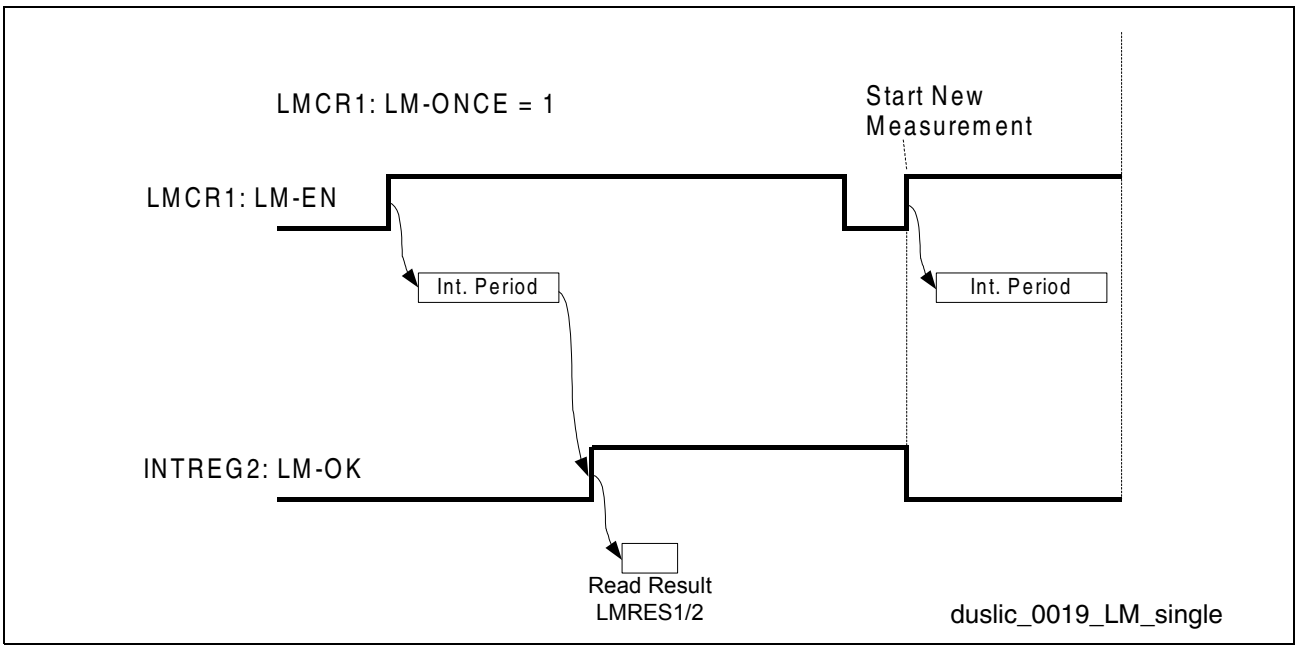


Figure 41 Single Measurement Sequence (AC & DC Level Metering)

Continuous Measurement Sequence (DC Level Metering)

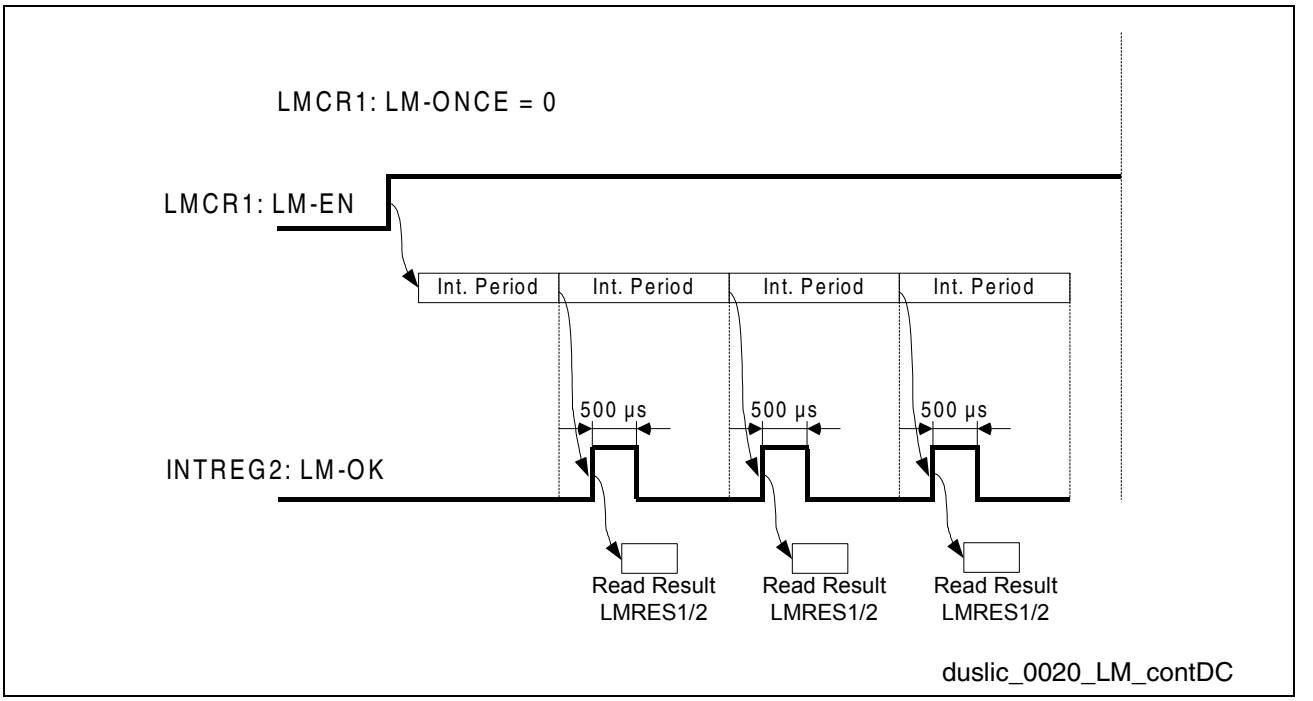


Figure 42 Continuous Measurement Sequence (DC Level Metering)

Continuous Measurement Sequence (AC Level Metering)

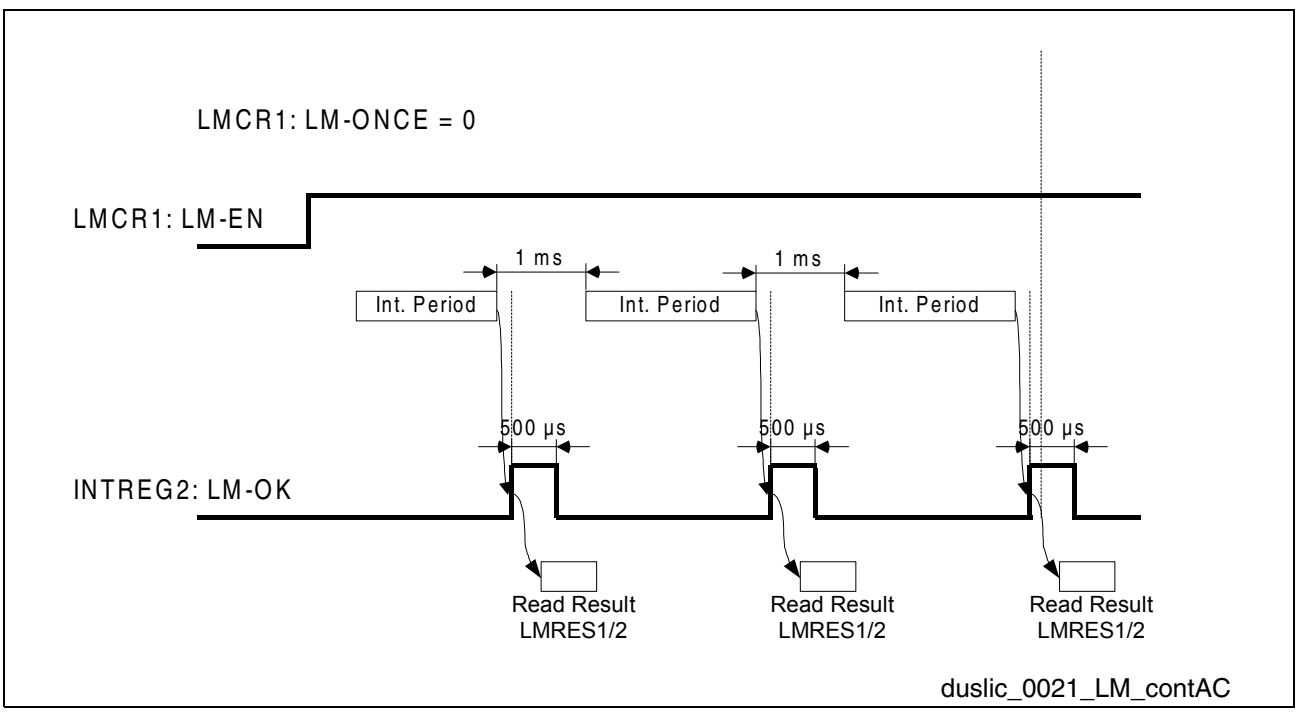


Figure 43 Continuous Measurement Sequence (AC Level Metering)

The integrated test and diagnostic functions of the DuSLIC allow to do measurements with and without an integrator. A measurement with the integrator is started by setting the bit LM-EN in register LMCR1 from 0 to 1.

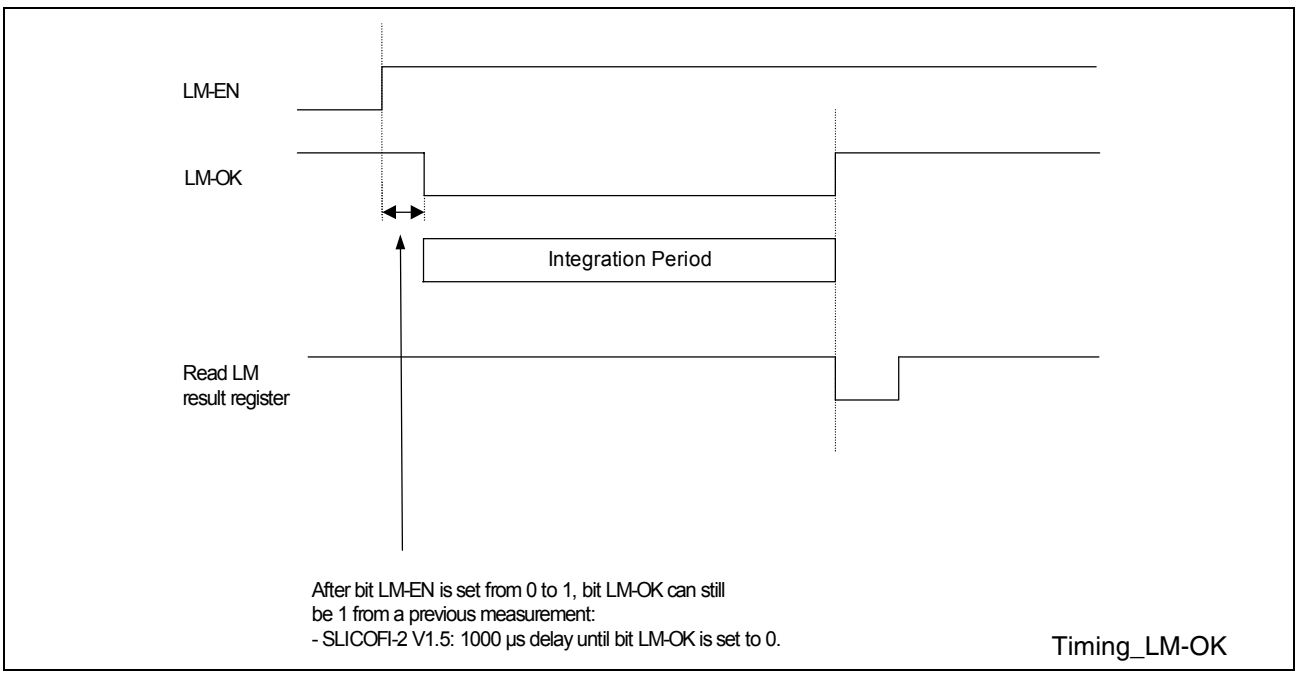


Figure 44 Timing LM-OK Bit

When using the integrator for doing levelmeter measurements, the LM-OK bit in register INTREG2 is used to indicate if the integration has started or is finished, respectively. After the bit LM-OK is set to 1 again, the result registers can be read to get the measurement result.

Figure 44 shows the timing of the bit LM-OK in relation to the start of the integration period (transition of LM-EN from 0 to 1) and in relation to a valid result in the result registers.

The user control software must take care of the mentioned timing relationship:

1. After starting the integrator by setting bit LM-EN from 0 to 1, the bit LM-OK could still be set to 1 from a previous measurement, which would indicate the end of the integration period while the actual integration is still going on.
   – With *SLICOFI-2x* Version 1.5, the firmware must wait at least 1 ms before polling the bit LM-OK.
2. After the integration is finished, the bit LM-OK is set to 1 by *SLICOFI-2x*.
   – With *SLICOFI-2x* Version 1.5, the LM-OK bit is set to 1 synchronous with the availability of the LM result. Therefore no delay is necessary before reading the levelmeter result registers.

3.8.2.5 DC Level Metering

The path of the DC level meter is shown in **Figure 40**. Hereby, the DC level meter results will be determined and prepared depending on certain configuration settings. The selected input signal becomes digitized after pre-filtering and analog-to-digital conversion. The DC level meter is selected and enabled as shown in **Table 19**:

Table 19 Selecting DC Level Meter Path

LM-SEL[3:0] in register LMCR2	DC Level Meter Path
0100	DC out voltage on DCP-DCN
0101	DC current on IT
1001	DC current on IL
1010	Voltage on IO3
1011	Voltage on IO4
1101	V_{DD}
1110	Offset of DC-pre-filter (short circuit on DC-pre-filter input)
1111	Voltage on IO4 – IO3

The effective sampling rate after the decimation stages is 2 kHz. The decimated value has a resolution of 19 bits. The offset compensation value (see **Chapter 3.8.2.8**) within the offset registers OFR1 (bits OFFSET-H[7:0]) and OFR2 (bits OFFSET-L[7:0]) can be set to eliminate the offset caused by the SLIC current sensor, pre-filter, and analog-to-digital converter. After the summation point the signal passes a programmable digital gain filter. The additional gain factor is either 1 or 16 depending on register LMCR1 (bit DC-AD16):

- LMCR1 (bit DC-AD16) = 0: No additional gain factor
- LMCR1 (bit DC-AD16) = 1: Additional gain factor of 16

The rectifier after the gain filter can be turned on/off with:

- LMCR2 (bit LM-RECT) = 0: Rectifier disabled
- LMCR2 (bit LM-RECT) = 1: Rectifier enabled

A shift-factor K_{INTDC} in front of the integrator prevents the level meter during an integration operation to create an overflow. If an overflow in the level meter occurs, the output result will be ± full scale (see **Table 18**).

If the shift factor K_{INTDC} is set to e.g. 1/8, the content of the level meter result register is the integration result divided by 8.

The shift factor K_{INTDC} is set in the CRAM (offset address 0x76):

CRAM:

Address 0x76: LMDC2/LMDC1
Address 0x77: 0/LMDC3

LMDC1, LMDC2 and LMDC3 are 4-bit nibbles which contain K_{INTDC}.

Table 20 K_{INTDC} Setting Table

LMDC1	LMDC2	LMDC3	K_{INTDC}
8	8	0	1
8	8	1	½
8	8	:	:
8	8	6	1/64
8	8	7	1/128

DuSLICOS allows automatic calculation of the coefficients for K_{INTDC} for I_{TRANS} measurement.

The according parameter is "DC Levelmeter current 50% full scale" (see DuSLICOS DC Control Parameters 4/4). The setting of this parameter affects the shift factor (K_{INTDC}) of the DC levelmeter. The set current will result in 50% full scale of the levelmeter result registers if the integration of the DC levelmeter is done over the integration period determined by the ring frequency. Example: if the DC levelmeter current 50% full scale is set to 2 mA and the actual current to be measured is 3 mA, the value of the levelmeter result register is 24575_D (75% full scale).

DuSLICOS uses finer steps as the examples listed in **Table 20**. If the user wants to set the K_{INTDC} factor manually, the listed steps should be sufficient.

The expected “Current for Ring Off-hook Detection” (see DuSLICOS DC Control Parameter 2/4) of 20 mA, for example, is entered in to the program and then K_{INTDC} is automatically calculated to achieve 50 % full scale if the current of 20 mA is integrated over the set ringer period.

The integration function accumulates and sums up the level meter values over a set time period. The time period is determined by the programmed ring frequency. A ring frequency f_{RING} of 20 Hz results in 100 samples ($N_{Samples}$), because of the 2 kHz effective DC sampling rate $f_{S,DC}$.

$$N_{Samples} = \frac{f_{S,\ DC}}{f_{RING}} = \frac{2000Hz}{f_{RING}}$$

The number of integration samples $N_{Samples}$ may also be programmed directly by accessing dedicated bytes in the Coefficient RAM (CRAM).

CRAM:

Address 0x73: RGF2/RGF1
Address 0x74: RGA1/RGF3

RGF1, RGF2 and RGF3 are 4-bit nibbles which control the ring frequency $f_{RING.}$

RGA1 is a 4-bit nibble that is calculated by DuSLICOS and which controls the ringer amplitude (see DuSLICOS byte file). To ensure that RGA1 is not changed, please perform a read/modify/write operation.

Table 21 $N_{Samples}$ Setting Table

RGF1	RGF2	RGF3	f_{RING}	$N_{Samples}$
8	8	0	500	4
8	8	1	250	8
8	8	:	:	:
8	8	6	7.81	256
8	8	7	3.91	512

The integration function can be turned on and off by bit LM-EN in register LMCR1.

The level meter result of the selected signal source will be stored in the result registers LMRES1 (bits LM-VAL-H[7:0]) and LMRES2 (bits LM-VAL-L[7:0]) depending on the LM-SEL[3:0] bits in register LMCR2. The result registers get frequently updated every 500 µs if bit LM-EN in register LMCR1 = 0, or after an integration period, if bit LM-EN in register LMCR1 = 1. If the bit LM-ONCE in register LMCR1 is set to 1, then the integration is executed only once. To start again, bit LM-EN must be changed from 0 to 1. The level meter source/result can be transferred to the PCM/IOM-2 Interface, depending on the bit LM2PCM in register LMCR1.

Table 22 shows the level meter results without and with integrator function. The integrator is enabled if bit LM-EN in register LMCR1 = 1.

The level meter result LM_{Value} is a 16 bit two´s complement value of LM-VAL-H[7:0] and LM-VAL-L[7:0].

The factor LM_{Result} used in **Table 22** is defined:

$$LM_{Result} = \frac{LM_{Value}}{32768}$$

- Example for positive value of LM_{Result}:

LM-VAL-H = “0010 0100" = 0x24

LM-VAL-L = “1010 0101" = 0xA5

LM_{Value} = 0x24A5 = 9381

LM_{Result} = 0.2863

- Example for negative value of LM_{Result}:

LM-VAL-H = “1001 1001" = 0x99

LM-VAL-L = “0110 0010" = 0x62

LM_{Value} = 0x9962 = –26270

LM_{Result} = –0.8017

Table 22 Level Meter Results with and without Integrator Function

	LM-EN = 0 (without Integrator)	LM-EN = 1 (with Integrator)
I_{TRANS}[1]: Power Down Resistive	$I_{TRANS} = LM_{Result} \times \frac{K_{IT,\ PDR}}{R_{IT2}} \times V_{AD}$ $I_{TRANS} = LM_{Result} \times 7.966\ mA$	$I_{TRANS} = LM_{Result} \times \frac{K_{IT,\ PDR} \times V_{AD}}{R_{IT2} \times N_{Samples} \times K_{INTDC}}$ $I_{TRANS} = LM_{Result} \times \frac{7.966\ mA}{N_{Samples} \times K_{INTDC}}$
I_{TRANS}[1]: any other mode	$I_{TRANS} = LM_{Result} \times \frac{K_{IT}}{R_{IT2}} \times V_{AD}$ $I_{TRANS} = LM_{Result} \times 79.66\ mA$	$I_{TRANS} = LM_{Result} \times \frac{K_{IT} \times V_{AD}}{R_{IT2} \times N_{Samples} \times K_{INTDC}}$ $I_{TRANS} = LM_{Result} \times \frac{79.66\ mA}{N_{Samples} \times K_{INTDC}}$
I_{LONG}[2]	$I_{LONG} = -LM_{Result} \times \frac{K_{IL}}{R_{IL}} \times V_{AD}$ $I_{LONG} = -LM_{Result} \times 67.7\ mA$	$I_{LONG} = -LM_{Result} \times \frac{K_{IL} \times V_{AD}}{R_{IL} \times N_{Samples} \times K_{INTDC}}$ $I_{LONG} = -LM_{Result} \times \frac{67.7\ mA}{N_{Samples} \times K_{INTDC}}$
Voltage: IO3[3], IO4[4], IO4-IO3[5]	$V_{INPUT} = -LM_{Result} \times V_{AD}$	$V_{INPUT} = -LM_{Result} \times \frac{V_{AD}}{N_{Samples} \times K_{INTDC}}$
V_{DD}	$V_{DD} = -LM_{Result} \times 3.9\ V$	$V_{DD} = -LM_{Result} \times \frac{3.9\ V}{N_{Samples} \times K_{INTDC}}$
V_{DC}[6] with ACTL, ACTH	$V_{DC} = -LM_{Result} \times 76.35\ V$	$V_{DC} = -LM_{Result} \times \frac{76.35\ V}{N_{Samples} \times K_{INTDC}}$
V_{DC}[6] with ACTR, ringing mode	$V_{DC} = -LM_{Result} \times 152.7\ V$	$V_{DC} = -LM_{Result} \times \frac{152.7\ V}{N_{Samples} \times K_{INTDC}}$

1) DC current on pin IT (bits LM-SEL[3:0] = 0101)

2) DC current on pin IL (bits LM-SEL[3:0] = 1001)

3) Voltage on IO3 referenced to V_{VCM} (typical 1.5 V) (bits LM-SEL[3:0] = 1010)

4) Voltage on IO4 referenced to V_{VCM} (typical 1.5 V) (bits LM-SEL[3:0] = 1011)

5) Voltage on IO4 – IO3 referenced to V_{VCM} (typical 1.5 V) (bits LM-SEL[3:0] = 1111)

6) DC output voltage at SLIC measured via DCN – DCP (bits LM-SEL[3:0] = 0100)

K_{INTDC}	Shift Factor (see **Table 20**)	
$K_{IT,PDR}$	Value of the current divider in power down resistive mode	5
K_{IT}	Value of the current divider for transversal current	50
K_{IL}	Value of the current divider for longitudinal current	100
R_{IT2}	Sense resistor for transversal current	680 Ω
R_{IL}	Sense resistor for longitudinal current	1600 Ω
V_{AD}	Voltage at A/D converter referred to digital full scale	1.0834
V_{DC}	DC output voltage at SLIC measured via DCN – DCP	

Note: Measurement of pins IL, IO3, IO4, IO4-IO3 and VDD can cause problems in the DC loop. The measured value is always interpreted as I_{TRANS} current. This can disturb the DC regulation and the off-hook indication. In Active mode, the output of the DC loop can be frozen by setting the bit DC-HOLD to 1. In Ringburst mode, it is possible for DuSLIC to automatically switch back to Ringpause mode if the measurement result was interpreted as off-hook. This can be avoided by programming the off-hook current to the maximum value (79.66 mA).

Measurement of AC Signals via DC Level Meter

This method is applicable for a single frequency sinusoidal AC signal that is superimposed on a DC signal.

1. Set the ring frequency f_{RING} to the frequency of the signal to be measured. Multiples of the expected signal period may also be used.
2. Set the offset registers OFR1 and OFR2 to 0x00.
3. Measure the DC contents with disabled rectifier (bit LM-RECT = 0).
   The DC contents can be calculated as described in **Table 22**.
   Note: If there was an overflow inside the integrator during the integration period, the result will be ± full scale. Reduce the shift factor K_{INTDC} or the number of samples $N_{Samples}$ and start the measurement again.

4. The offset registers OFR1 and OFR2 must be programmed to the value

$$OFFSET = -\frac{LM_{Value}}{N_{Samples} \times K_{INTDC}}$$

   where OFR1 is the high byte and OFR2 is the low byte of the 16 bit word OFFSET.
5. Repeating the measurement of the DC content should result in a LM_{Value} of zero.
6. Perform a new measurement with the rectifier enabled (bit LM-RECT = 1). The result is the rectified mean value of the measured signal an can be calculated with the formulas of **Table 22**.
7. From this result, the peak value and the RMS value can be calculated:

$$V_{Peak} = \frac{|V|_{Mean} \times \pi}{2}$$

$$V_{RMS} = \frac{V_{Peak}}{\sqrt{2}}$$

3.8.2.6 AC Level Meter

The AC level meter is selected and enabled as shown in **Table 23**:

Table 23 Selecting AC Level Meter Path

LM-SEL[3:0] in register LMCR2	AC Level Meter Path
0000	AC level meter in transmit
0110	AC level meter in receive
0111	AC level meter receive + transmit

Figure 40 on **Page 96** shows the path of the AC/TTX level meter functions. The AC level meter allows access to the voice signal while the active voice signal is being processed. The input signal for the AC level meter might get processed with a programmable filter characteristic, such as a bandpass- or notch filter. Depending on the following settings, the bandpass or notch filter is turned on or off:

- Register LMCR2 bit LM-FILT = 0: No filter enabled (normal operation)
- Register LMCR2 bit LM-FILT = 1: Bandpass/notch filter characteristics enabled
- Register LMCR2 bit LM-NOTCH = 0: Notch filter enabled, bandpass filter disabled
- Register LMCR2 bit LM-NOTCH = 1: Bandpass filter enabled, notch filter disabled

The rectifier cannot be turned off, it is always active in the AC path. A shift-factor in front of the integrator prevents the level meter from creating an overflow during an integration operation. The shift-factor can be set by the coefficient LM-AC gain (see CRAM coefficient set **Table 35 "CRAM Coefficients" on Page 205**).

K_{INTAC} can be set via coefficient LM-AC:

CRAM:

Address 0x34: CG1/LM-AC

LM-AC is a 4-bit nibble which contains $K_{INTAC.}$

CG1 is a 4-bit nibble that is calculated by DuSLICOS and which controls the conference gain (see DuSLICOS byte file). To ensure that CG1 is not changed, please perform a read/modify/write operation.

Table 24 K_{INTAC} Setting Table

LM-AC	K_{INTAC}
0	1
1	½
:	:
6	1/64
7	1/128

The integration function accumulates and sums up the level meter values over a set time period. The time period from 1*16 ms to 16*16 ms is set by the bits LM-ITIME[3:0] in register LMCR3. The integration function can be turned on and off by bit LM-EN in register LMCR1.

The number of samples $N_{Samples}$ for the integrator is defined by:

$N_{Samples}$ = LM-ITIME * 8000

The level can be calculated by:

$$U_{dBm0} = 20 \times \log\left(LM_{Result} \times \frac{\pi}{2 \times K_{INT} \times N_{Samples}}\right) + 3.14$$

The result registers get frequently updated after an integration period, if bit LM-EN in register LMCR1 = 1. If the bit LM-ONCE in register LMCR1 is set to 1 then the integration is executed only once. To start again, bit LM-EN must be changed from 0 to 1.
The level meter result can be transferred to the PCM/IOM-2 Interface, depending on bit LM2PCM in register LMCR1.

Measurement of Currents via ITAC

To take current measurements via pin ITAC, all feedback loops (IM-filters and TH-filters) should be disabled. To simplify the formulas, the programmable receive and transmit gain is disabled.

This is done by setting the following bits:

Register BCR4: AR-DIS = 1, AX-DIS = 1, TH-DIS = 1,
IM-DIS = 1, FRR-DIS = 1, FRX-DIS = 1

Register TSTR4: OPIM-AN = 1, OPIM-4M = 1

Register LMCR1: TEST-EN = 1

This setting results in a receive gain of 11.88 dB caused by the internal filters. Based on this, a factor K_{AD} (analog to digital) can be defined:

$$K_{AD} = \frac{10^{\frac{filter_{AD}}{20}}}{V_{ADC}} = \frac{10^{\frac{11.88}{20}}}{1.2\ V} = 3.272\ V^{-1}$$

Transversal current I_{RMS} measured at SLIC:

$$_{RMS} = \frac{LM_{Result} \times K_{IT} \times \pi}{K_{AD} \times R_{ITAC} \times K_{INTAC} \times N_{Samples} \times 2 \times \sqrt{2}} = \frac{LM_{Result}}{K_{INTAC} \times N_{Samples}} \times 14.76\ mA$$

R_{ITAC}	Sense resistor for AC transversal current (R_{IT1} + R_{IT2})	1150 Ω
K_{AD}	Constant factor from Analog to Digital	3.272 V^{-1}
V_{ADC}	Voltage at A/D converter referred to digital full scale	1.2 V
K_{IT}	Value of the current divider for transversal current	50

To prevent overloading the analog input, the maximum AC transversal current may not be higher than 9 mA rms.

Usage of Tone Generator as Signal Source

To simplify the formulas, the programmable receive and transmit gain is disabled.

This is done by setting the following bits:

Register BCR4: AR-DIS = 1, AX-DIS = 1, TH-DIS = 1,
IM-DIS = 1, FRR-DIS = 1, FRX-DIS = 1

Register TSTR4: OPIM-AN = 1, OPIM-4M = 1

Register LMCR1: TEST-EN = 1

The tone generator level is influenced by a factor K_{TG}, which is set in the tone generator coefficients. The internal filter attenuation is 2.87 dB.

$$K_{DA} = V_{DAC} \times 10^{\frac{-2.87}{20}} \times \frac{Trapez}{\sqrt{2}} \times K_{AC,SLIC} = 1.2 \times 10^{\frac{-2.87}{20}} \times \frac{1.05}{\sqrt{2}} \times 6$$

K_{DA}	Constant factor from Digital to Analog	3.84 Vrms
$K_{AC,SLIC}$	Amplification factor of the SLIC	6
V_{DAC}	Voltage at D/A converter referred to digital full scale	1.2 V
Trapez	Crest factor of the trapezoidal signal	1.05

Output voltage between Tip and Ring:

$V_{OUT} = K_{DA} * K_{TG}$

The bytes below are valid for tone generator TG1 an a frequency of 1000 Hz.

CRAM:

Address 0x38: 0x08
Address 0x39: T11G/0
Address 0x40: T13G/T12G
Address 0x41: 0x05
Address 0x42: 0xB3
Address 0x43: 0x01

T11G, T12G and T13G are 4-bit nibbles which control the amplitude of the tone generator TG1.

Table 25 K_{TG} Setting Table

T11G	T12G	T13G	K_{TG}
8	9	1	7/8
8	0	8	½
8	1	8	¼
8	:	8	:
8	5	8	1/64
8	6	8	1/128
8	7	8	1/256

3.8.2.7 Level Meter Threshold

A threshold can be set for the level meter result. When the result exceeds the threshold, then bit LM-THRES in register INTREG 2 is set to 1. It is also possible to activate an interrupt when the LM-THRES bit changes by setting the bit LM-THM (level meter threshold mask bit) in register LMCR2 to 0.

The level meter threshold can be calculated with DuSLICOS or may be taken from **Table 26**.

CRAM:

Address 0x2C: LMTH2/LMTH1
Address 0x2D: 0/LMTH3

(LMTH1, LMTH2 and LMTH3 are 4 bit nibbles)

Table 26 Threshold Setting Table

LMTH1	LMTH2	LMTH3	Threshold
1	0	0	75.0 %
0	1	0	62.5 %
8	8	0	50.0 %
8	9	0	37.5 %
9	0	0	25.0 %
8	1	0	12.5 %
8	0	0	0.0 %

3.8.2.8 Current Offset Error Compensation

The current offset error caused by the current sensor inside the SLIC can be compensated by programming the compensation registers OFR1 and OFR2 accordingly. The current offset error can be measured with the DC level meter. The following settings are necessary to accomplish this:

- The DuSLIC must be set into the HIRT mode by setting the bits HIR and HIT in register BCR1 to 1.
  In HIRT mode, the line-drivers of the SLIC are shut down and no resistors are switched to the line. As a matter of fact, no current is present in that mode, but the current sensor wrongly indicates a current flowing (current offset error).
- The DC path for I_{TRANS} current level meter must be selected by setting the LM-SEL[3:0] bits in register LMCR2 to 0101 (see **Table 19**).
- The offset registers OFR1 and OFR2 must be set to 0000h.
- $I_{Off\text{-}Err}$ can be calculated like shown for "I_{TRANS}: any other mode" in **Table 22** (see the example below).

The current offset error can be eliminated by programming the offset registers OFR1 and OFR2 according to the inverse value of the measured current offset error.

Example:

$K_{INTDC} = 1$, $N_{Samples} = 256$, $LM_{Value} = 0x0605 = 1541$

$$LM_{Result} = \frac{LM_{Value}}{32768} = \frac{1541}{32768} = 0.047$$

$$I_{off-Err} = LM_{Result} \times \frac{79.66\ mA}{N_{Samples} \times K_{INTDC}} = 0.047 \times \frac{79.66\ mA}{256 \times 1} = 0.0146\ mA$$

$$OFFSET = -\frac{I_{Off-Err}}{79.66\ mA} \times 32768 = -\frac{0.0146\ mA}{79.66\ mA} \times 32768 \approx -6 = 0xFFFA$$

Short form:

$$OFFSET = -\frac{LM_{Value}}{N_{Samples} \times K_{INTDC}}$$

OFR1 = OFFSET-H = 0xFF

OFR2 = OFFSET-L = 0xFA

3.8.2.9 Loop Resistance Measurements

The DC loop resistance can be determined by supplying a constant DC voltage $V_{TR,DC}$ to the Ring- and Tip line and measuring the DC loop current via IT pin. The following steps are necessary to accomplish this:

- Program a certain ring offset voltage RO1, RO2, RO3 (see DuSLICOS DC Control Parameter 2/4).
- Select ring offset voltage RNG-OFFSET[1:0] in register LMCR3 either to 01, 10 or 11. If 00 is selected, the DC regulation would be still active and would not allow resistance measurement.
- Choose an operation mode, either Active High (ACTH) or Ring Pause.
- Select the DC path for level meter by setting the bits LM-SEL[3:0] in register LMCR2 to 0101 (DC current on IT).
- The transversal current can be determined by reading the level meter result registers LMRES1, LMRES2.
- Based on the known constant output voltage $V_{TR,DC}$ (DC voltage according to RNG-OFFSET[1:0]) and the measured I_{TRANS} current, the resistance can be calculated. It should be noted that the calculated resistance includes also the onboard resistors R_{PROT} and R_{STAB}.

In order to increase the accuracy of the result, either the current offset can be compensated or the measurement can be done differentially. The latter approach eliminates the current- and voltage offsets.

Figure 45 shows an example circuit for resistance measurement:

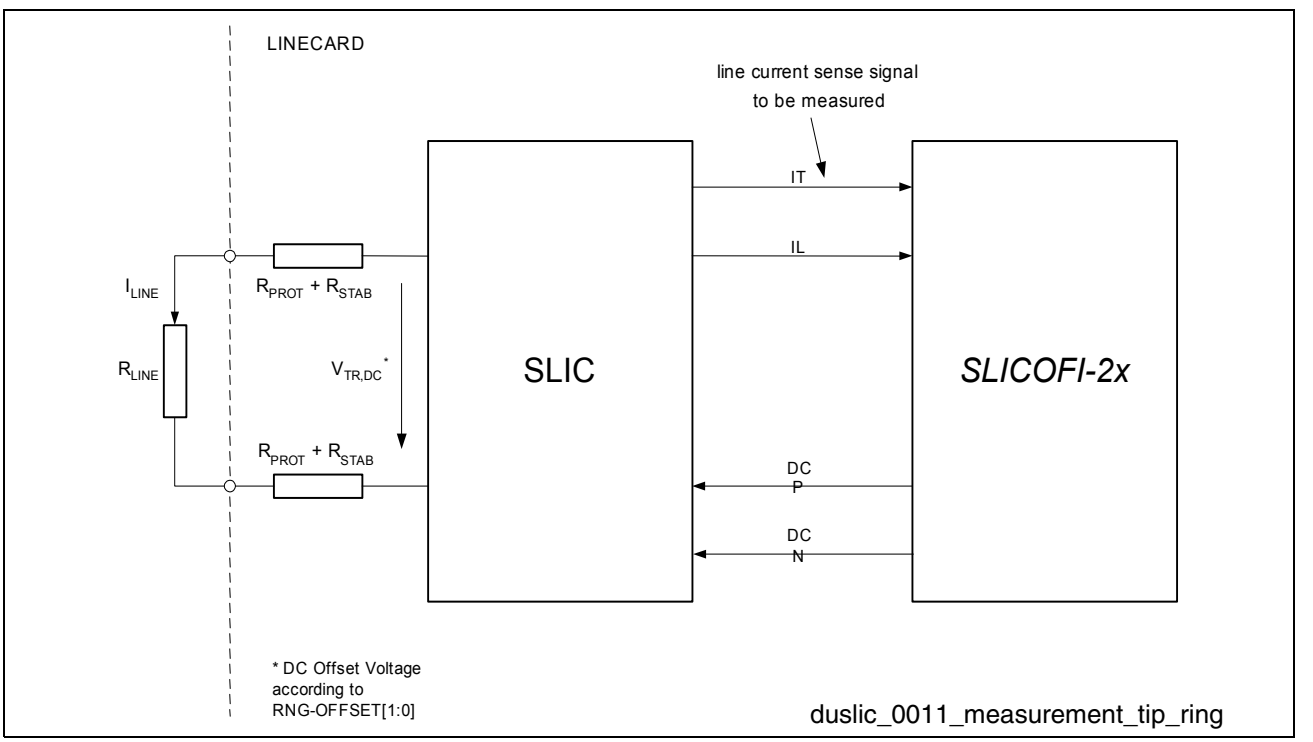


Figure 45 Example Resistance Measurement

Assumption:

- Loop resistance R_{loop} = 1000 Ω; $R_{loop} = R_{LINE} + 2*R_{PROT} + 2*R_{STAB}$
- Ring offset RO2 = 60 V (CRAM coefficient set accordingly). Ring offset RO2 is selected by setting bits RNG-OFFSET[1:0] in register LMCR3 to 10. The exact value for the Ring offset voltage can be determined from the *.res result file generated by DuSLICOS during the calculation of the appropriate coefficients.
- Select Active High (ACTH) mode by setting the line mode command CIDD/CIOP bits M2, M1, M0 to 010. In ACTH mode half of the ring offset voltage RO2 of e.g. 60 V will be present and applied to Ring and Tip.

Sequence to determine the loop resistance R_{loop} differentially:

- Select DC level meter by setting bits LM-SEL[3:0] in register LMCR2 to 0101.
- Read level meter result registers LMRES1, LMRES2.
- Switch into reverse polarity mode by setting bit REVPOL in register BCR1 to 1.
- Read level meter result registers LMRES1, LMRES2.

If the loop resistor connected between Ring and Tip is 1000 Ω ($R_{LINE} + R_{PROT} + R_{STAB}$), the expected current will be 30 mA, because the actual voltage applied to Ring and Tip is 30 V. Considering the fact that the current measurement in reverse polarity mode will also become inverted, the read results must be added. The sum of both level meter results (normal- and reverse polarity) should therefore be 60 mA current difference. **Figure 46** shows the differential measurement method and the elimination of the offsets.

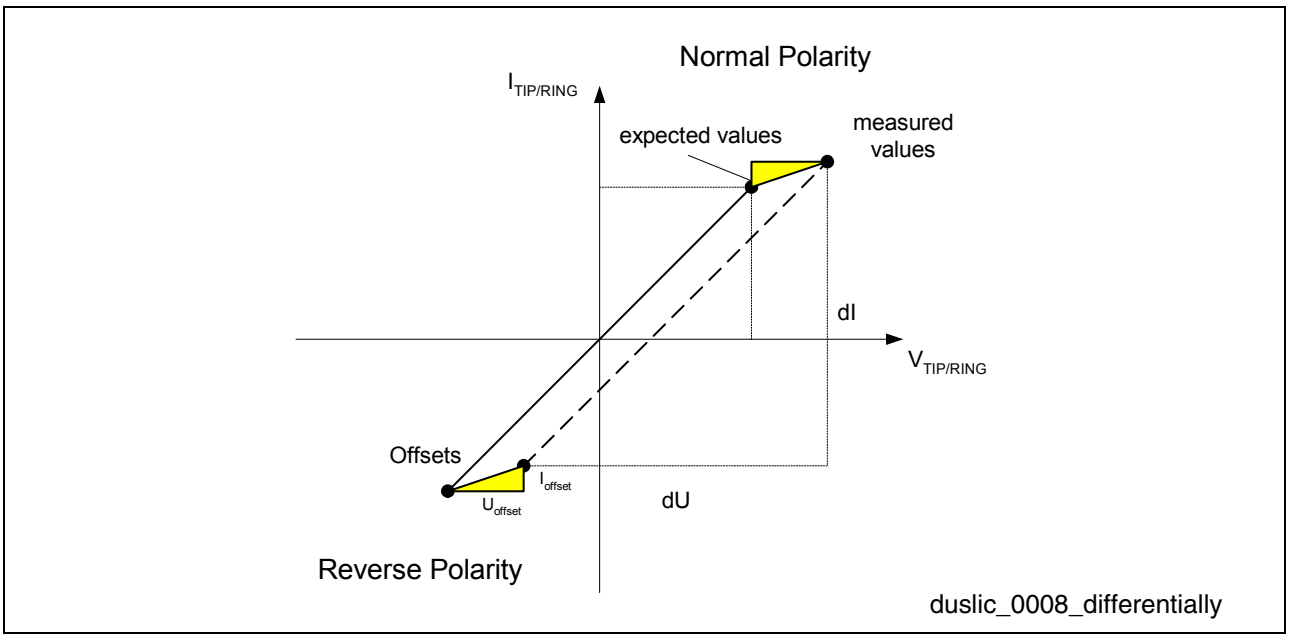


Figure 46 Differential Resistance Measurement

The following calculation shows the elimination of the voltage and current offset caused by output stage and current sensor. This differential measurement method eliminates the offsets caused by the SLIC current sensor and the offset caused by the DC voltage output (Ring offset voltage).

Differential Resistance Calculation:

$$I_{measure(normal)} = \frac{V_{TR,\ prog} + V_{offset}}{R} + I_{offset}$$

$$I_{measure(reverse)} = \frac{-V_{TR,\ prog} + V_{offset}}{R} + I_{offset}$$

$$measure(normal) - I_{measure(reverse)} = \frac{2 \times V_{TR,\ prog}}{R}$$

$$R = \frac{2 \times V_{TR,\ prog}}{I_{measure(normal)} - I_{measure(reverse)}} = R_{LINE} + R_{PROT} + R_{STAB}$$

3.8.2.10 Line Resistance Tip/GND and Ring/GND

The DuSLIC offers a choice of modes: either the Tip- or the Ring line or both can be set to high impedance by setting the bits HIR and HIT in register BCR1 accordingly. While one of the two lines is set to high impedance, the other line is still active and able to supply a known voltage. The transversal and/or longitudinal current can be measured and the line impedance can be calculated.

Because of one line (Tip or Ring) being high impedance, there is only current flowing in either Tip or Ring line. This causes the calculated current (according **Table 22**) to be half the actual value. Therefore, in either HIR or HIT mode, the calculated current must be multiplied by a factor of two.

3.8.2.11 Capacitance Measurements

Capacitance measurements with the DuSLIC are accomplished by using the integrated ramp generator function. The ramp generator is capable of applying a voltage ramp to the Ring- and Tip line with the flexibility of:

– Programmable slopes from 30 V/s to 2000 V/s
– Programmable start- and stop DC voltage offsets via ring offsets
– Programmable start time of the voltage ramp after enabling the level meter function

Figure 47 shows the voltage ramp and the voltage levels at the Ring and Tip line. The slope of the ramp can be programmed (refer to CRAM coefficients). The ring offset voltages RO1, RO2, and RO3 might be used as start and stop voltages. The ramp starts, for instance, at RO1 and stops at RO2. The current can be calculated as $i(t) = C_{Measure}*dU/dt$, where dU/dt is the slope and i(t) is the current that will be measured by the level meter. To accurately measure values, the integration must start after the current has settled to a constant value. This can be calculated by the time constant of the ringer load. It is recommended that the programmable ring generator delay be set higher than three times the time constant of the ringer load. When there is a resistor in parallel to the capacitor (for example, leakage), it is recommended to measure symmetrically around

the voltage zero crossing. This can be achieved by programming the ring generator delay appropriately (see DuSLICOS DC Control Parameter 2/4). The integration time for the current measurement is determined by the ring frequency (refer to CRAM coefficients, see **Table 21**). After the integration time, measurement stops automatically only if the bit LM-ONCE in register LMCR1 is set. Otherwise, the level meter would continuously measure the current even if the ramp is finished and turned into its constant voltage position. Because of the constant voltage, no current will flow.

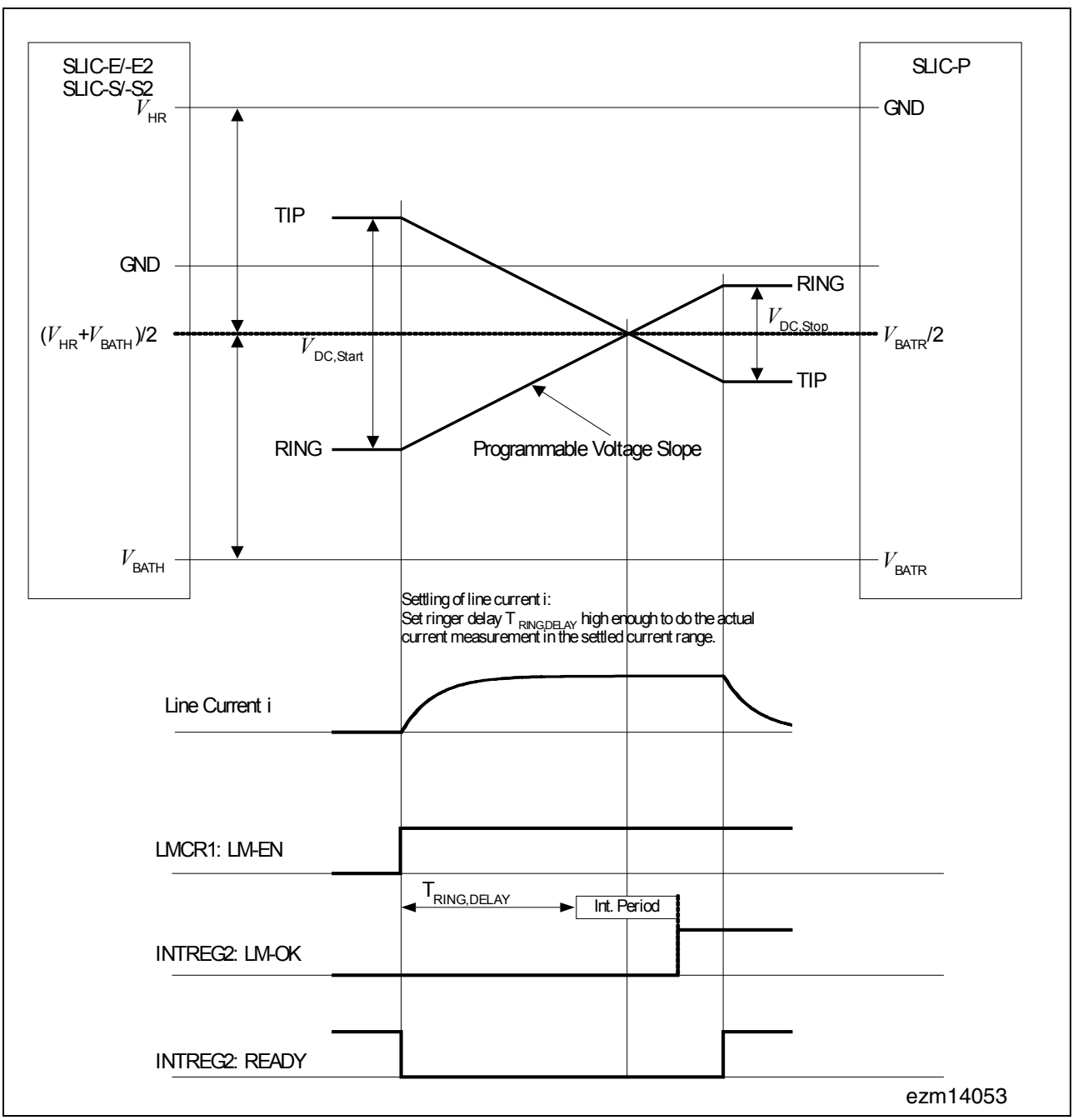


Figure 47 Capacitance Measurement

Example

- Assumptions:
  - Capacitance as object to be determined: $C_{Measure}$ = 9.8 µF
  - Resistor $R_{Measure}$ in series to $C_{Measure}$: $R_{Measure}$ = 6930 Ω
  - $\tau = R_{Measure}*C_{Measure}$ = 67.9 ms
- Calculating parameter values:
  - Choose Ring Offset voltage 1: RO1 = 70 V (Start voltage on Tip/Ring where the ramp should start; programmed by ring offset voltage RO1)
  - Choose Ring Offset voltage 2: RO2 = –30 V (End voltage on Tip/Ring where the ramp should stop; programmed by ring offset voltage RO2)
  - Choose slope of ramp while testing: dU/dt = 200 V/s
  - Time from start to stop of the ramp from RO1 to RO2 is 100 V/200 V/s = 500 ms
  - Time from start to zero cross is 70 V/200 V/s = 350 ms
  - Choose Integration time: $T_I = 1/f_{RING}$ = 1/100 Hz = 10 ms
  - Measure around zero cross →from 345 ms to 355 ms
  - $T_{RING,DELAY}$ is programmed to 345 ms
  - Check ring generator delay: $T_{RING,DELAY} > 3*\tau$ = 204 ms →OK!
  - Expected current $i = C_{Measure}*dU/dt$ = 1.96 mA
  - Choose current for DC levelmeter current 50% full scale $I_{LM,DC}$ = 2 mA
    Note: A current of 2 mA will result in LM_{Result} = 0.5 (half of the full scale value)

Program Sequence

- Set the following parameter values:

Parameter	Symbol & Value	DuSLICOS
Voltage slope of ramp generator	dU/dt = 200 V/s	DC Control Parameter 3/4
Ring frequency	f_{RING} = 100 Hz	DC Control Parameter 2/4
Ring generator delay	$T_{RING,DELAY}$ = 345 ms	DC Control Parameter 2/4
Ring offset voltage 1	RO1 = 70 V	DC Control Parameter 2/4
Ring offset voltage 2	RO2 = –30 V	DC Control Parameter 2/4
DC levelmeter current 50% full scale	$I_{LM,DC}$ = 2 mA	DC Control Parameter 4/4

- Integration time $T_I = 1/f_{RING}$ = 1/100 Hz = 10 ms
- Select the DC level meter by setting bits LM-SEL[3:0] in register LMCR2 to 0101
- Execute the level meter only once by setting bit LM-ONCE in register LMCR1 to 1.
- Apply Ring Offset voltage RO1 to Ring and Tip line by setting bits RNG-OFFSET[1:0] in register LMCR3 to 01.

- Enable the ramp generator by setting bit RAMP-EN in register LMCR2 to 1.
- Apply Ring Offset voltage RO2 to Ring and Tip line by setting bits RNG-OFFSET[1:0] in register LMCR3 to 10.
- Enable the level meter by setting bit LM-EN in register LMCR1 to 1.
  – Comment: The voltage ramp starts at RO1 and ramps up/down until RO2 is achieved. After the integration time, the result will be stored within LMRES1 and LMRES2 registers.
- Read the result registers LMRES1 and LMRES2

The actual current $I_{CMeasure}$ amounts to:

$$I_{CMeasure} = 2 \times I_{LM,\ DC} \times LM_{Result}$$

The capacitance $C_{Measure}$ calculates as:

$$C_{Measure} = \frac{I_{CMeasure}}{\frac{dU}{dt}}$$

Example:

LM_{Value} = 0x3AF2 = 15090

LM_{Result} = 0.4605

$I_{CMeasure}$ = 2*2 mA*0.4605 = 1.842 mA

$C_{Measure}$ = 1,842 mA/200 V/s = 9.21 µF

Note: To increase the accuracy an offset calibration can be performed. The voltage ramp can be applied when the line is set to high impedance by setting bits HIR and HIT in register BCR1. In this way, the offset currents can be measured and substracted later. As an alternative a rising and a falling ramp can be used to compensate current offsets.

3.8.2.12 Line Capacitance Measurements Ring and Tip to GND

The voltage ramp can be applied to either line, whereas the other line is set to high impedance by setting bits HIR and HIT in register BCR1 accordingly. In this way, capacitance measurements from Ring and Tip to GND may be accomplished. Because of one line being set to high impedance, the actual line current will be twice the calculated one (multiplication by a factor of two necessary).

3.8.2.13 Foreign- and Ring Voltage Measurements

The DuSLIC supports two user-programmable input/output pins (IO3, IO4) that can be used for measuring external voltages. If the pins IO3 and/or IO4 are led properly over a voltage divider to the Ring- and Tip wire, foreign voltages from external voltage sources supplied to the lines can be measured on either pin; even a differential measurement will

be supported (IO4-IO3). To select the input information that is to be taken for the measurement, set bits LM-SEL[3:0] in configuration register LMCR2 (see **Table 27**).

Table 27 Measurement Input Selection

LM-SEL[3:0] in Register LMCR2	Measurement Input
1010	Voltage on IO3
1011	Voltage on IO4
1111	Voltage IO4 – IO3

The measurement is accomplished by the DC level meter function.

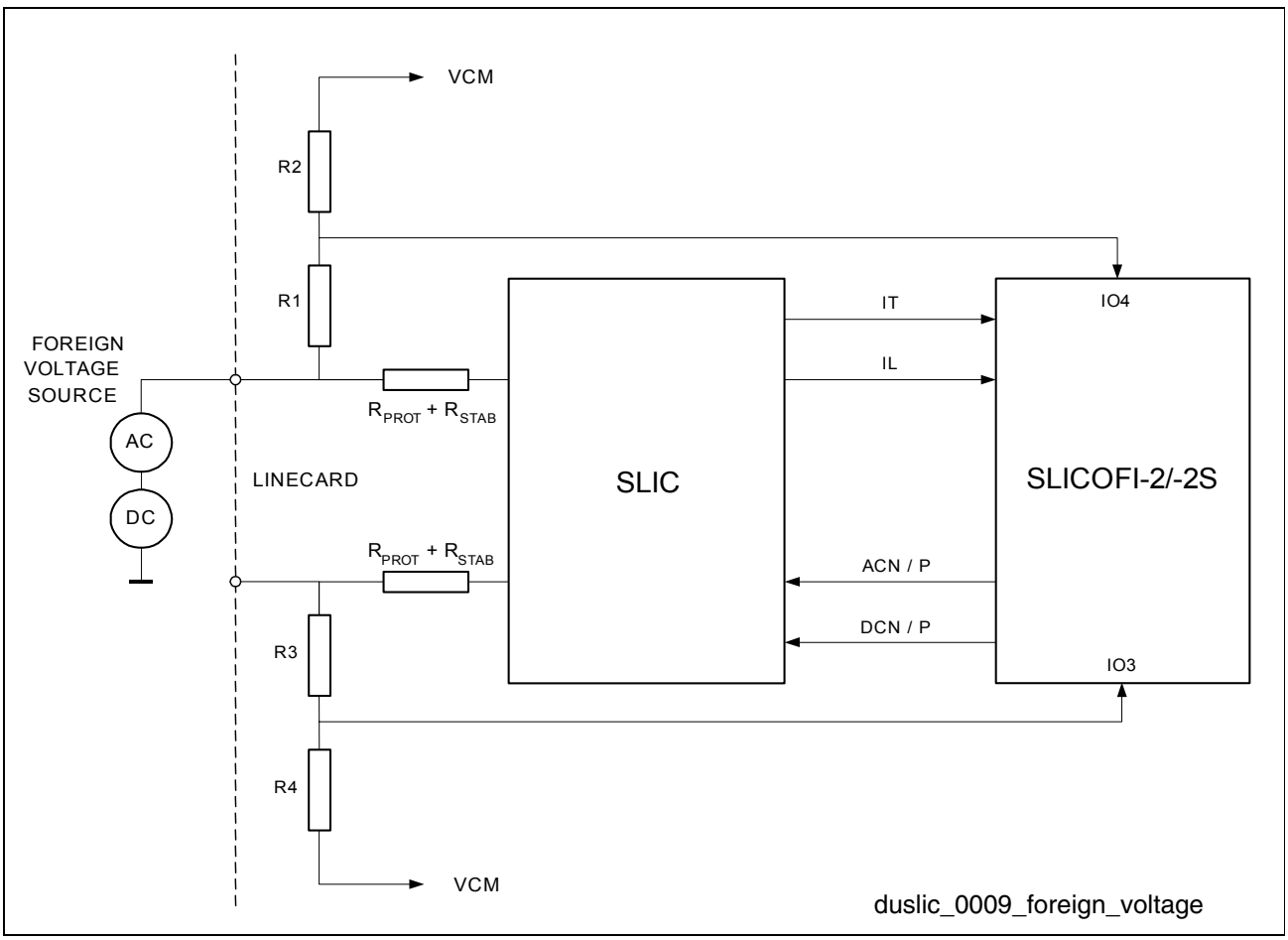


Figure 48 Foreign Voltage Measurement Principle

Figure 48 shows the connection and external resistors used for supporting foreign voltage measurements at the Ring and Tip lines.

Since the pins IO3 and IO4 support analog input functionality and are limited to a certain voltage range of V_{VCM} ± 1.0 V (typ. 1.5 V ± 1.0 V), the values for the voltage divider must be determined according to following conditions:

- Maximum level of the expected foreign voltages
- Voltage range of IO3 and IO4 = V_{VCM} ± 1.0 V

The voltage on IO3 or IO4 is measured with a reference to VCM. Hence, an input voltage of V_{VCM} on either input pin would result into zero output value. Whereas a voltage of V_{VCM} + 1 V would result into the negative full scale value, V_{VCM} – 1 V would result into the positive full scale value respectively. For that reason the voltage divider must be referenced to VCM. The unknown foreign voltage $V_{FOREIGN}$ can be calculated as:

$$V_{FOREIGN} = V_{INPUT} \times \frac{R1 + R2}{R2} + V_{VCM}$$

$V_{INPUT} = V_{IOx} – V_{VCM}$ (refer to **Table 22**)

V_{IOx} = Voltage on pins IOx (e.g. pins IO3, IO4)

The resistor directly connected to either Ring or Tip (R1, R3) should be high enough so that the loop impedance will not be affected by them. Several MΩ s, such as 10 MΩ, would be a reasonable value. The following example illustrates the potential voltage range that can be measured by choosing the values as:

- R1 = R3 = 10 MΩ
- R2 = R4 = 47 kΩ

The values given for the maximum and minimum voltage levels are:

- V_{VCM} = 1.5 V
- $V_{INPUT,max}$ = 1 V $\rightarrow V_{IOX,max}$ = 2.5 V
- $V_{INPUT,min}$ = –1 V $\rightarrow V_{IOX,min}$ = 0.5 V

$$V_{FOREIGN,\ max} = V_{INPUT,\ max} \times \frac{R1 + R2}{R2} + V_{VCM} = 215\ V$$

$$V_{FOREIGN,\ min} = V_{INPUT,\ min} \times \frac{R1 + R2}{R2} + V_{VCM} = -212\ V$$

The voltage range would span from 215 V to –212 V.

To measure small input voltages on IO3/IO4 more accurately, the integration function may be enabled by setting bit LM-EN in register LMCR1 to 1 (see **Figure 40**).

To measure the ring voltage supplied to either Ring or Tip or even both (balanced ringing) pins via IO3 and IO4, the rectifier can be enabled by setting bit LM-RECT in register LMCR2 to 1.

3.9 Signal Path and Test Loops

The following figures show the main AC and DC signal path and the integrated analog and digital loops of the DuSLIC-E/-E2/-P and DuSLIC-S/-S2. Please note the interconnections between the AC and DC pictures of the respective chip set.

3.9.1 AC Test Loops

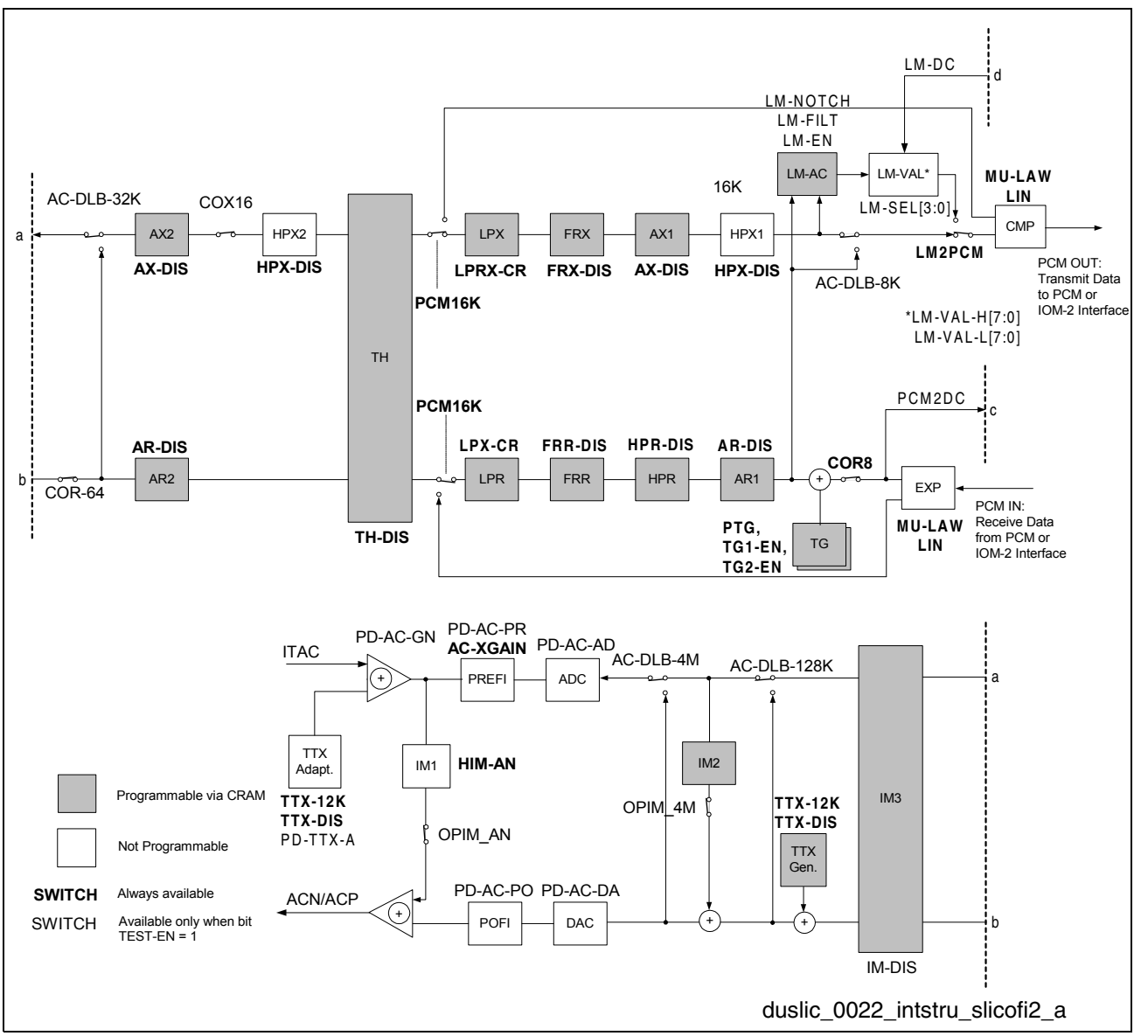


Figure 49 AC Test Loops DuSLIC-E/-E2/-P/-ES/-ES2

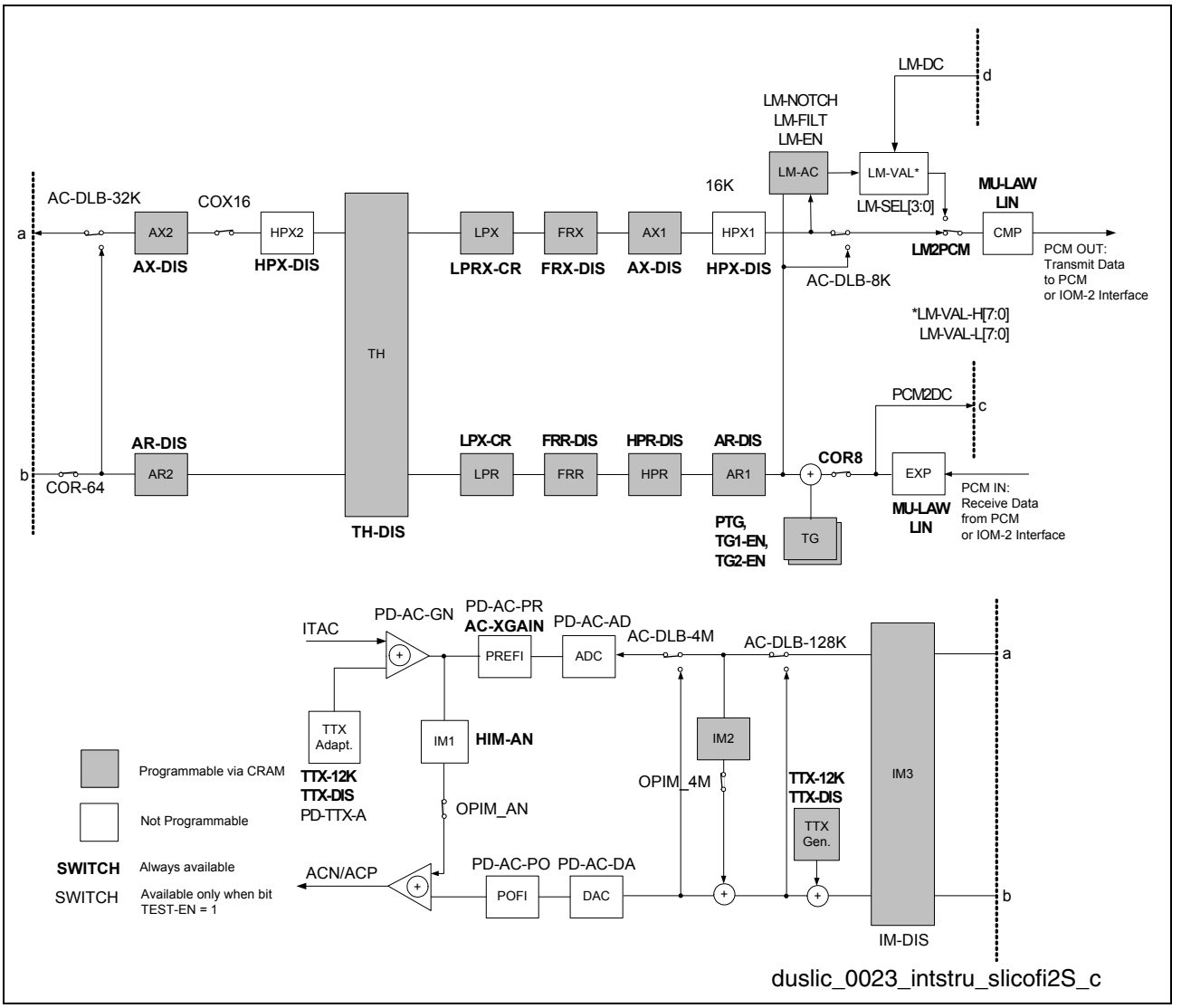


Figure 50 AC Test Loops DuSLIC-S/-S2/-SE/-SE2

3.9.2 DC Test Loops

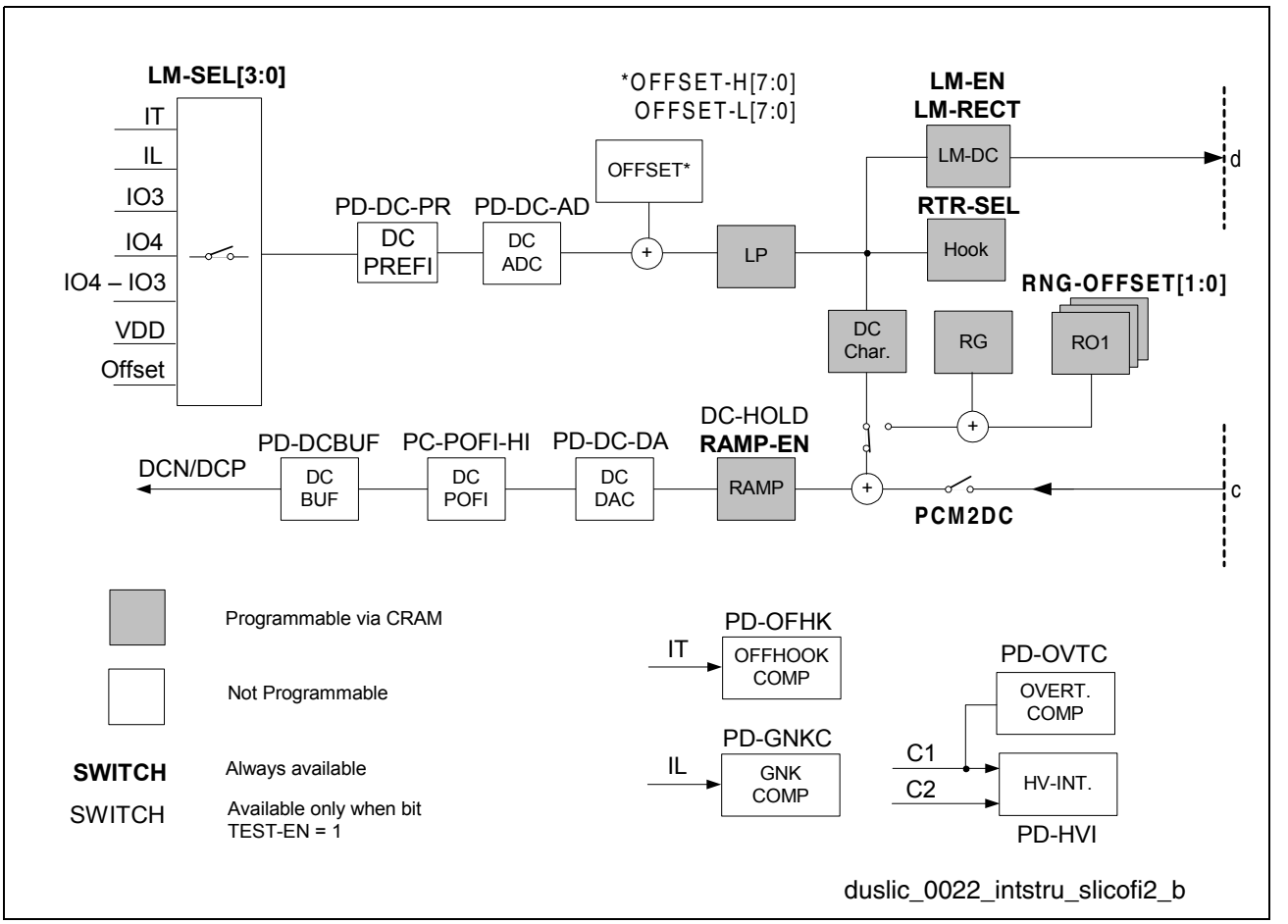


Figure 51 DC Test Loops DuSLIC

4 Interfaces

The DuSLIC offers two different interfaces to connect to a digital network:

- PCM Interface combined with a serial microcontroller interface
- IOM-2 Interface.

The PCM/$\overline{\text{IOM-2}}$ pin selects the interface mode.

– PCM/$\overline{\text{IOM-2}}$ = 0: IOM-2 mode.
– PCM/$\overline{\text{IOM-2}}$ = 1: PCM/µC mode.

The analog TIP/RING Interface connects the DuSLIC to the subscriber.

4.1 PCM Interface with a Serial Microcontroller Interface

In PCM/µC Interface mode, voice and control data are separated and handled by different pins of the *SLICOFI-2x*. Voice data are transferred via the PCM highways while control data are transferred using the Microcontroller Interface.

4.1.1 PCM Interface

The serial PCM Interface is used to transfer A-Law or µ-Law-compressed voice data. In test mode, the PCM Interface can also transfer linear data. The eight signals of the PCM Interface are used as follows (two PCM highways):

PCLK: PCM Clock, 128 kHz to 8192 kHz

FSC: Frame Synchronization Clock, 8 kHz

DRA: Receive Data Input for PCM Highway A

DRB: Receive Data Input for PCM Highway B

DXA: Transmit Data Output for PCM Highway A

DXB: Transmit Data Output for PCM Highway B

$\overline{\text{TCA}}$: Transmit Control Output for PCM Highway A. Active low during transmission

$\overline{\text{TCB}}$: Transmit Control Output for PCM Highway B. Active low during transmission

The FSC pulse identifies the beginning of a receive and transmit frame for both channels (see **Figure 52**). The PCLK clock signal synchronizes the data transfer on the DXA (DXB) and DRA (DRB) lines. On all channels, bytes are serialized with the MSB first. As a default setting, the rising edge indicates the start of the bit, while the falling edge is used to buffer the contents of the received data on DRA (DRB). If double clock rate is selected (PCLK clock rate is twice the data rate), the first rising edge indicates the start of a bit, while, by default, the second falling edge is used to buffer the contents of the data line DRA (DRB).

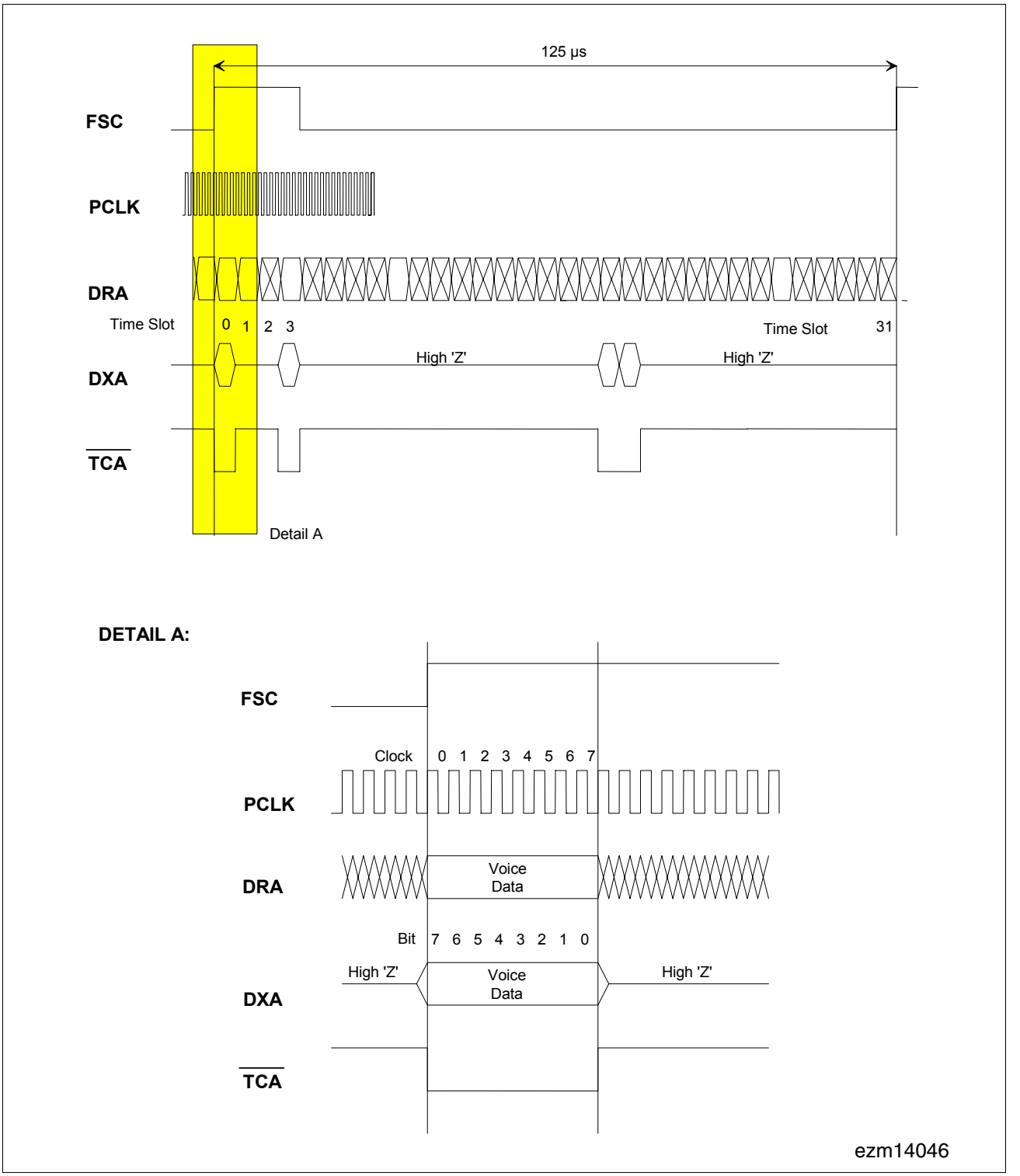


Figure 52 General PCM Interface Timing

The data rate of the interface can vary from 2*128 kbit/s to 2*8192 kbit/s (two highways). A frame may consist of up to 128 time slots of 8 bits each. The time slot and PCM highway assignment for each DuSLIC channel can be programmed. Receive and transmit time slots can also be programmed individually.

When DuSLIC is transmitting data on DXA (DXB), pin $\overline{\text{TCA}}$ ($\overline{\text{TCB}}$) is activated to control an external driving device.

The DRA/B and DXA/B pins may be connected to form a bidirectional data pin for special purposes, such as for the Serial Interface Port (SIP) with the Subscriber Line Data (SLD) bus. The SLD approach provides a common interface for analog or digital per-line components. For more details, please see the *ICs for Communications*[1] *User's Manual* available on request from Infineon Technologies.

Table 28 shows PCM Interface examples; other frequencies are also possible (such as 1536 kHz).

Table 28 *SLICOFI-2x* PCM Interface Configuration

Clock Rate PCLK [kHz]	**Single/Double Clock** [1/2]	**Time Slots** [per highway]	**Data Rate** [kbit/s per highway]
128	1	2	128
256	2	2	128
256	1	4	256
512	2	4	256
512	1	8	512
768	2	6	384
768	1	12	768
1024	2	8	512
1024	1	16	1024
2048	2	16	1024
2048	1	32	2048
4096	2	32	2048
4096	1	64	4096
8192	2	64	4096
8192	1	128	8192
f	1	f/64	f
f	2	f/128	f/2

Valid PCLK clock rates are: $f = n \times 64$ kHz ($2 \leq n \leq 128$)

1) Ordering No. B115-H6377-X-X-7600, published by Infineon Technologies.

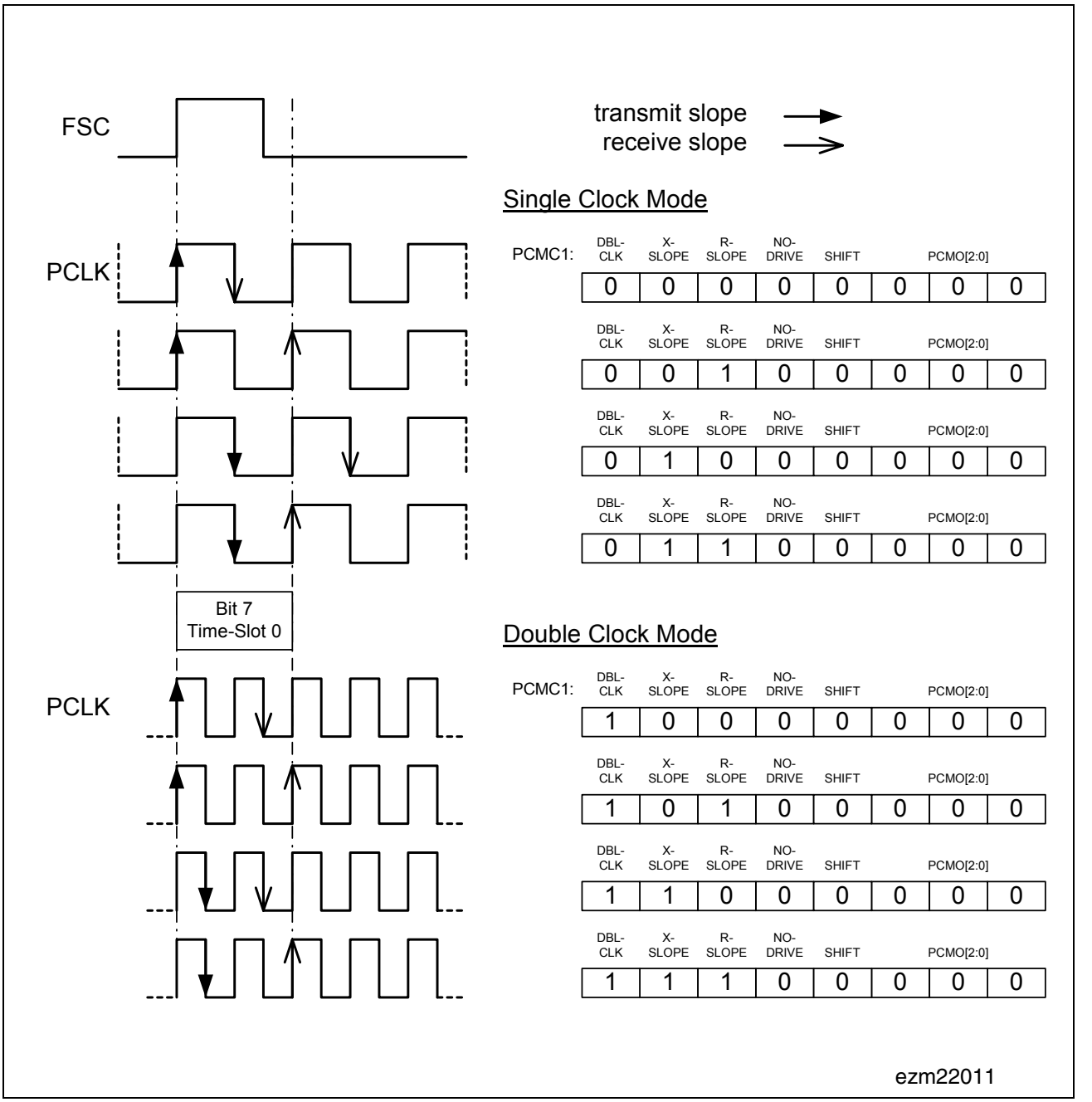


Figure 53 Setting the Slopes in Register PCMC1

4.1.2 Control of the Active PCM Channels

The *SLICOFI-2x* offers additional functionality on the PCM Interface including three-party conferencing and a 16 kHz sample rate. Five configuration bits and the PCM configuration registers control the activation of the PCM transmit channels. For details of the different functions see **Chapter 5.2**. **Table 29** gives an overview of the data transmission configuration of the PCM channels.

X1L is used only when linear data are transmitted. In this case, the time slot for X1 is defined by the number X1-TS from the PCMX1 register. The time slot for X1L is defined by the number X1-TS + 1.

Table 29 Active PCM Channel Configuration Bits

Control Bits					Transmit PCM Channel				
PCMX-EN	**CONF-EN**	**CONFX-EN**	**PCM16K**	**LIN**	**X1**	**X1L**	**X2**	**X3**	**X4**
0	0	0	–	–	–	–	–	–	–
1	0	0	0	0	PCM	–	–	–	–
1	0	0	0	1	HB	LB	–	–	–
0	1	0	–	–	–	–	PCM	PCM	–
1	1	0	0	0	PCM	–	PCM	PCM	–
1	1	0	0	1	HB	LB	PCM	PCM	–
0	0	1	–	–	–	–	PCM	PCM	PCM
1	0	1	0	0	PCM	–	PCM	PCM	PCM
1	0	1	0	1	HB	LB	PCM	PCM	PCM
0	1	1	–	–	–	–	PCM	PCM	PCM
1	1	1	0	0	PCM	–	PCM	PCM	PCM
1	1	1	0	1	HB	LB	PCM	PCM	PCM
1	–	–	1	0	DS1	–	–	DS2	–
1	–	–	1	1	HB1	–	LB1	HB2	LB2

Note: PCM means PCM-coded data (A-Law/μ-Law)
HB1 and HB2, and LB1 and LB2 indicate the high byte and low byte of linearly transmitted data for an 8 kHz (16 kHz) sample rate.

Note: Modes in rows with gray background are for testing purposes only.

4.1.3 Serial Microcontroller Interface

The microcontroller interface consists of four lines: $\overline{CS}$, DCLK, DIN and DOUT.

$\overline{CS}$: A synchronization signal starting a read or write access to *SLICOFI-2x*.

DCLK: A clock signal (up to 8.192 MHz) supplied to *SLICOFI-2x*.

DIN: Data input carries data from the master device to the *SLICOFI-2x*.

DOUT: Data output carries data from *SLICOFI-2x* to a master device.

There are two different command types. Reset commands have just one byte. Read/write commands have two command bytes with the address offset information located in the second byte.

A write command (see **Figure 54**) consists of two command bytes and the following data bytes. The first command byte determines whether the command is read or write, how the command field is to be used, and which DuSLIC channel (A or B) is written. The second command byte contains the address offset.

A read command (see **Figure 55**) consists of two command bytes written to DIN. After the second command byte is applied to DIN, a dump-byte consisting of 1s is written to DOUT. Data transfer starts with the first byte following the ‘dump-byte’.

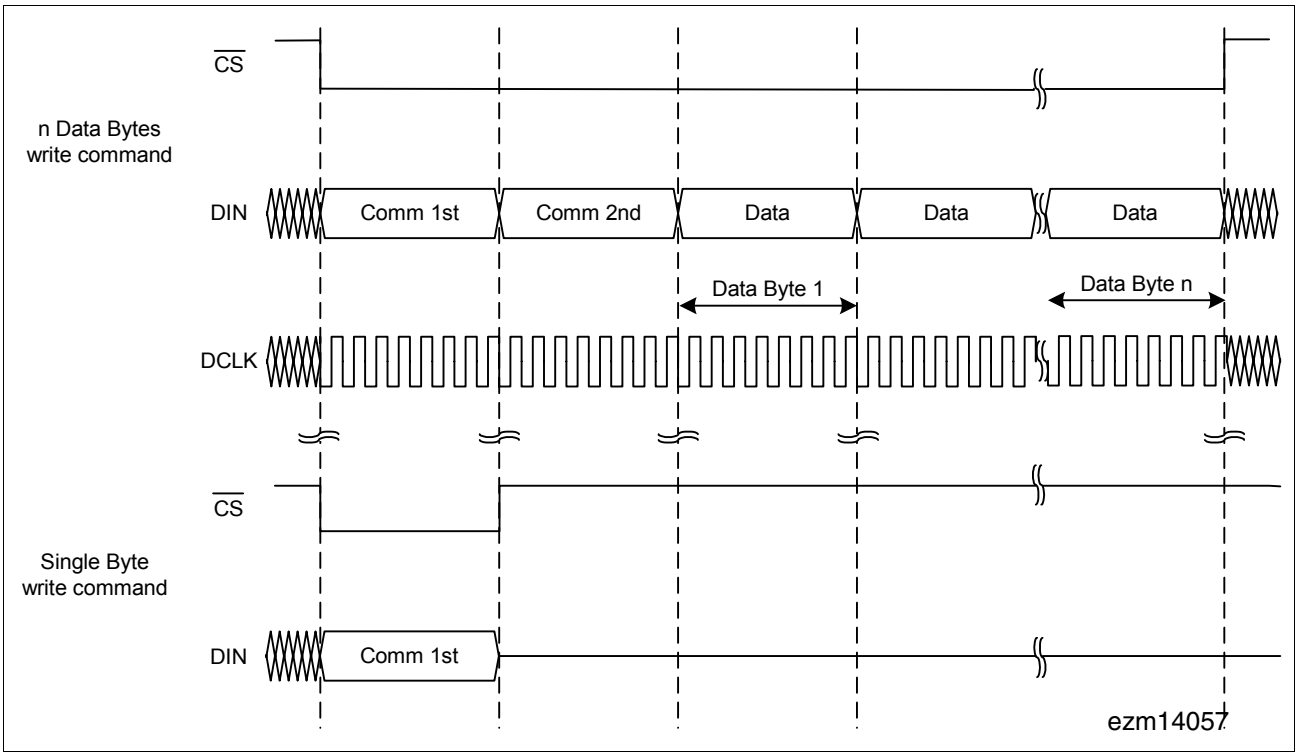


Figure 54 Serial Microcontroller Interface Write Access

*Note: Serial Microcontroller Interfaces Write Access shown in **Figure 54** is for n data bytes and single byte commands.*

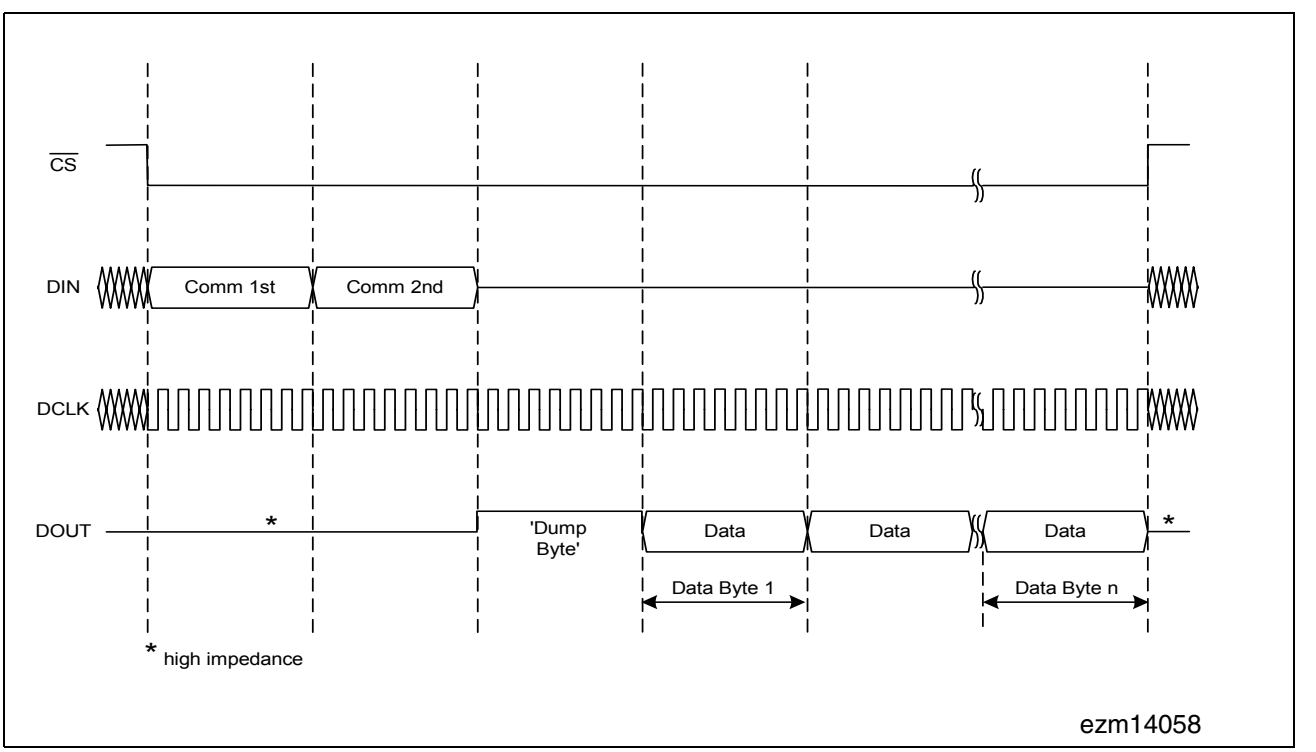


Figure 55 Serial Microcontroller Interface Read Access

Programming the Microcontroller Interface Without Clocks at FSC, MCLK, PCLK

The *SLICOFI-2x* can also be programmed via the µC Interface without any clocks connected to the FSC, MCLK, and PCLK pins. This can be useful in Power Down modes when additional power savings at the system level is necessary. In this case, a data clock of up to 1.024 MHz can be used on pin DCLK.

Because the *SLICOFI-2x* exits the basic reset routine only if clocks at the FSC, MCLK, and PCLK pins are applied, it is not possible to program the *SLICOFI-2x* without any clocks at these pins directly after the hardware reset or power on reset.

Note: It is necessary to first exit the basic reset routine with the clocks applied in oder to get the system running.

4.2 The IOM-2 Interface

IOM-2 defines an industry-standard serial bus for interconnecting telecommunication ICs for a broad range of applications – typically ISDN-based applications.

The IOM-2 bus provides a symmetrical full-duplex communication link containing data, control/programming and status channels. Providing data, control, and status information via a serial channel reduces the pin count and cost by simplifying the line card layout.

The IOM-2 Interface consists of two data lines and two clock lines as follows:

DU: Data Upstream carries data from the *SLICOFI-2x* to a master device.

DD: Data Downstream carries data from the master device to the *SLICOFI-2x*.

FSC: A Frame Synchronization Signal (8 kHz) supplied to *SLICOFI-2x*.

DCL: A Data Clock Signal (2048 kHz or 4096 kHz) supplied to *SLICOFI-2x*.

SLICOFI-2x handles data as described in the IOM-2 specification for analog devices. This specification is available on request from Infineon Technologies.

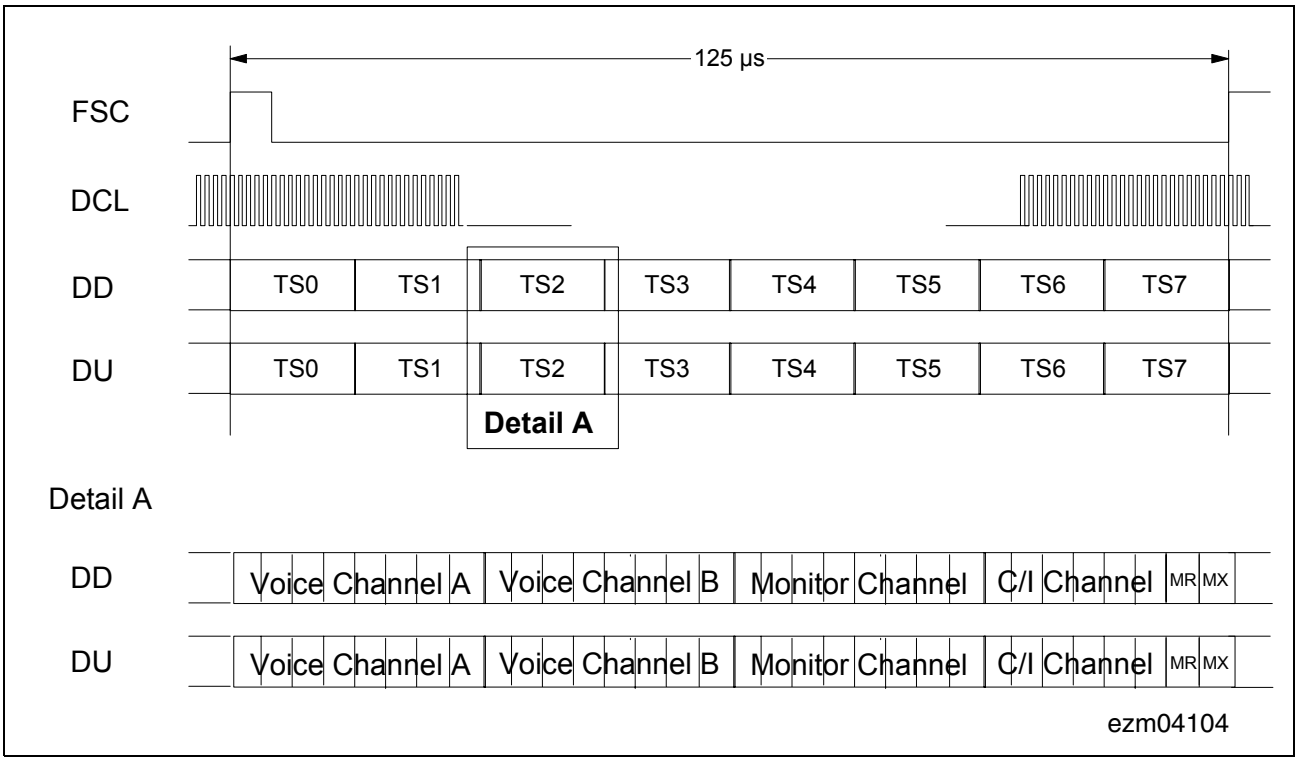


Figure 56 IOM-2 I/F Timing for up to 16 Voice Channels (Per 8 kHz Frame)

The information is multiplexed into frames that are transmitted at an 8 kHz rate. The frames are subdivided into eight sub-frames (see **Figure 56**), with one sub-frame dedicated to each transceiver or pair of codecs (in this case, each sub-frame is dedicated to two *SLICOFI-2x* channels). The sub-frames provide channels for data, programming, and status information for a single transceiver or codec pair.

Figure 57 and **Figure 58** show IOM-2 Interface timings for the two possible Data Clock (DCL) signal frequencies:

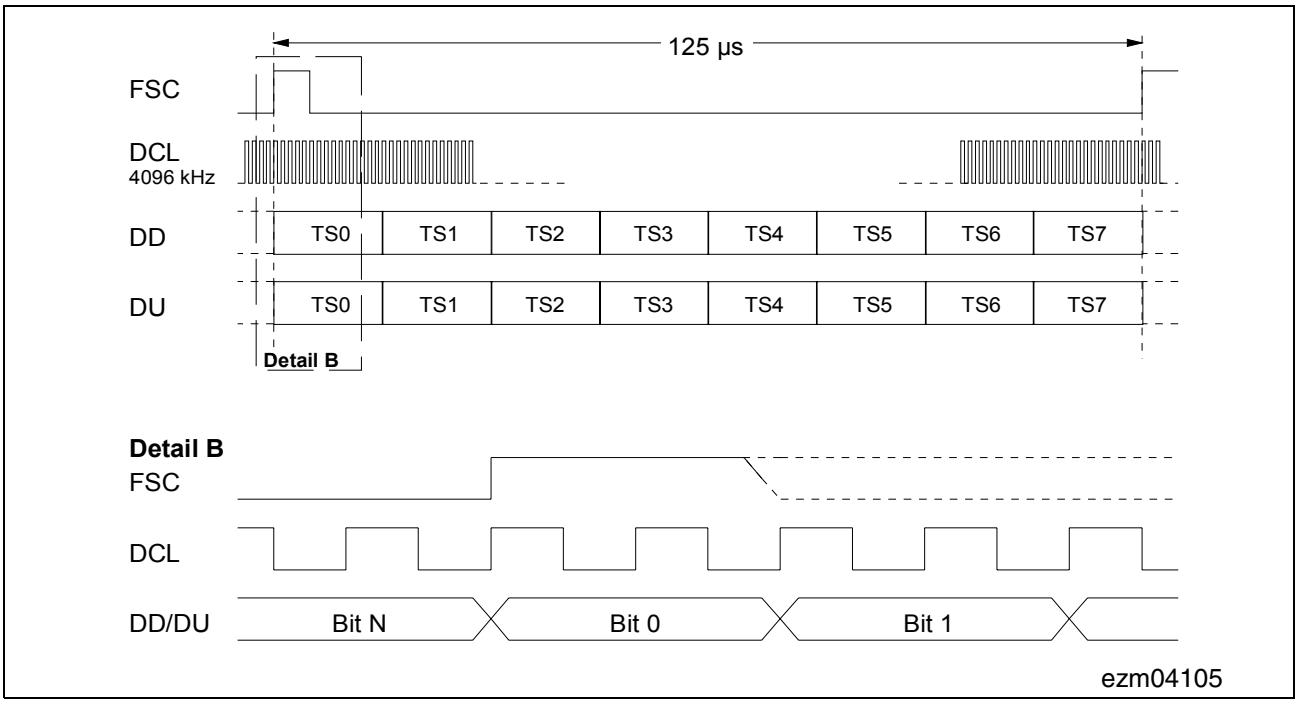


Figure 57 IOM-2 Interface Timing (DCL = 4096 kHz, Per 8 kHz Frame)

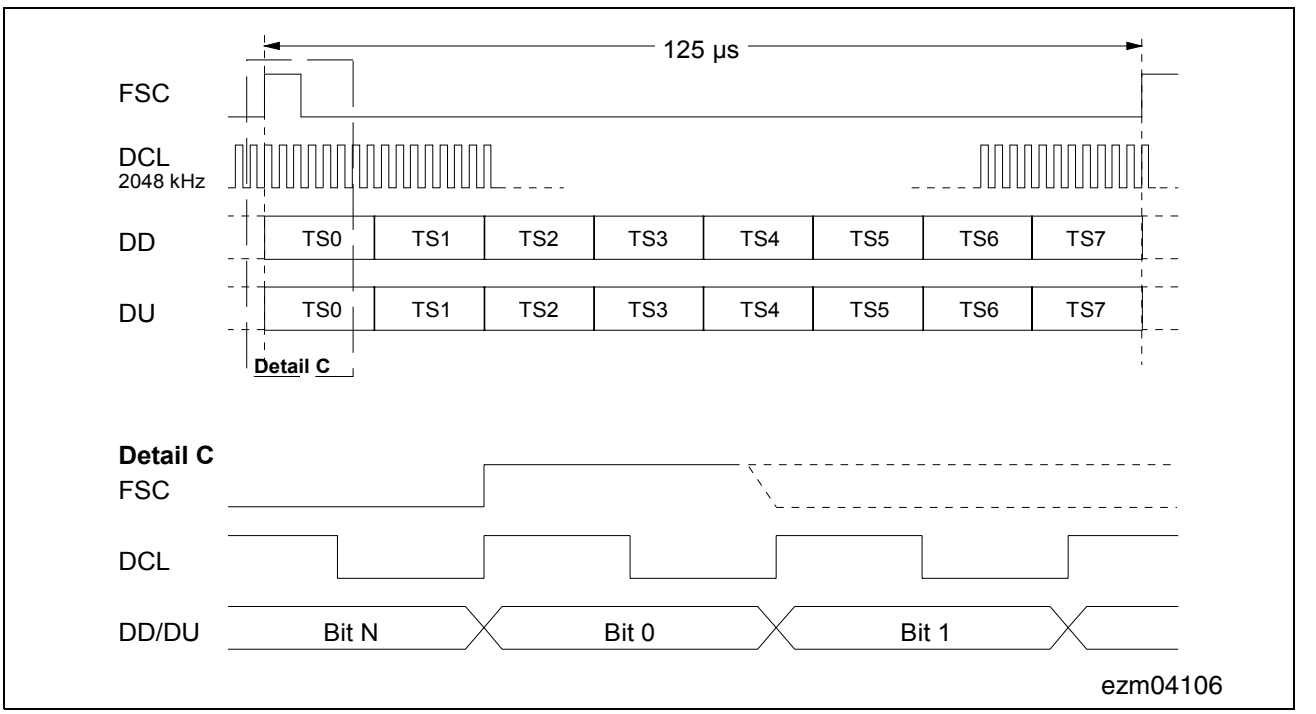


Figure 58 IOM-2 Interface Timing (DCL = 2048 kHz, Per 8 kHz Frame)

Both DuSLIC channels (see **Figure 56**) can be assigned to one of the eight time slots. Set the IOM-2 time slot selection as shown in **Table 30** by pin-strapping. In this way, up to 16 channels can be handled with one IOM-2 Interface on the linecard.

Table 30 IOM-2 Time Slot Assignment

TS2	TS1	TS0	IOM-2 Operating Mode
0	0	0	Time slot 0; DCL = 2048, 4096 kHz
0	0	1	Time slot 1; DCL = 2048, 4096 kHz
0	1	0	Time slot 2; DCL = 2048, 4096 kHz
0	1	1	Time slot 3; DCL = 2048, 4096 kHz
1	0	0	Time slot 4; DCL = 2048, 4096 kHz
1	0	1	Time slot 5; DCL = 2048, 4096 kHz
1	1	0	Time slot 6; DCL = 2048, 4096 kHz
1	1	1	Time slot 7; DCL = 2048, 4096 kHz

2 MHz or 4 MHz DCL is selected by the SEL24 pin:

SEL24 = 0: DCL = 2048 kHz

SEL24 = 1: DCL = 4096 kHz

4.2.1 IOM-2 Interface Monitor Transfer Protocol

Monitor Channel Operation

The monitor channel is used for the transfer of maintenance information between two functional blocks. Using two monitor control bits (MR and MX) per direction, the data is transferred in a complete handshake procedure. The MR and MX bits in the fourth byte (C/I channel) of the IOM-2 frame are used for the handshake procedure of the monitor channel.

The monitor channel transmission operates on a pseudo-asynchronous basis:

Data transfer (in bits) on the bus is synchronized to Frame Sync FSC.

Data flow (in bytes) is asynchronously controlled by the handshake procedure.

For example: Data is placed onto the DD-Monitor-Channel by the monitor transmitter of the master device (bit DD-MX is activated: set to 0). This data transfer will be repeated within each frame (125 µs rate) until it is acknowledged by the *SLICOFI-2x* monitor receiver by setting the bit DU-MR to 0, which is checked by the monitor transmitter of the master device. The data rate on IOM-2 monitor channels is 4 kbits/s.

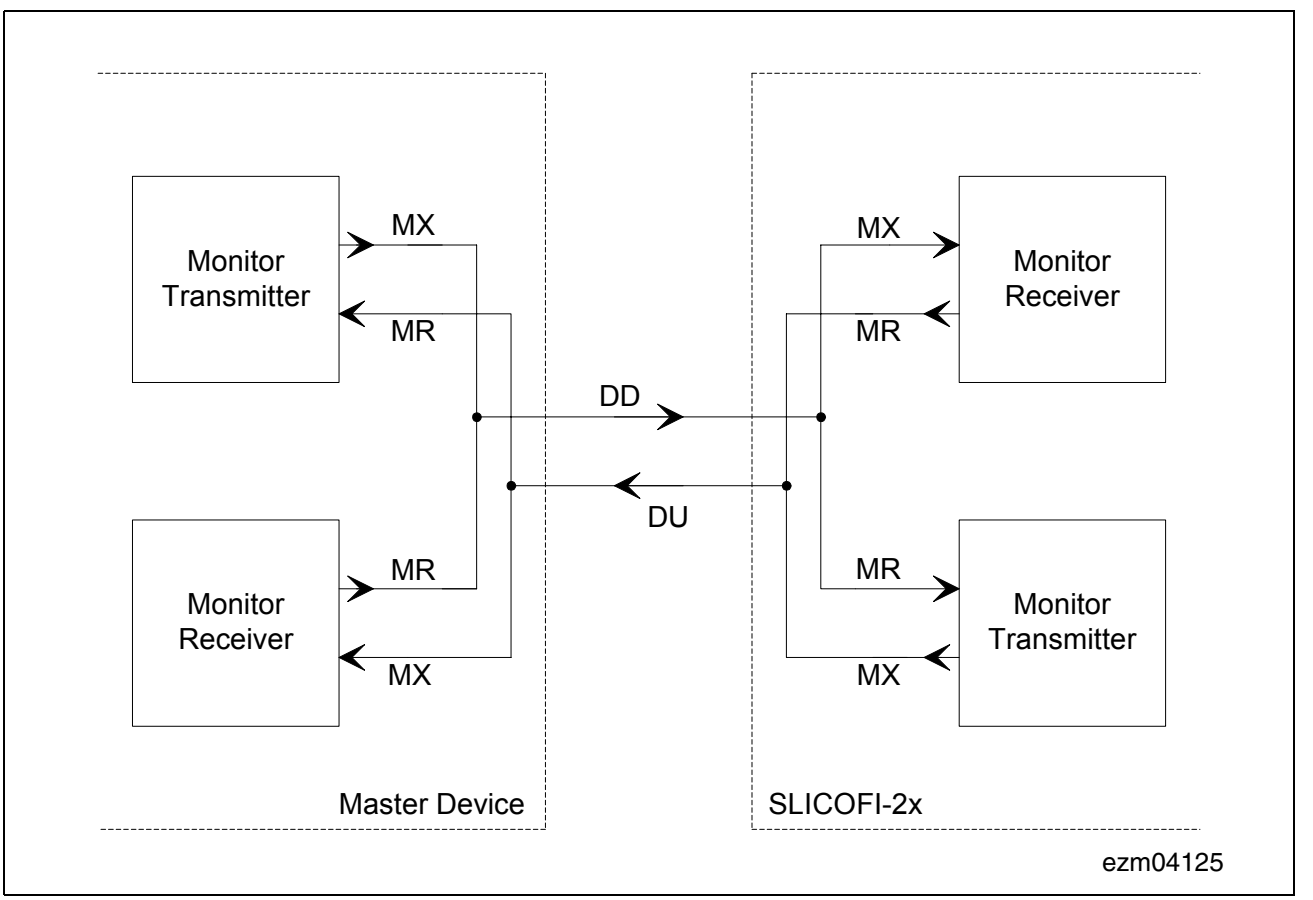


Figure 59 IOM-2 Interface Monitor Transfer Protocol

Monitor Handshake Procedure

The monitor channel works in three states

Idle state:	A pair of inactive (set to 1) MR and MX bits during two or more consecutive frames: End of Message (EOM)
Sending state:	MX bit is activated (set to 0) by the monitor transmitter, together with data bytes (can be changed) on the monitor channel
Acknowledging:	MR bit is set to active (set to 0) by the monitor receiver, together with a data byte remaining in the monitor channel.

A start of a transmission is initiated by a monitor transmitter in sending out an active MX bit together with the first byte of data (the address of the receiver) to be transmitted in the monitor channel.

The monitor channel remains in this state until the addressed monitor receiver acknowledges the received data by sending out an active MR bit, which means that the data transmission is repeated each 125 µs frame (minimum is one repetition). At this time, the monitor transmitter evaluates the MR bit.

Flow control can only take place when the transmitter's MX and the receiver's MR bit are in active state.

Because the receiver is capable of receiving the monitor data at least twice (in two consecutive frames), it is able to check for data errors. If two different bytes are received, the receiver will wait for the receipt of two identical successive bytes (last look function).

A collision resolution mechanism (checks if another device is trying to send data at the same time) is implemented in the transmitter. This is done by looking for the inactive (1) phase of the MX bit and making a per-bit collision check on the transmitted monitor data (check if there are transmitted 1s on DU/DD line; DU/DD line are open-drain lines).

Any abort leads to a reset of the *SLICOFI-2x* command stack, the device is ready to receive new commands.

To maximize speed during data transfers, the transmitter anticipates the falling edge of the receiver's acknowledgment.

Due to the programming structure, duplex operation is not possible. Sending any data to the *SLICOFI-2x* while transmission is active is not allowed.

Data transfer to the *SLICOFI-2x* starts with a *SLICOFI-2x*-specific address byte (81_H).

Attention: Each byte on the monitor channel must be sent at least twice according to the IOM-2 Monitor handshake procedure.

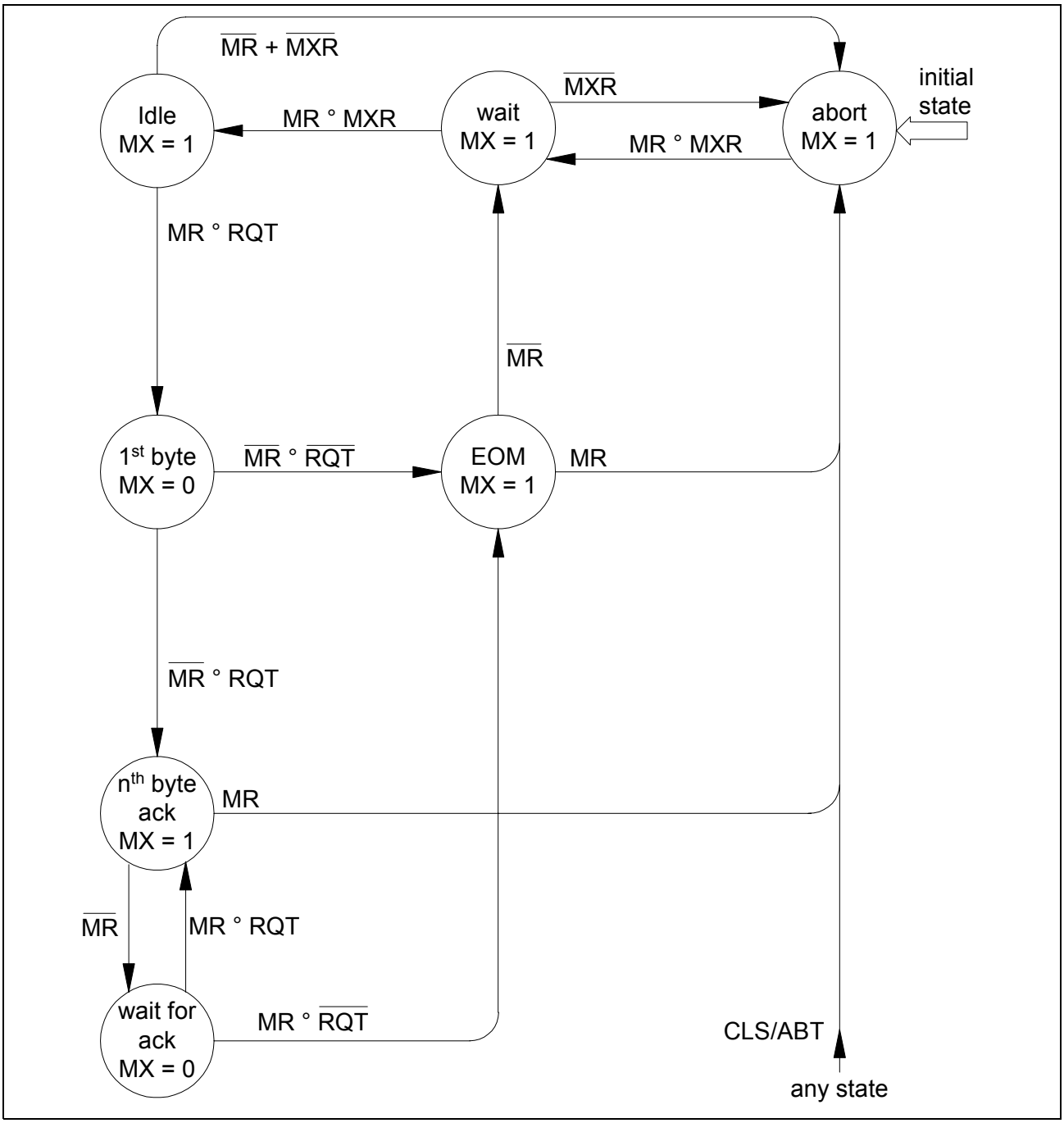


Figure 60 State Diagram of the *SLICOFI-2x* Monitor Transmitter

MR … MR bit received on DD line

MX … MX bit calculated and expected on DU line

MXR … MX bit sampled on DU line

CLS … Collision within the monitor data byte on DU line

RQT … Request for transmission form internal source

ABT … Abort request/indication

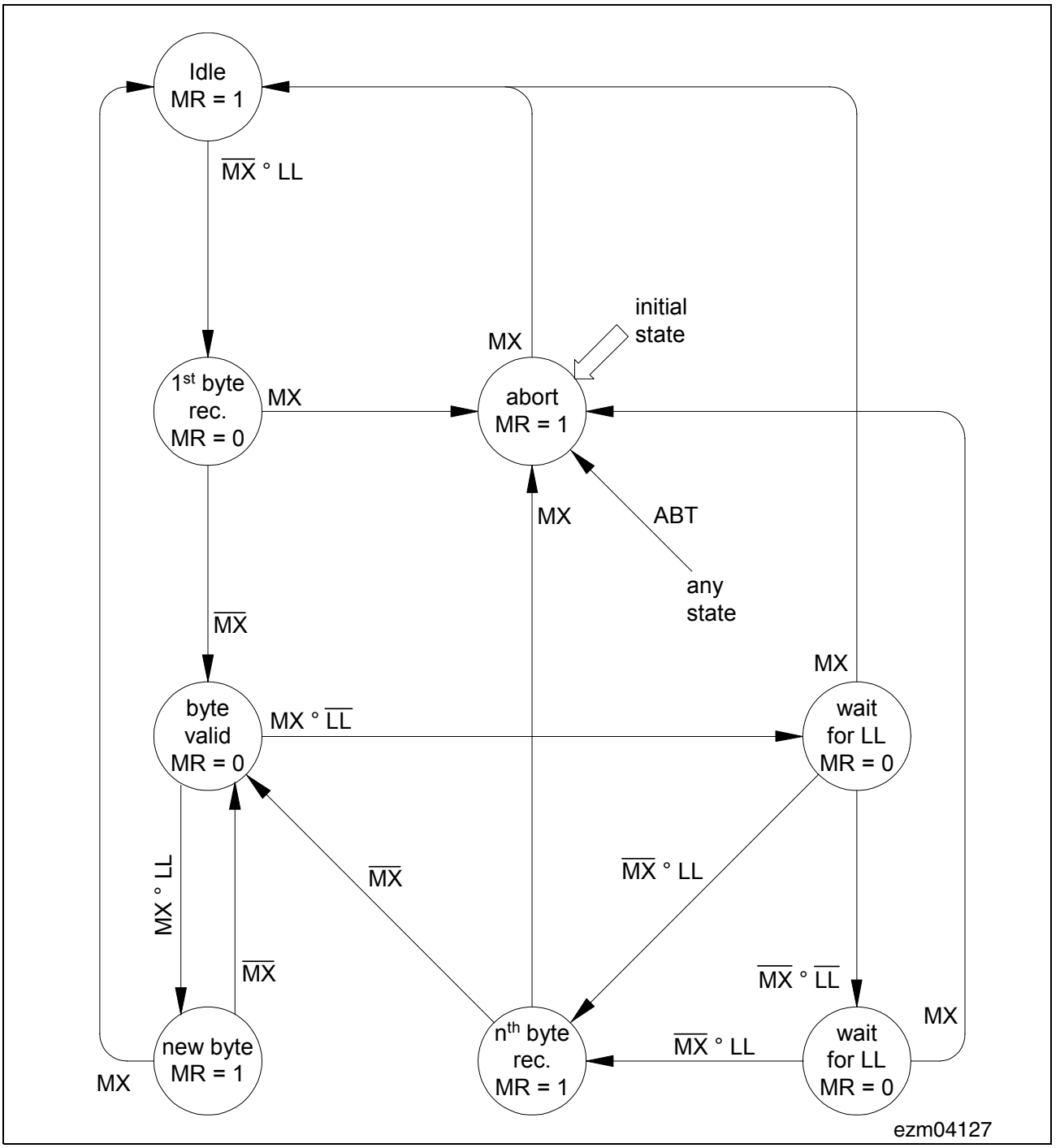


Figure 61 State Diagram of the *SLICOFI-2x* Monitor Receiver

MR … MR bit calculated and transmitted on DU line

MX … MX bit received data downstream (DD line)

LL … Last look of monitor byte received on DD line

ABT … Abort indication to internal source

Address Byte

Messages to and from the *SLICOFI-2x* start with the following byte:

Bit	7	6	5	4	3	2	1	0
	1	0	0	0	0	0	0	1

4.2.2 *SLICOFI-2x* Identification Command

For the IOM-2 Interface only, a two-byte identification command is defined for analog line IOM-2 devices to unambiguously identify different devices by software. A device requesting the identification of the *SLICOFI-2x* will send the following two byte code:

1	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

Each device will then respond with its specific identification code. For the *SLICOFI-2x*, this two byte identification code is:

1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	1

4.2.3 Operation with IOM-2 TE Devices (1.536 MHz)

The DuSLIC can be operated either in PCM/µC mode or IOM-2 mode. In case of IOM-2 mode the DuSLIC supports the standard IOM-2 data clock rates of 4.096 MHz (double clock) or 2.048 MHz (single clock).

Some applications however require the IOM-2 TE mode which uses a clock rate of 1.536 MHz and a data rate of 768 kBit/s, respectively.

As the IOM-2 mode of the DuSLIC doesn´t support a clock rate of 1.536 MHz, the PCM/µC mode is used: It is possible to operate the DuSLIC in PCM/µC mode at 1.536 MHz and to connect its PCM interface directly to the IOM-2 interface of the host device as shown in **Figure 62**.

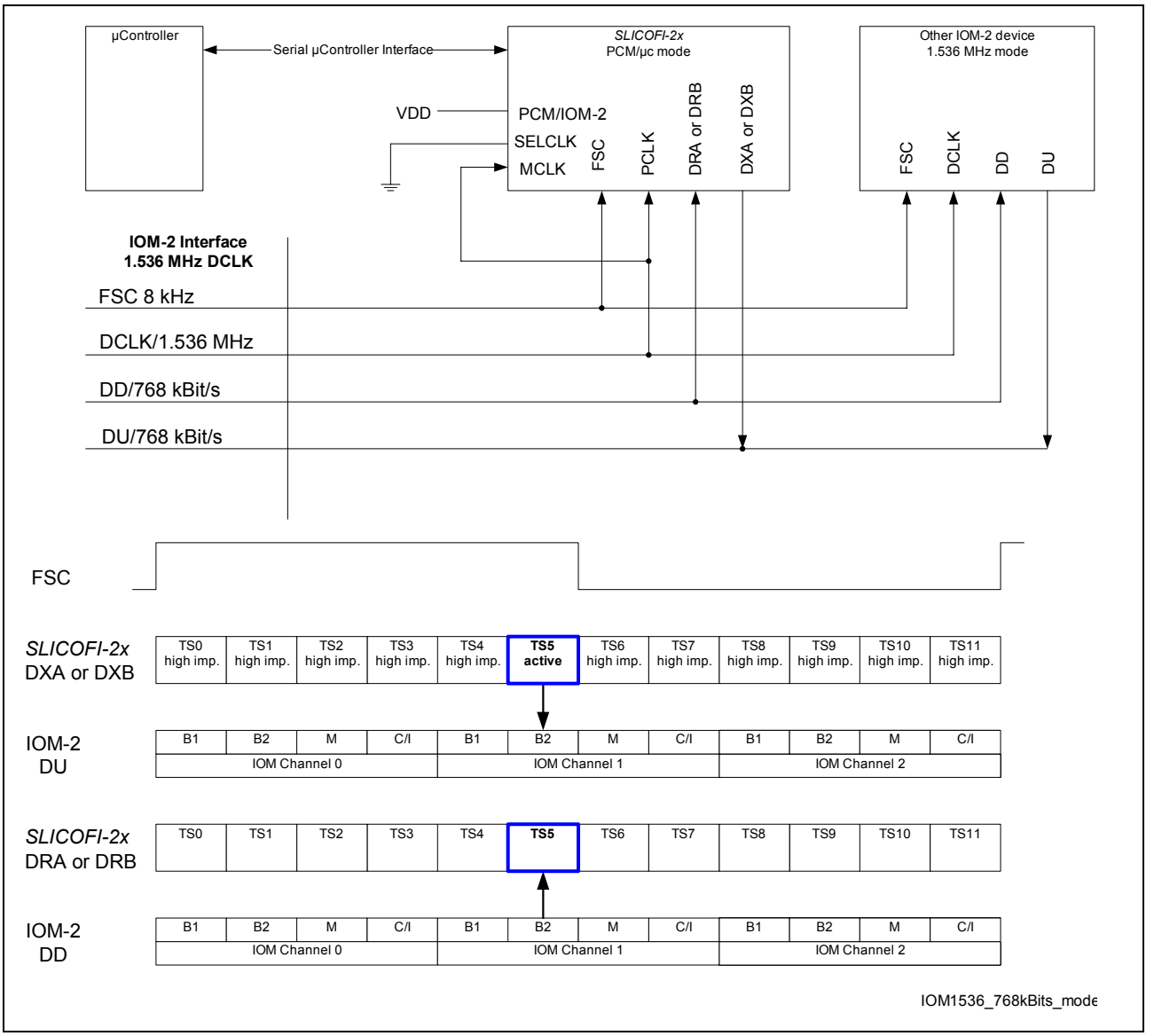


Figure 62 PCM/mC Mode used for IOM-2 TE Interface at 1.536 MHz

As shown in **Figure 62** the *SLICOFI-2x* is operated in PCM/µC mode. The controlling is done via the serial µC interface by a microcontroller, whereas the voice data is mapped from the PCM output of the *SLICOFI-2x* to the IOM-2 interface and vice versa. Special care has to be taken about the time slot counting: in the example shown in **Figure 62**, the PCM timeslot TS5 corresponds to the B2 channel of IOM channel 1.

The *SLICOFI-2x* has to be programmed for PCM double clock rate (bit DBL-CLK in register PCM1). The PCM time slot (receive and transmit) can be programmed with register PCMR1 and PCMX1.

As the DXA/B output of the *SLICOFI-2x* is only active in the selected time slot and is high impedance in other time slots, the PCM output of the *SLICOFI-2x* can be directly connected to the IOM-2 bus without any additional hardware (provided that the driving capability of the *SLICOFI-2x* is strong enough for the connected IOM-2 bus).

It has also to be considered that the *SLICOFI-2x* offers 3.3 V logic levels for the PCM voice data. If the driving capability or the 3.3 V level of the *SLICOFI-2x* are not sufficient, an external driver/levelshifter has to be used. The *SLICOFI-2x* offers appropriate signals for controlling an external bus driver.

4.3 TIP/RING Interface

The TIP/RING Interface is the interface that connects the subscriber to the DuSLIC. It meets ITU-T Recommendation Q.552 for Z Interface and applicable LSSGR.

For the performance of the TIP/RING Interface, see **Chapter 6.1** and **Chapter 6.2**; for application circuits, see **Chapter 7**.

5 *SLICOFI-2x* Command Structure and Programming

With the commands described in this chapter, the *SLICOFI-2x* can be programmed, configured, and tested very flexibly via the microcontroller interface or via the IOM-2 interface monitor channel. The command structure uses one-byte and two-byte commands to ensure a highly flexible and quick programming procedure for the most common commands.

Structure of the First Command Byte

The first command byte includes the R/W bit, the addresses of the different channels, and the command type.

Bit	7	6	5	4	3	2	1	0
	RD	**OP**	**ADR[2:0]**			**CMD[2:0]**		

RD Read Data

RD = 0 Write data to chip.

RD = 1 Read data from chip.

OP Selects the usage of the CMD field

OP = 0 The CMD field works as a Command/Indication Operation (CIOP) command and acts like the M[2:0] bits located in the CIDD byte of the IOM Interface. See **Table 31**.

Bit	7	6	5	4	3	2	1	0
	0	**0**	**ADR[2:0]**			**M2**	**M1**	**M0**

OP = 1 The CMD field acts as the SOP, COP, or POP command described below (microcontroller interface mode only).

Table 31 M2, M1, M0: General Operating Mode

Command/Indication Operation (CIOP)			*SLICOFI-2x* Operating Mode (for details see "Overview of all DuSLIC Operating Modes" on Page 74)
M2	M1	M0	
1	1	1	Sleep, Power Down (PDRx)
0	0	0	Power Down High Impedance (PDH)
0	1	0	Any Active mode
1	0	1	Ringing (ACTR Burst On)
1	1	0	Active with Metering
1	0	0	Ground Start
0	0	1	Ring Pause

ADR[2:0] Channel address for the subsequent data

ADR[2:0] = 0 0 0 Channel A

ADR[2:0] = 0 0 1 Channel B

(other codes reserved for future use)

CMD[2:0] Command for programming the *SLICOFI-2x* (OP = 1) or command equivalent to the CIDD channel bits M[2:0] in microcontroller interface mode (OP = 0)
The first four commands have no second command byte following.
All necessary information is present in the first command byte.

CMD[2:0] = 0 0 0 Soft reset of the chip (reset routine for all channels will reset all configuration registers, CRAM data is not affected).

CMD[2:0] = 0 0 1 Soft reset for the specified channel A or B in ADR field

CMD[2:0] = 0 1 0 Resychronization of the PCM interface (only available when pin PCM/$\overline{\text{IOM-2}}$ = 1)

CMD[2:0] = 0 1 1 Reserved for future use

The second four commands are followed by a second command byte that defines additional information, such as specifying sub-addresses of the CRAM.

CMD[2:0] = 1 0 0 SOP command (Status Operation; programming, and monitoring of all status-relevant data).

CMD[2:0] = 1 0 1 COP command (Coefficient Operation; programming, and monitoring of all coefficients in the CRAM).

CMD[2:0] = 1 1 0 POP command (Signal Processing Operation Programming).

CMD[2:0] = 1 1 1 Reserved for production tests

Structure of the Second Command Byte

The second command byte specifies a particular SOP, COP, or POP command, depending on the CMD[2:0] bits of the first command byte. In the following sections, the contents of this register are described for each command group.

The second command byte specifies the initial offset for the subsequent data bytes. After each data byte is transferred, the internal offset is incremented automatically. Therefore, it is possible to send a varied number of data bytes with one SOP, COP, or POP command. Writing over read-only registers will not destroy their contents.

Register Description Example

At the beginning of each register description, a single line gives information about:

- Offset: Offset of register address (hex)
- Name: Short name of the register
- Detailed Name: Detailed name of the register
- Reset Value: Value of the register after reset (hex)
  "hw" – value depends on specific hardware fuses
- Test Status: "T" – the register has no effect unless the TEST-EN bit in register LMCR1 is set to 1
- Channel Selection: "N" – the register affects both *SLICOFI-2x* channels, "Y" – the register affects a specific *SLICOFI-2x* channel

The line is organized as follows (with example):

Offset	Name	Detailed Name	Reset Value	Test	Per Channel
27_H	TSTR1	Test Register 1	00_H	T	Y

5.1 Overview of Commands

SOP STATUS OPERATION

Bit	7	6	5	4	3	2	1	0
Byte 1	RD	1	ADR[2:0]			1	0	0
Byte 2	OFFSET[7:0]							

COP COEFFICIENT OPERATION

Bit	7	6	5	4	3	2	1	0
Byte 1	RD	1	ADR[2:0]			1	0	1
Byte 2	OFFSET[7:0]							

POP POP OPERATION (only SLICOFI-2 PEB 3265 used for DuSLIC-E/-E2/-P)

Bit	7	6	5	4	3	2	1	0
Byte 1	RD	1	ADR[2:0]			1	1	0
Byte 2	OFFSET[7:0]							

5.2 SLICOFI-2 Command Structure and Programming

This section describes only the SLICOFI-2 PEB 3265 command structure and programming.

5.2.1 SOP Command

The Status Operation (SOP) command provides access to the configuration and status registers of the SLICOFI-2. Common registers change the mode of the entire SLICOFI-2 chip. All other registers are channel-specific. It is possible to access single or multiple registers. Multiple register access is achieved by an automatic offset increment. Write access to read-only registers is ignored and does not abort the command sequence. Offsets may change in future versions of the SLICOFI-2.

Attention: To ensure proper functionality, it is essential that all unused register bits have to be filled with zeros.

5.2.1.1 SOP Register Overview

00_H REVISION — Revision Number (read-only)

REV[7:0]

01_H CHIPID 1 — Chip Identification 1 (read-only)

for internal use only

02_H CHIPID 2 — Chip Identification 2 (read-only)

for internal use only

03_H CHIPID 3 — Chip Identification 3 (read-only)

for internal use only

04_H FUSE1 — Fuse Register 1

for internal use only

05_H PCMC1 — PCM Configuration Register 1

DBL-CLK	X-SLOPE	R-SLOPE	NO-DRIVE-0	SHIFT	PCMO[2:0]

06_H XCR Extended Configuration Register

EDSP-EN	ASYNCH-R	0	0	0	0

07_H INTREG1 Interrupt Register 1 (read-only)

INT-CH	HOOK	GNDK	GNKP	ICON	VTRLIM	OTEMP	SYNC-FAIL

08_H INTREG2 Interrupt Register 2 (read-only)

LM-THRES	READY	RSTAT	LM-OK	IO[4:1]-DU

09_H INTREG3 Interrupt Register 3 (read-only)

DTMF-OK	DTMF-KEY[4:0]	UTDR-OK	UTDX-OK

$0A_H$ INTREG4 Interrupt Register 4 (read-only)

EDSP-FAIL	0	0	0	CIS-BOF	CIS-BUF	CIS-REQ	CIS-ACT

$0B_H$ CHKR1 Checksum Register 1 (High Byte) (read-only)

SUM-OK	CHKSUM-H[6:0]

$0C_H$ CHKR2 Checksum Register 2 (Low Byte) (read-only)

CHKSUM-L[7:0]

$0D_H$ LMRES1 Level Metering Result 1 (High Byte) (read-only)

LM-VAL-H[7:0]

$0E_H$ LMRES2 Level Metering Result 2 (Low Byte) (read-only)

LM-VAL-L[7:0]

$0F_H$ FUSE2 Fuse Register 2

for internal use only

10_H FUSE3 Fuse Register 3

for internal use only

11_H MASK Mask Register

READY-M	HOOK-M	GNDK-M	GNKP-M	ICON-M	VTRLIM-M	OTEMP-M	SYNC-M

12_H IOCTL1 I/O Control Register 1

IO[4:1]-INEN	IO[4:1]-M

13_H IOCTL2 I/O Control Register 2

IO[4:1]-OEN	IO[4:1]-DD

14_H IOCTL3 I/O Control Register 3

DUP[3:0]	DUP-IO[3:0]

15_H BCR1 Basic Configuration Register 1

HIR	HIT	SLEEP-EN	REVPOL	ACTR	ACTL	SEL-SLIC[1:0]

16_H BCR2 Basic Configuration Register 2

REXT-EN	SOFT-DIS	TTX-DIS	TTX-12K	HIM-AN	AC-XGAIN	UTDX-SRC	PDOT-DIS

17_H BCR3 Basic Configuration Register 3

MU-LAW	LIN	PCM16K	PCMX-EN	CONFX-EN	CONF-EN	LPRX-CR	CRAM-EN

18_H BCR4 Basic Configuration Register 4

TH-DIS	IM-DIS	AX-DIS	AR-DIS	FRX-DIS	FRR-DIS	HPX-DIS	HPR-DIS

19_H BCR5 Basic Configuration Register 5

-EN	UTDX-EN	CIS-AUTO	CIS-EN	LEC-OUT	LEC-EN	DTMF-SRC	DTMF-EN

$1A_H$ DSCR DTMF Sender Configuration Register

DG-KEY[3:0]	COR8	PTG	TG2-EN	TG1-EN

$1B_H$ Reserved

0	0	0	0	0	0	0	0

$1C_H$ LMCR1 Level Metering Configuration Register 1

TEST-EN	LM-EN	LM-THM	PCM2DC	LM2 PCM	LM-ONCE	LM-MASK	DC-AD16

$1D_H$ LMCR2 Level Metering Configuration Register 2

LM-NOTCH	LM-FILT	LM-RECT	RAMP-EN	LM-SEL[3:0]

$1E_H$ LMCR3 Level Metering Configuration Register 3

AC-SHORT-EN	RTR-SEL	LM-ITIME[3:0]	RNG-OFFSET[1:0]

$1F_H$ OFR1 Offset Register 1 (High Byte)

OFFSET-H[7:0]

20_H OFR2 Offset Register 2 (Low Byte)

OFFSET-L[7:0]

21_H PCMR1 PCM Receive Register 1

R1-HW	R1-TS[6:0]

22_H PCMR2 PCM Receive Register 2

R2-HW	R2-TS[6:0]

23_H PCMR3 PCM Receive Register 3

R3-HW	R3-TS[6:0]

24_H PCMR4 PCM Receive Register 4

R4-HW	R4-TS[6:0]

25_H PCMX1 PCM Transmit Register 1

X1-HW	X1-TS[6:0]

26_H PCMX2 PCM Transmit Register 2

X2-HW	X2-TS[6:0]

27_H PCMX3 PCM Transmit Register 3

X3-HW	X3-TS[6:0]

28_H PCMX4 PCM Transmit Register 4

X4-HW	X4-TS[6:0]

29_H TSTR1 Test Register 1

PD-AC-PR	PD-AC-PO	PD-AC-AD	PD-AC-DA	PD-AC-GN	PD-GNKC	PD-OFHC	PD-OVTC

$2A_H$ TSTR2 Test Register 2

PD-DC-PR	0	PD-DC-AD	PD-DC-DA	PD-DCBUF	0	PD-TTX-A	PD-HVI

$2B_H$ TSTR3 Test Register 3

0	0	AC-DLB-4M	AC-DLB-128K	AC-DLB-32K	AC-DLB-8K	0	0

$2C_H$ TSTR4 Test Register 4

OPIM-AN	OPIM-4M	COR-64	COX-16	0	0	0	0

$2D_H$ TSTR5 Test Register 5

0	0	0	DC-POFI-HI	DC-HOLD	0	0	0

5.2.1.2 SOP Register Description

00_H	**REVISION**	Revision Number (read-only)	**curr. rev.**		**N**

Bit	7	6	5	4	3	2	1	0
	REV[7:0]							

REV[7:0] Current revision number of the SLICOFI-2.

01_H	**CHIPID 1**	Chip Identification 1 (read-only)	**hw**		**N**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

02_H	**CHIPID 2**	Chip Identification 2 (read-only)	**hw**		**N**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

03_H	**CHIPID 3**	Chip Identification 3 (read-only)	**hw**		**N**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

04_H	**FUSE1**	**Fuse Register 1**	**hw**		**N**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

05_H	PCMC1	PCM Configuration Register 1	00_H		N

Bit	7	6	5	4	3	2	1	0
	DBL-CLK	X-SLOPE	R-SLOPE	NO-DRIVE-0	SHIFT	PCMO[2:0]		

DBL-CLK Clock mode for the PCM interface (see **Figure 53** on **Page 125**)

DBL-CLK = 0 Single-clocking is used.

DBL-CLK = 1 Double-clocking is used.

X-SLOPE Transmit slope (see **Figure 53** on **Page 125**)

X-SLOPE = 0 Transmission starts with rising edge of the clock.

X-SLOPE = 1 Transmission starts with falling edge of the clock.

R-SLOPE Receive slope (see **Figure 53** on **Page 125**)

R-SLOPE = 0 Data is sampled with falling edge of the clock.

R-SLOPE = 1 Data is sampled with rising edge of the clock.

NO-DRIVE-0 Driving mode for bit 0 (only available in single-clocking mode).

NO-DRIVE = 0 Bit 0 is driven the entire clock period.

NO-DRIVE = 1 Bit 0 is driven during the first half of the clock period only.

SHIFT Shifts the access edges by one clock cycle in double-clocking mode.

SHIFT = 0 No shift takes place.

SHIFT = 1 Shift takes place.

PCMO[2:0] All PCM timing is moved by PCMO data periods against the FSC signal.

PCMO[2:0] = 0 0 0 No offset is added.

PCMO[2:0] = 0 0 1 One data period is added.

…

PCMO[2:0] = 1 1 1 Seven data periods are added.

06_H	XCR	Extended Configuration Register	00_H		N

Bit	7	6	5	4	3	2	1	0
	EDSP-EN	**ASYNCH-R**	**0**	**0**	**0**	**0**		

EDSP-EN Enables the Enhanced Digital Signal Processor EDSP.

EDSP-EN = 0 Enhanced Digital Signal Processor is switched off.

EDSP-EN = 1 Enhanced Digital Signal Processor is switched on.

ASYNCH-R Enables asynchronous ringing in case of internal or external ringing.

ASYNCH-R = 0 Internal or external ringing with zero crossing selected.

ASYNCH-R = 1 Asynchronous ringing selected.

Note: When internal ringing is used, the ringing signal can be turned off without waiting for zero crossing.

07_H	INTREG1	Interrupt Register 1 (read-only)	80_H		Y

Bit	7	6	5	4	3	2	1	0
	INT-CH	HOOK	GNDK	GNKP	ICON	VTRLIM	OTEMP	SYNC-FAIL

INT-CH Interrupt channel bit. This bit indicates that the corresponding channel caused the last interrupt. Will be automatically set to zero after all interrupt registers were read.

INT-CH = 0 No interrupt in corresponding channel.

INT-CH = 1 Interrupt caused by corresponding channel.

HOOK Indicates on-hook or off-hook for the loop in all operating modes (via the ITx pin); filtered by the DUP (Data Upstream Persistence) counter and interrupt generation masked by the HOOK-M bit. Indicates ground start in case of ground start mode is selected. A change of this bit generates an interrupt.

HOOK = 0 On-hook.

HOOK = 1 Off-hook detected.

GNDK Indicates ground key information in all active modes via the IL pin; filtered for AC suppression by the DUP counter and interrupt generation masked by the GNDK-M bit. A change of this bit generates an interrupt.

GNDK = 0 No ground key indicated.

GNDK = 1 Ground key indication; longitudinal current (threshold 17 mA) detected.

GNKP Ground key polarity. Indicating the active Ground Key level (positive/negative) interrupt generation masked by the GNKP-M bit. A change of this bit generates an interrupt. This bit can be used to obtain information about interference voltage influence.

GNKP = 0 Negative ground key threshold level active.

GNKP = 1 Positive ground key threshold level active.

ICON Constant current information. Filtered by DUP-IO counter and interrupt generation masked by the ICON-M bit. A change of this bit generates an interrupt.

ICON = 0 Resistive or constant voltage feeding.

ICON = 1 Constant current feeding.

VTRLIM Exceeding of a programmed voltage threshold for the TIP/RING voltage, filtered by the DUP-IO counter and interrupt generation masked by the VTRLIM-M bit. A change of this bit causes an interrupt.

The voltage threshold for the TIP/RING voltage is set in CRAM (calculated with DuSLICOS DC Control Parameter 2/4: Tip-Ring Threshold).

VTRLIM = 0 Voltage at Tip/Ring is below the limit.

VTRLIM = 1 Voltage at Tip/Ring is above the limit.

OTEMP Thermal overload warning from the SLIC-E/-E2/-P line drivers masked by the OTEMP-M bit. An interrupt is only generated if the OTEMP bit changes from 0 to1.

OTEMP = 0 Temperature at SLIC-E/-E2/-P is below the limit.

OTEMP = 1 Temperature at SLIC-E/-E2/-P is above the limit.

In case of bit PDOT-DIS = 0 (register BCR2) the DuSLIC is switched automatically into PDH mode and OTEMP is hold at 1 until the SLICOFI-2 is set to PDH by a CIOP/CIDD command.

SYNC-FAIL Failure of the Synchronization of the IOM-2/PCM interface. An interrupt is only generated if the SYNC-FAIL bit changes from 0 to1.

Resynchronization of the PCM interface can be done with the Resynchronization command (see **Chapter 5**)

SYNC-FAIL = 0 Synchronization OK.

SYNC-FAIL = 1 Synchronization failure.

08_H	INTREG2	Interrupt Register 2 (read-only)	20_H		Y

Bit	7	6	5	4	3	2	1	0
	LM-THRES	READY	RSTAT	LM-OK	IO[4:1]-DU			

After a hardware reset, the RSTAT bit is set and generates an interrupt. Therefore the default value of INTREG2 is 20_H. After reading all four interrupt registers, the INTREG2 value changes to $4F_H$.

LM-THRES Indication whether the level metering result is above or below the threshold set by the CRAM coefficients

LM-THRES = 0 Level metering result is below threshold.

LM-THRES = 1 Level metering result is above threshold.

READY Indication whether the ramp generator has finished. An interrupt is only generated if the READY bit changes from 0 to 1. Upon a new start of the ramp generator, the bit is set to 0. For further information regarding soft reversal see **Chapter 2.7.2.1**.

READY = 0 Ramp generator active.

READY = 1 Ramp generator not active.

RSTAT Hardware reset status since last interrupt.

RSTAT = 0 No hardware reset has occurred since the last interrupt.

RSTAT = 1 Hardware reset has occurred since the last interrupt.

LM-OK Level metering sequence has finished. An interrupt is only generated if the LM-OK bit changes from 0 to 1.

LM-OK = 0 Level metering result not ready.

LM-OK = 1 Level metering result ready.

IO[4:1]-DU Data on I/O pins 1 to 4 filtered by DUP-IO counter and interrupt generation masked by the IO[4:1]-DU-M bits. A change of any of this bits generates an interrupt.

09_H	INTREG3	Interrupt Register 3 (read-only)	00_H		Y

Bit	7	6	5	4	3	2	1	0
	DTMF-OK	DTMF-KEY[4:0]					UTDR-OK	UTDX-OK

DTMF-OK Indication of a valid DTMF Key by the DTMF receiver. A change of this bit generates an interrupt.

DTMF-OK = 0 No valid DTMF Key was encountered by the DTMF receiver.

DTMF-OK = 1 A valid DTMF Key was encountered by the DTMF receiver.

DTMF-KEY[4:0] Valid DTMF keys decoded by the DTMF receiver.

Table 32 Valid DTMF Keys (Bit DTMF-KEY4 = 1)

f_{LOW} [Hz]	f_{HIGH} [Hz]	DIGIT	DTMF-KEY4	DTMF-KEY3	DTMF-KEY2	DTMF-KEY1	DTMF-KEY0
697	1209	1	1	0	0	0	1
697	1336	2	1	0	0	1	0
697	1477	3	1	0	0	1	1
770	1209	4	1	0	1	0	0
770	1336	5	1	0	1	0	1
770	1477	6	1	0	1	1	0
852	1209	7	1	0	1	1	1
852	1336	8	1	1	0	0	0
852	1477	9	1	1	0	0	1
941	1336	0	1	1	0	1	0
941	1209	*	1	1	0	1	1
941	1477	#	1	1	1	0	0
697	1633	A	1	1	1	0	1
770	1633	B	1	1	1	1	0

Table 32 Valid DTMF Keys (Bit DTMF-KEY4 = 1) (cont'd)

f_{LOW} [Hz]	f_{HIGH} [Hz]	DIGIT	DTMF-KEY4	DTMF-KEY3	DTMF-KEY2	DTMF-KEY1	DTMF-KEY0
852	1633	C	1	1	1	1	1
941	1633	D	1	0	0	0	0

UTDR-OK Universal Tone Detection Receive (such as Fax/Modem tones)

UTDR-OK = 0 No specific tone signal was detected.

UTDR-OK = 1 A specific tone signal was detected.

UTDX-OK Universal Tone Detection Transmit (such as Fax/Modem tones)

UTDX-OK = 0 No specific tone signal was detected.

UTDX-OK = 1 A specific tone signal was detected.

$0A_H$	**INTREG4**	Interrupt Register 4 (read-only)	00_H		**Y**

Bit	7	6	5	4	3	2	1	0
	EDSP-FAIL	**0**	**0**	**0**	**CIS-BOF**	**CIS-BUF**	**CIS-REQ**	**CIS-ACT**

EDSP-FAIL Indication of a malfunction of the Enhanced Digital Signal Processor EDSP.

EDSP-FAIL = 0 Enhanced Digital Signal Processor EDSP normal operation.

EDSP-FAIL = 1 Enhanced Digital Signal Processor EDSP failure. It is necessary to restart this DSP with bit EDSP-EN in the XCR register set.

CIS-BOF Caller ID buffer overflow. An interrupt is only generated if the CIS-BOF bit changes from 0 to 1.

CIS-BOF = 0 Not data buffer overflow has occurred.

CIS-BOF = 1 Too many bytes have been written to the data buffer for Caller ID generation. Caller ID generation is aborted and the buffer is cleared.

CIS-BUF Caller ID buffer underflow. An interrupt is only generated if the CIS-BUF bit changes from 0 to 1.

CIS-BUF = 0 Data buffer for Caller ID generation is filled.

CIS-BUF = 1 Data buffer for Caller ID generation is empty (underflow).

CIS-REQ Caller ID data request. An interrupt is only generated if the CIS-REQ bit changes from 0 to 1.

CIS-REQ = 0 Caller ID data buffer requests no data.

CIS-REQ = 1 Caller ID data buffer requests more data to transmit, when the amount of data stored in the buffer is less than the buffer request size.

CIS-ACT Caller ID generator active.

This is a status bit only. No interrupt will be generated.

CIS-ACT = 0 Caller ID generator is not active.

CIS-ACT = 1 Caller ID generator is active.

$0B_H$	**CHKR1**	Checksum Register 1 (High Byte) (read-only)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	SUM-OK	**CHKSUM-H[6:0]**						

SUM-OK Information about the validity of the checksum. The checksum is valid if the internal checksum calculation is finished.

Checksum calculation:

For (cram_adr = 0 to 159) do
cram_dat = cram[cram_adr]
csum[14:0] = (csum[13:0] &[1] '0') xor
('0000000' & cram_dat[7:0]) xor
('000000000000' & csum[14] & csum[14])
End

SUM-OK = 0 CRAM checksum is not valid.

SUM-OK = 1 CRAM checksum is valid.

1) "&" means a concatenation; not the logic operation

CHKSUM-H[6:0] CRAM checksum High Byte

$0C_H$	**CHKR2**	Checksum Register 2 (Low Byte) (read-only)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	CHKSUM-L[7:0]							

CHKSUM-L[7:0] CRAM checksum Low Byte

$0D_H$	**LMRES1**	Level Metering Result 1 (High Byte) (read-only)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	LM-VAL-H[7:0]							

LM-VAL-H[7:0] LM result High Byte
(selected by the LM-SEL bits in the LMCR2 register)

$0E_H$	**LMRES2**	Level Metering Result 2 (Low Byte) (read-only)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	LM-VAL-L[7:0]							

LM-VAL-L[7:0] LM result Low Byte
(selected by the LM-SEL bits in the LMCR2 register)

$0F_H$	**FUSE2**	Fuse Register 2	**hw**		**Y**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

10_H	**FUSE3**	Fuse Register 3	hw		Y

Bit	7	6	5	4	3	2	1	0
	for internal use only							

11_H	MASK	Mask Register	FF_H		Y

Bit	7	6	5	4	3	2	1	0
	READY-M	HOOK-M	GNDK-M	GNKP-M	ICON-M	VTRLIM-M	OTEMP-M	SYNC-M

The mask bits in the mask register only influence the generation of an interrupt. Even if the mask bit is set to 1, the corresponding status bit in the INTREGx registers is updated to show the current status of the corresponding event.

READY-M Mask bit for Ramp Generator READY bit

READY-M = 0 An interrupt is generated if the READY bit changes from 0 to 1.

READY-M = 1 Changes of the READY bit do not generate interrupts.

HOOK-M Mask bit for Off-hook Detection HOOK bit

HOOK-M = 0 Each change of the HOOK bit generates an interrupt.

HOOK-M = 1 Changes of the HOOK bit do not generate interrupts.

GNDK-M Mask bit for ground key detection GNDK bit

GNDK-M = 0 Each change of the GNDK bit generates an interrupt.

GNDK-M = 1 Changes of the GNDK bit do not generate interrupts.

GNKP-M Mask bit for ground key level GNKP bit

GNKP-M = 0 Each change of the GNKP bit generates an interrupt.

GNKP-M = 1 Changes of the GNKP bit do not generate interrupts.

ICON-M Mask bit for Constant Current Information ICON bit

ICON-M = 0 Each change of the ICON bit generates an interrupt.

ICON-M = 1 Changes of the ICON bit do not generate interrupts.

VTRLIM-M Mask bit for Programmed Voltage Limit VTRLIM bit

VTRLIM-M = 0 Each change of the VTRLIM bit generates an interrupt.

VTRLIM-M = 1 Changes of the VTRLIM bit do not generate interrupts.

OTEMP-M Mask bit for Thermal Overload Warning OTEMP bit

OTEMP-M = 0	A change of the OTEMP bit from 0 to 1 generates an interrupt.
OTEMP-M = 1	A change of the OTEMP bit from 0 to 1 does not generate interrupts.

SYNC-M Mask bit for Synchronization Failure SYNC-FAIL bit

SYNC-M = 0	A change of the SYNC-FAIL bit from 0 to 1 generates an interrupt.
SYNC-M = 1	A change of the SYNC-FAIL bit from 0 to 1 does not generate interrupts.

12_H	IOCTL1	I/O Control Register 1	$0F_H$		Y

Bit	7	6	5	4	3	2	1	0
	IO[4:1]-INEN				IO[4:1]-M			

The mask bits IO[4:1]-M only influence the generation of an interrupt. Even if the mask bit is set to 1, the corresponding status bit in the INTREGx registers is updated to show the current status of the corresponding event.

IO4-INEN Input enable for programmable I/O pin IO4

IO4-INEN = 0 Input Schmitt trigger of pin IO4 is disabled.

IO4-INEN = 1 Input Schmitt trigger of pin IO4 is enabled.

IO3-INEN Input enable for programmable I/O pin IO3

IO3-INEN = 0 Input Schmitt trigger of pin IO3 is disabled.

IO3-INEN = 1 Input Schmitt trigger of pin IO3 is enabled.

IO2-INEN Input enable for programmable I/O pin IO2

IO2-INEN = 0 Input Schmitt trigger of pin IO2 is disabled.

IO2-INEN = 1 Input Schmitt trigger of pin IO2 is enabled.

IO1-INEN Input enable for programmable I/O pin IO1

IO1-INEN = 0 Input Schmitt trigger of pin IO1 is disabled.

IO1-INEN = 1 Input Schmitt trigger of pin IO1 is enabled.

IO4-M Mask bit for IO4-DU bit

IO4-M = 0 Each change of the IO4 bit generates an interrupt.

IO4-M = 1 Changes of the IO4 bit do not generate interrupts.

IO3-M Mask bit for IO3-DU bit

IO3-M = 0 Each change of the IO3 bit generates an interrupt.

IO3-M = 1 Changes of the IO3 bit do not generate interrupts.

IO2-M Mask bit for IO2-DU bit

IO2-M = 0 Each change of the IO2 bit generates an interrupt.

IO2-M = 1 Changes of the IO2 bit do not generate interrupts.

IO1-M Mask bit for IO1-DU bit

IO1-M = 0 Each change of the IO1 bit generates an interrupt.

IO1-M = 1 Changes of the IO1 bit do not generate interrupts.

13_H	IOCTL2	I/O Control Register 2	00_H		Y

Bit	7	6	5	4	3	2	1	0
	IO[4:1]-OEN				IO[4:1]-DD			

IO4-OEN Enabling output driver of the IO4 pin

IO4-OEN = 0 The output driver of the IO4 pin is disabled.

IO4-OEN = 1 The output driver of the IO4 pin is enabled.

IO3-OEN Enabling output driver of the IO3 pin

IO3-OEN = 0 The output driver of the IO3 pin is disabled.

IO3-OEN = 1 The output driver of the IO3 pin is enabled.

IO2-OEN Enabling output driver of the IO2 pin.

If SLIC-P is selected (bits SEL-SLIC [1:0] in register BCR1 set to 01), pin IO2 cannot be controlled by the user but is utilized by the SLICOFI-2 to control the C3 input of SLIC-P.

IO2-OEN = 0 The output driver of the IO2 pin is disabled.

IO2-OEN = 1 The output driver of the IO2 pin is enabled.

IO1-OEN Enabling output driver of the IO1 pin.

If external ringing is selected (bit REXT-EN in register BCR2 set to 1), pin IO1 cannot be controlled by the user but is utilized by the SLICOFI-2 to control the ring relay.

IO1-OEN = 0 The output driver of the IO1 pin is disabled.

IO1-OEN = 1 The output driver of the IO1 pin is enabled.

IO4-DD Value for the programmable I/O pin IO4 if programmed as an output pin.

IO4-DD = 0 The corresponding pin is driving a logic 0.

IO4-DD = 1 The corresponding pin is driving a logic 1.

IO3-DD Value for the programmable I/O pin IO3 if programmed as an output pin.

IO3-DD = 0 The corresponding pin is driving a logic 0.

IO3-DD = 1 The corresponding pin is driving a logic 1.

IO2-DD Value for the programmable I/O pin IO2 if programmed as an output pin.

IO2-DD = 0 The corresponding pin is driving a logic 0.

IO2-DD = 1 The corresponding pin is driving a logic 1.

IO1-DD Value for the programmable I/O pin IO1 if programmed as an output pin.

IO1-DD = 0 The corresponding pin is driving a logic 0.

IO1-DD = 1 The corresponding pin is driving a logic 1.

14_H	IOCTL3	I/O Control Register 3	94_H		Y

Bit	7	6	5	4	3	2	1	0
	DUP[3:0]				DUP-IO[3:0]			

DUP[3:0] Data Upstream Persistence Counter end value. Restricts the rate of interrupts generated by the HOOK bit in the interrupt register INTREG1. The interval is programmable from 1 to 16 ms in steps of 1 ms (reset value is 10 ms).

The DUP[3:0] value affects the blocking period for ground key detection (see **Chapter 2.6**).

DUP[3:0]	HOOK Active, Ringing	HOOK Power Down	GNDK	GNDK $f_{min,ACsup}$ 1)
0000	1	2 ms	4 ms	125 Hz
0001	2	4 ms	8 ms	62.5 Hz
...				
1111	16	32 ms	64 ms	7.8125 Hz

1) Minimum frequency for AC suppression.

DUP-IO[3:0] Data Upstream Persistence Counter end value for

- the I/O pins when used as digital input pins.
- the bits ICON and VTRLIM in register INTREG1.

The interval is programmable from 0.5 to 60.5 ms in steps of 4 ms (reset value is 16.5 ms).

15_H	BCR1	Basic Configuration Register 1	00_H		Y

Bit	7	6	5	4	3	2	1	0
	HIR	HIT	SLEEP-EN	REVPOL	ACTR	ACTL	SEL-SLIC[1:0]	

HIR This bit modifies different basic modes. In ringing mode, an unbalanced ringing on the RING wire (ROR) is enabled. In Active mode, high impedance on the RING wire is activated (HIR). If the HIT bit is set in addition to the HIR bit, the HIRT mode is activated.

HIR = 0 Normal operation (ringing mode).

HIR = 1 Controls SLIC-E/-E2/-P interface and sets the RING wire to high impedance (Active mode).

HIT This bit modifies different basic modes. In ringing mode, an unbalanced ringing on the TIP wire (ROT) is enabled. In Active mode, high impedance on the TIP wire is performed (HIT). If the HIR bit is set in addition to the HIT bit, the HIRT mode is activated.

HIT = 0 Normal operation (ringing mode).

HIT = 1 Controls SLIC-E/-E2/-P interface and sets the TIP wire to high impedance (Active mode).

SLEEP-EN Enables Sleep mode of the DuSLIC channel. Valid only in the Power Down mode of the SLICOFI-2.

SLEEP-EN = 0 Sleep mode is disabled.

SLEEP-EN = 1 Sleep mode is enabled.

Note: SLEEP-EN has to be set before entering the Power Down mode.

REVPOL Reverses the polarity of DC feeding

REVPOL = 0 Normal polarity.

REVPOL = 1 Reverse polarity.

ACTR Selection of extended battery feeding in Active mode. Also changes the voltage in Power Down Resistive mode for SLIC-P. In this case, V_{BATR} for SLIC-P and $V_{HR} - V_{BATH}$ for SLIC-E/-E2 is used.

ACTR = 0 No extended battery feeding selected.

ACTR = 1 Extended battery feeding selected.

ACTL Selection of the low battery supply voltage V_{BATL} on SLIC-E/-E2/-P if available. Valid only in the Active mode of the SLICOFI-2.

ACTL = 0 Low battery supply voltage on SLIC-E/-E2/-P is not selected.

ACTL = 1 Low battery supply voltage on SLIC-E/-E2/-P is selected.

SEL-SLIC[1:0] Selection of the current SLIC type used. For SLIC-E/-E2 and SLIC-P, the appropriate predefined mode table has to be selected.

SEL-SLIC[1:0] = 0 0 SLIC-E/-E2 selected.

SEL-SLIC[1:0] = 0 1 SLIC-P selected.

SEL-SLIC[1:0] = 1 0 SLIC-P selected for extremely power sensitive applications.

SEL-SLIC[1:0] = 1 1 Reserved for future use.

For SLIC-P two selections are possible.

- The standard SLIC-P selection automatically uses the IO2 pin of the SLICOFI-2 to control the C3 pin of the SLIC-P. By using pin C3 as well as the pins C1 and C2, all possible operating modes of the SLIC-P V1.1 can be selected. For SLIC-P V1.2 only the operating modes with 90 mA current limitation can be selected (ACTL90, ACTH90, ACTR90).

Note: If with SLIC-P V1.2 the 60 mA current limitation modes (ACTL60, ACTH60, ACTR60) are to be used, then the SLIC type SEL-SLIC[1:0] = 10 has to be programmed. In this case the C3 pin of the SLIC-P V1.2 can also be controlled by the IO2 pin of the SLICOFI-2. However, the IO2 pin has then to be programmed manually by the user according to the SLIC-P V1.2 interface code table.

- For extremely power sensitive applications using external ringing with SLIC-P SEL-SLIC[1:0] = 10 should be chosen. In this case, internal unbalanced ringing is not needed and therefore there is no need to switch the C3 pin of the SLIC-P to 'High'. The C3 pin of the SLIC-P must be connected to GND and the IO2 pin of the SLICOFI-2 is programmable by the user.
  There is no need for a high battery voltage for ringing either. This mode uses V_{BATR} for the on-hook voltage (e.g. –48 V) in Power Down Resistive (PDR) mode and the other battery supply voltages (e.g. V_{BATH} = –24 V and V_{BATL} = –18 V) can be used for the off-hook state. This will help to save power because the lowest possible battery voltage can be selected (see DuSLIC Voltage and Power Application Note).

16_H	BCR2	Basic Configuration Register 2	00_H		Y

Bit	7	6	5	4	3	2	1	0
	REXT-EN	SOFT-DIS	TTX-DIS	TTX-12K	HIM-AN	AC-XGAIN	UTDX-SRC	PDOT-DIS

REXT-EN Enables the use of an external ring signal generator. Synchronization is done via the RSYNC pin and the Ring Burst Enable signal is transferred via the IO1 pin.

REXT-EN = 0 External ringing is disabled.

REXT-EN = 1 External ringing enabled.

SOFT-DIS Polarity soft reversal (to minimize noise on DC feeding)

SOFT-DIS = 0 Polarity soft reversal active.

SOFT-DIS = 1 Polarity hard reversal.

TTX-DIS Disables the generation of TTX bursts for metering signals. If TTX bursts are disabled, reverse polarity will be used instead.

TTX-DIS = 0 TTX bursts are enabled.

TTX-DIS = 1 TTX bursts are disabled, reverse polarity used.

TTX-12K Selection of TTX frequencies

TTX-12K = 0 Selects 16 kHz TTX signals instead of 12 kHz signals.

TTX-12K = 1 12 kHz TTX signals.

HIM-AN Higher impedance in analog impedance matching loop.

The value of this bit must correspond to the selection done in the DUSLICOS tool when calculating the coefficients. If the coefficients are calculated with standard impedance in analog impedance matching loop, HIM-AN must be set to 0; if the coefficients are calculated with high impedance in analog impedance matching loop, HIM-AN must be set to 1.

HIM-AN = 0 Standard impedance in analog impedance matching loop

HIM-AN = 1 High impedance in analog impedance matching loop

AC-XGAIN Analog gain in transmit direction (should be set to zero).

AC-XGAIN = 0 No additional analog gain in transmit direction.

AC-XGAIN = 1 Additional 6 dB analog amplification in transmit direction.

UTDX-SRC Universal Tone Detector transmit source.
Any change of bit UTDX-SRC only becomes effective, if bit UTDX-EN in register BCR5 is changed from 0 to 1.

UTDX-SRC	UTDX-SUM	LEC-EN	Signal Source for UTDX
0	0	don't care	Transmit
0	0	don't care	Transmit
0	1	0	Receive + Transmit
0	1	1	Receive + Transmit
1	don't care	0	Transmit
1	don't care	0	Transmit
1	don't care	1	Lec-Output
1	don't care	1	Lec-Output

(see **Figure 29** on **Page 56**)

PDOT-DIS Power Down Overtemperature Disable

PDOT-DIS = 0 When overtemperature is detected, the SLIC is automatically switched into Power Down High Impedance mode (PDH). This is the safe operation mode for the SLIC-E/-E2/-P in case of overtemperature. To leave the automatically activated PDH mode, DuSLIC must be switched manually to PDH mode and then in the mode as desired (otherwise the OTEMP bit in INTREG1 will not change back to 0).

PDOT-DIS = 1 When overtemperature is detected, the SLIC-E/-E2/-P does not automatically switch into Power Down High Impedance mode. In this case, the output current of the SLIC-E/-E2/-P buffers is limited to a value that keeps the SLIC-E/-E2/-P temperature below the upper temperature limit.

The OTEMP bit in INTREG1 changes back to 0 if the SLIC temperature is below the threshold again.

The INT registers may be locked in addition if OTEMP-M = 0.

Note: Transients on Tip/Ring can cause false overtemperature alarms, because the OTEMP signal is not deglitched. To avoid this situation it is recommended to switch off the automatic power down on overtemperature (PDOT-DIS = 1) and integrate a function for overtemperature handling in the interrupt service routine.

17_H	BCR3	Basic Configuration Register 3	00_H		Y

Bit	7	6	5	4	3	2	1	0
	MU-LAW	**LIN**	**PCM16K**	**PCMX-EN**	**CONFX-EN**	**CONF-EN**	**LPRX-CR**	**CRAM-EN**

MU-LAW Selects the PCM Law

MU-LAW = 0 A-Law enabled.

MU-LAW = 1 µ-Law enabled.

LIN Voice transmission in a 16-bit linear representation for test purposes.

Note: Voice transmission on the other channel is inhibited if one channel is set to linear mode and the IOM-2-interface is used. In the PCM/microcontroller interface mode, both channels can be in linear mode using two consecutive PCM timeslots on the highways. A proper timeslot selection must be specified.

LIN = 0 PCM mode enabled (8 bit, A-Law or µ-Law).

LIN = 1 Linear mode enabled (16 bit).

PCM16K Selects 16-kHz sample rate for the PCM interface.

PCM16K = 0 16-kHz mode disabled (8 kHz sampling rate).

PCM16K = 1 16-kHz mode enabled.

PCMX-EN Enables writing of subscriber voice data to the PCM highway.

PCMX-EN = 0 Writing of subscriber voice data to PCM highway is disabled.

PCMX-EN = 1 Writing of subscriber voice data to PCM highway is enabled.

CONFX-EN Enables an external three-party conference.

CONFX-EN = 0 External conference is disabled.

CONFX-EN = 1 External conference is enabled.

CONF-EN Selection of three-party conferencing for this channel. The voice data of this channel and the voice data from the corresponding conferencing channels (see **Chapter 4.1.1**) are added and fed to analog output (see **Chapter 2.10**).

CONF-EN = 0 Three-party conferencing is not selected.

CONF-EN = 1 Three-party conferencing is selected.

LPRX-CR Select CRAM coefficients for the filter characteristic of the LPR/LPX filters. These coefficients may be enabled in case of a modem transmission to improve modem performance.

LPRX-CR = 0 Coefficients from ROM are used.

LPRX-CR = 1 Coefficients from CRAM are used.

CRAM-EN Coefficients from CRAM are used for programmable filters and DC loop behavior.

CRAM-EN = 0 Coefficients from ROM are used.

CRAM-EN = 1 Coefficients from CRAM are used.

18_H	BCR4	Basic Configuration Register 4	00_H		Y

Bit	7	6	5	4	3	2	1	0
	TH-DIS	IM-DIS	AX-DIS	AR-DIS	FRX-DIS	FRR-DIS	HPX-DIS	HPR-DIS

TH-DIS Disables the TH filter.

TH-DIS = 0 TH filter is enabled.

TH-DIS = 1 TH filter is disabled (H_{TH} = 0).

IM-DIS Disables the IM filter.

IM-DIS = 0 IM filter is enabled.

IM-DIS = 1 IM filter is disabled (H_{IM} = 0).

AX-DIS Disables the AX filter.

AX-DIS = 0 AX filter is enabled.

AX-DIS = 1 AX filter is disabled (H_{AX} = 1).

AR-DIS Disables the AR filter.

AX-DIS = 0 AR filter is enabled.

AX-DIS = 1 AR filter is disabled (H_{AR} = 1).

FRX-DIS Disables the FRX filter.

FRX-DIS = 0 FRX filter is enabled.

FRX-DIS = 1 FRX filter is disabled (H_{FRX} = 1).

FRR-DIS Disables the FRR filter.

FRR-DIS = 0 FRR filter is enabled.

FRR-DIS = 1 FRR filter is disabled (H_{FRR} = 1).

HPX-DIS Disables the high-pass filter in transmit direction.

HPX-DIS = 0 High-pass filter is enabled.

HPX-DIS = 1 High-pass filter is disabled (H_{HPX} = 1).

HPR-DIS Disables the high-pass filter in receive direction.

HPR-DIS = 0 High-pass filter is enabled.

HPR-DIS = 1 High-pass filter is disabled (H_{HPR} = 1).

19_H	BCR5	Basic Configuration Register 5	00_H		Y

Bit	7	6	5	4	3	2	1	0
	UTDR-EN	UTDX-EN	CIS-AUTO	CIS-EN	LEC-OUT	LEC-EN	DTMF-SRC	DTMF-EN

UTDR-EN Enables the Universal Tone detection in receive direction.

UTDR-EN = 0 Universal Tone detection is disabled.

UTDR-EN = 1 Universal Tone detection is enabled.

UTDX-EN Enables the Universal Tone detection in transmit direction.

UTDX-EN = 0 Universal Tone detection is disabled.

UTDX-EN = 1 Universal Tone detection is enabled.

CIS-AUTO Controls the turn-off behavior of the Caller ID sender.

CIS-AUTO = 0 The Caller ID sender stops when CIS-EN is switched to 0.

CIS-AUTO = 1 The Caller ID sender continues sending data until the data buffer is empty.

CIS-EN Enables the Caller ID sender in the SLICOFI-2.

Note: The Caller ID sender is configured directly by programming the according POP registers. Caller ID data are written to a 48 byte RAM buffer. According to the buffer request size, this influences the CIS-REQ and CIS-BUF bits.

CIS-EN = 0 Caller ID sender is disabled and Caller ID data buffer is cleared after all data are sent or if CIS-AUTO = 0.

CIS-EN = 1 Caller ID sender is enabled and Caller ID data can be written to the data buffer. After the last data bit is sent, stop bits are sent to the subscriber.

Caller ID data are sent to the subscriber when the number of bytes written to the buffer exceeds CIS-BRS + 2.

LEC-OUT Line Echo Cancellation result for transmit path.

LEC-OUT = 0 Line Echo Cancellation result used for DTMF only.

LEC-OUT = 1 Line Echo Cancellation result fed to transmit path.

LEC-EN Line Echo Cancellation

LEC-EN = 0 Line Echo Cancellation for DTMF disabled.

LEC-EN = 1 Line Echo Cancellation for DTMF enabled.

DTMF-SRC Selects data source for DTMF receiver.
Any change of bit DTMF-SRC only becomes effective, if bit DTMF-EN is changed from 0 to 1.

DTMF-SRC = 0 The Transmit path data (with or without LEC) is used for the DTMF detection.

DTMF-SRC = 1 The Receive path data is used for the DTMF detection.

DTMF-EN Enables the DTMF receiver of the SLICOFI-2. The DTMF receiver will be configured properly by programming registers in the EDSP.

DTMF-EN = 0 DTMF receiver is disabled.

DTMF-EN = 1 DTMF receiver is enabled.

$1A_H$	DSCR	DTMF Sender Configuration Register	00_H		Y

Bit	7	6	5	4	3	2	1	0
	DG-KEY[3:0]				COR8	PTG	TG2-EN	TG1-EN

DG-KEY[3:0] Selects one of sixteen DTMF keys generated by the two tone generators. The key will be generated if TG1-EN and TG2-EN are 1.

Table 33 DTMF Keys

f_{LOW} [Hz]	f_{HIGH} [Hz]	DIGIT	DG-KEY3	DG-KEY2	DG-KEY1	DG-KEY0
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

COR8 Cuts off receive path at 8 kHz before the tone generator summation point. Allows sending of tone generator signals with no overlaid voice.

COR8 = 0 Cut off receive path disabled.

COR8 = 1 Cut off receive path enabled.

PTG Programmable coefficients for tone generators will be used.

PTG = 0 Frequencies set by DG-KEY are used for both tone generators.
Tone generator TG1 level: –5 dBm0
Tone generator TG2 level: –3 dBm0

PTG = 1 CRAM coefficients used for both tone generators.
Tone generator TG1 and TG2 frequencies and levels can be programmed in the DuSLICOS DC Control Parameters 3/4. The levels are set in dBm0:
Level[dBm] = Level[dBm0] + L_R[dBr]

TG2-EN Enables tone generator two

TG2-EN = 0 Tone generator is disabled.

TG2-EN = 1 Tone generator is enabled.

TG1-EN Enables tone generator one

TG1-EN = 0 Tone generator is disabled.

TG1-EN = 1 Tone generator is enabled.

$1B_H$		Reserved	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

$1C_H$	LMCR1	Level Metering Configuration Register 1	22_H		Y

Bit	7	6	5	4	3	2	1	0
	TEST-EN	LM-EN	LM-THM	PCM2DC	LM2PCM	LM-ONCE	LM-MASK	DC-AD16

TEST-EN Activates the SLICOFI-2 test features controlled by test registers TSTR1 to TSTR5.

TEST-EN = 0 SLICOFI-2 test features are disabled.

TEST-EN = 1 SLICOFI-2 test features are enabled.

Note: The Test Register bits can be programmed before the TEST-EN bit is set to 1.

LM-EN Enables level metering. A positive transition of this bit starts level metering (AC and DC).

LM-EN = 0 Level metering stops.

LM-EN = 1 Level metering enabled.

LM-THM Level metering threshold mask bit

LM-THM = 0 A change of the LM-THRES bit (register INTREG2) generates an interrupt.

LM-THM = 1 No interrupt is generated.

PCM2DC PCM voice channel data added to the DC-output.

PCM2DC = 0 Normal operation.

PCM2DC = 1 PCM voice channel data is added to DC output.

LM2PCM Level metering source/result (depending on LM-EN bit) feeding to PCM or IOM-2 interface.

LM2PCM = 0 Normal operation.

LM2PCM = 1 Level metering source/result is fed to the PCM or IOM-2 interface.

LM-ONCE Level metering execution mode.

LM-ONCE = 0	Level metering is executed continuously.
LM-ONCE = 1	Level metering is executed only once. To start the Level Meter again, the LM-EN bit must again be set from 0 to 1.

LM-MASK Interrupt masking for level metering.

LM-MASK = 0	An interrupt is generated after level metering.
LM-MASK = 1	No interrupt is generated.

DC-AD16 Additional digital amplification in the DC AD path for level metering.

DC-AD16 = 0	Additional gain factor 16 disabled.
DC-AD16 = 1	Additional gain factor 16 enabled.

$1D_H$	LMCR2	Level Metering Configuration Register 2	00_H		Y

Bit	7	6	5	4	3	2	1	0
	LM-NOTCH	**LM-FILT**	**LM-RECT**	**RAMP-EN**	**LM-SEL[3:0]**			

LM-NOTCH Selection of a notch filter instead of the band-pass filter for level metering.

LM-NOTCH = 0 Notch filter selected.

LM-NOTCH = 1 Band-pass filter selected.

LM-FILT Enabling of a programmable band-pass or notch filter for level metering.

LM-FILT = 0 Normal operation.

LM-FILT = 1 Band-pass/notch filter enabled.

LM-RECT Rectifier in DC Level Meter

LM-RECT = 0 Rectifier disabled.

LM-RECT = 1 Rectifier enabled.

RAMP-EN The ramp generator works together with the RNG-OFFSET bits in LMCR3 and the LM-EN bit to create different voltage slopes in the DC-Path.

RAMP-EN = 0 Ramp generator disabled.

RAMP-EN = 1 Ramp generator enabled.

LM-SEL[3:0] Selection of the source for the level metering.

LM-SEL[3:0] = 0 0 0 0 AC level metering in transmit

LM-SEL[3:0] = 0 0 0 1 Real part of TTX (TTX_{REAL})

LM-SEL[3:0] = 0 0 1 0 Imaginary part of TTX (TTX_{IMG})

LM-SEL[3:0] = 0 0 1 1 Not used

LM-SEL[3:0] = 0 1 0 0 DC out voltage on DCN-DCP

LM-SEL[3:0] = 0 1 0 1 DC current on IT

LM-SEL[3:0] = 0 1 1 0 AC level metering in receive

LM-SEL[3:0] = 0 1 1 1	AC level metering in receive and transmit
LM-SEL[3:0] = 1 0 0 0	Not used
LM-SEL[3:0] = 1 0 0 1	DC current on IL
LM-SEL[3:0] = 1 0 1 0	Voltage on IO3
LM-SEL[3:0] = 1 0 1 1	Voltage on IO4
LM-SEL[3:0] = 1 1 0 0	Not used
LM-SEL[3:0] = 1 1 0 1	V_{DD}
LM-SEL[3:0] = 1 1 1 0	Offset of DC-Prefi (short circuit on DC-Prefi input)
LM-SEL[3:0] = 1 1 1 1	Voltage on IO4 – IO3

$1E_H$	LMCR3	Level Metering Configuration Register 3	00_H		Y

Bit	7	6	5	4	3	2	1	0
	AC-SHORT-EN	**RTR-SEL**	**LM-ITIME[3:0]**				**RNG-OFFSET[1:0]**	

AC-SHORT-EN The input pin ITAC will be set to a lower input impedance so that the capacitor C_{ITAC} can be recharged faster during a soft reversal which makes it more silent during conversation.

AC-SHORT-EN = 0 Input impedance of the ITAC pin is standard.

AC-SHORT-EN = 1 Input impedance of the ITAC pin is lowered.

RTR-SEL Ring Trip method selection.

RTR-SEL = 0 Ring Trip with a DC offset is selected.

RTR-SEL = 1 AC Ring Trip is selected. Recommended for short lines only.

LM-ITIME[3:0] Integration Time for AC Level Metering.

LM-ITIME[3:0] = 0 0 0 0 16 ms

LM-ITIME[3:0] = 0 0 0 1 2 × 16 ms

LM-ITIME[3:0] = 0 0 1 0 3 × 16 ms

…

LM-ITIME[3:0] = 1 1 1 1 16 × 16 ms

RNG-OFFSET[1:0] Selection of the Ring Offset source.

RNG-OFFSET[1:0]	Ring Offset Voltage in Given Mode		
	Active ACTH ACTL	Active Ring ACTR	Ring Pause Ringing
0 0	Voltage given by DC regulation	Voltage given by DC regulation	Ring Offset RO1 Hook Threshold Ring
0 1	Ring Offset RO1/2 (no DC regulation)	Ring Offset RO1 (no DC regulation)	Ring Offset RO1 Hook Threshold Ring
1 0	Ring Offset RO2/2 (no DC regulation)	Ring Offset RO2 (no DC regulation)	Ring Offset RO2 Hook Message Waiting
1 1	Ring Offset RO3/2 (no DC regulation)	Ring Offset RO3 (no DC regulation)	Ring Offset RO3 Hook Message Waiting

By setting the RAMP-EN bit to 1, the ramp generator is started by setting LM-EN from 0 to 1 (see **Figure 63**).
Exception: Transition of RNG-OFFSET from 10 to 11 or 11 to 10 where the ramp generator is started automatically (see **Figure 63**).

For Ring Offset RO1, the usual “Hook Threshold Ring” is used. Using Ring Offset RO2 or RO3 in any ringing mode (Ringing and Ring Pause) also changes the hook thresholds. In this case the “Hook Message Waiting” threshold is used automatically.

When using the Ring Offsets RO2 and RO3 for Message Waiting, an additional lamp current is expected. In this case, the Hook Message Waiting threshold should be programmed higher than the Hook Threshold Ring.

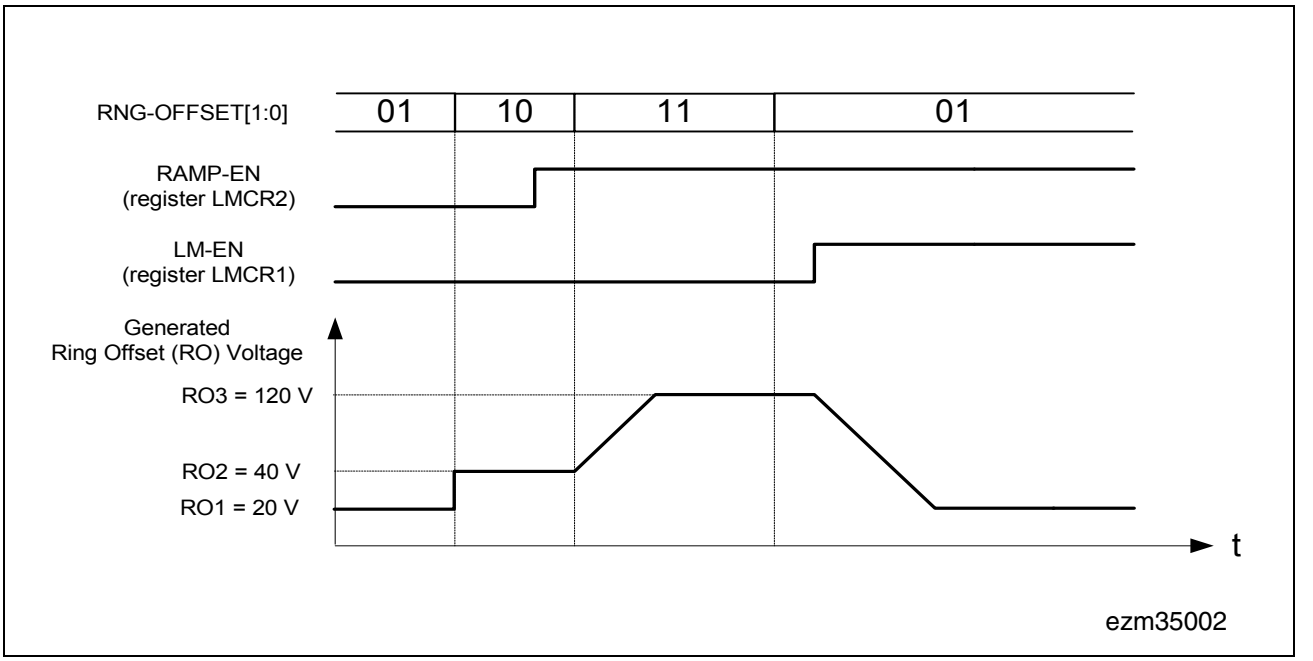


Figure 63 Example for Switching Between Different Ring Offset Voltages

The three programmable Ring Offsets are typically used for the following purposes:

Table 34 Typical Usage for the three Ring Offsets

Ring Offset Voltage	Application
Ring Offset RO1	Ringing
Ring Offset RO2	Low voltage for message waiting lamp
Ring Offset RO3	High voltage for message waiting lamp

Besides the typical usage described in **Table 34**, the Ring Offsets RO1, RO2, and RO3 can also be used for the generation of different custom waveforms (see **Figure 63**).

$1F_H$	**OFR1**	Offset Register 1 (High Byte)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	OFFSET-H[7:0]							

OFFSET-H[7:0] Offset register High Byte.

20_H	**OFR2**	Offset Register 2 (Low Byte)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	OFFSET-L[7:0]							

OFFSET-L[7:0] Offset register Low Byte.

The value of this register together with OFFSET-H is added to the input of the DC loop to compensate for a given offset of the current sensors in the SLIC-E/-E2/-P.

21_H	PCMR1	PCM Receive Register 1	00_H		Y

Bit	7	6	5	4	3	2	1	0
	R1-HW	R1-TS[6:0]						

This register is not applicable and is not used in IOM-2 mode. It is only enabled in PCM/microcontroller mode.

R1-HW Selection of the PCM highway for receiving PCM data or the higher byte of the first data sample if a linear 16-kHz PCM mode is selected.

R1-HW = 0 PCM highway A is selected.

R1-HW = 1 PCM highway B is selected.

R1-TS[6:0] Selection of the PCM timeslot used for data reception.

Note: The programmed PCM timeslot must correspond to the available slots defined by the PCLK frequency. No reception will occur if a slot outside the actual numbers of slots is programmed. In linear mode (bit LIN = 1 in register BCR3), R1-TS defines the first of two consecutive slots used for reception.

22_H	PCMR2	PCM Receive Register 2	00_H		Y

Bit	7	6	5	4	3	2	1	0
	R2-HW	R2-TS[6:0]						

This register is not applicable and is not used in IOM-2 mode. It is only enabled in PCM/microcontroller mode.

R2-HW Selection of the PCM highway for receiving conferencing data for conference channel B or the lower byte of the first data sample if a linear 16-kHz PCM mode is selected.

R2-HW = 0 PCM highway A is selected.

R2-HW = 1 PCM highway B is selected.

R2-TS[6:0] Selection of the PCM timeslot used for receiving data (see description of PCMR1 register).

23_H	PCMR3	PCM Receive Register 3	00_H		Y

Bit	7	6	5	4	3	2	1	0
	R3-HW	R3-TS[6:0]						

This register is not applicable and is not used in IOM-2 mode. It is only enabled in PCM/microcontroller mode.

R3-HW Selection of the PCM highway for receiving conferencing data for conference channel C or the higher byte of the second data sample if a linear 16-kHz PCM mode is selected.

R3-HW = 0 PCM highway A is selected.

R3-HW = 1 PCM highway B is selected.

R3-TS[6:0] Selection of the PCM timeslot used for receiving data (see description of PCMR1 register).

24_H	PCMR4	PCM Receive Register 4	00_H		Y

Bit	7	6	5	4	3	2	1	0
	R4-HW	R4-TS[6:0]						

This register is not applicable and is not used in IOM-2 mode. It is only enabled in PCM/microcontroller mode.

R4-HW Selection of the PCM highway for receiving conferencing data for conference channel D or the lower byte of the second data sample if a linear 16-kHz PCM mode is selected.

R4-HW = 0 PCM highway A is selected.

R4-HW = 1 PCM highway B is selected.

R4-TS[6:0] Selection of the PCM timeslot used for receiving data (see description of PCMR1 register).

25_H	PCMX1	PCM Transmit Register 1	00_H		Y

Bit	7	6	5	4	3	2	1	0
	X1-HW	X1-TS[6:0]						

This register is not applicable and is not used in IOM-2 mode. It is only enabled in PCM/microcontroller mode.

X1-HW Selection of the PCM highway for transmitting PCM data or the higher byte of the first data sample if a linear 16-kHz PCM mode is selected.

X1-HW = 0 PCM highway A is selected.

X1-HW = 1 PCM highway B is selected.

X1-TS[6:0] Selection of the PCM timeslot used for data transmission.

Note: The programmed PCM timeslot must correspond to the available slots defined by the PCLK frequency. No transmission will occur if a slot outside the actual numbers of slots is programmed. In linear mode X1-TS defines the first of two consecutive slots used for transmission. PCM data transmission is controlled by the bits 6 through 2 in register BCR3.

26_H	PCMX2	PCM Transmit Register 2	00_H		Y

Bit	7	6	5	4	3	2	1	0
	X2-HW	X2-TS[6:0]						

This register is not applicable and is not used in IOM-2 mode. It is only enabled in PCM/microcontroller mode.

X2-HW Selection of the PCM highway for transmitting conferencing data for conference channel C + S or C + D or the lower byte of the first data sample if a linear 16-kHz PCM mode is selected.

X2-HW = 0 PCM highway A is selected.

X2-HW = 1 PCM highway B is selected.

X2-TS[6:0] Selection of the PCM timeslot used for transmitting data (see description of PCMX1 register).

27_H	PCMX3	PCM Transmit Register 3	00_H		Y

Bit	7	6	5	4	3	2	1	0
	X3-HW	X3-TS[6:0]						

This register is not applicable and is not used in IOM-2 mode. It is only enabled in PCM/microcontroller mode.

X3-HW Selection of the PCM highway for transmitting conferencing data for conference channel B + S or B + D or the lower byte of the first data sample if a linear 16-kHz PCM mode is selected.

X3-HW = 0 PCM highway A is selected.

X3-HW = 1 PCM highway B is selected.

X3-TS[6:0] Selection of the PCM timeslot used for transmitting data (see description of PCMX1 register).

28_H	PCMX4	PCM Transmit Register 4	00_H		Y

Bit	7	6	5	4	3	2	1	0
	X4-HW	X4-TS[6:0]						

This register is not applicable and is not used in IOM-2 mode. It is only enabled in PCM/microcontroller mode.

X4-HW Selection of the PCM highway for transmitting conferencing data for conference channel B + C or the lower byte of the first data sample if a linear 16-kHz PCM mode is selected.

X4-HW = 0 PCM highway A is selected.

X4-HW = 1 PCM highway B is selected.

X4-TS[6:0] Selection of the PCM timeslot used for transmitting data (see description of PCMX1 register).

29_H	TSTR1	Test Register 1	00_H	T	Y

Bit	7	6	5	4	3	2	1	0
	PD-AC-PR	PD-AC-PO	PD-AC-AD	PD-AC-DA	PD-AC-GN	PD-GNKC	PD-OFHC	PD-OVTC

Register setting is only active if bit TEST-EN in register LMCR1 is set to 1.

PD-AC-PR AC-PREFI Power Down

PD-AC-PR = 0 Normal operation.

PD-AC-PR = 1 Power Down mode.

PD-AC-PO AC-POFI Power Down

PD-AC-PO = 0 Normal operation.

PD-AC-PO = 1 Power Down mode.

PD-AC-AD AC-ADC Power Down

PD-AC-AD = 0 Normal operation.

PD-AC-AD = 1 Power Down mode, transmit path is inactive.

PD-AC-DA AC-DAC Power Down

PD-AC-DA = 0 Normal operation.

PD-AC-DA = 1 Power Down mode, receive path is inactive.

PD-AC-GN AC-Gain Power Down

PD-AC-GN = 0 Normal operation.

PD-AC-GN = 1 Power Down mode.

PD-GNKC Ground key comparator (GNKC) is set to Power Down

PD-GNKC = 0 Normal operation.

PD-GNKC = 1 Power Down mode.

PD-OFHC Off-hook comparator (OFHC) Power Down

PD-OFHC = 0 Normal operation.

PD-OFHC = 1 Power Down mode.

PD-OVTC Overtemperature comparator (OVTC) Power Down

PD-OVTC = 0 Normal operation.

PD-OVTC = 1 Power Down mode.

$2A_H$	TSTR2	Test Register 2	00_H	T	Y

Bit	7	6	5	4	3	2	1	0
	PD-DC-PR	**0**	**PD-DC-AD**	**PD-DC-DA**	**PD-DCBUF**	**0**	**PD-TTX-A**	**PD-HVI**

Register setting is only active if bit TEST-EN in register LMCR1 is set to 1.

PD-DC-PR DC-PREFI Power Down

PD-DC-PR = 0 Normal operation.

PD-DC-PR = 1 Power Down mode.

PD-DC-AD DC-ADC Power Down

PD-DC-AD = 0 Normal operation.

PD-DC-AD = 1 Power Down mode, transmit path is inactive.

PD-DC-DA DC-DAC Power Down

PD-DC-DA = 0 Normal operation.

PD-DC-DA = 1 Power Down mode, receive path is inactive.

PD-DCBUF DC-BUFFER Power Down

PD-DCBUF = 0 Normal operation.

PD-DCBUF = 1 Power Down mode.

PD-TTX-A TTX Adaptation DAC and POFI Power Down

PD-TTX-A = 0 Normal operation.

PD-TTX-A = 1 Power Down mode.

PD-HVI HV interface (to SLIC-E/-E2/-P) Power Down

PD-HVI = 0 Normal operation.

PD-HVI = 1 Power Down mode.

$2B_H$	TSTR3	Test Register 3	00_H	T	Y

Bit	7	6	5	4	3	2	1	0
	0	**0**	**AC-DLB-4M**	**AC-DLB-128K**	**AC-DLB-32K**	**AC-DLB-8K**	**0**	**0**

Register setting is only active if bit TEST-EN in register LMCR1 is set to 1.

AC-DLB-4M AC digital loop via a 4-MHz bitstream. (Loop encloses all digital hardware in the AC path. Together with DLB-DC, a pure digital test is possible because there is no influence from the analog hardware.)

AC-DLB-4M = 0 Normal operation.

AC-DLB-4M = 1 Digital loop closed.

AC-DLB-128K AC digital loop via 128 kHz

AC-DLB-128K = 0 Normal operation.

AC-DLB-128K = 1 Digital loop closed.

AC-DLB-32K AC digital loop via 32 kHz

AC-DLB-32K = 0 Normal operation.

AC-DLB-32K = 1 Digital loop closed.

AC-DLB-8K AC digital loop via 8 kHz

AC-DLB-8K = 0 Normal operation.

AC-DLB-8K = 1 Digital loop closed.

$2C_H$	TSTR4	Test Register 4	00_H	T	Y

Bit	7	6	5	4	3	2	1	0
	OPIM-AN	**OPIM-4M**	**COR-64**	**COX-16**	**0**	**0**	**0**	**0**

Register setting is only active if bit TEST-EN in register LMCR1 is set to 1.

OPIM-AN Open Impedance Matching Loop in the analog part.

OPIM-AN = 0 Normal operation.

OPIM-AN = 1 Loop opened.

OPIM-4M Open fast digital Impedance Matching Loop in the hardware filters.

OPIM-4M = 0 Normal operation.

OPIM-4M = 1 Loop opened.

COR-64 Cut off the AC receive path at 64 kHz (just before the IM filter).

COR-64 = 0 Normal operation.

COR-64 = 1 Receive path is cut off.

COX-16 Cut off the AC transmit path at 16 kHz.(The TH filters can be tested without the influence of the analog part.)

COX-16 = 0 Normal operation.

COX-16 = 1 Transmit path is cut off.

$2D_H$	TSTR5	Test Register 5	00_H	T	Y

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**DC-POFI-HI**	**DC-HOLD**	**0**	**0**	**0**

Register setting is only active if bit TEST-EN in register LMCR1 is set to 1.

DC-POFI-HI Higher value for DC post filter limit

DC-POFI-HI = 0 Limit frequency is set to 100 Hz (normal operation).

DC-POFI-HI = 1 Limit frequency is set to 300 Hz.

DC-HOLD Actual DC output value hold (value of the last DSP filter stage will be kept)

DC-HOLD = 0 Normal operation.

DC-HOLD = 1 DC output value hold.

5.2.2 COP Command

The Coefficient Operation (COP) command gives access to the CRAM data of the DSPs. It is organized in the same way as the SOP command. The offset value allows a direct as well as a block access to the CRAM. Writing beyond the allowed offset will be ignored, reading beyond it will give unpredictable results. The value of a specific CRAM coefficient is calculated by the DuSLICOS software.

Attention: To ensure proper functionality, it is essential that all unused register bits have to be filled with zeros.

Bit	7	6	5	4	3	2	1	0
Byte 1	**RD**	**1**	**ADR[2:0]**			**1**	**0**	**1**
Byte 2	**OFFSET[7:0]**							

RD Read Data

RD = 0 Write data to chip.

RD = 1 Read data from chip.

ADR[2:0] Channel address for the subsequent data

ADR[2:0] = 0 0 0 Channel A

ADR[2:0] = 0 0 1 Channel B

(other codes reserved for future use)

Offset [7:0]	Short Name	Long Name
00_H	TH1	Transhybrid Filter Coefficients Part 1
08_H	TH2	Transhybrid Filter Coefficients Part 2
10_H	TH3	Transhybrid Filter Coefficients Part 3
18_H	FRR	Frequency-response Filter Coefficients Receive Direction
20_H	FRX	Frequency-response Filter Coefficients Transmit Direction
28_H	AR	Amplification/Attenuation Stage Coefficients Receive
30_H	AX	Amplification/Attenuation Stage Coefficients Transmit
38_H	PTG1	Tone Generator 1 Coefficients
40_H	PTG2	Tone Generator 2 Coefficients
48_H	LPR	Low Pass Filter Coefficients Receive
50_H	LPX	Low Pass Filter Coefficients Transmit
58_H	TTX	Teletax Coefficients
60_H	IM1	Impedance Matching Filter Coefficients Part 1
68_H	IM2	Impedance Matching Filter Coefficients Part 2
70_H	RINGF	Ringer Frequency and Amplitude Coefficients (DC loop)
78_H	RAMPF	Ramp Generator Coefficients (DC loop)
80_H	DCF	DC Characteristics Coefficients (DC loop)
88_H	HF	Hook Threshold Coefficients (DC loop)
90_H	TPF	Low-pass Filter Coefficients (DC loop)
98_H		Reserved

Table 35 CRAM Coefficients

Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0	Offset [7:0]	
Transhybrid Coefficient Part 1								00_H	TH1
Transhybrid Coefficient Part 2								08_H	TH2
Transhybrid Coefficient Part 3								10_H	TH3
FIR Filter in Receive Direction								18_H	FRR
FIR Filter in Transmit Direction								20_H	FRX
LM Threshold				2nd Gain Stage Receive		1st Gain Stage Receive		28_H	AR
Band-pass for AC LM			Conference Gain	LM-AC	2nd Gain Stage Transmit		1st Gain Stage Transmit	30_H	AX
TG1 Band-pass					TG1 Gain		TG1 Frequency	38_H	PTG1 [1]
TG2 Band-pass					TG2 Gain		TG2 Frequency	40_H	PTG2 [1]
LPR								48_H	LPR [2]
LPX								50_H	LPX [2]
FIR Filter for TTX					TTX Slope		TTX Level	58_H	TTX
IM K Factor	IM FIR Filter							60_H	IM1_F
IM 4 MHz Filter			IM WDF Filter					68_H	IM2_F
LM DC Gain	Ring Generator Amplitude		Ring Generator Frequency		Ring Generator Low-pass		Ring Offset RO1	70_H	RINGF
Extended Battery Feeding Gain	Soft Reversal End		Constant Ramp CR		Soft Ramp SS		Ring Delay RD	78_H	RAMPF
Res. in Resistive Zone R_{K12}	Res. in Constant Current Zone R_I		Constant Current I_{K1}		Knee Voltage V_{K1}		Open Circuit Volt. V_{LIM}	80_H	DCF
Hook Message Waiting	Hook Threshold AC Ring Trip		Hook Threshold Ring		Hook Threshold Active		Hook Threshold Power Down	88_H	HF
Ring Offset RO3	Ring Offset RO2		Voltage Level V_{TR}		DC Low-pass Filter TP2		DC Low-pass Filter TP1	90_H	TPF
Reserved								98_H	
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		

CRAM coefficients are enabled by setting bit CRAM-EN in register BCR3 to 1, except coefficients marked [1] and [2]:
Coefficients marked[1] are enabled by setting bit PTG in register DSCR to 1.
Coefficients marked[2] are enabled by setting bit LPRX-CR in register BCR3 to 1.

5.2.2.1 CRAM Programming Ranges

Table 36 CRAM Programming Ranges

Parameter	Programming Range
Constant Current I_{K1}	0...50 mA, Δ < 0.5 mA
Hook Message Waiting, Hook Thresholds	0..25 mA, Δ < 0.7 mA 25...50 mA, Δ < 1.3 mA
Ring Generator Frequency f_{RING}	3..40 Hz, Δ < 1 Hz 40..80 Hz, Δ < 2 Hz > 80 Hz, Δ < 4 Hz
Ring Generator Amplitude	0..20 V, Δ < 1.7 V 20..85 V, Δ < 0.9 V
Ring Offset RO1, RO2, RO3	0..25 V, Δ < 0.6 V 25..50 V, Δ < 1.2 V 50..100 V, Δ < 2.4 V, max. 150 V
Knee Voltage V_{K1}, Open Circuit Voltge V_{LIM}	0..25 V, Δ < 0.6 V 25..50 V, Δ < 1.2 V > 50 V, Δ < 2.4 V
Resistance in Resistive Zone R_{K12}	0..1000 Ω, Δ < 30 Ω
Resistance in Constant Current Zone R_I	1.8 kΩ..4.8 kΩ, Δ < 120 Ω 4.8 kΩ..9.6 kΩ, Δ < 240 Ω 9.6 kΩ..19 kΩ, Δ < 480 Ω 19 kΩ..38 kΩ, Δ < 960 Ω, max. 40 kΩ

5.2.3 POP Command

The Signal Processing Operation Programming (POP) command provides access to the Enhanced Digital Signal Processor (EDSP) registers of the SLICOFI-2.

Before using an EDSP function the according POP registers have to be programmed.

Any change in any of the POP registers (except registers CIS-DAT and CIS/LEC-MODE) is only updated with enabling the corresponding device. For example a change of the center frequency f_C of the UTD is handled by changing the registers UTD-CF-H and UTD-CF-L, switching off the UTD and switching it on again.

The POP registers do no have default values after any kind of reset.

Attention: To ensure proper functionality, the POP registers have to be programmed before EDSP-EN = 1.
Furthermore, all unused POP register bits must be filled with zeros.

5.2.3.1 Sequence for POP Register Programming

Please note that the NLP coefficients share the memory location with DTMF and LEC coefficients. The coefficients are programmed in the following order (Before the first activation of the EDSP all POP registers have to be programmed. By activation of the individual functions the contents of the double-used registers are then taken over.):

1. Program the LEC coefficients.
   By setting bit LEC-EN in register BCR5 to 1, the coefficients are copied into the EDSP and the LEC is activated.
2. Program the DTMF coefficients.
   By setting bit DTMF-EN in register BCR5 to 1, the coefficients are copied into the EDSP and the DTMF receiver is activated.
3. Program the NLP coefficients.
   By setting bit NLP-EN in POP register CIS/LEC-Mode to 1, the coefficients are copied into the EDSP and the NLP is activated. Please note that the NLP can only be activated, when also the LEC is active.
   If the NLP coefficients have been programmed in a prior session, it is possible to activate the NLP using the old NLP configuration by setting bit NLP-OLDC in POP register NLP-CTRL to 1.

Attention: NLP coefficients are only available with SLICOFI-2 Version 1.5

5.2.3.2 POP Register Overview

Attention: NLP coefficients are only available with SLICOFI-2 Version 1.5

00_H	CIS-DAT	Caller ID Sender Data Buffer (write-only)		
30_H	DTMF-LEV	DTMF Receiver Level Byte		
	0		b	e
30_H	NLP-POW-LPF	NLP Power Estimation LP Fast Time Constant		
	POW-LPF			
31_H	DTMF-TWI	DTMF Receiver Twist Byte		
	TWI			
31_H	NLP-POW-LPS	NLP Power Estimation LP Slow Time Constant		
	POW-LPS			
32_H	DTMF-NCF-H	DTMF Receiver Notch Filter Center Frequency High Byte		
	NCF-H			
32_H	NLP-BN-LEV-X	NLP Background Noise Estimation Transmit Level		
	BN-LEV-X			
33_H	DTMF-NCF-L	DTMF Receiver Notch Filter Center Frequency Low Byte		
	NCF-L			
33_H	NLP-BN-LEV-R	NLP Background Noise Estimation Receive Level		
	BN-LEV-R			
34_H	DTMF-NBW-H	DTMF Receiver Notch Filter Bandwidth High Byte		
	NBW-H			
34_H	NLP-BN-INC	NLP Background Noise Estimation Increment		
	BN-INC			
35_H	DTMF-NBW-L	DTMF Receiver Notch Filter Bandwidth Low Byte		
	NBW-L			
35_H	NLP-BN-DEC	NLP Background Noise Estimation Decrement		
	BN-DEC			

36_H DTMF-GAIN — Gain Stage Control for DTMF Input Signal

e	m

36_H NLP-BN-MAX — NLP Background Noise Estimation Maximum Noise

BN-MAX

37_H NLP-BN-ADJ — NLP Background Noise Estimation Noise Adjustment

BN-ADJ

38_H NLP-RE-MIN-ERLL — NLP Residual Echo Minimum ERL for LEC + Line

RE-MIN-ERLL

39_H NLP-RE-EST-ERLL — NLP Residual Echo Estimated ERL for LEC + Line

RE-EST-ERLL

$3A_H$ LEC-LEN — Line Echo Cancellation Length

LEN

$3A_H$ NLP-SD-LEV-X — NLP Speech Detection Transmit Direction Level

SD-LEV-X

$3B_H$ LEC-POWR — Line Echo Cancellation Power Detection Level

POWR

$3B_H$ NLP-SD-LEV-R — NLP Speech Detection Receive Direction Level

SD-LEV-R

$3C_H$ LEC-DELP — Line Echo Cancellation Delta Power

DELP

$3C_H$ NLP-SD-LEV-BN — NLP Speech Detection BN Level

SD-LEV-BN

$3D_H$ LEC-DELQ — Line Echo Cancellation Delta Quality

DELQ

$3D_H$ NLP-SD-LEV-RE — NLP Speech Detection RE Level

SD-LEV-RE

$3E_H$ LEC-GAIN-XI — Line Echo Cancellation Input Gain Transmit

e	m

$3E_H$ NLP-SD-OT-DT — NLP Speech Detection Overhang Tone for Double Talk

SD-OT-DT

$3F_H$ LEC-GAIN-RI — Line Echo Cancellation Input Gain Receive

e	m

$3F_H$ NLP-ERL-LIN-LP — NLP Echo Return Loss Line LP Time Constant

ERL-LIN-LP

40_H LEC-GAIN-XO — Line Echo Cancellation Output Gain Transmit

e	m

40_H NLP-ERL-LEC-LP — NLP Echo Return Loss LEC LP Time Constant

ERL-LEC-LP

41_H NLP-CT-LEV-RE — NLP Control RE Level

CT-LEV-RE

42_H NLP-CTRL — NLP Control

0	0	0	0	0	NLP-NM	NLP-NG	NLP-OLDC

43_H CIS-LEV-H — Caller ID Sender Level High Byte

LEV-H

44_H CIS-LEV-L — Caller ID Sender Level Low Byte

LEV-L

45_H CIS-BRS — Caller ID Sender Buffer Request Size

BRS

46_H CIS-SEIZ-H — Caller ID Sender Number of Seizure Bits High Byte

SEIZ-H

47_H CIS-SEIZ-L Caller ID Sender Number of Seizure Bits Low Byte

SEIZ-L

48_H CIS-MARK-H Caller ID Sender Number of Mark Bits High Byte

MARK-H

49_H CIS-MARK-L Caller ID Sender Number of Mark Bits Low Byte

MARK-L

$4A_H$ CIS/LEC-MODE CIS/LEC Mode Setting

LEC-ADAPT	LEC-FREEZE	UTDX-SUM	UTDR-SUM	0	NLP-EN	CIS-FRM	CIS-V23

$4B_H$ UTD-CF-H Universal Tone Detection Center Frequency High Byte

CF-H

$4C_H$ UTD-CF-L Universal Tone Detection Center Frequency Low Byte

CF-L

$4D_H$ UTD-BW-H Universal Tone Detection Bandwidth High Byte

BW-H

$4E_H$ UTD-BW-L Universal Tone Detection Bandwidth Low Byte

BW-L

$4F_H$ UTD-NLEV Universal Tone Detection Noise Level

NLEV

50_H UTD-SLEV-H Universal Tone Detection Signal Level High Byte

SLEV-H

51_H UTD-SLEV-L Universal Tone Detection Signal Level Low Byte

SLEV-L

52_H UTD-DELT Universal Tone Detection Delta

DELT-H

53_H UTD-RBRK Universal Tone Detection Recognition Break Time

RBRK

54_H UTD-RTIME Universal Tone Detection Recognition Time

RTIME

55_H UTD-EBRK UTD Allowed Tone End Detection Break Time

EBRK

56_H UTD-ETIME UTD Tone End Detection Time

ETIME

5.2.3.3 POP Register Description

Attention: NLP coefficients are only available with SLICOFI-2 Version 1.5

00_H	**CIS-DAT**	Caller ID Sender Data Buffer (write-only)			**Y**

Bit	7	6	5	4	3	2	1	0
	Byte 0							
	Byte 1							
	Byte 2							
	•							
	•							
	•							
	Byte 47							

30_H	**DTMF-LEV**	DTMF Receiver Level Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	0			**b**		**e**		

Minimum DTMF Signal Detection Level $Level_{DTMFdet}$

- for DTMF detection in transmit:

$Level_{DTMFdet}[dB] = Level_{DTMFdet}[dBm0] – 3.14 + G_{DTMF}[dB]$

$Level_{DTMFdet}[dB] = Level_{DTMFdet}[dBm] – L_x[dBr] – 3.14 + G_{DTMF}[dB]$

- for DTMF detection in receive:

$Level_{DTMFdet}[dB] = Level_{DTMFdet}[dBm0] – 3.14 + AR1[dB] + G_{DTMF}[dB]$

$Level_{DTMFdet}[dB] = Level_{DTMFdet}[dBm] – L_R[dBr] – 3.14 + AR1[dB] + G_{DTMF}[dB]$

AR1[dB]: The exact value for AR1 is shown in the DuSLICOS result file;
approximate value AR1 $\approx$ L_R for $L_R \leq$ –2 dBr, AR1 $\approx$ –2 dB for $L_R >$ –2 dBr.

$Level_{DTMFdet}[dB] = –30 – b – 3 \times e[dB]$

$–54\ dB \leq Level_{DTMFdet} \leq –30\ dB$

with

$0 \leq e \leq 7$

$0 \leq b \leq 3$

Alternative representation

$b = MOD[(–Level_{DTMFdet}[dB] – 30),3]$

$e = INT[(–Level_{DTMFdet}[dB] – 30)/3]$

Note: MOD = Modulo function, INT = Integer function

30_H	**NLP-POW-LPF**	NLP Power Estimation LP Fast Time Constant			**Y**

Bit	7	6	5	4	3	2	1	0
	POW-LPF							

NLP Power Estimation Low Pass Fast Time Constant:

The $T_{POW-LPF}$ time constant is used for increasing signals.

POW-LPF = $255/T_{POW-LPF}$[ms]

1 ms $\leq T_{POW-LPF} \leq$ 255 ms

Table 37 Range of $T_{POW-LPF}$

POW-LPF	**$T_{POW-LPF}$[ms]**
0xFF	1
…	
0x01	255

31_H	**DTMF-TWI**	DTMF Receiver Twist Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	TWI							

DTMF Receiver Twist Byte:

The DTMF receiver twist byte defines the maximum allowed difference between the signal levels of the two tones for DTMF detection:

$TWI = 2 \times Twist_{acc}[dB]$

$0\ dB \leq Twist_{acc} \leq 12\ dB$

Table 38 Range of $Twist_{acc}$

POW-LPS	**$Twist_{acc}$[dB]**
0x00	0
…	
0x18	12

31_H	**NLP-POW-LPS**	NLP Power Estimation LP Slow Time Constant			**Y**

Bit	7	6	5	4	3	2	1	0
	POW-LPS							

NLP Power Estimation Low Pass Slow Time Constant:

The $T_{POW-LPS}$ time constant is used for decreasing signals.

POW-LPS = $1024/T_{POW-LPS}$[ms]

4 ms < $T_{POW-LPS}$ ≤1024 ms

Table 39 Range of $T_{POW-LPS}$

POW-LPS	**$T_{POW-LPS}$[ms]**
0xFF	4
…	
0x01	1024

32_H	**DTMF-NCF-H**	DTMF Receiver Notch Filter Center Frequency High Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	NCF-H							

This byte belongs to the **DTMF-NCF-L** byte described on **Page 219**.

32_H	NLP-BN-LEV-X	NLP Background Noise Estimation Transmit Level			Y

Bit	7	6	5	4	3	2	1	0
	BN-LEV-X							

NLP Background Noise Estimation Transmit Level:

If the transmit signal $S_{LEC,TIN}$ (**Figure 24**) is below $Pow_{BN-LEV-X}$ and the receive signal is below $Pow_{BN-LEV-R}$ (see **Page 220**), the background noise estimator uses the transmit signal for the background noise estimation. Otherwise the background noise estimator is frozen.

$Pow_{BN-LEV-X}[dB] = S_{X,BN-LEV}[dBm0] - 3.14 + G_{LEC-XI}[dB] - 20*\log_{10}(\pi/2)$

$S_{X,BN-LEV}[dBm0]$: Power detection level at digital output for freezing the background noise estimator

$BN-LEV-X = (6.02 \times 16 + Pow_{BN-LEV-X}[dB]) \times 2/(5 \times \log_{10}2)$
$= (96.32 + Pow_{BN-LEV-X}[dB]) \times 1.329$

$-96\ dB \leq Pow_{BN-LEV-X} \leq 0\ dB$

Table 40 Range of $Pow_{BN-LEV-X}$

BN-LEV-X	$Pow_{BN-LEV-X}[dB]$
0x00	–96
…	
0x7F	0

33_H	**DTMF-NCF-L**	DTMF Receiver Notch Filter Center Frequency Low Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	NCF-L							

DTMF Receiver Notch Filter Center Frequency:

$$NCF = 32768 \times \cos\left(2\pi \frac{f_{NCF}[Hz]}{8000}\right) = NCF\text{-}L + 256 \times NCF\text{-}H$$

$0\ Hz \leq f_{NCF} \leq 2000\ Hz$

The bytes are calculated as follows:

NCF-L = MOD (NCF,256) = NCF & 0x00FF

NCF-H = INT (NCF/256) = NCF >> 8

The echo of the dial tone can activate the double talk detection which means that the DTMF tone will not be detected. Therefore a notchfilter can be programmed to filter out the echo of the dialtone, because the frequency of the dialtone is known. The center frequency and the bandwith of the notch filter can be programmed.

33_H	NLP-BN-LEV-R	NLP Background Noise Estimation Receive Level			Y

Bit	7	6	5	4	3	2	1	0
	BN-LEV-R							

NLP Background Noise Estimation Receive Level:

If the transmit signal is below $Pow_{BN\text{-}LEV\text{-}X}$ (see **Page 218**) and the receive signal $S_{LEC,R}$ (see **Figure 29**) is below $Pow_{BN\text{-}LEV\text{-}R}$, the background noise estimator uses the transmit signal for the background noise estimation. Otherwise the background noise estimator is frozen.

$Pow_{BN\text{-}LEV\text{-}R}[dB] = S_{R,BN\text{-}LEV}[dBm0] - 3.14 + AR1[dB] + G_{LEC\text{-}RI}[dB] - 20*\log_{10}(\pi/2)$

$S_{R,BN\text{-}LEV}[dBm0]$: Power detection level at digital input for freezing the background noise estimator

AR1[dB]: The exact value for AR1 is shown in the DuSLICOS result file;
approximate value AR1 $\approx$ L_R for $L_R \leq -2$ dBr, AR1 $\approx$ –2 dB for $L_R > -2$ dBr.

$BN\text{-}LEV\text{-}R = (6.02 \times 16 + Pow_{BN\text{-}LEV\text{-}R}[dB]) \times 2/(5 \times \log_{10}2)$
$= (96.32 + Pow_{BN\text{-}LEV\text{-}R}[dB]) \times 1.329$

$-96\ dB \leq Pow_{BN\text{-}LEV\text{-}R} \leq 0\ dB$

Table 41 Range of $Pow_{BN\text{-}LEV\text{-}R}$

BN-LEV-R	$Pow_{BN\text{-}LEV\text{-}R}[dB]$
0x00	–96
…	
0x7F	0

34_H	DTMF-NBW-H	DTMF Receiver Notch Filter Bandwidth High Byte			Y

Bit	7	6	5	4	3	2	1	0
	NBW-H							

This byte belongs to the **DTMF-NBW-L** byte described on **Page 222**.

34_H	NLP-BN-INC	NLP Background Noise Estimation Increment			Y

Bit	7	6	5	4	3	2	1	0
	BN-INC							

NLP Background Noise Estimation Increment:

The T_{BN-INC} increment time constant for the background noise estimation will be used, when the input signal is higher than the actual estimated background noise value.

BN-INC = 0.680330873 × T_{BN-INC}[dB/sec.]

1.5 dB/sec. ≤T_{BN-INC} ≤375 dB/sec.

Table 42 Range of T_{BN-INC}

BN-INC	T_{BN-INC}[dB/sec.]
0x01	1.5
…	
0xFF	375

35_H	**DTMF-NBW-L**	DTMF Receiver Notch Filter Bandwidth Low Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	NBW-L							

DTMF Receiver Notch Filter Bandwidth:

$$NBW = 65536 \times \frac{a}{1+a} = NBW\text{-}L + 256 \times NBW\text{-}H$$

with

$$a = \tan\left(\pi \cdot \frac{F_{NBW}[Hz]}{8000}\right)$$

$0\ Hz \leq F_{NBW} \leq 2000\ Hz$

NBW_L = MOD (NBW,256)

NBW_H = INT (NBW/256)

35_H	**NLP-BN-DEC**	NLP Background Noise Estimation Decrement			**Y**

Bit	7	6	5	4	3	2	1	0
	BN-DEC							

NLP Background Noise Estimation Decrement:

The T_{BN-DEC} decrement time constant for the background noise estimation will be used, when the input signal is lower than the actual estimated background noise value.

BN-DEC = 0.680330873 × T_{BN-DEC}[dB/sec.]

1.5 dB/sec. ≤T_{BN-DEC} ≤375 dB/sec.

Table 43 Range of T_{BN-DEC}

BN-DEC	**T_{BN-DEC}[dB/sec.]**
0x01	1.5
…	
0xFF	375

36_H	DTMF-GAIN	Gain Stage Control for DTMF Input Signal			Y

Bit	7	6	5	4	3	2	1	0
	e			m				

DTMF Input Signal Gain:

$G_{DTMF}[dB] = 20 \times \log_{10}16 + 20 \times \log_{10}[g/32768] \approx 24.08 + 20 \times \log_{10}[g/32768]$

$-24.08\ dB \leq G_{DTMF} \leq 23.95\ dB$

with

$g = 2^{(9-e)} \times (32 + m)$ and

$0 \leq m \leq 31,\ 0 \leq e \leq 7$

Table 44 Ranges of G_{DTMF}[dB] dependent on "e"

e	DTMF Input Signal Gain G_{DTMF} [dB] Range
0	$23.95\ dB \geq G_{DTMF} \geq 18.06\ dB$
1	$17.93\ dB \geq G_{DTMF} \geq 12.04\ dB$
7	$-18.20\ dB \geq G_{DTMF} \geq -24.08\ dB$

Alternative representation:

Choose "e" as the next integer value which is higher than or equal to:

$$e \geq 3 - \log_2 G_{DTMF} = 3 - \frac{\log_{10} G_{DTMF}}{\log_{10} 2} \approx 3 - \frac{G_{DTMF}[dB]}{6.02}$$

$$m = G_{DTMF} \times 2^{2+e} - 32 = 10^{\frac{G_{DTMF}[dB]}{20}} \times 2^{2+e} - 32$$

Table 45 Example for DTMF-GAIN Calculation

G_{DTMF}[dB]	G_{DTMF}	e	m	DTMF-GAIN
0	1	3	0	0x60
–6.02	0.5	4	0	0x80
6.02	2	2	0	0x40

36_H	NLP-BN-MAX	NLP Background Noise Estimation Maximum Noise			Y

Bit	7	6	5	4	3	2	1	0
	BN-MAX							

NLP Background Noise Estimation Maximum Noise:

The maximum allowed background noise BN-MAX is a coefficient that limits the background noise estimator so that the estimated background noise cannot exceed $S_{X,BN-MAX}$.

$Pow_{BN-MAX}[dB] = S_{X,BN-MAX}[dBm0] – 3.14 – G_{LEC-XO}[dB] – 20*\log_{10}(\pi/2)$

$S_{X,BN-MAX}[dBm0]$: Maximum background noise at digital output

$BN\text{-}MAX = (6.02 \times 16 + Pow_{BN-MAX}[dB]) \times 2/(5 \times \log_{10}2)$
$= (96.32 + Pow_{BN-MAX}[dB]) \times 1.329$

$–96\ dB \leq Pow_{BN-MAX} \leq 0\ dB$

Table 46 Range of Pow_{BN-MAX}

BN-MAX	Pow_{BN-MAX}[dB]
0x00	–96
…	
0x7F	0

37_H	**NLP-BN-ADJ**	NLP Background Noise Estimation Noise Adjustment			**Y**

Bit	7	6	5	4	3	2	1	0
	BN-ADJ							

NLP Background Noise Estimation Noise Adjustment:

The BN-ADJ coefficient adjusts the estimated background noise. It is possible to subtract ($Delta_{BN\text{-}ADJ} < 0$) or to add ($Delta_{BN\text{-}ADJ} > 0$) a constant level of noise from (to) the estimated background noise.

$BN\text{-}ADJ = Delta_{BN\text{-}ADJ}[dB] \times 2/(5 \times \log_{10}2) = Delta_{BN\text{-}ADJ}[dB] \times 1.329$

$-96\ dB \leq Delta_{BN\text{-}ADJ} \leq 96\ dB$

Table 47 Range for $Delta_{BN\text{-}ADJ}$

BN-ADJ	$Delta_{BN\text{-}ADJ}$[dB]
0x81	–96
…	
0x7F	96

38_H	**NLP-RE-MIN-ERLL**	NLP Residual Echo Minimum ERL for LEC + Line			**Y**

Bit	7	6	5	4	3	2	1	0
	RE-MIN-ERLL							

NLP Residual Echo Minimum Echo Return Loss for LEC + Line:

The RE-MIN-ERLL coefficients defines, when the NLP should switch from the simple mode to the comfort mode. If the estimated echo return loss for the hybrid plus the echo return loss for the LEC is higher than $ERLL_{RE-MIN}$, the NLP switches to the comfort mode. In comfort mode, the NLP estimates the residual echo by itself.

RE-MIN-ERLL = $(2/(5 \times \log_{10}2)) \times ERLL_{RE-MIN}$ [dB]

$ERLL_{RE-MIN}$ [dB] = $S_{LEC,R}$[dB] – $S_{LEC,TOUT}$[dB] = $S_R - S_X + AR1 + G_{LEC,RI} + G_{LEC,X0}$

(see **Figure 29**)

The echo return loss is the difference between the signal level in receive direction S_R and the echo level in transmit direction S_X.

0 dB ≤$ERLL_{RE-MIN}$ ≤96 dB

Table 48 Range of $ERLL_{RE-MIN}$

RE-MIN-ERLL	$ERLL_{RE-MIN}$[dB]
0x00	0
…	
0x7F	96

39_H	**NLP-RE-EST-ERLL**	NLP Residual Echo Estimated ERL for LEC + Line			**Y**

Bit	7	6	5	4	3	2	1	0
	RE-EST-ERLL							

NLP Residual Echo Estimated Echo Return Loss for LEC + Line:

After being enabled, the NLP has no information regarding the echo return loss of the hybrid and the LEC. Therefore the NLP has two modes for the residual echo estimation: A simple mode, which is used after the NLP activation and a comfort mode which is used when the internal filters have usable values.

In the simple mode the equation for the residual echo RE is:

$RE = S_{LEC,R} - ERLL_{RE-EST}$

Due to the equation above, $ERLL_{RE-EST}$ should be equal to the worst case echo return loss for the hybrid (which is exactly the worst case echo return loss between the LEC receive input signal and the LEC transmit input signal).

For DuSLIC, the worst case echo return loss can be estimated by:

$ERLL_{RE-EST} = AR1 + G_{LEC,RI} + G_{LEC,XI} - L_R + L_X$

AR1[dB]: The exact value for AR1 is shown in the DuSLICOS result file;
approximate value AR1 $\approx$ L_R for $L_R \leq -2$ dBr, AR1 $\approx$ –2 dB for $L_R > -2$ dBr.

For $L_R \leq -2$ dBr: $ERLL_{RE-EST} \approx G_{LEC,RI} + G_{LEC,XI} + L_X$

A negative $ERLL_{RE-EST}$ value means that there is gain in the loop while a positive $ERLL_{RE-EST}$ value means that there is attenuation in the loop.

RE-EST-ERLL = $ERLL_{RE-EST}[dB] \times 2/(5 \times \log_{10}2) = ERLL_{RE-EST}[dB] \times 1.329$

$-96\ dB \leq ERLL_{RE-EST} \leq 96\ dB$

Table 49 Range of $ERLL_{RE-EST}$

RE-EST-ERLL	$ERLL_{RE-EST}$[dB]
0x81	–96
…	
0x7F	96

$3A_H$	LEC-LEN	Line Echo Cancellation Length			Y

Bit	7	6	5	4	3	2	1	0
	LEN							

Line Echo Cancellation Length:

LEN = LEC Length[ms]/0.125

LEC Length has to be entered in multiples of 0.125 ms.

The selected LEC Length has to be higher than the maximum line echo length but not higher than 8 ms.

0.125 ms ≤LEC Length ≤8 ms

Table 5-1 Range of LEC Length

LEN	LEC Length
0x01	0.125 ms
…	
0x40	8 ms

$3A_H$	**NLP-SD-LEV-X**	NLP Speech Detection Transmit Direction Level			**Y**

Bit	7	6	5	4	3	2	1	0
	SD-LEV-X							

NLP Speech Detection Transmit Direction Level:

As a condition for valid speech detection in transmit direction, the transmit signal level has to be higher than $S_{SD\text{-}LEV\text{-}X}$.
For other conditions see SD-LEV-BN on **Page 234** and SD-LEV-RE on **Page 236**.

$S_{SD\text{-}LEV\text{-}X}[dB] = S_X + G_{LEC,XI}$

SD-LEV-X = $(2/(5 \times \log_{10}2)) \times (96.3 + S_{SD\text{-}LEV\text{-}X}[dB])$

$-96\ dB \leq S_{SD\text{-}LEV\text{-}X} \leq 0\ dB$

Table 50 Range of $S_{SD\text{-}LEV\text{-}X}$

SD-LEV-X	**$S_{SD\text{-}LEV\text{-}X}$[dB]**
0x00	–96
…	
0x7F	0

$3B_H$	LEC-POWR	Line Echo Cancellation Power Detection Level			Y

Bit	7	6	5	4	3	2	1	0
	POWR							

Minimum Power Detection Level for Line Echo Cancellation:

$Pow_{LECR}[dB] = S_{R,LEC\text{-}POWR}[dBm0] - 3.14 + AR1[dB] + G_{LEC\text{-}RI}[dB] - 20*\log_{10}(\pi/2)$

$S_{R,LEC\text{-}POWR}[dBm0]$: Minimum Power Detection Level for Line Echo Cancellation at digital input

AR1[dB]: The exact value for AR1 is shown in the DuSLICOS result file; approximate value AR1 $\approx$ L_R for $L_R \leq -2$ dBr, AR1 $\approx$ –2 dB for $L_R > -2$ dBr.

$POWR = (6.02 \times 16 + Pow_{LECR}[dB]) \times 2/(5 \times \log_{10}2)$
$= (96.32 + Pow_{LECR}[dB]) \times 1.329$

$-96\ dB \leq Pow_{LECR} \leq 0\ dB$

Table 51 Range of Pow_{LECR}

POWR	Pow_{LECR}[dB]
0x00	–96
…	
0x7F	0

Example:

AR1 = –3 dB

$S_{R,LEC\text{-}POWR}$ = –40 dBm0

Pow_{LECR} = –46.14 dB

POWR = 66.69 $\approx$ 67 = 0x43

$3B_H$	**NLP-SD-LEV-R**	NLP Speech Detection Receive Direction Level			**Y**

Bit	7	6	5	4	3	2	1	0
	SD-LEV-R							

NLP Speech Detection Receive Direction Level:

If the receive signal level is below $S_{SD\text{-}LEV\text{-}R}$, the receive speech detector doesn't detect speech. The transmit and receive speech detectors are used for detecting double talk.

$SD\text{-}LEV\text{-}R = (2/(5 \times \log_{10}2)) \times (96.3 + S_{SD\text{-}LEV\text{-}R}[dB])$

$S_{SD\text{-}LEV\text{-}R} = S_R + AR1 + G_{LEC,RI}$

$-96\ dB \leq S_{SD\text{-}LEV\text{-}R} \leq 0\ dB$

Table 52 Range of $S_{SD\text{-}LEV\text{-}R}$

SD-LEV-R	**$S_{SD\text{-}LEV\text{-}R}$[dB]**
0x00	–96
…	
0x7F	0

$3C_H$	LEC-DELP	Line Echo Cancellation Delta Power			Y

Bit	7	6	5	4	3	2	1	0
	DELP							

Line Echo Cancellation Delta Power for Double Talk Detection (DTD):

$DeltaP_{LEC}[dB] = (S_R - S_X)_{DTDThr}[dB] + AR1[dB] + G_{LEC\text{-}RI}[dB] - G_{LEC\text{-}XI}[dB]$

$(S_R - S_X)_{DTDThr}[dB]$: Double Talk Detection threshold

AR1[dB]: The exact value for AR1 is shown in the DuSLICOS result file;
approximate value AR1 ≈ L_R for $L_R \leq -2$ dBr, AR1 ≈ –2 dB for $L_R > -2$ dBr.

$DELP = DeltaP_{LEC}[dB] \times 2/(5 \times \log_{10}2) = DeltaP_{LEC}[dB] \times 1.329$

$-96\ dB \leq DeltaP_{LEC} \leq 96\ dB$

Table 53 Range of $DeltaP_{LEC}$

DELP	$DeltaP_{LEC}$[dB]
0x81	–96
0x80	no detection
…	
0x7F	96

Example:

AR1 = –3 dB

expected echo signal < –15 dB → $(S_R - S_X)_{DTDThr}$ = –15 dB

$DeltaP_{LEC}$ = 12 dB

DELP = 16 = 0x10

$3C_H$	**NLP-SD-LEV-BN**	NLP Speech Detection Receive BN Level			**Y**

Bit	7	6	5	4	3	2	1	0
	SD-LEV-BN							

NLP Speech Detection Background Noise Level:

As a condition for valid speech detection in transmit direction, the transmit signal level S_X has to be higher than the estimated background noise plus $Delta_{SD\text{-}LEV\text{-}BN}$.
For other conditions see SD-LEV-X on **Page 230** and SD-LEV-RE on **Page 236**.

SD-LEV-BN = $(2/(5 \times \log_{10}2)) \times Delta_{SD\text{-}LEV\text{-}BN}[dB])$

0 dB $\leq Delta_{SD\text{-}LEV\text{-}BN} \leq$96 dB

Table 54 Range of $Delta_{SD\text{-}LEV\text{-}BN}$

SD-LEV-BN	**$Delta_{SD\text{-}LEV\text{-}BN}$[dB]**
0x00	0
…	
0x7F	96

$3D_H$	LEC-DELQ	Line Echo Cancellation Delta Quality			Y

Bit	7	6	5	4	3	2	1	0
	DELQ							

Line Echo Cancellation Delta Quality Between Shadow Filter and Main Filter:

The higher DeltaQ is, the less copying between shadow filter and main filter takes place and the higher is the quality.

DELQ = DeltaQ[dB] $\times$ 2/(5 $\times$ $\log_{10}2$) = DeltaQ[dB] $\times$ 1.329

0 dB $\leq$DeltaQ $\leq$10 dB

Table 55 Examples for DeltaQ

DELQ	DeltaQ[dB]
0x08	6.02
0x04	3.01 (typical)
0x03	2.26
0x02	1.505

$3D_H$	**NLP-SD-LEV-RE**	NLP Speech Detection Receive RE Level			**Y**

Bit	7	6	5	4	3	2	1	0
	SD-LEV-RE							

NLP Speech Detection Residual Echo Level:

As a condition for valid speech detection in transmit direction, the transmit signal level S_X has to be higher than the estimated residual echo plus $Delta_{SD\text{-}LEV\text{-}RE}$. Therefore, SD-LEV-RE prevents false decisions of the speech detector. A false decision can be a too optimistic estimation for the LEC echo return loss. Due to the hangover time for double talk (see SD-OT-DT on **Page 238**), this level should be higher than the control level residual echo coefficient (see CT-LEV-RE on **Page 243**).
For other valid speech detection conditions see SD-LEV-X on **Page 230** and SD-LEV-BN on **Page 234**.

$SD\text{-}LEV\text{-}RE = (2/(5 \times \log_{10}2)) \times Delta_{SD\text{-}LEV\text{-}RE}[dB])$

$0\ dB \leq Delta_{SD\text{-}LEV\text{-}RE} \leq 96\ dB$

Table 56 Range of $Delta_{SD\text{-}LEV\text{-}RE}$

SD-LEV-RE	**$Delta_{SD\text{-}LEV\text{-}RE}$[dB]**
0x00	0
…	
0x7F	96

$3E_H$	LEC-GAIN-XI	Line Echo Cancellation Input Gain Transmit			Y

Bit	7	6	5	4	3	2	1	0
	e			m				

Line Echo Cancellation Input Gain Transmit:
It is important, that $G_{LEC\text{-}XI}$[dB] will not be changed, so $G_{LEC\text{-}XI}$[dB] = $-G_{LEC\text{-}X0}$[dB]

$G_{LEC\text{-}XI}[dB] = 20 \times \log_{10}16 + 20 \times \log_{10}[g/32768] \approx 24.08 + 20 \times \log_{10}[g/32768]$

$-24.08\ dB \leq G_{LEC\text{-}XI} \leq 23.95\ dB$

with

$g = 2^{9-e} \times (32 + m)$ and

$0 \leq m \leq 31,\ 0 \leq e \leq 7$

Table 57 Ranges of $G_{LEC\text{-}XI}$[dB] Dependent on "e"

e	Input Gain $G_{LEC\text{-}XI}$[dB] Range
0	$23.95\ dB \geq G_{LEC\text{-}XI} \geq 18.06\ dB$
1	$17.93\ dB \geq G_{LEC\text{-}XI} \geq 12.04\ dB$
7	$-18.20\ dB \geq G_{LEC\text{-}XI} \geq -24.08\ dB$

Alternative representation:

Choose "e" as the next integer number which is bigger than or equal to:

$$e \geq 3 - \log_2 G_{LEC-XI} = 3 - \frac{\log_{10} G_{LEC-XI}}{\log_{10} 2} \approx 3 - \frac{G_{LEC-XI}[dB]}{6.02}$$

$$m = G_{LEC-XI} \times 2^{2+e} - 32 = 10^{\frac{G_{LEC-XI}[dB]}{20}} \times 2^{2+e} - 32$$

Table 58 Example for LEC-GAIN-XI Calculation

$G_{LEC\text{-}XI}$[dB]	$G_{LEC\text{-}XI}$	e	m	LEC-GAIN-XI
0	1	3	0	0x60
–6.02	0.5	4	0	0x80
6.02	2	2	0	0x40

$3E_H$	**NLP-SD-OT-DT**	NLP Speech Detection Overhang Time for Double Talk			**Y**

Bit	7	6	5	4	3	2	1	0
	SD-OT-DT							

NLP Speech Detection Overhang Time for Double Talk:

Double talk exists, when speech is detected at the same time by the receive and the transmit speech detector. In that case, the NLP will be bypassed. To make sure that the silent end of a speech signal can pass the NLP, the bypass is extended by the overhang time $t_{SD\text{-}OT\text{-}DT}$.

SD-OT-DT = 0.5 × $t_{SD\text{-}OT\text{-}DT}$[ms]

2 ms ≤$t_{SD\text{-}OT\text{-}DT}$ ≤500 ms

Table 59 Range of $t_{SD\text{-}OT\text{-}DT}$

SD-OT-DT	**$t_{SD\text{-}OT\text{-}DT}$[ms]**
0x01	2
…	
0xFA	500

$3F_H$	LEC-GAIN-RI	Line Echo Cancellation Input Gain Receive			Y

Bit	7	6	5	4	3	2	1	0
	e			m				

Line Echo Cancellation Input Gain Receive:

$G_{LEC\text{-}RI}[dB] = 20 \times \log_{10}16 + 20 \times \log_{10}[g/32768] \approx 24.08 + 20 \times \log_{10}[g/32768]$

$-24.08\ dB \leq G_{LEC\text{-}RI} \leq 23.95\ dB$

with

$g = 2^{9-e} \times (32 + m)$ and

$0 \leq m \leq 31,\ 0 \leq e \leq 7$

Table 60 Ranges of $G_{LEC\text{-}RI}[dB]$ Dependent on "e"

e	Input Gain $G_{LEC\text{-}RI}[dB]$ Range
0	$23.95\ dB \geq G_{LEC\text{-}RI} \geq 18.06\ dB$
1	$17.93\ dB \geq G_{LEC\text{-}RI} \geq 12.04\ dB$
7	$-18.20\ dB \geq G_{LEC\text{-}RI} \geq -24.08\ dB$

Alternative representation:

Choose "e" as the next integer number which is bigger than or equal to:

$$e \geq 3 - \log_2 G_{LEC-RI} = 3 - \frac{\log_{10} G_{LEC-RI}}{\log_{10} 2} \approx 3 - \frac{G_{LEC-RI}[dB]}{6.02}$$

$$m = G_{LEC-RI} \times 2^{2+e} - 32 = 10^{\frac{G_{LEC-RI}[dB]}{20}} \times 2^{2+e} - 32$$

Table 61 Example for LEC-GAIN-RI Calculation

$G_{LEC\text{-}RI}[dB]$	$G_{LEC\text{-}RI}$	e	m	LEC-GAIN-RI
0	1	3	0	0x60
–6.02	0.5	4	0	0x80
6.02	2	2	0	0x40

$3F_H$	**NLP-ERL-LIN-LP**	NLP Echo Return Loss Line LP Time Constant			**Y**

Bit	7	6	5	4	3	2	1	0
	ERL-LIN-LP							

NLP Echo Return Loss Line Low Pass Time Constant:

$T_{ERL\text{-}LIN\text{-}LP}$ is a time constant for the hybrid echo return estimation.

ERL-LIN-LP = 16384/$T_{ERL\text{-}LIN\text{-}LP}$[ms]

64.25 ms ≤$T_{ERL\text{-}LIN\text{-}LP}$ ≤16.384 s

Table 62 Range of $T_{ERL\text{-}LIN\text{-}LP}$

ERL-LIN-LP	$T_{ERL\text{-}LIN\text{-}LP}$[ms]
0xFF	64.25
…	
0x01	16384

40_H	LEC-GAIN-XO	Line Echo Cancellation Output Gain Transmit			Y

Bit	7	6	5	4	3	2	1	0
	e			m				

Line Echo Cancellation Output Gain Transmit:

It is important, that $G_{LEC\text{-}X0}$[dB] will not be changed, so $G_{LEC\text{-}X0}$[dB] = $-G_{LEC\text{-}XI}$[dB]

$G_{LEC\text{-}X0}[dB] = 20 \times \log_{10}16 + 20 \times \log_{10}[g/32768] \approx 24.08 + 20 \times \log_{10}[g/32768]$

$-24.08\ dB \leq G_{LEC\text{-}X0} \leq 23.95\ dB$

with

$g = 2^{9-e} \times (32 + m)$ and

$0 \leq m \leq 31,\ 0 \leq e \leq 7$

Table 63 Ranges of $G_{LEC\text{-}X0}$[dB] Dependent on "e"

e	Output Gain $G_{LEC\text{-}X0}$[dB] Range
0	$23.95\ dB \geq G_{LEC\text{-}X0} \geq 18.06\ dB$
1	$17.93\ dB \geq G_{LEC\text{-}X0} \geq 12.04\ dB$
7	$-18.20\ dB \geq G_{LEC\text{-}X0} \geq -24.08\ dB$

Alternative representation:

Choose "e" as the next integer number which is bigger than or equal to:

$$e \geq 3 - \log_2 G_{LEC-X0} = 3 - \frac{\log_{10} G_{LEC-X0}}{\log_{10} 2} \approx 3 - \frac{G_{LEC-X0}[dB]}{6.02}$$

$$m = G_{LEC-X0} \times 2^{2+e} - 32 = 10^{\frac{G_{LEC-X0}[dB]}{20}} \times 2^{2+e} - 32$$

Table 64 Example for LEC-GAIN-X0 Calculation

$G_{LEC\text{-}X0}$[dB]	$G_{LEC\text{-}X0}$	e	m	LEC-GAIN-X0
0	1	3	0	0x60
–6.02	0.5	4	0	0x80
6.02	2	2	0	0x40

40_H	**NLP-ERL-LEC-LP**	NLP Echo Return Loss LEC LP Time Constant			**Y**

Bit	7	6	5	4	3	2	1	0
	ERL-LEC-LP							

NLP Echo Return Loss LEC Low Pass Time Constant:

$T_{ERL-LEC-LP}$ is a time constant for the LEC echo return estimation.

ERL-LEC-LP = 16384/$T_{ERL-LEC-LP}$[ms]

64.25 ms ≤$T_{ERL-LEC-LP}$ ≤16.384 s

Table 65 Range of $T_{ERL-LEC-LP}$

ERL-LEC-LP	$T_{ERL-LEC-LP}$[ms]
0xFF	64.25
…	
0x01	16384

41_H	**NLP-CT-LEV-RE**	NLP Control RE Level			**Y**

Bit	7	6	5	4	3	2	1	0
	CT-LEV-RE							

NLP Control Level Residual Echo:

If the speech level after the LEC is above the estimated residual echo plus $Delta_{CT\text{-}LEV\text{-}RE}$, the NLP is inactive (bypassed). Otherwise the NLP is active, when there is no double talk.

$CT\text{-}LEV\text{-}RE = (2/(5 \times \log_{10}2)) \times Delta_{CT\text{-}LEV\text{-}RE}[dB])$

$0\ dB \leq Delta_{CT\text{-}LEV\text{-}RE} \leq 96\ dB$

Table 66 Range of $Delta_{CT\text{-}LEV\text{-}RE}$

CT-LEV-RE	**$Delta_{CT\text{-}LEV\text{-}RE}$[dB]**
0x00	0
…	
0x7F	96

42_H	**NLP-CTRL**	NLP Control			**Y**

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**0**	**0**	**NLP-NM**	**NLP-NG**	**NLP-OLDC**

NLP-NM When the echo path is cut of by the NLP, there are two possible ways to add a comfort noise to the line. This ensures that the subscriber doesn´t assume a dead line.

NLP-NM = 0 White noise is selected.

NLP-NM = 1 Sign noise (spectrum shaped noise) is selected.

NLP-NG

NLP-NG = 0 The noise generator is off.

NLP-NG = 1 The noise generator is active.

NLP-OLDC

NLP-OLDC = 0 After the activation of the NLP the coefficients are copied from the I/O-buffer to the local RAM.

NLP-OLDC = 1 The NLP uses the old coefficients.

43_H	CIS-LEV-H	Caller ID Sender Level High Byte			Y

Bit	7	6	5	4	3	2	1	0
	LEV-H							

44_H	CIS-LEV-L	Caller ID Sender Level Low Byte			Y

Bit	7	6	5	4	3	2	1	0
	LEV-L							

Caller ID Sender Level:

$Lev_{CIS}[dB] = Lev_{CIS}[dBm0] – 3.14 – 3.37$

$Lev_{CIS}[dB] = Lev_{CIS}[dBm] – L_R[dBr] – 3.14 – 3.37$

$LEV = 32767 \times 10^{(Lev_{CIS}[dB]/20)}$

$–90.31\ dB \leq Lev_{CIS} \leq 0\ dB$

LEV-L = MOD (LEV,256)

LEV-H = INT (LEV/256)

Table 67 Range of Lev_{CIS}

LEV	Lev_{CIS}[dB]
0	$-\infty$ (signal off)
1	–90.31
32767	0

45_H	CIS-BRS	Caller ID Sender Buffer Request Size			Y

Bit	7	6	5	4	3	2	1	0
	BRS							

Caller ID Sender Buffer Request Size:

0 ≤BRS ≤46

CIS-BRS is a threshold to be set within the Caller ID sender buffer (CIS-DAT, 48 bytes).

If the number of bytes in the CID sender buffer falls below the buffer request size, an interrupt is generated. This is the indication to fill up the buffer again.

The first bit will be sent if the number of bytes in the CID sender buffer exceeds the buffer request size (start sending with BRS + 1 number of bytes).

The buffer request size BRS must always be smaller than the number of bytes to be sent:

BRS < Number of bytes to be sent

Typical values: 10 - 30.

46_H	**CIS-SEIZ-H**	Caller ID Sender Number of Seizure Bits High Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	SEIZ-H							

47_H	**CIS-SEIZ-L**	Caller ID Sender Number of Seizure Bits Low Byte			**Y**

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	SEIZ-L							

Caller ID Sender Number of Seizure Bits:
(only if High Level Framing is selected in the CIS/LEC-MODE register (see **Page 248**))

0 ≤SEIZ ≤32767

SEIZ-L = MOD (SEIZ,256)

SEIZ-H = INT (SEIZ/256)

48_H	**CIS-MARK-H**	Caller ID Sender Number of Mark Bits High Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	MARK-H							

49_H	**CIS-MARK-L**	Caller ID Sender Number of Mark Bits Low Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	MARK-L							

Caller ID Sender Number of Mark Bits:
(only if High Level Framing is selected in the CIS/LEC-MODE register)

$0 \leq MARK \leq 32767$

MARK-L = MOD (MARK,256)

MARK-H = INT (MARK/256)

$4A_H$	**CIS/LEC-MODE**	CIS/LEC Mode Setting			**Y**

Bit	7	6	5	4	3	2	1	0
	LEC-ADAPT	**LEC-FREEZE**	**UTDX-SUM**	**UTDR-SUM**	**0**	**NLP-EN**	**CIS-FRM**	**CIS-V23**

Attention: Bit 3 must be set to 0.

LEC-ADAPT Line Echo Cancellation Adaptation Start. The LEC-ADAPT bit is only evaluated if the LEC-EN is changed from 0 to 1.

To initialize the LEC coefficients to 0 requires the LEC-ADAPT bit set to 0 followed by the LEC-EN bit changed from 0 to 1.

It is not possible to reset the LEC coefficients to 0 while the LEC is running. The LEC has to be disabled first by setting bit LEC-EN to 0 and then it is necessary to enable the LEC again (LEC-EN = 1, LEC-ADAPT = 0). If valid coefficients from a former LEC adaptation are present in the RAM, it is possible to activate the LEC with this coefficents by setting bit LEC-ADAPT to 1.

It is also possible to read out adapted coefficients from the LEC for external storage and to reuse these coefficients as a start up value for the next connection (see the available Application Notes).

LEC-ADAPT = 0 Line Echo Cancellation coefficients initialized with zero.

LEC-ADAPT = 1 Line Echo Cancellation coefficients initialized with old coefficients.

LEC-FREEZE Line Echo Cancellation Adaptation Freeze

LEC-FREEZE = 0 No freezing of coefficients

LEC-FREEZE = 1 Freezing of coefficients

CIS-FRM Caller ID Sender Framing

CIS-FRM = 0 Low-level framing: all data for CID transmissions must be written to the CID Buffer including channel seizure and mark sequence, start and stop bits.

CIS-FRM = 1 High-level framing: channel seizure and mark sequence as well as start and stop bits are automatically inserted by the SLICOFI-2x. Only transmission bytes from the Data Packet (see **Figure 30**) have to be written to the CIS buffer.

CIS-V23 Caller ID Sender Mode

CIS-V23 = 0 Bell 202 selected

CIS-V23 = 1 V.23 selected

$4B_H$	**UTD-CF-H**	Universal Tone Detection Center Frequency High Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	CF-H							

$4C_H$	**UTD-CF-L**	Universal Tone Detection Center Frequency Low Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	CF-L							

Universal Tone Detection Center Frequency:

$$CF = 32768 \times \cos\left(\frac{2\pi f_c[Hz]}{8000}\right)$$

$0 < f_C < 4000$ Hz

CF-L = MOD (CF,256)

CF-H = INT (CF/256)

$4D_H$	**UTD-BW-H**	Universal Tone Detection Bandwidth High Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	BW-H							

$4E_H$	**UTD-BW-L**	Universal Tone Detection Bandwidth Low Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	BW-L							

Universal Tone Detection Bandwidth:

$$BW = 65536 \times \frac{a}{1 + a}$$

with

$$a = \tan\left(\frac{f_{BW}[Hz] \times \pi}{8000}\right)$$

$0 < f_{BW} < 2000$ Hz

BW-L = MOD (BW,256)

BW-H = INT (BW/256)

$4F_H$	**UTD-NLEV**	Universal Tone Detection Noise Level			**Y**

Bit	7	6	5	4	3	2	1	0
	NLEV							

Universal Tone Detection Noise Level:

$NLEV = 32768 \times 10^{(Lev_N[dB])/20}$

$-96\ dB \leq Lev_N \leq -42.18\ dB$

50_H	**UTD-SLEV-H**	Universal Tone Detection Signal Level High Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	SLEV-H							

51_H	**UTD-SLEV-L**	Universal Tone Detection Signal Level Low Byte			**Y**

Bit	7	6	5	4	3	2	1	0
	SLEV-L							

Universal Tone Detection Signal Level:

Calculation for Transmit:

$Lev_S[dB] = Lev_S[dBm0] - 3.14 - 20*\log_{10}(\pi/2)$

$Lev_S[dB] = Lev_S[dBm] - L_x[dBr] - 3.14 - 20*\log_{10}(\pi/2)$

Calculation for Receive:

$Lev_S[dB] = Lev_S[dBm0] - 3.14 + AR1[dB] - 20*\log_{10}(\pi/2)$

$Lev_S[dB] = Lev_S[dBm] - L_R[dBr] - 3.14 + AR1[dB] - 20*\log_{10}(\pi/2)$

AR1[dB]: The exact value for AR1 is shown in the DuSLICOS result file; approximate value AR1 $\approx$ L_R for $L_R \leq -2$ dBr, AR1 $\approx$ –2 dB for $L_R > -2$ dBr.

$SLEV = 32768 \times 10^{(Lev_S[dB])/20} - NLEV$

$-96 \text{ dB} \leq Lev_S \leq 0 \text{ dB}$

Signal Level:

SLEV-L = MOD (SLEV,256)

SLEV-H = INT (SLEV/256)

UTD for Receive and Transmit:

By enabling the UTD, the coefficients in the UTD registers are copied to the main memory. Therefore, different coefficients can be set for receive and transmit direction.

52_H	UTD-DELT	Universal Tone Detection Delta			Y

Bit	7	6	5	4	3	2	1	0
	DELT							

Universal Tone Detection Delta Inband/Outband:

$DELT = Sign(Delta_{UTD}) \times 128 \times 10^{-|Delta_{UTD}[dB]|/20}$

$-42\ dB \leq Delta_{UTD} \leq 42\ dB$

Example:

Detection of a tone that is between 1975 Hz and 2025 Hz $\rightarrow f_C$ = 2000 Hz

- f_{BW} = 50 Hz
  Tone at 2025 Hz: Outband = –3 dB, Inband = –3 dB (see **Table 68**)
  $Delta_{UTD}$ = 0 dB →DELT = 128 = 0x80
- f_{BW} = 500 Hz
  Tone at 2025 Hz: Outband = –20 dB, Inband = –0.04 dB (see **Table 68**)
  $Delta_{UTD} \approx$ 20 dB →DELT = 13 = 0x0D

Table 68 UTD Inband/Outband Attenuation

f	Outband	Inband
$f_C \pm f_{BW}/0.2$	–0.04 dB	–20 dB
$f_C \pm f_{BW}/2$	–3 dB	–3 dB
$f_C \pm f_{BW}/20$	–20 dB	–0.04 dB
$f_C \pm f_{BW}/200$	–40 dB	–0 dB

53_H	**UTD-RBRK**	Universal Tone Detection Recognition Break Time			**Y**

Bit	7	6	5	4	3	2	1	0
	RBRK							

Allowed Recognition Break Time for Universal Tone Detection:

RBRK = RBRKTime[ms]/4

RBRKTime must be entered in multiples of 4 ms.

0 ms ≤RBRKTime ≤1000 ms

For an example, see **Figure 64**.

54_H	**UTD-RTIME**	Universal Tone Detection Recognition Time			**Y**

Bit	7	6	5	4	3	2	1	0
	RTIME							

Universal Tone Detection Recognition Time:

RTIME = RTime[ms]/16

RTime must be entered in multiples of 16 ms.

0 ms ≤RTime ≤4000 ms

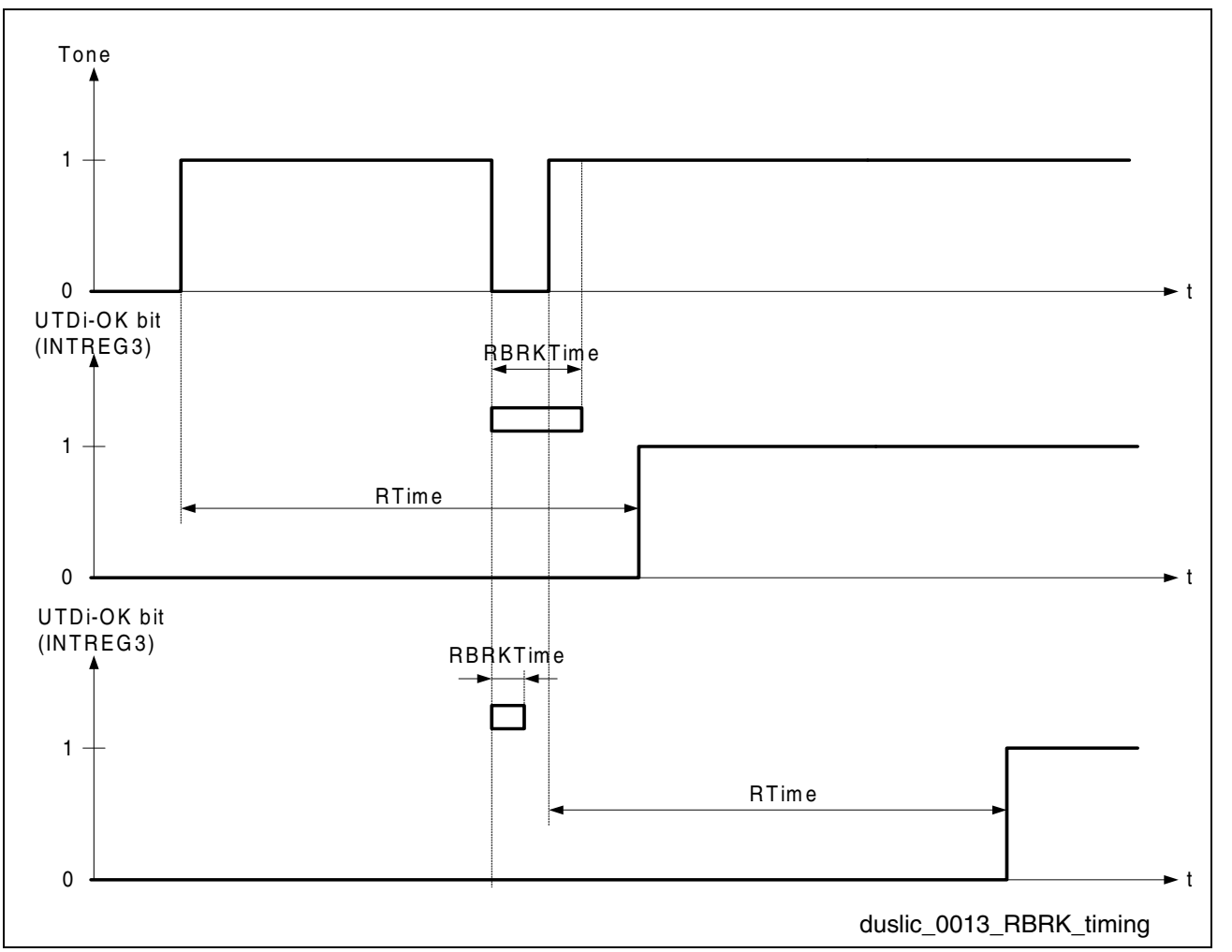


Figure 64 Example for UTD Recognition Timing

55_H	**UTD-EBRK**	UTD Allowed Tone End Detection Break Time			**Y**

Bit	7	6	5	4	3	2	1	0
	EBRK							

Allowed tone end detection break time for Universal Tone Detection:

EBRK = EBRKTime [ms]

0 ms ≤EBRKTime ≤255 ms

For an example, see **Figure 65**.

56_H	UTD-ETIME	UTD Tone End Detection Time			Y

Bit	7	6	5	4	3	2	1	0
	ETIME							

Tone End Detection Time for Universal Tone Detection:

ETIME = ETime[ms]/4

ETime must be entered in multiples of 4 ms.

0 ms ≤ETime ≤1000 ms

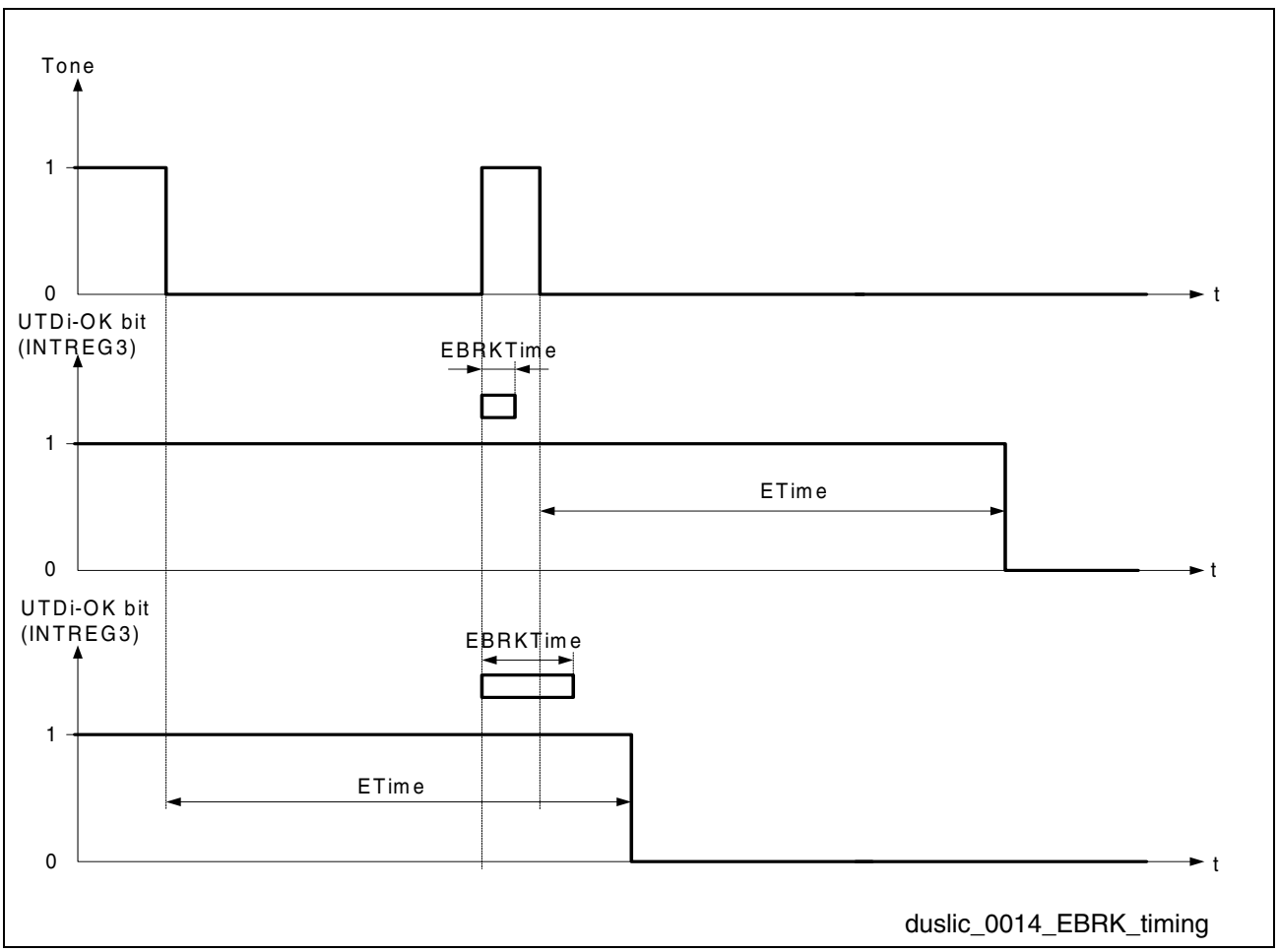


Figure 65 Example for UTD Tone End Detection Timing

5.2.3.4 Recommended NLP Coefficients

Table 69 shows recommended NLP register values and the respective parameter values.

Table 69 Recommended NLP Coefficients

Register Name	Register Value	Parameter Value
NLP-POW-LPF	0x6A	$T_{POW-LPF}$ = 2.4 msec
NLP-POW-LPS	0x2A	$T_{POW-LPS}$ = 24.4 msec
NLP-BN-LEV-X	0x44	$Pow_{BN-LEV-X}$ = –45.1 dB
NLP-BN-LEV-R	0x44	$Pow_{BN-LEV-R}$ = –45.1 dB
NLP-BN-INC	0x10	T_{BN-INC} = 23.5 dB/sec
NLP-BN-DEC	0x40	T_{BN-DEC} = 94.1 dB/sec
NLP-BN-MAX	0x40	Pow_{BN-MAX} = –48.0 dB
NLP-BN-ADJ	0x04	$Delta_{BN-ADJ}$ = 3.0 dB
NLP-RE-MIN-ERLL	0x10	$ERLL_{RE-MIN}$ = 12.0 dB
NLP-RE-EST-ERLL	0x0C	$ERLL_{RE-EST}$ = 9.0 dB
NLP-SD-LEV-X	0x44	$S_{SD-LEV-X}$ = –45.1 dB
NLP-SD-LEV-R	0x44	$S_{SD-LEV-R}$ = –45.1 dB
NLP-SD-LEV-BN	0x0C	$Delta_{SD-LEV-BN}$ = 9.0 dB
NLP-SD-LEV-RE	0x10	$Delta_{SD-LEV-RE}$ = 12.0 dB
NLP-SD-OT-DT	0x3C	$t_{SD-OT-DT}$ = 120.0 msec
NLP-ERL-LIN-LP	0x20	$T_{ERL-LIN-LP}$ = 512.0 msec
NLP-ERL-LEC-LP	0x10	$T_{ERL-LEC-LP}$ = 1024.0 msec
NLP-CT-LEV-RE	0x0C	$Delta_{CT-LEV-RE}$ = 9.0 dB

5.2.4 IOM-2 Interface Command/Indication Byte

The Command/Indication (C/I) channel is used to communicate real time status information and for fast controlling of the DuSLIC. Data on the C/I channel are continuously transmitted in each frame until new data are sent.

Data Downstream C/I – Channel Byte (Receive) – IOM-CIDD

The first six CIDD data bits control the general operating modes for both DuSLIC channels. According to the IOM-2 specifications, new data must be present for at least two frames to be accepted.

Table 70 M2, M1, M0: General Operating Mode

CIDD			SLICOFI-2 Operating Mode (for details see “Overview of all DuSLIC Operating Modes” on Page 74)
M2	M1	M0	
1	1	1	Sleep, Power Down (PDRx)
0	0	0	Power Down High Impedance (PDH)
0	1	0	Any Active mode
1	0	1	Ringing (ACTR Burst On)
1	1	0	Active with Metering
1	0	0	Ground Start
0	0	1	Ring Pause

	CIDD	Data Downstream C/I – Channel Byte			N

Bit	7	6	5	4	3	2	1	0
	M2A	M1A	M0A	M2B	M1B	M0B	MR	MX

M2A, M1A, M0A Select operating mode for DuSLIC channel A

M2B, M1B, M0B Select operating mode for DuSLIC channel B

MR, MX Handshake bits Monitor Receive and Transmit (see “IOM-2 Interface Monitor Transfer Protocol” on Page 133)

Data Upstream C/I – Channel Byte (Transmit) – IOM-CIDU

This byte is used to quickly transfer the most important and time-critical information from the DuSLIC. Each transfer from the DuSLIC lasts for at least 2 consecutive frames.

	CIDU	Data Upstream C/I – Channel Byte	00_H		N

Bit	7	6	5	4	3	2	1	0
	INT-CHA	HOOKA	GNDKA	INT-CHB	HOOKB	GNDKB	MR	MX

INT-CHA Interrupt information channel A
INT-CHA = 0 No interrupt in channel A
INT-CHA = 1 Interrupt in channel A

HOOKA Hook information channel A
HOOKA = 0 On-hook channel A
HOOKA = 1 Off-hook channel A

GNDKA Ground key information channel A
GNDKA = 0 No longitudinal current detected
GNDKA = 1 Longitudinal current detected in channel A

INT-CHB Interrupt information channel B
INT-CHB = 0 No interrupt in channel B
INT-CHB = 1 Interrupt in channel B

HOOKB Hook information channel B
HOOKB = 0 On-hook Channel B
HOOKB = 1 Off-hook Channel B

GNDKB Ground key information channel B
GNDKB = 0 No longitudinal current detected
GNDKB = 1 Longitudinal current detected in channel B

MR, MX Handshake bits Monitor Receive and Transmit
(see **“IOM-2 Interface Monitor Transfer Protocol” on Page 133**)

5.2.5 Programming Examples of the SLICOFI-2

5.2.5.1 Microcontroller Interface

SOP Write to Channel 0 Starting After the Channel Specific Read-only Registers

01000100	First command byte (SOP write for channel 0)
00010101	Second command byte (Offset to BCR1 register)
00000000	Contents of BCR1 register
00000000	Contents of BCR2 register
00010001	Contents of BCR3 register
00000000	Contents of BCR4 register
00000000	Contents of BCR5 register

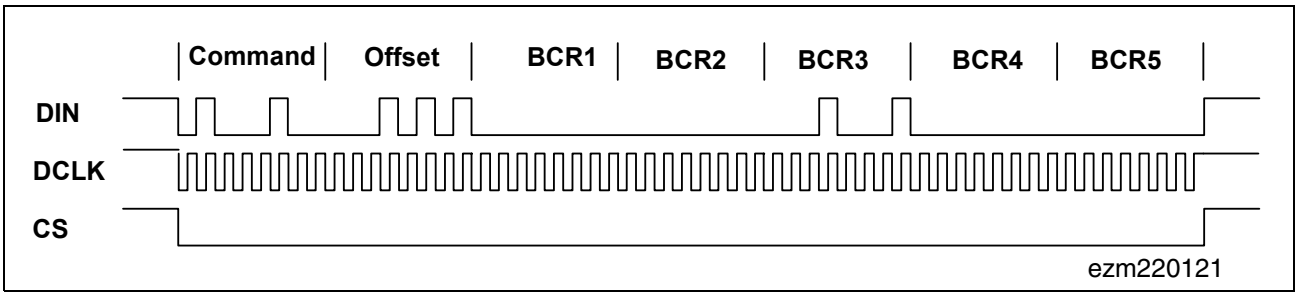


Figure 66 Waveform of Programming Example SOP-Write to Channel 0

SOP Read from Channel 1 Reading Out the Interrupt Registers

11001100	First command byte (SOP read for channel 1).
00000111	Second command byte (Offset to Interrupt register 1).

The SLICOFI-2 will send data when it has completely received the second command byte.

11111111	Dump byte (This byte is always FF_H).
11000000	Interrupt register INTREG1 (An interrupt has occurred, Off-hook was detected).
00000010	Interrupt register INTREG2 (I/O pin 2 is ‘1’).
00000000	Interrupt register INTREG3
00000000	Interrupt register INTREG4

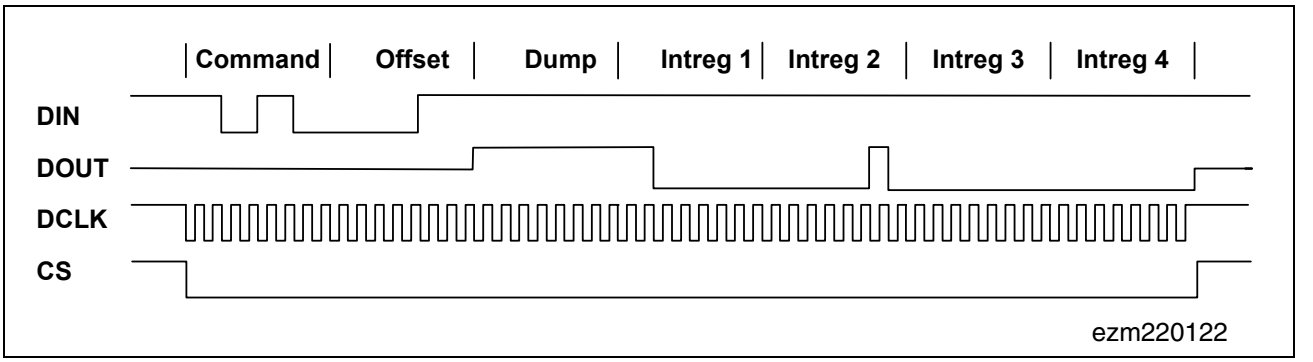


Figure 67 Waveform of Programming Example SOP Read from Channel 0

5.2.5.2 IOM-2 Interface

An example with the same programming sequence as before, using the IOM-2 interface is presented here to show the differences between the microcontroller interface and the IOM-2 interface.

SOP Write to Channel 0 Starting After the Channel-Specific Read-only Registers

Monitor data down	MR/MX	Monitor data up	MR/MX	Comment
10000001	10	11111111	01	IOM-2 address second byte
01000100	11	11111111	01	First command byte (SOP write for channel 0)
01000100	10	11111111	11	First command byte second time
00010101	11	11111111	01	Second command byte (Offset to BCR1 register)
00010101	10	11111111	11	Second command byte second time
00000000	11	11111111	01	Contents of BCR1 register
00000000	10	11111111	11	Contents of BCR1 register second time
00000000	11	11111111	01	Contents of BCR2 register
00000000	10	11111111	11	Contents of BCR2 register second time
00010001	11	11111111	01	Contents of BCR3 register
00010001	10	11111111	11	Contents of BCR3 register second time
00000000	11	11111111	01	Contents of BCR4 register
00000000	10	11111111	11	Contents of BCR4 register second time
11111111	11	11111111	01	No more information (dummy byte)
11111111	11	11111111	11	Signaling EOM (end of message) by holding MX bit at ‘1’.

Because the SLICOFI-2 has an open command structure, there is no fixed command length. The IOM-2 handshake protocol allows for an infinite length of a data stream. Therefore, the host must terminate the data transfer by sending an end-of-message signal (EOM) to the SLICOFI-2. The SLICOFI-2 will abort the transfer only if the host tries to write or read beyond the allowed maximum offset given by the different types of commands. Each transfer must start with the SLICOFI-2-specific IOM-2 address (81_H)

and must end with an EOM of the handshake bits. Appending a command immediately to its predecessor without an EOM in between is not allowed.

When reading interrupt registers, SLICOFI-2 stops the transfer after the fourth register in IOM-2 mode. This is to prevent some host chips from reading 16 bytes because they cannot terminate the transfer after n bytes.

SOP-Read from Channel 1 Reading Out the Interrupt Registers

Monitor data down	MR/MX	Monitor data up	MR/MX	Comment
10000001	10	1111111111		IOM-2 address first byte
10000001	10	1111111101		IOM-2 address second byte
11001100	11	1111111101		First command byte (SOP read for channel 1)
11001100	10	1111111111		First command byte second time
00001000	11	1111111101		Second command byte (offset to interrupt register 1)
00001000	10	1111111111		Second command byte second time
11111111	11	1111111101		Acknowledgement for the second command byte
11111111	11	1000000110		IOM-2 Address first byte (answer)
11111111	01	1000000110		IOM-2 Address second byte
11111111	01	1100000011		Interrupt register INTREG1
11111111	11	1100000010		Interrupt register INTREG1 second time
11111111	01	0000001011		Interrupt register INTREG2
11111111	11	0000001010		Interrupt register INTREG2 second time
11111111	01	0000000011		Interrupt register INTREG3
11111111	11	0000000010		Interrupt register INTREG3 second time
11111111	01	0000000011		Interrupt register INTREG4
11111111	11	0000000010		Interrupt register INTREG4 second time
11111111	11	0100110111		SLICOFI-2 sends the next register
11111111	11	1111111111		SLICOFI-2 aborts transmission

5.3 SLICOFI-2S Command Structure and Programming

This section describes only the SLICOFI-2S PEB 3264 command structure and programming. Therefore, this section pertains only to the DuSLIC-S and DuSLIC-S2 chip sets.

5.3.1 SOP Command

The Status Operation (SOP) command provides access to the configuration and status registers of the SLICOFI-2S. Common registers change the mode of the entire SLICOFI-2S chip. All other registers are channel-specific. It is possible to access single or multiple registers. Multiple register access is achieved by an automatic offset increment. Write access to read-only registers is ignored and does not abort the command sequence. Offsets may change in future versions of the SLICOFI-2S.

Attention: To ensure proper functionality, it is essential that all unused register bits have to be filled with zeros.

5.3.1.1 SOP Register Overview

00_H REVISION — Revision Number (read-only)

REV[7:0]

01_H CHIPID 1 — Chip Identification 1 (read-only)

for internal use only

02_H CHIPID 2 — Chip Identification 2 (read-only)

for internal use only

03_H CHIPID 3 — Chip Identification 3 (read-only)

for internal use only

04_H FUSE1 — Fuse Register 1

for internal use only

05_H PCMC1 — PCM Configuration Register 1

DBL-CLK	X-SLOPE	R-SLOPE	NO-DRIVE-0	SHIFT	PCMO[2:0]

06_H XCR Extended Configuration Register

0	ASYNCH-R	0	0	0	0	0	0

07_H INTREG1 Interrupt Register 1 (read-only)

INT-CH	HOOK	GNDK	GNKP	ICON	VTRLIM	OTEMP	SYNC-FAIL

08_H INTREG2 Interrupt Register 2 (read-only)

0	READY	RSTAT	0	IO[4:1]-DU

09_H INTREG3 Interrupt Register 3 (read-only)

0	0	0	0	0	0	0	0

$0A_H$ INTREG4 Interrupt Register 4 (read-only)

0	0	0	0	0	0	0	0

$0B_H$ CHKR1 Checksum Register 1 (High Byte) (read-only)

SUM-OK	CHKSUM-H[6:0]

$0C_H$ CHKR2 Checksum Register 2 (Low Byte) (read-only)

CHKSUM-L[7:0]

$0D_H$ LMRES1 Level Metering Result 1 (High Byte) (read-only)

LM-VAL-H[7:0]

$0E_H$ LMRES2 Level Metering Result 2 (Low Byte) (read-only)

LM-VAL-L[7:0]

$0F_H$ FUSE2 Fuse Register 2

for internal use only

10_H FUSE3 Fuse Register 3

for internal use only

11_H MASK Mask Register

READY-M	HOOK-M	GNDK-M	GNKP-M	ICON-M	VTRLIM-M	OTEMP-M	SYNC-M

12_H IOCTL1 I/O Control Register 1

IO[4:1]-INEN	IO[4:1]-M

13_H IOCTL2 I/O Control Register 2

IO[4:1]-OEN	IO[4:1]-DD

14_H IOCTL3 I/O Control Register 3

DUP[3:0]	DUP-IO[3:0]

15_H BCR1 Basic Configuration Register 1

HIR	HIT	0	REVPOL	ACTR	ACTL	SEL-SLIC[1:0]

16_H BCR2 Basic Configuration Register 2

REXT-EN	SOFT-DIS	TTX-DIS[1)]	TTX-12K[2)]	HIM-AN	AC-XGAIN	0	PDOT-DIS

17_H BCR3 Basic Configuration Register 3

MU-LAW	LIN	0	PCMX-EN	0	0	0	CRAM-EN

18_H BCR4 Basic Configuration Register 4

TH-DIS	IM-DIS	AX-DIS	AR-DIS	FRX-DIS	FRR-DIS	HPX-DIS	HPR-DIS

19_H Reserved

0	0	0	0	0	0	0	0

$1A_H$ DSCR DTMF Sender Configuration Register

DG-KEY[3:0]	COR8	PTG	TG2-EN	TG1-EN

$1B_H$ Reserved

0	0	0	0	0	0	0	0

$1C_H$ LMCR1 Level Metering Configuration Register 1

TEST-EN	LM-EN	LM-THM	PCM2DC	LM2 PCM	LM-ONCE	LM-MASK	DC-AD16

$1D_H$ LMCR2 Level Metering Configuration Register 2

LM-NOTCH	LM-FILT	LM-RECT	RAMP-EN	LM-SEL[3:0]

$1E_H$ LMCR3 Level Metering Configuration Register 3

AC-SHORT-EN	RTR-SEL	LM-ITIME[3:0]	RNG-OFFSET[1:0]

$1F_H$ OFR1 Offset Register 1 (High Byte)

OFFSET-H[7:0]

20_H OFR2 Offset Register 2 (Low Byte)

OFFSET-L[7:0]

21_H PCMR1 PCM Receive Register 1

R1-HW	R1-TS[6:0]

22_H Reserved

23_H Reserved

24_H Reserved

25_H PCMX1 PCM Transmit Register 1

X1-HW	X1-TS[6:0]

26_H Reserved

27_H Reserved

28_H Reserved

29_H TSTR1 Test Register 1

PD-AC-PR	PD-AC-PO	PD-AC-AD	PD-AC-DA	PD-AC-GN	PD-GNKC	PD-OFHC	PD-OVTC

$2A_H$ TSTR2 Test Register 2

PD-DC-PR	0	PD-DC-AD	PD-DC-DA	PD-DCBUF	0	PD-TTX-A[2)]	PD-HVI

$2B_H$ TSTR3 Test Register 3

0	0	AC-DLB-4M	AC-DLB-128K	AC-DLB-32K	AC-DLB-8K	0	0

$2C_H$ TSTR4 Test Register 4

OPIM-AN	OPIM-4M	COR-64	COX-16	0	0	0	0

$2D_H$ TSTR5 Test Register 5

0	0	0	DC-POFI-HI	DC-HOLD	0	0	0

[1)] Only for DuSLIC-S; is set to 1 for DuSLIC-S2.

[2)] Only for DuSLIC-S; is set to 0 for DuSLIC-S2.

5.3.1.2 SOP Register Description

00_H	**REVISION**	Revision Number (read-only)	**curr. rev.**		**N**

Bit	7	6	5	4	3	2	1	0
	REV[7:0]							

REV[7:0] Current revision number of the SLICOFI-2S.

01_H	**CHIPID 1**	Chip Identification 1 (read-only)	**hw**		**N**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

02_H	**CHIPID 2**	Chip Identification 2 (read-only)	**hw**		**N**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

03_H	**CHIPID 3**	Chip Identification 3 (read-only)	**hw**		**N**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

04_H	**FUSE1**	Fuse Register 1	**hw**		**N**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

05_H	PCMC1	PCM Configuration Register 1	00_H		N

Bit	7	6	5	4	3	2	1	0
	DBL-CLK	X-SLOPE	R-SLOPE	NO-DRIVE-0	SHIFT	PCMO[2:0]		

DBL-CLK Clock mode for the PCM interface (see **Figure 53** on **Page 125**).

DBL-CLK = 0 Single clocking is used.

DBL-CLK = 1 Double clocking is used.

X-SLOPE Transmit Slope (see **Figure 53** on **Page 125**).

X-SLOPE = 0 Transmission starts with rising edge of the clock.

X-SLOPE = 1 Transmission starts with falling edge of the clock.

R-SLOPE Receive Slope (see **Figure 53** on **Page 125**).

R-SLOPE = 0 Data is sampled with falling edge of the clock.

R-SLOPE = 1 Data is sampled with rising edge of the clock.

NO-DRIVE-0 Driving Mode for Bit 0 (only available in single-clocking mode).

NO-DRIVE = 0 Bit 0 is driven the entire clock period.

NO-DRIVE = 1 Bit 0 is driven during the first half of the clock period only.

SHIFT Shifts the access edges by one clock cycle in double clocking mode.

SHIFT = 0 No shift takes place.

SHIFT = 1 Shift takes place.

PCMO[2:0] All PCM timing is moved by PCMO data periods against the FSC signal.

PCMO[2:0] = 0 0 0 No offset is added.

PCMO[2:0] = 0 0 1 One data period is added.

…

PCMO[2:0] = 1 1 1 Seven data periods are added.

06_H	XCR	Extended Configuration Register	00_H		N

Bit	7	6	5	4	3	2	1	0
	0	**ASYNCH-R**	**0**	**0**	**0**	**0**	**0**	**0**

ASYNCH-R Enables asynchronous ringing in case of internal or external ringing.

ASYNCH-R = 0 Internal or external ringing with zero crossing selected

ASYNCH-R = 1 Asynchronous ringing selected.

07_H	INTREG1	Interrupt Register 1 (read-only)	80_H		Y

Bit	7	6	5	4	3	2	1	0
	INT-CH	HOOK	GNDK	GNKP	ICON	VTRLIM	OTEMP	SYNC-FAIL

INT-CH Interrupt channel bit. This bit indicates that the corresponding channel caused the last interrupt. Will be set automatically to zero after all interrupt registers have been read.

INT-CH = 0 No interrupt in corresponding channel.

INT-CH = 1 Interrupt caused by corresponding channel.

HOOK On/Off-hook information for the loop in all operating modes, filtered by DUP (Data Upstream Persistence) counter and interrupt generation masked by the HOOK-M bit. A change of this bit generates an interrupt.

HOOK = 0 On-hook.

HOOK = 1 Off-hook.

GNDK Ground key or ground start information via the IL pin in all active modes, filtered for AC suppression by the DUP counter and interrupt generation masked by the GNDK-M bit. A change of this bit generates an interrupt.

GNDK = 0 No longitudinal current detected.

GNDK = 1 Longitudinal current detected (ground key or ground start).

GNKP Ground key polarity. Indicates the active ground key level (positive/negative) interrupt generation masked by the GNKP-M bit. A change of this bit generates an interrupt. This bit can be used to obtain information about interference voltage influence.

GNKP = 0 Negative ground key threshold level active.

GNKP = 1 Positive ground key threshold level active.

ICON Constant current information. Filtered by DUP-IO counter and interrupt generation masked by the ICON-M bit. A change of this bit generates an interrupt.

ICON = 0 Resistive or constant voltage feeding.

ICON = 1 Constant current feeding.

VTRLIM Exceeding of a programmed voltage threshold for the TIP/RING voltage, filtered by the DUP-IO counter and interrupt generation masked by the VTRLIM-M bit. A change of this bit causes an interrupt.

The voltage threshold for the TIP/RING voltage is set in CRAM (calculated with DuSLICOS DC Control Parameter 2/4: Tip-Ring Threshold).

VTRLIM = 0 Voltage at Tip/Ring is below the limit.

VTRLIM = 1 Voltage at Tip/Ring is above the limit.

OTEMP Thermal overload warning from the SLIC-S/-S2 line drivers masked by the OTEMP-M bit. An interrupt is only generated if the OTEMP bit changes from 0 to1.

OTEMP = 0 Temperature at SLIC-S/-S2 is below the limit.

OTEMP = 1 Temperature at SLIC-S/-S2 is above the limit.

In case of bit PDOT-DIS = 0 (register BCR2) the DuSLIC is switched automatically into PDH mode and OTEMP is hold at 1 until the SLICOFI-2S is set to PDH by a CIOP/CIDD command.

SYNC-FAIL Failure of the synchronization of the IOM-2/PCM Interface. An interrupt is only generated if the SYNC-FAIL bit changes from 0 to 1.

Resynchronization of the PCM interface can be done with the Resynchronization command (see **Chapter 5**)

SYNC-FAIL = 0 Synchronization OK.

SYNC-FAIL = 1 Synchronization failure.

08_H	INTREG2	Interrupt Register 2 (read-only)	20_H		Y

Bit	7	6	5	4	3	2	1	0
	0	READY	RSTAT	0	IO[4:1]-DU			

After a hardware reset, the RSTAT bit is set and generates an interrupt. Therefore, the default value of INTREG2 is 20_H. After reading all four interrupt registers, the INTREG2 value changes to $4F_H$.

READY Indicates whether ramp generator has finished. An interrupt is only generated if the READY bit changes from 0 to 1. At a new start of the ramp generator, the bit is set to 0. For further information regarding soft reversal see **Chapter 2.7.2.1**.

READY = 0 Ramp generator active.

READY = 1 Ramp generator not active.

RSTAT Reset status since last interrupt.

RSTAT = 0 No reset has occurred since the last interrupt.

RSTAT = 1 Reset has occurred since the last interrupt.

IO[4:1]-DU Data on I/O pins 1 to 4 filtered by the DUP-IO counter and interrupt generation masked by the IO[4:1]-DU-M bits. A change of any of these bits generates an interrupt.

09_H	INTREG3	Interrupt Register 3 (read-only)	00_H		Y

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0

$0A_H$	INTREG4	Interrupt Register 4 (read-only)	00_H		Y

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0

$0B_H$	**CHKR1**	Checksum Register 1 (High Byte) (read-only)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	SUM-OK	**CHKSUM-H[6:0]**						

SUM-OK Information about the validity of the checksum. The checksum is valid if the internal checksum calculation is finished.

Checksum calculation:

For (cram_adr = 0 to 159) do
cram_dat = cram[cram_adr]
csum[14:0] = (csum[13:0] &[1)] '0') xor
('0000000' & cram_dat[7:0]) xor
('0000000000000' & csum[14] & csum[14])
End

SUM-OK = 0 CRAM checksum is not valid.

SUM-OK = 1 CRAM checksum is valid.

1) "&" means a concatenation; not the logic operation

CHKSUM-H[6:0] CRAM checksum High Byte

$0C_H$	**CHKR2**	Checksum Register 2 (Low Byte) (read-only)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	CHKSUM-L[7:0]							

CHKSUM-L[7:0] CRAM-checksum Low Byte

$0D_H$	**LMRES1**	Level Metering Result 1 (High Byte) (read-only)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	LM-VAL-H[7:0]							

LM-VAL-H[7:0] LM result High Byte
(selected by the LM-SEL bits in the LMCR2 register)

$0E_H$	**LMRES2**	Level Metering Result 2 (Low Byte) (read-only)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	LM-VAL-L[7:0]							

LM-VAL-L[7:0] LM result Low Byte
(selected by the LM-SEL bits in the LMCR2 register)

$0F_H$	**FUSE2**	Fuse Register 2	**hw**		**Y**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

10_H	**FUSE3**	Fuse Register 3	**hw**		**Y**

Bit	7	6	5	4	3	2	1	0
	for internal use only							

11_H	MASK	Mask Register	FF_H		Y

Bit	7	6	5	4	3	2	1	0
	READY-M	HOOK-M	GNDK-M	GNKP-M	ICON-M	VTRLIM-M	OTEMP-M	SYNC-M

The mask bits in the mask register influence only the generation of an interrupt. Even if the mask bit is set to 1, the corresponding status bit in the INTREGx registers is updated to show the current status of the corresponding event.

READY-M Mask bit for Ramp Generator READY bit

READY-M = 0 An interrupt is generated if the READY bit changes from 0 to 1.

READY-M = 1 Changes of the READY bit don't generate interrupts.

HOOK-M Mask bit for Off-Hook Detection HOOK bit

HOOK-M = 0 Each change of the HOOK bit generates an interrupt.

HOOK-M = 1 Changes of the HOOK bit don't generate interrupts.

GNDK-M Mask bit for ground key detection GNDK bit

GNDK-M = 0 Each change of the GNDK bit generates an interrupt.

GNDK-M = 1 Changes of the GNDK bit do not generate interrupts.

GNKP-M Mask bit for ground key level GNKP bit

GNKP-M = 0 Each change of the GNKP bit generates an interrupt.

GNKP-M = 1 Changes of the GNKP bit do not generate interrupts.

ICON-M Mask bit for Constant Current Information ICON bit

ICON-M = 0 Each change of the ICON bit generates an interrupt.

ICON-M = 1 Changes of the ICON bit do not generate interrupts.

VTRLIM-M Mask bit for Programmed Voltage Limit VTRLIM bit

VTRLIM-M = 0 Each change of the VTRLIM bit generates an interrupt.

VTRLIM-M = 1 Changes of the VTRLIM bit do not generate interrupts.

OTEMP-M Mask bit for Thermal Overload Warning OTEMP bit

OTEMP-M = 0	A change of the OTEMP bit from 0 to 1 generates an interrupt.
OTEMP-M = 1	A change of the OTEMP bit from 0 to 1 does not generate interrupts.

SYNC-M Mask bit for Synchronization Failure SYNC-FAIL bit

SYNC-M = 0	A change of the SYNC-FAIL bit from 0 to 1 generates an interrupt.
SYNC-M = 1	A change of the SYNC-FAIL bit from 0 to 1 does not generate interrupts.

12_H	IOCTL1	I/O Control Register 1	$0F_H$		Y

Bit	7	6	5	4	3	2	1	0
	IO[4:1]-INEN				IO[4:1]-M			

The mask bits IO[4:1]-M influence only the generation of an interrupt. Even if the mask bit is set to 1, the corresponding status bit in the INTREGx registers is updated to show the current status of the corresponding event.

IO4-INEN Input enable for programmable I/O pin IO4

IO4-INEN = 0 Input Schmitt trigger of pin IO4 is disabled.

IO4-INEN = 1 Input Schmitt trigger of pin IO4 is enabled.

IO3-INEN Input enable for programmable I/O pin IO3

IO3-INEN = 0 Input Schmitt trigger of pin IO3 is disabled.

IO3-INEN = 1 Input Schmitt trigger of pin IO3 is enabled.

IO2-INEN Input enable for programmable I/O pin IO2

IO2-INEN = 0 Input Schmitt trigger of pin IO2 is disabled.

IO2-INEN = 1 Input Schmitt trigger of pin IO2 is enabled.

IO1-INEN Input enable for programmable I/O pin IO1

IO1-INEN = 0 Input Schmitt trigger of pin IO1 is disabled.

IO1-INEN = 1 Input Schmitt trigger of pin IO1 is enabled.

IO4-M Mask bit for IO4-DU bit

IO4-M = 0 Each change of the IO4 bit generates an interrupt.

IO4-M = 1 Changes of the IO4 bit do not generate interrupts.

IO3-M Mask bit for IO3-DU bit

IO3-M = 0 Each change of the IO3 bit generates an interrupt.

IO3-M = 1 Changes of the IO3 bit do not generate interrupts.

IO2-M Mask bit for IO2-DU bit

IO2-M = 0 Each change of the IO2 bit generates an interrupt.

IO2-M = 1 Changes of the IO2 bit do not generate interrupts.

IO1-M Mask bit for IO1-DU bit

IO1-M = 0 Each change of the IO1 bit generates an interrupt.

IO1-M = 1 Changes of the IO1 bit do not generate interrupts.

13_H	IOCTL2	I/O Control Register 2	00_H		Y

Bit	7	6	5	4	3	2	1	0
	IO[4:1]-OEN				IO[4:1]-DD			

IO4-OEN Enabling the output driver of pin IO4

IO4-OEN = 0 The output driver of pin IO4 is disabled.

IO4-OEN = 1 The output driver of pin IO4 is enabled.

IO3-OEN Enabling the output driver of pin IO3

IO3-OEN = 0 The output driver of pin IO3 is disabled.

IO3-OEN = 1 The output driver of pin IO3 is enabled.

IO2-OEN Enabling the output driver of pin IO2

IO2-OEN = 0 The output driver of pin IO2 is disabled.

IO2-OEN = 1 The output driver of pin IO2 is enabled.

IO1-OEN Enabling the output driver of pin IO1

If external ringing is selected (bit REXT-EN in register BCR2 set to 1), pin IO1 cannot be controlled by the user but is utilized by the SLICOFI-2S to control the ring relay.

IO1-OEN = 0 The output driver of pin IO1 is disabled.

IO1-OEN = 1 The output driver of pin IO1 is enabled.

IO4-DD Value for the programmable I/O pin IO4 if programmed as an output pin.

IO4-DD = 0 The corresponding pin is driving a logical 0.

IO4-DD = 1 The corresponding pin is driving a logical 1.

IO3-DD Value for the programmable I/O pin IO3 if programmed as an output pin.

IO3-DD = 0 The corresponding pin is driving a logical 0.

IO3-DD = 1 The corresponding pin is driving a logical 1.

IO2-DD Value for the programmable I/O pin IO2 if programmed as an output pin.

IO2-DD = 0 The corresponding pin is driving a logical 0.

IO2-DD = 1 The corresponding pin is driving a logical 1.

IO1-DD Value for the programmable I/O pin IO1 if programmed as an output pin.

IO1-DD = 0 The corresponding pin is driving a logical 0.

IO1-DD = 1 The corresponding pin is driving a logical 1.

14_H	IOCTL3	I/O Control Register 3	94_H		Y

Bit	7	6	5	4	3	2	1	0
	DUP[3:0]				DUP-IO[3:0]			

DUP[3:0] Data Upstream Persistence Counter end value. Restricts the rate of interrupts generated by the HOOK bit in the interrupt register INTREG1. The interval is programmable from 1 to 16 ms in steps of 1 ms (reset value is 10 ms).

The DUP[3:0] value affects the blocking period for ground key detection (see **Chapter 2.6**).

DUP[3:0]	HOOK Active, Ringing	HOOK Power Down	GNDK	GNDK $f_{min,ACsup}$ 1)
0000	1	2 ms	4 ms	125 Hz
0001	2	4 ms	8 ms	62.5 Hz
...				
1111	16	32 ms	64 ms	7.8125 Hz

1) Minimum frequency for AC suppression.

DUP-IO[3:0] Data Upstream Persistence Counter end value for

- the I/O pins when used as digital input pins.
- the bits ICON and VTRLIM in register INTREG1.

The interval is programmable from 0.5 to 60.5 ms in steps of 4 ms (reset value is 16.5 ms).

15_H	BCR1	Basic Configuration Register 1	00_H		Y

Bit	7	6	5	4	3	2	1	0
	HIR	**HIT**	**0**	**REVPOL**	**ACTR**	**ACTL**	**SEL-SLIC[1:0]**	

HIR This bit modifies different basic modes. In ringing mode, an unbalanced ringing on the RING-wire (ROR) is enabled. In Active mode, high impedance on the RING-wire is performed (HIR). It enables the HIRT-mode, together with the HIT bit.

HIR = 0 Normal operation (ringing mode).

HIR = 1 Controls SLIC-S/-S2-interface and sets the RING wire to high impedance (Active mode).

HIT This bit modifies different basic modes. In ringing mode, an unbalanced ringing on the TIP-wire (ROT) is enabled. In Active mode, high impedance on the TIP-wire is performed (HIT). It enables the HIRT-mode, together with the HIR bit.

HIT = 0 Normal operation (ringing mode).

HIT = 1 Controls SLIC-S/-S2-interface and sets the TIP-wire to high impedance (Active mode).

REVPOL Reverse polarity of DC feeding

REVPOL = 0 Normal polarity.

REVPOL = 1 Reverse polarity.

ACTR Selection of extended battery feeding in Active mode.
In this case $V_{HR} - V_{BATH}$ for SLIC-S/-S2 is used.

ACTR = 0 No extended battery feeding selected.

ACTR = 1 Extended battery feeding selected.

ACTL Selection of the low battery supply voltage V_{BATL} on SLIC-S/-S2 if available. Valid only in Active mode of the SLICOFI-2S.

ACTL = 0	Low battery supply voltage on SLIC-S/-S2 is not selected.
ACTL = 1	Low battery supply voltage on SLIC-S/-S2 is selected.

SEL-SLIC[1:0] Selection of the current SLIC type used. For SLIC-E/-E2 and SLIC-P, the appropriate predefined mode table has to be selected.

SEL-SLIC[1:0] = 0 0	SLIC-E/-E2 selected.
SEL-SLIC[1:0] = 0 1	SLIC-P selected.
SEL-SLIC[1:0] = 1 0	SLIC-P selected for extremely power sensitive applications using external ringing.
SEL-SLIC[1:0] = 1 1	Reserved for future use.

For SLIC-P two selections are possible.

- The standard SLIC-P selection automatically uses the IO2 pin of the SLICOFI-2 to control the C3 pin of the SLIC-P. By using pin C3 as well as the pins C1 and C2, all possible operating modes of the SLIC-P can be selected. For SLIC-P 1.2 only the operating modes with 90 mA current limitation can be selected (ACTL90, ACTH90, ACTR90).

Note: If with SLIC-P V1.2 the 60 mA current limitation modes (ACTL60, ACTH60, ACTR60) are to be used, then the SLIC type SEL-SLIC[1:0] = 10 has to be programmed. In this case the C3 pin of the SLIC-P V1.2 can also be controlled by the IO2 pin of the SLICOFI-2. However, the IO2 pin has then to be programmed manually by the user according to the SLIC-P V1.2 interface code table.

- For extremely power sensitive applications using external ringing with SLIC-P SEL-SLIC[1:0] = 10 should be chosen. In this case, internal unbalanced ringing is not needed and therefore there is no need to switch the C3 pin of the SLIC-P to 'High'. The C3 pin of the SLIC-P must be connected to GND and the IO2 pin of the SLICOFI-2 is programmable by the user.
  There is no need for a high battery voltage for ringing either. This mode uses V_{BATR} for the on-hook voltage (e.g. –48 V) in Power Down Resistive (PDR) mode and the other battery supply voltages (e.g. V_{BATH} = –24 V and V_{BATL} = –18 V) can be used for the off-hook state. This will help to save power because the lowest possible battery voltage can be selected (see DuSLIC Voltage and Power Application Note).

16_H	BCR2	Basic Configuration Register 2	00_H		Y

Bit	7	6	5	4	3	2	1	0
	REXT-EN	**SOFT-DIS**	**TTX-DIS[1)]**	**TTX-12K[2)]**	**HIM-AN**	**AC-XGAIN**	**0**	**PDOT-DIS**

[1)] Only for DuSLIC-S, is set to 1 for DuSLIC-S2

[2)] Only for DuSLIC-S, is set to 0 for DuSLIC-S2

REXT-EN Enables the use of an external ring-signal generator. The synchronization is done via the RSYNC pin and the ring-burst-enable signal is transferred via the IO1 pin.

REXT-EN = 0 External ringing is disabled.

REXT-EN = 1 External ringing enabled.

SOFT-DIS Polarity soft reversal (to minimize noise on DC feeding)

SOFT-DIS = 0 Polarity soft reversal active.

SOFT-DIS = 1 Polarity hard reversal.

TTX-DIS Disables the generation of TTX bursts for metering signals. If they are disabled, reverse polarity is used instead.

TTX-DIS = 0 TTX bursts are enabled.

TTX-DIS = 1 TTX bursts are disabled, reverse polarity used.

TTX-12K Selection of TTX frequencies

TTX-12K = 0 Selects 16 kHz TTX signals instead of 12 kHz signals.

TTX-12K = 1 12 kHz TTX signals.

HIM-AN Higher impedance in analog impedance matching loop.

The value of this bit must correspond to the selection done in the DUSLICOS tool when calculating the coefficients. If the coefficients are calculated with standard impedance in analog impedance matching loop, HIM-AN must be set to 0; if the coefficients are calculated with high impedance in analog impedance matching loop, HIM-AN must be set to 1.

HIM-AN = 0	Standard impedance in analog impedance matching loop
HIM-AN = 1	High impedance in analog impedance matching loop

AC-XGAIN Analog gain in transmit direction (should be set to zero).

AC-XGAIN = 0	No additional analog gain in transmit direction.
AC-XGAIN = 1	Additional 6 dB analog amplification in transmit direction.

PDOT-DIS Power Down Overtemperature Disable

PDOT-DIS = 0	When overtemperature is detected, the SLIC-S/-S2 is automatically switched into Power Down High Impedance mode (PDH). This is the safe operation mode for the SLIC-S/-S2 in case of overtemperature. To leave the automatically activated PDH mode, DuSLIC must be switched manually to PDH mode and then in the mode as desired.
PDOT-DIS = 1	When overtemperature is detected, the SLIC-S/-S2 does not automatically switch into Power Down High Impedance mode. In this case, the output current of the SLIC-S/-S2 buffers is limited to a value which keeps the SLIC-S/-S2 temperature below the upper temperature limit.

17_H	BCR3	Basic Configuration Register 3	00_H		Y

Bit	7	6	5	4	3	2	1	0
	MU-LAW	**LIN**	**0**	**PCMX-EN**	**0**	**0**	**0**	**CRAM-EN**

MU-LAW Selects the PCM Law

MU-LAW = 0 A-Law enabled.

MU-LAW = 1 µ-Law enabled.

LIN Voice transmission in a 16-bit linear representation for test purposes.

Note: Voice transmission on the other channel is inhibited if one channel is set to linear mode and the IOM-2 interface is used. In PCM/microcontroller interface mode, both channels can be in linear mode using two consecutive PCM timeslots on the highways. A proper timeslot selection must be specified.

LIN = 0 PCM mode enabled (8 bit, A-Law, or µ-Law).

LIN = 1 Linear mode enabled (16 bit).

PCMX-EN Enables writing of subscriber voice data to the PCM highway.

PCMX-EN = 0 Writing of subscriber voice data to PCM highway is disabled.

PCMX-EN = 1 Writing of subscriber voice data to PCM highway is enabled.

CRAM-EN Coefficients from CRAM are used for programmable filters and DC loop behavior.

CRAM-EN = 0 Coefficients from ROM are used.

CRAM-EN = 1 Coefficients from CRAM are used.

18_H	BCR4	Basic Configuration Register 4	00_H		Y

Bit	7	6	5	4	3	2	1	0
	TH-DIS	IM-DIS	AX-DIS	AR-DIS	FRX-DIS	FRR-DIS	HPX-DIS	HPR-DIS

TH-DIS Disables the TH filter.

TH-DIS = 0 TH filter is enabled.

TH-DIS = 1 TH filter is disabled (H_{TH} = 0).

IM-DIS Disables the IM filter.

IM-DIS = 0 IM filter is enabled.

IM-DIS = 1 IM filter is disabled (H_{IM} = 0).

AX-DIS Disables the AX filter.

AX-DIS = 0 AX filter is enabled.

AX-DIS = 1 AX filter is disabled (H_{AX} = 1).

AR-DIS Disables the AR filter.

AX-DIS = 0 AR filter is enabled.

AX-DIS = 1 AR filter is disabled (H_{AR} = 1).

FRX-DIS Disables the FRX filter.

FRX-DIS = 0 FRX filter is enabled.

FRX-DIS = 1 FRX filter is disabled (H_{FRX} = 1).

FRR-DIS Disables the FRR filter.

FRR-DIS = 0 FRR filter is enabled.

FRR-DIS = 1 FRR filter is disabled (H_{FRR} = 1).

HPX-DIS Disables the high-pass filter in transmit direction.

HPX-DIS = 0 High-pass filter is enabled.

HPX-DIS = 1 High-pass filter is disabled (H_{HPX} = 1).

HPR-DIS Disables the high-pass filter in receive direction.

HPR-DIS = 0 High-pass filter is enabled.

HPR-DIS = 1 High-pass filter is disabled (H_{HPR} = 1).

19_H		Reserved	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

$1A_H$	DSCR	DTMF Sender Configuration Register	00_H		Y

Bit	7	6	5	4	3	2	1	0
	DG-KEY[3:0]				COR8	PTG	TG2-EN	TG1-EN

DG-KEY[3:0] Selects one of sixteen DTMF keys generated by the 2 tone generators. The key will be generated if both TG1-EN and TG2-EN are 1.

Table 71 DTMF Keys

f_{LOW} [Hz]	f_{HIGH} [Hz]	DIGIT	DG-KEY3	DG-KEY2	DG-KEY1	DG-KEY0
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

COR8 Cuts off the receive path at 8 kHz before the tone generator summation point. Allows sending of tone generator signals without overlaid voice.

COR8 = 0 Cut off receive path disabled.

COR8 = 1 Cut off receive path enabled.

PTG Programmable coefficients for tone generators will be used.

PTG = 0 Frequencies set by DG-KEY are used for both tone generators.
Tone generator TG1 level: –5 dBm0
Tone generator TG2 level: –3 dBm0

PTG = 1 CRAM coefficients used for both tone generators.
Tone generator TG1 and TG2 frequencies and levels can be programmed in the DuSLICOS DC Control Parameters 3/4. The levels are set in dBm0:
Level[dBm] = Level[dBm0] + L_R[dBr]

TG2-EN Enables tone generator two

TG2-EN = 0 Tone generator is disabled.

TG2-EN = 1 Tone generator is enabled.

TG1-EN Enables tone generator one

TG1-EN = 0 Tone generator is disabled.

TG1-EN = 1 Tone generator is enabled.

$1B_H$		Reserved	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

$1C_H$	LMCR1	Level Metering Configuration Register 1	22_H		Y

Bit	7	6	5	4	3	2	1	0
	TEST-EN	LM-EN	LM-THM	PCM2DC	LM2PCM	LM-ONCE	LM-MASK	DC-AD16

TEST-EN Activates the SLICOFI-2S test features controlled by test registers TSTR1 to TSTR5.

TEST-EN = 0 SLICOFI-2S test features are disabled.

TEST-EN = 1 SLICOFI-2S test features are enabled.

Note: The Test Register bits can be programmed before the TEST-EN bit is set to 1.

LM-EN Enables level metering. A positive transition of this bit starts level metering (AC and DC).

LM-EN = 0 Level metering stops.

LM-EN = 1 Level metering enabled.

LM-THM Level metering threshold mask bit

LM-THM = 0 A change of the LM-THRES bit (register INTREG2) generates an interrupt.

LM-THM = 1 No interrupt is generated.

PCM2DC PCM voice channel data added to the DC-output.

PCM2DC = 0 Normal operation.

PCM2DC = 1 PCM voice channel data is added to DC output.

LM2PCM Level metering source/result (depending on LM-EN bit) feeding to PCM or IOM-2 interface.

LM2PCM = 0 Normal operation.

LM2PCM = 1 Level metering source/result is fed to the PCM or IOM-2 interface.

LM-ONCE Level metering execution mode.

LM-ONCE = 0	Level metering is executed continuously.
LM-ONCE = 1	Level metering is executed only once. To start the Level Meter again, the LM-EN bit must again be set from 0 to 1.

LM-MASK Interrupt masking for level metering.

LM-MASK = 0	An interrupt is generated after level metering.
LM-MASK = 1	No interrupt is generated.

DC-AD16 Additional digital amplification in the DC AD path for level metering.

DC-AD16 = 0	Additional gain factor 16 disabled.
DC-AD16 = 1	Additional gain factor 16 enabled.

$1D_H$	LMCR2	Level Metering Configuration Register 2	00_H		Y

Bit	7	6	5	4	3	2	1	0
	LM-NOTCH	**LM-FILT**	**LM-RECT**	**RAMP-EN**	**LM-SEL[3:0]**			

LM-NOTCH Selection of a notch filter instead of the band-pass filter for level metering.

LM-NOTCH = 0 Notch filter selected.

LM-NOTCH = 1 Band-pass filter selected.

LM-FILT Enabling of a programmable band-pass or notch filter for level metering.

LM-FILT = 0 Normal operation.

LM-FILT = 1 Band-pass/notch filter enabled.

LM-RECT Rectifier in DC Level Meter

LM-RECT = 0 Rectifier disabled.

LM-RECT = 1 Rectifier enabled.

RAMP-EN The ramp generator works together with the RNG-OFFSET bits in LMCR3 and the LM-EN bit to create different voltage slopes in the DC-Path.

RAMP-EN = 0 Ramp generator disabled.

RAMP-EN = 1 Ramp generator enabled.

LM-SEL[3:0] Selection of the source for the level metering.

LM-SEL[3:0] = 0 0 0 0 AC level metering in transmit

LM-SEL[3:0] = 0 0 0 1 Real part of TTX (TTX_{REAL})

LM-SEL[3:0] = 0 0 1 0 Imaginary part of TTX (TTX_{IMG})

LM-SEL[3:0] = 0 0 1 1 Not used

LM-SEL[3:0] = 0 1 0 0 DC out voltage on DCN-DCP

LM-SEL[3:0] = 0 1 0 1 DC current on IT

LM-SEL[3:0] = 0 1 1 0 AC level metering in receive

LM-SEL[3:0] = 0 1 1 1	AC level metering in receive and transmit
LM-SEL[3:0] = 1 0 0 0	Not used
LM-SEL[3:0] = 1 0 0 1	DC current on IL
LM-SEL[3:0] = 1 0 1 0	Voltage on IO3
LM-SEL[3:0] = 1 0 1 1	Voltage on IO4
LM-SEL[3:0] = 1 1 0 0	Not used
LM-SEL[3:0] = 1 1 0 1	V_{DD}
LM-SEL[3:0] = 1 1 1 0	Offset of DC-Prefi (short circuit on DC-Prefi input)
LM-SEL[3:0] = 1 1 1 1	Voltage on IO4 – IO3

$1E_H$	LMCR3	Level Metering Configuration Register 3	00_H		Y

Bit	7	6	5	4	3	2	1	0
	AC-SHORT-EN	**RTR-SEL**	**LM-ITIME[3:0]**				**RNG-OFFSET[1:0]**	

AC-SHORT-EN The input pin ITAC will be set to a lower input impedance so that the capacitor C_{ITAC} can be recharged faster during a soft reversal which makes it more silent during conversation.

AC-SHORT-EN = 0 Input impedance of the ITAC pin is standard.

AC-SHORT-EN = 1 Input impedance of the ITAC pin is lowered.

RTR-SEL Ring Trip method selection.

RTR-SEL = 0 Ring Trip with a DC offset is selected.

RTR-SEL = 1 AC Ring Trip is selected. Recommended for short lines only.

LM-ITIME[3:0] Integration Time for AC Level Metering.

LM-ITIME[3:0] = 0 0 0 0 16 ms

LM-ITIME[3:0] = 0 0 0 1 2 × 16 ms

LM-ITIME[3:0] = 0 0 1 0 3 × 16 ms

…

LM-ITIME[3:0] = 1 1 1 1 16 × 16 ms

RNG-OFFSET[1:0] Selection of the Ring Offset source.

RNG-OFFSET[1:0]	Ring Offset Voltage in Given Mode		
	Active ACTH ACTL	Active Ring ACTR	Ring Pause Ringing
0 0	Voltage given by DC regulation	Voltage given by DC regulation	Ring Offset RO1 Hook Threshold Ring
0 1	Ring Offset RO1/2 (no DC regulation)	Ring Offset RO1 (no DC regulation)	Ring Offset RO1 Hook Threshold Ring
1 0	Ring Offset RO2/2 (no DC regulation)	Ring Offset RO2 (no DC regulation)	Ring Offset RO2 Hook Message Waiting
1 1	Ring Offset RO3/2 (no DC regulation)	Ring Offset RO3 (no DC regulation)	Ring Offset RO3 Hook Message Waiting

By setting the RAMP-EN bit to 1, the ramp generator is started by setting LM-EN from 0 to 1 (see **Figure 68**).
Exception: Transition of RNG-OFFSET from 10 to 11 or 11 to 10 where the ramp generator is started automatically (see **Figure 68**).

For Ring Offset RO1, the usual “Hook Threshold Ring” is used. Using Ring Offset RO2 or RO3 in any ringing mode (Ringing and Ring Pause) also changes the hook thresholds. In this case the “Hook Message Waiting” threshold is used automatically.

When using the Ring Offsets RO2 and RO3 for Message Waiting, an additional lamp current is expected. In this case, the Hook Message Waiting threshold should be programmed higher than the Hook Threshold Ring.

ook Threshold Ring.

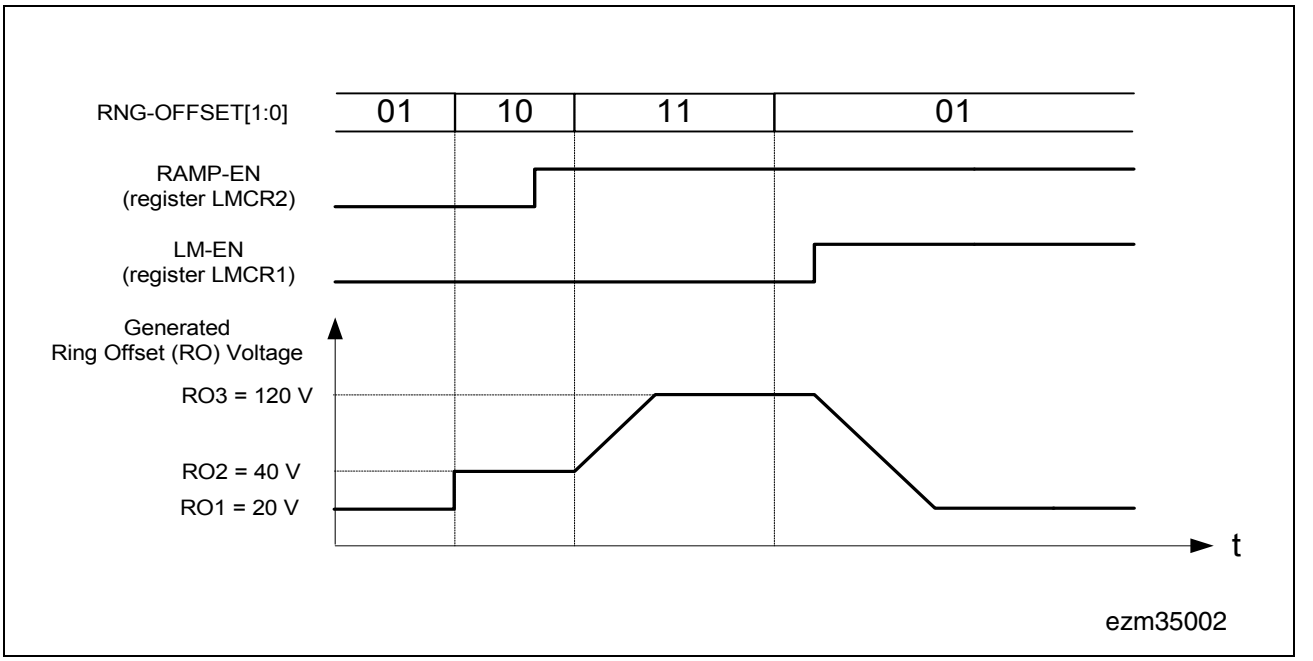


Figure 68 Example for Switching Between Different Ring Offset Voltages

The three programmable Ring Offsets are typically used for the following purposes:

Table 72 Typical Usage for the three Ring Offsets

Ring Offset Voltage	Application
Ring Offset RO1	Ringing
Ring Offset RO2	Low voltage for message waiting lamp
Ring Offset RO3	High voltage for message waiting lamp

Besides the typical usage described in **Table 72**, the Ring Offsets RO1, RO2, and RO3 can also be used for the generation of different custom waveforms (see **Figure 68**).

$1F_H$	**OFR1**	Offset Register 1 (High Byte)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	OFFSET-H[7:0]							

OFFSET-H[7:0] Offset register High Byte.

20_H	**OFR2**	Offset Register 2 (Low Byte)	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0
	OFFSET-L[7:0]							

OFFSET-L[7:0] Offset register Low Byte.

The value of this register together with OFFSET-H is added to the input of the DC loop to compensate a given offset of the current sensors in the SLIC-S/-S2.

21_H	PCMR1	PCM Receive Register 1	00_H		Y

Bit	7	6	5	4	3	2	1	0
	R1-HW	R1-TS[6:0]						

R1-HW Selection of the PCM highway for receiving PCM data or the higher byte of the first data sample if linear 16 kHz PCM mode is selected.

R1-HW = 0 PCM highway A is selected.

R1-HW = 1 PCM highway B is selected.

R1-TS[6:0] Selection of the PCM timeslot used for data reception.

Note: The programmed PCM timeslot must correspond to the available slots defined by the PCLK frequency. No reception will occur if a slot outside the actual numbers of slots is programmed. In linear mode (bit LIN = 1 in register BCR3) R1-TS defines the first of two consecutive slots used for reception.

22_H		Reserved	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0

23_H		Reserved	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0

24_H		Reserved	**00_H**		**Y**

Bit	7	6	5	4	3	2	1	0

25_H	PCMX1	PCM Transmit Register 1	00_H		Y

Bit	7	6	5	4	3	2	1	0
	X1-HW	X1-TS[6:0]						

X1-HW Selection of the PCM highway for transmitting PCM data or the higher byte of the first data sample if linear 16 kHz PCM mode is selected.

X1-HW = 0 PCM highway A is selected.

X1-HW = 1 PCM highway B is selected.

X1-TS[6:0] Selection of the PCM timeslot used for data transmission.

Note: The programmed PCM timeslot must correspond to the available slots defined by the PCLK frequency. No transmission will occur if a slot outside the actual numbers of slots is programmed. In linear mode, X1-TS defines the first of two consecutive slots used for transmission. PCM data transmission is controlled by bits 6 to 2 in register BCR3.

26_H		Reserved	00_H		Y

Bit	7	6	5	4	3	2	1	0

27_H		Reserved	00_H		Y

Bit	7	6	5	4	3	2	1	0

28_H		Reserved	00_H		Y

Bit	7	6	5	4	3	2	1	0

29_H	TSTR1	Test Register 1	00_H	T	Y

Bit	7	6	5	4	3	2	1	0
	PD-AC-PR	PD-AC-PO	PD-AC-AD	PD-AC-DA	PD-AC-GN	PD-GNKC	PD-OFHC	PD-OVTC

Register setting is active only if bit TEST-EN in register LMCR1 is set to 1.

PD-AC-PR AC-PREFI Power Down

PD-AC-PR = 0 Normal operation.

PD-AC-PR = 1 Power down mode.

PD-AC-PO AC-POFI Power Down

PD-AC-PO = 0 Normal operation.

PD-AC-PO = 1 Power down mode.

PD-AC-AD AC-ADC Power Down

PD-AC-AD = 0 Normal operation.

PD-AC-AD = 1 Power down mode, transmit path is inactive.

PD-AC-DA AC-DAC Power Down

PD-AC-DA = 0 Normal operation.

PD-AC-DA = 1 Power down mode, receive path is inactive.

PD-AC-GN AC-Gain Power Down

PD-AC-GN = 0 Normal operation.

PD-AC-GN = 1 Power down mode.

PD-GNKC Ground key comparator (GNKC) is set to Power Down

PD-GNKC = 0 Normal operation.

PD-GNKC = 1 Power down mode.

PD-OFHC Off-hook comparator (OFHC) Power Down

PD-OFHC = 0 Normal operation.

PD-OFHC = 1 Power down mode.

PD-OVTC Overtemperature comparator (OVTC) Power Down

PD-OVTC = 0 Normal operation.

PD-OVTC = 1 Power down mode.

$2A_H$	TSTR2	Test Register 2	00_H	T	Y

Bit	7	6	5	4	3	2	1	0
	PD-DC-PR	**0**	**PD-DC-AD**	**PD-DC-DA**	**PD-DCBUF**	**0**	**PD-TTX-A**[1)]	**PD-HVI**

[1)] Only for DuSLIC-S; for DuSLIC-S2, is set to 0.

Register setting is active only if bit TEST-EN in register LMCR1 is set to 1.

PD-DC-PR DC-PREFI Power Down

PD-DC-PR = 0 Normal operation.

PD-DC-PR = 1 Power down mode.

PD-DC-AD DC-ADC Power Down

PD-DC-AD = 0 Normal operation.

PD-DC-AD = 1 Power down mode, transmit path is inactive.

PD-DC-DA DC-DAC Power Down

PD-DC-DA = 0 Normal operation.

PD-DC-DA = 1 Power down mode, receive path is inactive.

PD-DCBUF DC-BUFFER Power Down

PD-DCBUF = 0 Normal operation.

PD-DCBUF = 1 Power down mode.

PD-TTX-A TTX adaptation DAC and POFI Power Down

PD-TTX-A = 0 Normal operation.

PD-TTX-A = 1 Power down mode.

PD-HVI HV interface (to SLIC-S/-S2) Power Down

PD-HVI = 0 Normal operation.

PD-HVI = 1 Power down mode.

$2B_H$	TSTR3	Test Register 3	00_H	T	Y

Bit	7	6	5	4	3	2	1	0
	0	**0**	**AC-DLB-4M**	**AC-DLB-128K**	**AC-DLB-32K**	**AC-DLB-8K**	**0**	**0**

Register setting is active only if bit TEST-EN in register LMCR1 is set to 1.

AC-DLB-4M AC digital loop via 4 MHz bitstream. (The loop encloses all digital hardware in the AC path. Together with DLB-DC, a pure digital test is possible because there is no influence of the analog hardware.)

AC-DLB-4M = 0 Normal operation.

AC-DLB-4M = 1 Digital loop closed.

AC-DLB-128K AC digital loop via 128 kHz

AC-DLB-128K = 0 Normal operation.

AC-DLB-128K = 1 Digital loop closed.

AC-DLB-32K AC digital loop via 32 kHz

AC-DLB-32K = 0 Normal operation.

AC-DLB-32K = 1 Digital loop closed.

AC-DLB-8K AC digital loop via 8 kHz

AC-DLB-8K = 0 Normal operation.

AC-DLB-8K = 1 Digital loop closed.

$2C_H$	TSTR4	Test Register 4	00_H	T	Y

Bit	7	6	5	4	3	2	1	0
	OPIM-AN	**OPIM-4M**	**COR-64**	**COX-16**	**0**	**0**	**0**	**0**

Register setting is active only if bit TEST-EN in register LMCR1 is set to 1.

OPIM-AN Open Impedance Matching Loop in the analog part.

OPIM-AN = 0 Normal operation.

OPIM-AN = 1 Loop opened.

OPIM-4M Open fast digital Impedance Matching Loop in the hardware filters.

OPIM-4M = 0 Normal operation.

OPIM-4M = 1 Loop opened.

COR-64 Cut off the AC receive path at 64 kHz (just before the IM filter).

COR-64 = 0 Normal operation.

COR-64 = 1 Receive path is cut off.

COX-16 Cut off the AC transmit path at 16 kHz. (The TH filters can be tested without the influence of the analog part.)

COX-16 = 0 Normal operation.

COX-16 = 1 Transmit path is cut off.

$2D_H$	TSTR5	Test Register 5	00_H	T	Y

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**DC-POFI-HI**	**DC-HOLD**	**0**	**0**	**0**

Register setting is only active if bit TEST-EN in register LMCR1 is set to 1.

DC-POFI-HI DC post filter limit frequency higher value

DC-POFI-HI = 0 Limit frequency is set to 100 Hz (normal operation).

DC-POFI-HI = 1 Limit frequency is set to 300 Hz.

DC-HOLD Actual DC output value hold (value of the last DSP filter stage will be kept)

DC-HOLD = 0 Normal operation.

DC-HOLD = 1 DC output value hold.

5.3.2 COP Command

The Coefficient Operation (COP) command gives access to the CRAM data of the DSPs. It is organized in the same way as the SOP command. The offset value allows a direct as well as a block access to the CRAM. Writing beyond the allowed offset will be ignored, reading beyond it will give unpredictable results.
The value of a specific CRAM coefficient is calculated by the DuSLICOS software.

Attention: To ensure proper functionality, it is essential that all unused register bits have to be filled with zeros.

Bit	7	6	5	4	3	2	1	0
Byte 1	**RD**	**1**	**ADR[2:0]**			**1**	**0**	**1**
Byte 2	**OFFSET[7:0]**							

RD Read Data

RD = 0 Write data to chip.

RD = 1 Read data from chip.

ADR[2:0] Channel address for the subsequent data

ADR[2:0] = 0 0 0 Channel A

ADR[2:0] = 0 0 1 Channel B

(other codes reserved for future use)

CRAM coefficients are enabled by setting bit CRAM-EN in register BCR3 to 1, except

Offset [7:0]	Short Name	Long Name
00_H	TH1	Transhybrid Filter Coefficients Part 1
08_H	TH2	Transhybrid Filter Coefficients Part 2
10_H	TH3	Transhybrid Filter Coefficients Part 3
18_H	FRR	Frequency-response Filter Coefficients Receive Direction
20_H	FRX	Frequency-response Filter Coefficients Transmit Direction
28_H	AR	Amplification/Attenuation Stage Coefficients Receive
30_H	AX	Amplification/Attenuation Stage Coefficients Transmit
38_H	PTG1	Tone Generator 1 Coefficients
40_H	PTG2	Tone Generator 2 Coefficients
48_H	LPR	Low Pass Filter Coefficients Receive
50_H	LPX	Low Pass Filter Coefficients Transmit
58_H	TTX	Teletax Coefficients
60_H	IM1	Impedance Matching Filter Coefficients Part 1
68_H	IM2	Impedance Matching Filter Coefficients Part 2
70_H	RINGF	Ringer Frequency and Amplitude Coefficients (DC loop)
78_H	RAMPF	Ramp Generator Coefficients (DC loop)
80_H	DCF	DC-Characteristics Coefficients (DC loop)
88_H	HF	Hook Threshold Coefficients (DC loop)
90_H	TPF	Low Pass Filter Coefficients (DC loop)
98_H		Reserved

Table 73 CRAM Coefficients

Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0	Offset [7:0]	
Transhybrid Coefficient Part 1								00_H	TH1
Transhybrid Coefficient Part 2								08_H	TH2
Transhybrid Coefficient Part 3								10_H	TH3
FIR Filter in Receive Direction								18_H	FRR
FIR Filter in Transmit Direction								20_H	FRX
2nd Gain Stage Receive				1st Gain Stage Receive				28_H	AR
2nd Gain Stage Transmit				1st Gain Stage Transmit				30_H	AX
TG1 Band-pass				TG1 Gain		TG1 Frequency		38_H	PTG1[1)]
TG2 Band-pass				TG2 Gain		TG2 Frequency		40_H	PTG2[1)]
Reserved								48_H	
Reserved								50_H	
FIR Filter for TTX				TTX Slope		TTX Level		58_H	TTX
IM K Factor		IM FIR Filter						60_H	IM1_F
IM 4 MHz Filter				IM WDF Filter				68_H	IM2_F
Ring Generator Amplitude		Ring Generator Frequency		Ring Generator Lowpass		Ring Offset RO1		70_H	RINGF
Extended Battery Feeding Gain		Soft Reversal End		Constant Ramp CR		Soft Ramp SS		Ring Delay RD	78_H	RAMPF
Res. in Resistive Zone R_{K12}		Res. in Constant Current Zone R_I		Constant Current I_{K1}		Knee Voltage V_{K1}		Open Circuit Volt. V_{LIM}	80_H	DCF
Hook Message Waiting		Hook Threshold AC Ring Trip		Hook Threshold Ring		Hook Threshold Active		Hook Threshold Power Down	88_H	HF
Voltage Level V_{TR}		DC Lowpass Filter TP2		DC Lowpass Filter TP1				90_H	TPF
Reserved								98_H	

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		

coefficients PTG1 and PTG2[1)] which are enabled by setting bit PTG in register DSCR to 1.

5.3.2.1 CRAM Programming Ranges

Table 74 CRAM Programming Ranges

Parameter	Programming Range
Constant Current I_{K1}	0...50 mA, Δ < 0.5 mA
Hook Message Waiting, Hook Thresholds	0..25 mA, Δ < 0.7 mA 25...50 mA, Δ < 1.3 mA
Ring Generator Frequency f_{RING}	3..40 Hz, Δ < 1 Hz 40..80 Hz, Δ < 2 Hz > 80 Hz, Δ < 4 Hz
Ring Generator Amplitude	0..20 V, Δ < 1.7 V 20..85 V, Δ < 0.9 V
Ring Offset RO1	0..25 V, Δ < 0.6 V 25..50 V, Δ < 1.2 V 50..100 V, Δ < 2.4 V, max. 150 V
Knee Voltage V_{K1}, Open Circuit Voltge V_{LIM}	0..25 V, Δ < 0.6 V 25..50 V, Δ < 1.2 V > 50 V, Δ < 2.4 V
Resistance in Resistive Zone R_{K12}	0..1000 Ω, Δ < 30 Ω
Resistance in Constant Current Zone R_I	1.8 kΩ..4.8 kΩ, Δ < 120 Ω 4.8 kΩ..9.6 kΩ, Δ < 240 Ω 9.6 kΩ..19 kΩ, Δ < 480 Ω 19 kΩ..38 kΩ, Δ < 960 Ω, max. 40 kΩ

5.3.3 IOM-2 Interface Command/Indication Byte

The Command/Indication (C/I) channel is used to communicate real time status information and for fast control of the DuSLIC. Data on the C/I channel are continuously transmitted in each frame until new data are sent.

Data Downstream C/I – Channel Byte (Receive) – IOM-CIDD

The first six CIDD data bits control the general operating modes for both DuSLIC channels. According to the IOM-2 specification, new data must be present for at least two frames to be accepted.

Table 75 M2, M1, M0: General Operating Mode

CIDD			SLICOFI-2S Operating Mode (for details see “Overview of all DuSLIC Operating Modes” on Page 74)
M2	M1	M0	
1	1	1	Sleep, Power Down (PDRx)
0	0	0	Power Down High Impedance (PDH)
0	1	0	Any Active mode
1	0	1	Ringing (ACTR Burst On)
1	1	0	Active with Metering
1	0	0	Ground Start
0	0	1	Ring Pause

	CIDD	Data Downstream C/I – Channel Byte			N

Bit	7	6	5	4	3	2	1	0
	M2A	M1A	M0A	M2B	M1B	M0B	MR	MX

M2A, M1A, M0A Select operating mode for DuSLIC channel A

M2B, M1B, M0B Select operating mode for DuSLIC channel B

MR, MX Handshake bits Monitor Receive and Transmit (see “IOM-2 Interface Monitor Transfer Protocol” on Page 133)

Data Upstream C/I – Channel Byte (Transmit) – IOM-CIDU

This byte is used to quickly transfer the most important and time-critical information from the DuSLIC. Each transfer from the DuSLIC lasts for at least two consecutive frames.

	CIDU	Data Upstream C/I – Channel Byte	00_H		N

Bit	7	6	5	4	3	2	1	0
	INT-CHA	HOOKA	GNDKA	INT-CHB	HOOKB	GNDKB	MR	MX

INT-CHA Interrupt information channel A
INT-CHA = 0 No interrupt in channel A
INT-CHA = 1 Interrupt in channel A

HOOKA Hook information channel A
HOOKA = 0 On-hook channel A
HOOKA = 1 Off-hook channel A

GNDKA Ground key information channel A
GNDKA = 0 No longitudinal current detected
GNDKA = 1 Longitudinal current detected in channel A

INT-CHB Interrupt information channel B
INT-CHB = 0 No interrupt in channel B
INT-CHB = 1 Interrupt in channel B

HOOKB Hook information channel B
HOOKB = 0 On-hook channel B
HOOKB = 1 Off-hook channel B

GNDKB Ground key information channel B
GNDKB = 0 No longitudinal current detected
GNDKB = 1 Longitudinal current detected in channel B

MR, MX Handshake bits Monitor Receive and Transmit
(see **“IOM-2 Interface Monitor Transfer Protocol” on Page 133**)

5.3.4 Programming Examples of the SLICOFI-2S

5.3.4.1 Microcontroller Interface

SOP Write to Channel 0 Starting After the Channel-Specific Read-Only Registers

01000100 First command byte (SOP write for channel 0)
00010101 Second command byte (offset to BCR1 register)
00000000 Contents of BCR1 register
00000000 Contents of BCR2 register
00010001 Contents of BCR3 register
00000000 Contents of BCR4 register
00000000 Contents of BCR5 register

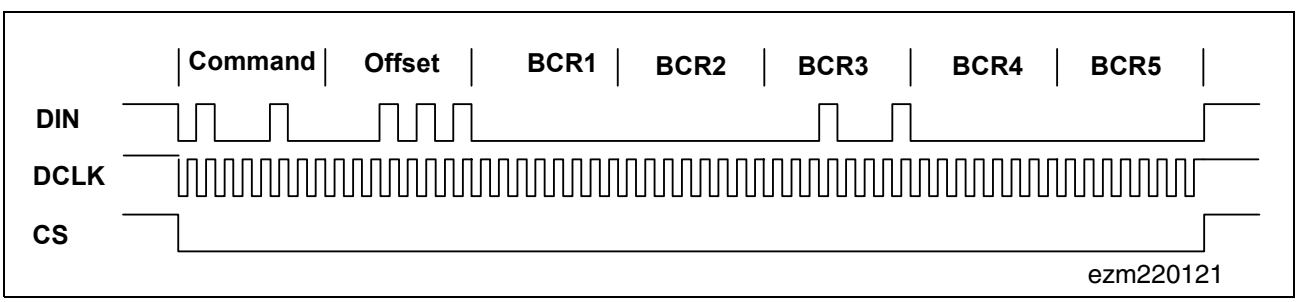


Figure 69 Waveform of Programming Example SOP Write to Channel 0

SOP Read from Channel 1 Reading Out the Interrupt Registers

11001100 First command byte (SOP read for channel 1).
00000111 Second command byte (offset to Interrupt register 1).

The SLICOFI-2S will send data when it has completely received the second command byte.

11111111 Dump byte (this byte is always FF_H).
11000000 Interrupt register INTREG1 (an interrupt has occurred, Off-hook was detected).
00000010 Interrupt register INTREG2 (I/O pin 2 is 1).
00000000 Interrupt register INTREG3
00000000 Interrupt register INTREG4

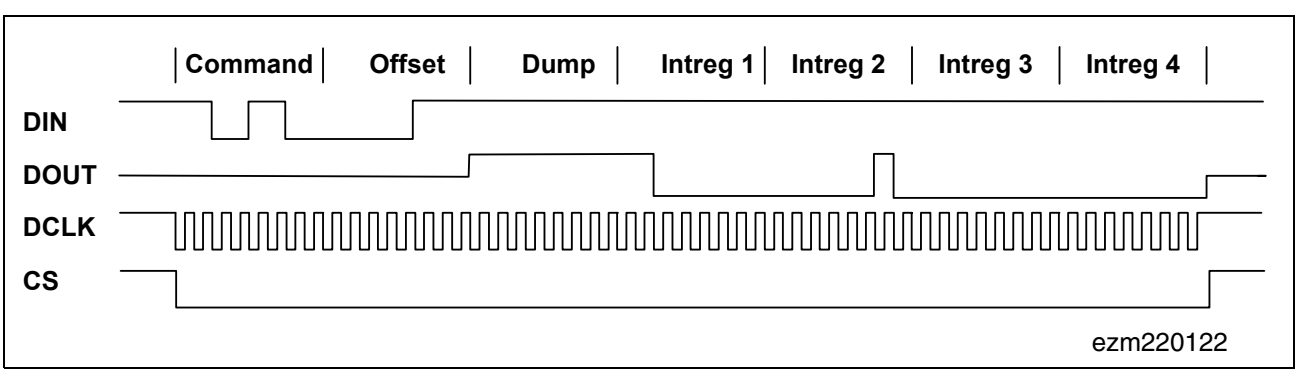


Figure 70 Waveform of Programming Example SOP Read from Channel 0

5.3.4.2 IOM-2 Interface

An example with the same programming sequence as before, using the IOM-2 interface is presented here to show the differences between the microcontroller interface and the IOM-2 interface.

SOP Write to Channel 0 Starting After the Channel-Specific Read-Only Registers

Monitor data down	MR/MX	Monitor data up	MR/MX	Comment
10000001	10	11111111	11	IOM-2 address first byte
10000001	10	11111111	01	IOM-2 address second byte
01000100	11	11111111	01	First command byte (SOP write for channel 0)
01000100	10	11111111	11	First command byte second time
00010101	11	11111111	01	Second command byte (offset to BCR1 register)
00010101	10	11111111	11	Second command byte second time
00000000	11	11111111	01	Contents of BCR1 register
00000000	10	11111111	11	Contents of BCR1 register second time
00000000	11	11111111	01	Contents of BCR2 register
00000000	10	11111111	11	Contents of BCR2 register second time
00010001	11	11111111	01	Contents of BCR3 register
00010001	10	11111111	11	Contents of BCR3 register second time
00000000	11	11111111	01	Contents of BCR4 register
00000000	10	11111111	11	Contents of BCR4 register second time
11111111	11	11111111	01	No more information (dummy byte)
11111111	11	11111111	11	Signaling EOM (end of message) by holding MX bit at ‘1’.

Because the SLICOFI-2S has an open command structure, no fixed command length is given. The IOM-2 handshake protocol allows for an infinite length of a data stream; therefore, the host must terminate the data transfer by sending an end-of-message signal (EOM) to the SLICOFI-2S. The SLICOFI-2S will abort the transfer only if the host tries to write or read beyond the allowed maximum offsets given by the different types of commands. Each transfer must start with the SLICOFI-2S-specific IOM-2 Address (81_H) and must end with an EOM of the handshake bits. Appending a command immediately to its predecessor without an EOM in between is not allowed.

When reading interrupt registers, SLICOFI-2S stops the transfer after the fourth register in IOM-2 mode. This is to prevent some host chips from reading 16 bytes because they cannot terminate the transfer after n bytes.

SOP-Read from Channel 1 Reading Out the Interrupt Registers

Monitor data down	MR/MX	Monitor data up	MR/MX	Comment
10000001	10	11111111	11	IOM-2 address first byte
10000001	10	11111111	01	IOM-2 address second byte
11001100	11	11111111	01	First command byte (SOP read for channel 1)
11001100	10	11111111	11	First command byte second time
00001000	11	11111111	01	Second command byte (offset to interrupt register 1)
00001000	10	11111111	11	Second command byte second time
11111111	11	11111111	01	Acknowledgement for the second command byte
11111111	11	10000001	10	IOM-2 Address first byte (answer)
11111111	01	10000001	10	IOM-2 Address second byte
11111111	01	11000000	11	Interrupt register INTREG1
11111111	11	11000000	10	Interrupt register INTREG1 second time
11111111	01	00000010	11	Interrupt register INTREG2
11111111	11	00000010	10	Interrupt register INTREG2 second time
11111111	01	00000000	11	Interrupt register INTREG3
11111111	11	00000000	10	Interrupt register INTREG3 second time
11111111	01	00000000	11	Interrupt register INTREG4
11111111	11	00000000	10	Interrupt register INTREG4 second time
11111111	11	01001101	11	SLICOFI-2S sends the next register
11111111	11	11111111	11	SLICOFI-2S aborts transmission

6 Electrical Characteristics

6.1 AC Transmission DuSLIC

The target figures in this specification are based on the subscriber linecard requirements. The proper adjustment of the programmable filters (transhybrid balancing, impedance matching, frequency-response correction) requires the consideration of the complete analog environment of the *SLICOFI-2x* device.

Functionality and performance are guaranteed for T_A = 0 to 70 °C by production testing. Extented temperature range operation at –40 °C < T_A < 85 °C is guaranteed by design, characterization and periodically sampling and testing production devices at the temperature extremes.

Test Conditions

T_A = –40 °C to 85 °C, unless otherwise stated.

$V_{DDD} = V_{DDA} = V_{DDB} = V_{DDR} = V_{DDPLL}$ = 3.3 V ±5%;

$V_{GNDA} = V_{GNDB} = V_{GNDR} = V_{GNDD} = V_{GNDPLL}$ = 0 V

R_L > 600 Ω; C_L < 10 pF

L_R = 0 … –10 dBr

L_X = 0 … +3 dBr

f = 1014 Hz; 0 dBm0; A-Law or µ-Law;

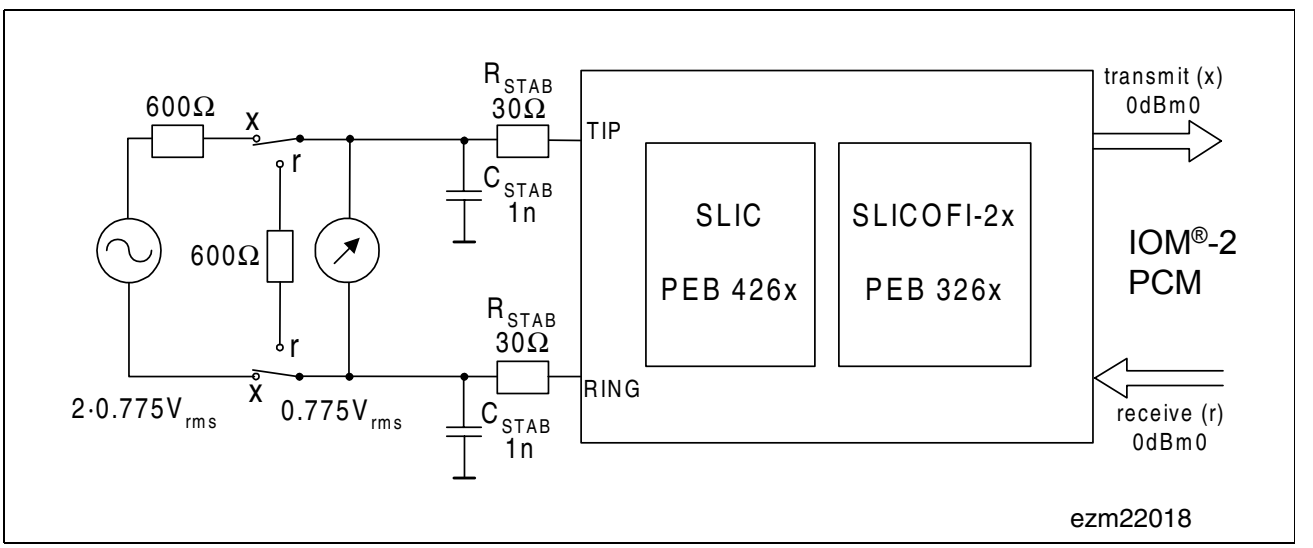


Figure 71 Signal Definitions Transmit, Receive

*Note: To ensure the stability of the SLIC output buffer, R_{STAB} and C_{STAB} must be set to the values R_{STAB} = 30 Ω and C_{STAB} ≥ 300 pF (1 nF in the test circuit **Figure 71**). For electromagnetic compatibility, C_{STAB} must be set to the much higher value of C_{STAB} = 15 nF.*

The 0 dBm0 definitions for Receive and Transmit are:

A 0 dBm0 AC signal in transmit direction is equivalent to 0.775 Vrms (referred to an impedance of 600 Ω).

A 0 dBm0 AC signal in receive direction is equivalent to 0.775 Vrms (referred to an impedance of 600 Ω).

L_R = –10 dBr means:

A signal of 0 dBm0 at the digital input corresponds to –10 dBm at the analog interface.

L_X = +3 dBr means:

A signal of 3 dBm at the analog interface corresponds to 0 dBm0 at the digital output.

Table 76 AC Transmission

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Longitudinal current capability AC	I_{ll}	per active line	30	–	–	mArms
Overload level	V_{TR}	300 - 4000 Hz	2.3	–	–	Vrms
Transmission Performance (2-wire)						
Return loss	RL	200 - 3600 Hz	26	–	–	dB
Insertion Loss (2-wire to 4-wire and 4-wire to 2-wire)						
Gain accuracy – Transmit	G_X	0 dBm0, 1014 Hz	–0.25	–	+0.25	dB
Gain accuracy – Receive	G_R	0 dBm0, 1014 Hz	–0.25	–	+0.25	dB
Gain variation with temperature –40 … +85 °C	–	–	–	–	±0.1	dB

Table 76 AC Transmission (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Frequency Response (see Figure 73 and Figure 74)						
Receive loss Frequency variation	G_{RAF}	Reference frequency 1014 Hz, signal level 0 dBm0, H_{FRR} = 1				
		f = 0 - 300 Hz	–0.25	–	–	dB
		f = 300 - 400 Hz	–0.25	–	0.9	dB
		f = 400 - 600 Hz	–0.25	–	0.65	dB
		f = 600 - 2400 Hz	–0.25	–	0.25	dB
		f = 2400 - 3000 Hz	–0.25	–	0.45	dB
		f = 3000 - 3400 Hz	–0.25	–	1.4	dB
		f = 3400 - 3600 Hz	–0.25	–	–	dB
Transmit loss Frequency variation	G_{XAF}	Reference frequency 1014 Hz, signal level 0 dBm0, H_{FRX} = 1				
		f = 0 - 200 Hz	0	–	–	dB
		f = 200 - 300 Hz	–0.25	–	–	dB
		f = 300 - 400 Hz	–0.25	–	0.9	dB
		f = 400 - 600 Hz	–0.25	–	0.65	dB
		f = 600 - 2400 Hz	–0.25	–	0.25	dB
		f = 2400 - 3000 Hz	–0.25	–	0.45	dB
		f = 3000 - 3400 Hz	–0.25	–	1.4	dB
		f = 3400 - 3600 Hz	–0.25	–	–	dB

Table 76 AC Transmission (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Gain Tracking (see Figure 75 and Figure 76)						
Transmit gain Signal level variation	G_{XAL}	Sinusoidal test method f = 1014 Hz, reference level –10 dBm0				
		VF_XI = –55 to –50 dBm0	–1.4	–	1.4	dB
		VF_XI = –50 to –40 dBm0	–0.5	–	0.5	dB
		VF_XI = –40 to +3 dBm0	–0.25	–	0.25	dB
Receive gain Signal level variation	G_{RAL}	Sinusoidal test method f = 1014 Hz, reference level –10 dBm0				
		D_R0 = –55 to –50 dBm0	–1.4	–	1.4	dB
		D_R0 = –50 to –40 dBm0	–0.5	–	0.5	dB
		D_R0 = –40 to +3 dBm0	–0.25	–	0.25	dB
Balance return loss		300 - 3400 Hz	26	–	–	dB
Group Delay (see Figure 77)						
Transmit delay, absolute	D_{XA}	f = 500 - 2800 Hz	400	490	585	µs
Receive delay, absolute	D_{RA}	f = 500 - 2800 Hz	290	380	475	µs
Group delay, Receive and Transmit, relative to 1500 Hz	D_{XR}	f = 500 - 600 Hz	–	–	300	µs
		f = 600 - 1000 Hz	–	–	150	µs
		f = 1000 - 2600 Hz	–	–	100	µs
		f = 2600 - 2800 Hz	–	–	150	µs
		f = 2800 - 3000 Hz	–	–	300	µs
Overload compression A/D	OC	–	–	–	–	–

Table 76 AC Transmission (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Longitudinal Balance (according to ITU-T O.9)						
Longitudinal conversion loss	L-T	300 - 1000 Hz				
		DuSLIC-S/-E/-P	53	58	–	dB
		DuSLIC-S2/-E2	60	65	–	dB
		3400 Hz				
		DuSLIC-S/-E/-P	52	55	–	dB
		DuSLIC-S2/-E2	56	59	–	dB
Input longitudinal interference loss	L-4	300 - 1000 Hz				
		DuSLIC-S/-E/-P	53	58	–	dB
		DuSLIC-S2/-E2	60	65	–	dB
		3400 Hz				
		DuSLIC-S/-E/-P	52	55	–	dB
		DuSLIC-S2/-E2	56	59	–	dB
Transversal to longitudinal	T-L	300 - 4000 Hz	46	–	–	dB
Longitudinal signal generation	4-L	300 - 4000 Hz	46	–	–	dB
TTX Signal Generation						
TTX signal	V_{TTX}	at 200 Ω	–	–	2.5	Vrms
Out-of-Band Noise (Single Frequency Inband –25 dBm0)						
Transversal	V_{TR}	12 kHz - 200 kHz	–	–55	–50	dBm
Longitudinal	V_{TR}	12 kHz - 200 kHz	–	–55	–50	dBm
Out-of-Band Idle Channel Noise at Analog Output Measured with 3 kHz Bandwidth						
	V_{TR}	10 kHz	–	–	–50	dBm
	V_{TR}	300 kHz	–	–	–50	dBm
	V_{TR}	500 kHz	–	–	–70	dBm
	V_{TR}	1000 kHz	–	–	–70	dBm

Table 76 AC Transmission (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Out-of-Band Signals at Analog Output (Receive) (see Figure 78)						
Out-of-Band Signals at Analog Input (Transmit) (see Figure 79)						
Total Harmonic Distortion						
2-wire to 4-wire	THD4	–7 dBm0, 300 - 3400 Hz	–	–50	–44	dB
4-wire to 2-wire	THD2	–7 dBm0, 300 - 3400 Hz	–	–50	–44	dB
Idle Channel Noise						
2-wire port (receive)	N_{RP}	Psophometric				
A-Law		TTX disabled	–	–	–74	dBmp
		TTX enabled	–	–	–70	dBmp
µ-Law	N_{RC}	C message				
		TTX disabled	–	–	16	dBrnC
		TTX enabled	–	–	20	dBrnC
PCM side (transmit)	N_{TP}	Psophometric				
A-Law		TTX disabled	–	–	–69	dBm0p
		TTX enabled	–	–	–67	dBm0p
µ-Law	N_{TC}	C message				
		TTX disabled	–	–	18	dBrnC
		TTX enabled	–	–	20	dBrnC

Table 76 AC Transmission (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Distortion (Sinusoidal Test Method, see Figure 81, Figure 80 and Figure 82)						
Signal to total distortion Transmit	STD_X	Output connection: L_X = 0 dBr f = 1014 Hz (C message-weighted for µ-Law, psophometrically weighted for A-Law), TTX-DIS = 1				
		–45 dBm0	24	–	–	dB
		–40 dBm0	29	–	–	dB
		–30 dBm0	35	–	–	dB
		–20 dBm0	36	–	–	dB
		–10 dBm0	36	–	–	dB
		3 dBm0	36	–	–	dB
Signal to total distortion Transmit	STD_X	Output connection: L_X = 0 dBr f = 1014 Hz (C message-weighted for µ-Law, psophometrically weighted for A-Law), TTX-DIS = 0				
		–45 dBm0	23	–	–	dB
		–40 dBm0	28	–	–	dB
		–30 dBm0	34	–	–	dB
		–20 dBm0	36	–	–	dB
		–10 dBm0	36	–	–	dB
		3 dBm0	36	–	–	dB
Signal to total distortion Receive	STD_R	Input connection: L_R = –7 dBr f = 1014 Hz (C message-weighted for µ-Law, psophometrically weighted for A-Law), TTX-DIS = 1				
		–45 dBm0	21	–	–	dB
		–40 dBm0	26	–	–	dB
		–30 dBm0	33	–	–	dB
		–20 dBm0	35.5	–	–	dB
		–10 dBm0	36	–	–	dB
		3 dBm0	36	–	–	dB

Table 76 AC Transmission (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Signal to total distortion Receive	STD_R	Input connection: L_R = –7 dBr f = 1014 Hz (C message-weighted for µ-Law, psophometrically weighted for A-Law), TTX-DIS = 0				
		–45 dBm0	19	–	–	dB
		–40 dBm0	23.5	–	–	dB
		–30 dBm0	31	–	–	dB
		–20 dBm0	35.5	–	–	dB
		–10 dBm0	36	–	–	dB
		3 dBm0	36	–	–	dB
Signal to total distortion Receive	STD_R	Input connection: L_R = 0 dBr f = 1014 Hz (C message-weighted for µ-Law, psophometrically weighted for A-Law), TTX-DIS = 1				
		–45 dBm0	24	–	–	dB
		–40 dBm0	29	–	–	dB
		–30 dBm0	35	–	–	dB
		–20 dBm0	36	–	–	dB
		–10 dBm0	36	–	–	dB
		3 dBm0	36	–	–	dB
Signal to total distortion Receive	STD_R	Input connection: L_R = 0 dBr f = 1014 Hz (C message-weighted for µ-Law, psophometrically weighted for A-Law), TTX-DIS = 0				
		–45 dBm0	23	–	–	dB
		–40 dBm0	28	–	–	dB
		–30 dBm0	34	–	–	dB
		–20 dBm0	36	–	–	dB
		–10 dBm0	36	–	–	dB
		3 dBm0	36	–	–	dB

Table 76 AC Transmission (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Power Supply Rejection Ratio						
V_{DD}/V_{TR} (SLIC)	PSRR	300 - 3400 Hz ACTL, ACTH	33	–	–	dB
V_{DDi}/V_{TR} (*SLICOFI-2x*) i = A, B, D, R, PLL	PSRR	300 - 3400 Hz ACTL, ACTH	27	–	–	dB
V_{BATH}/V_{TR}, V_{BATL}/V_{TR} (SLIC)	PSRR	300 - 3400 Hz	33	–	–	dB

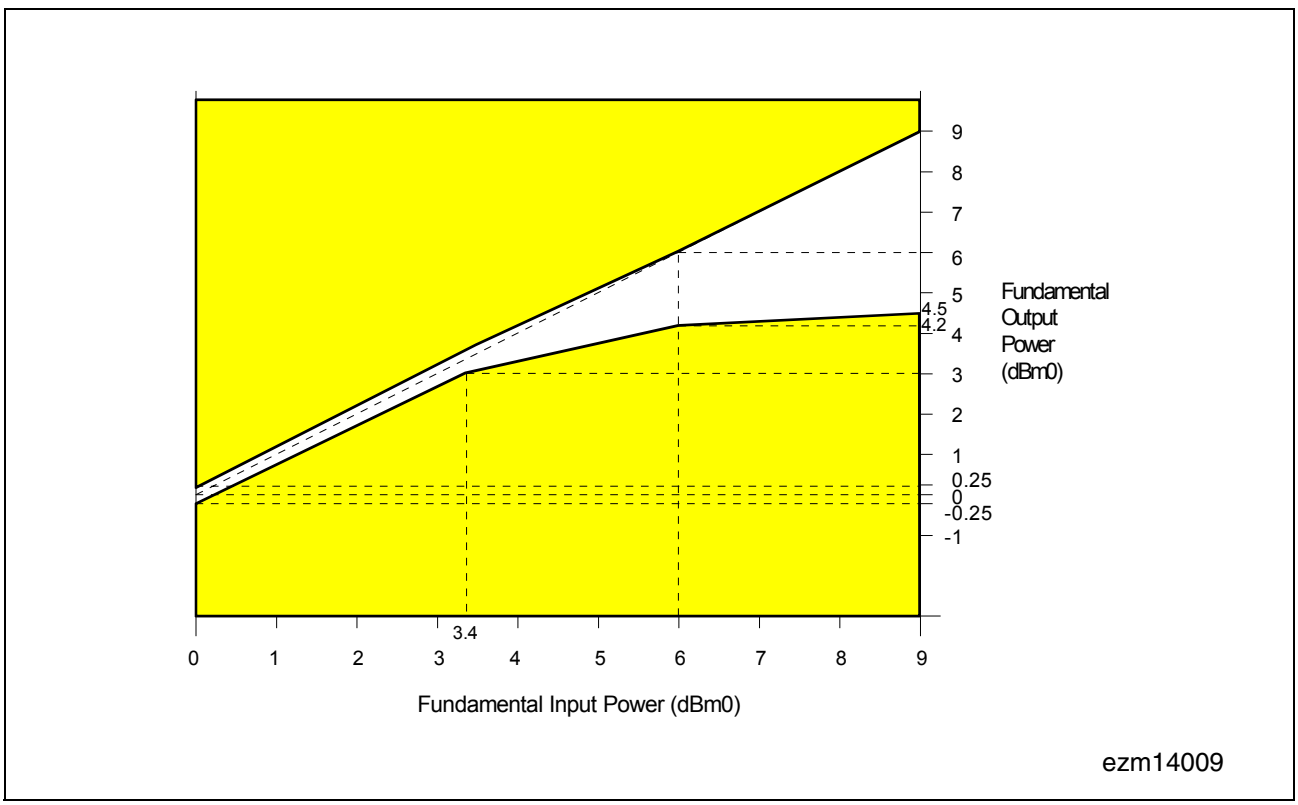


Figure 72 Overload Compression

6.1.1 Frequency Response

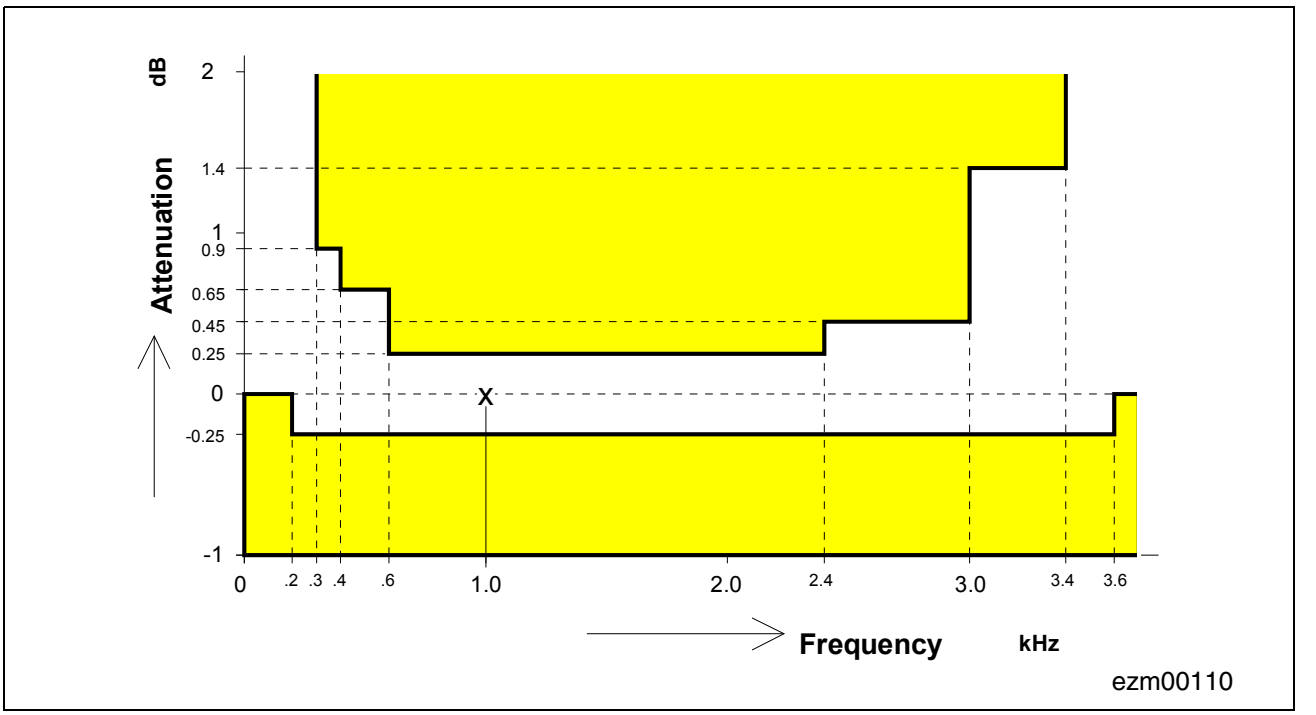


Figure 73 Frequency Response Transmit

Reference frequency 1 kHz, signal level 0 dBm0, H_{FRX} = 1

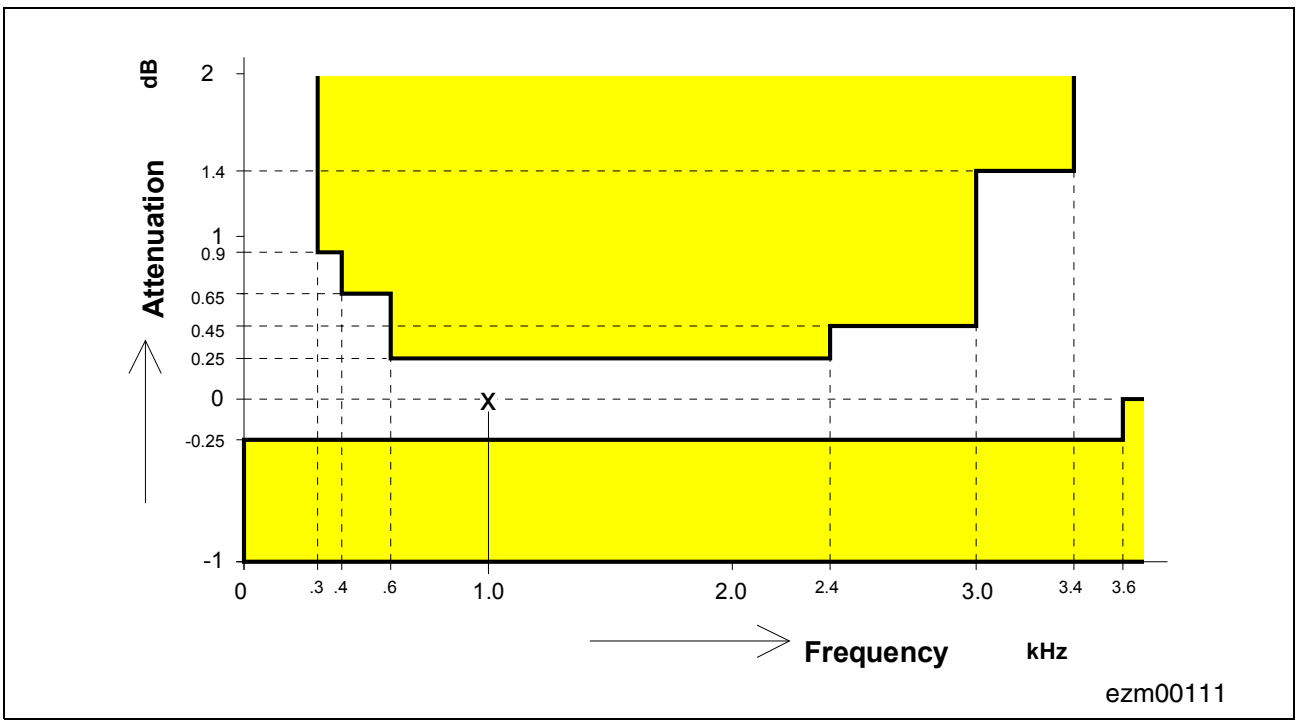


Figure 74 Frequency Response Receive

Reference frequency 1 kHz, signal level 0 dBm0, H_{FRR} = 1

6.1.2 Gain Tracking (Receive or Transmit)

The gain deviations stay within the limits in the figures below.

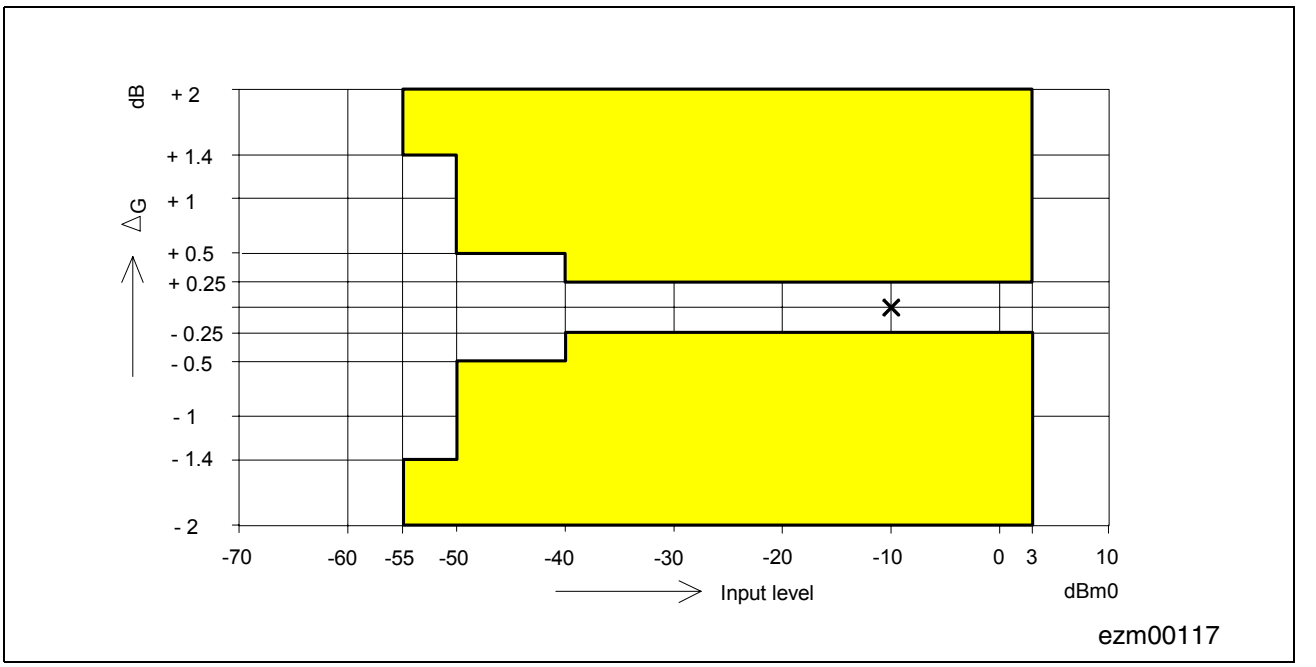


Figure 75 Gain Tracking Receive

Measured with a sine wave of f = 1014 Hz, reference level is –10 dBm0

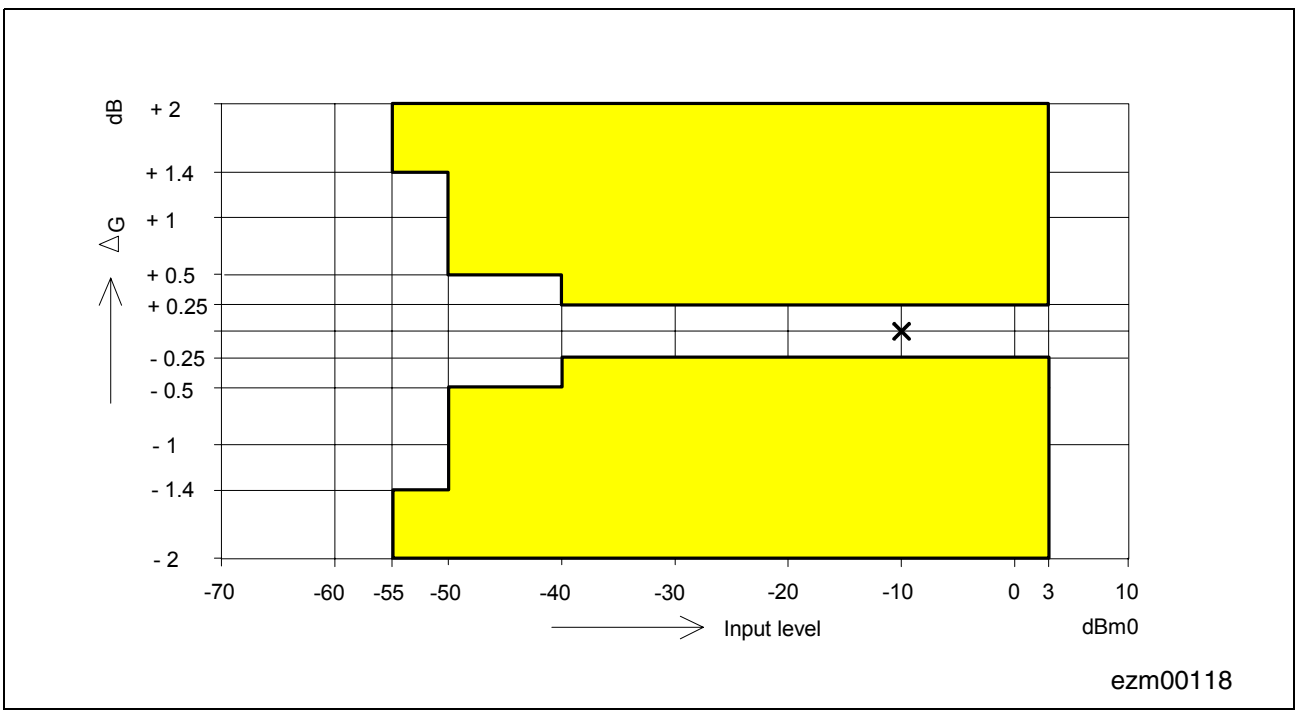


Figure 76 Gain Tracking Transmit

Measured with a sine wave of f = 1014 Hz, reference level is –10 dBm0

6.1.3 Group Delay

Minimum delays occur when both Frequency Response Receive and Transmit filters (bit FRR-DIS and bit FRX-DIS in register BCR4 set to 1) are disabled. That includes the delay through A/D and D/A converters. Specific filter programming may cause additional group delays. Absolute Group delay also depends on the programmed time slot.

Group delay distortion stays within the limits in the figures below.

Table 77 Group Delay Absolute Values: Signal level 0 dBm0

Parameter	Symbol	Limit Values			Unit	Test Condition	Fig.
		min.	typ.	max.			
Transmit delay	D_{XA}	400	490	585	µs	f = 1.5 kHz	–
Receive delay	D_{RA}	290	380	475	µs	f = 1.5 kHz	–

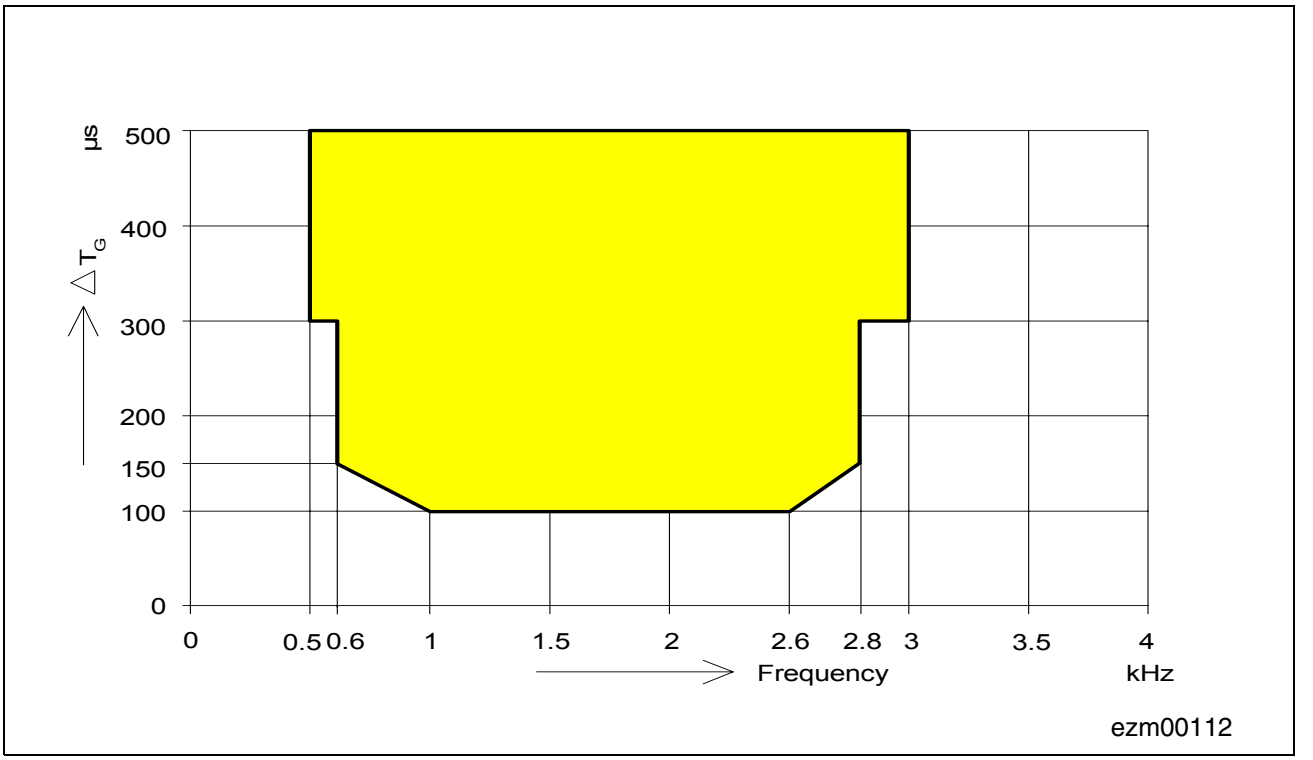


Figure 77 Group Delay Distortion Receive and Transmit

Signal level 0 dBm0

6.1.4 Out-of-Band Signals at Analog Output (Receive)

With a 0 dBm0 sine wave with a frequency of f (300 Hz to 3.4 kHz) applied to the digital input, the level of any resulting out-of-band signal at the analog output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog output.

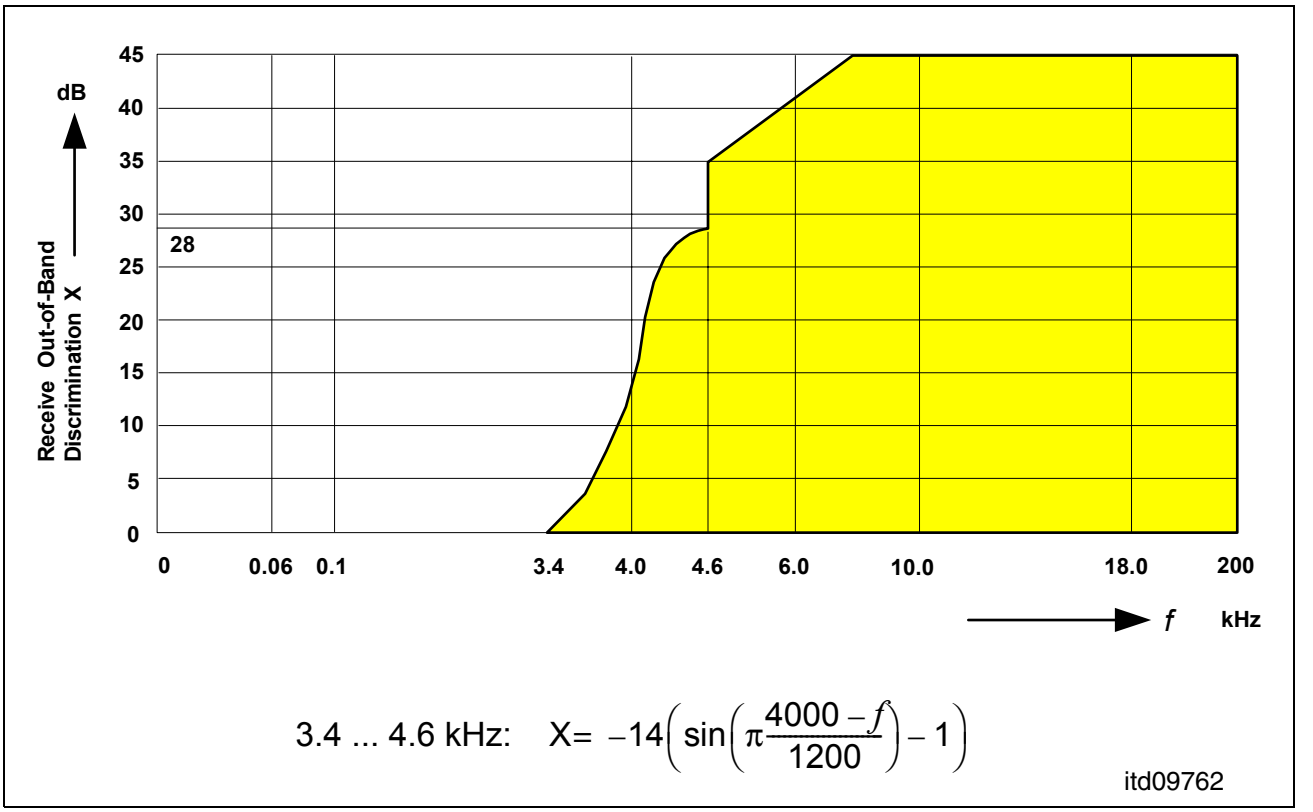
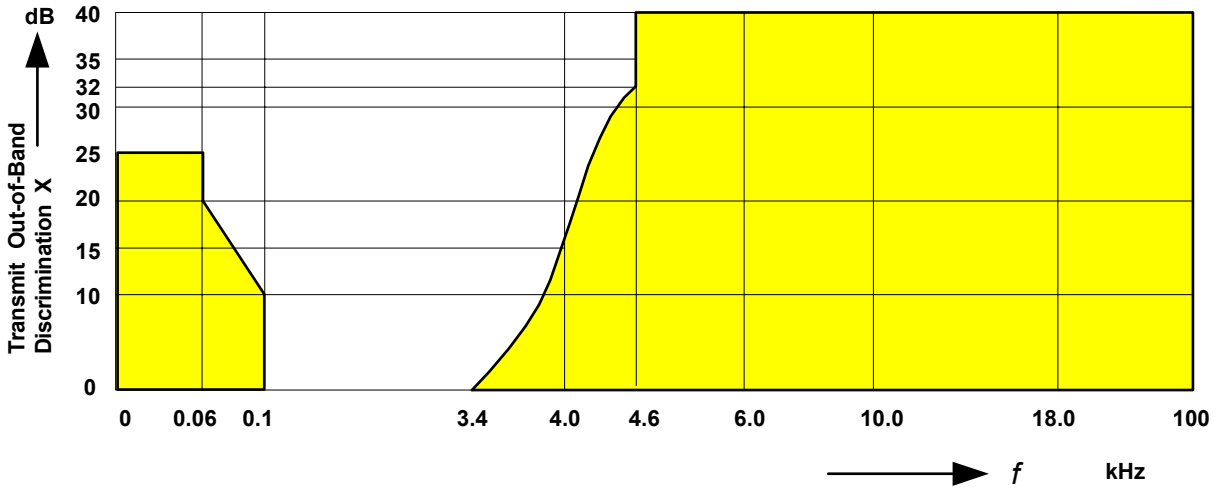


Figure 78 Out-of-Band Signals at Analog Output (Receive)

6.1.5 Out-of-Band Signals at Analog Input (Transmit)

With a 0 dBm0 out-of-band sine wave signal with a frequency of f (< 100 Hz or 3.4 kHz to 100 kHz) applied to the analog input, the level of any resulting frequency component at the digital output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog input.[1)]



$$3.4 \ldots 4.0\ \text{kHz}: \quad X = -14\left(\sin\left(\pi\frac{4000 - f}{1200}\right) - 1\right)$$

$$4.0 \ldots 4.6\ \text{kHz}: \quad X = -18\left(\sin\left(\pi\frac{4000 - f}{1200}\right) - \frac{7}{9}\right)$$

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Figure 79 Out-of-Band Signals at Analog Input (Transmit)

1) Poles at 12 kHz ±150 Hz and 16 kHz ±150 Hz respectively and harmonics will be provided

6.1.6 Total Distortion Measured with Sine Wave

The signal to total distortion ratio exceeds the limits in the following figure:

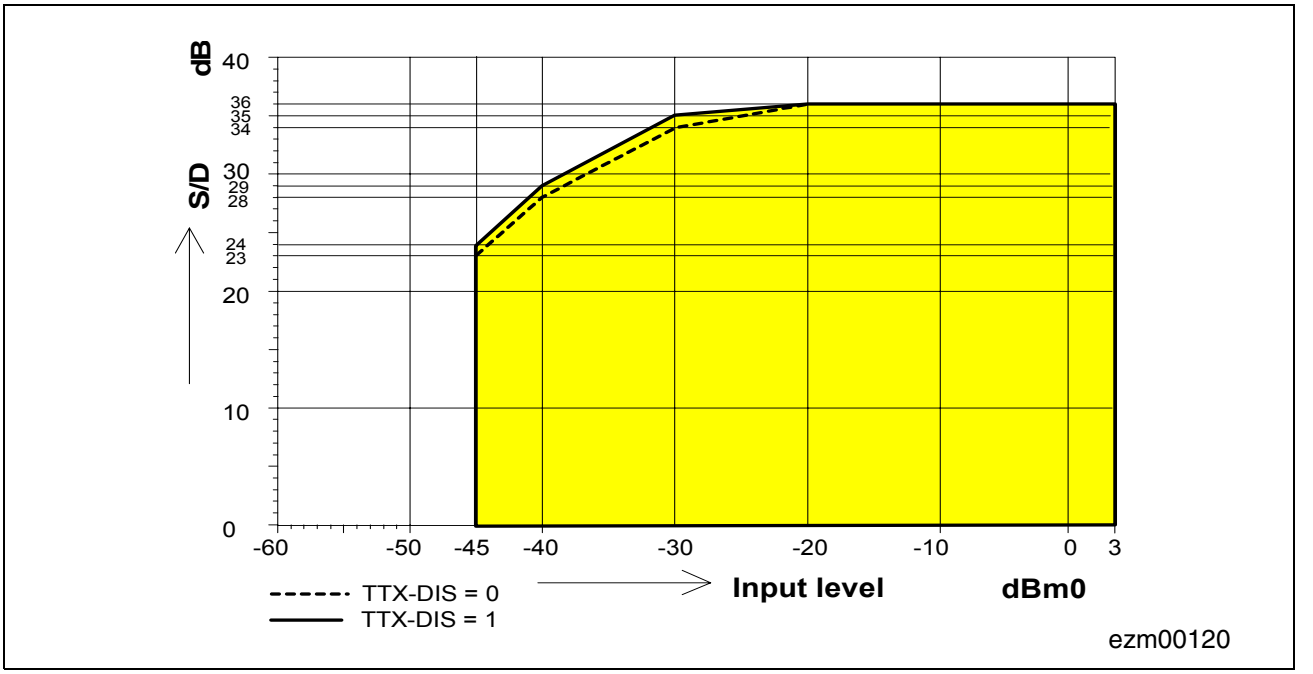


Figure 80 Total Distortion Transmit (L_X = 0 dBr)

Measured with a sine wave of f = 1014 Hz (C message-weighted for µ-Law, psophometrically weighted for A-Law)

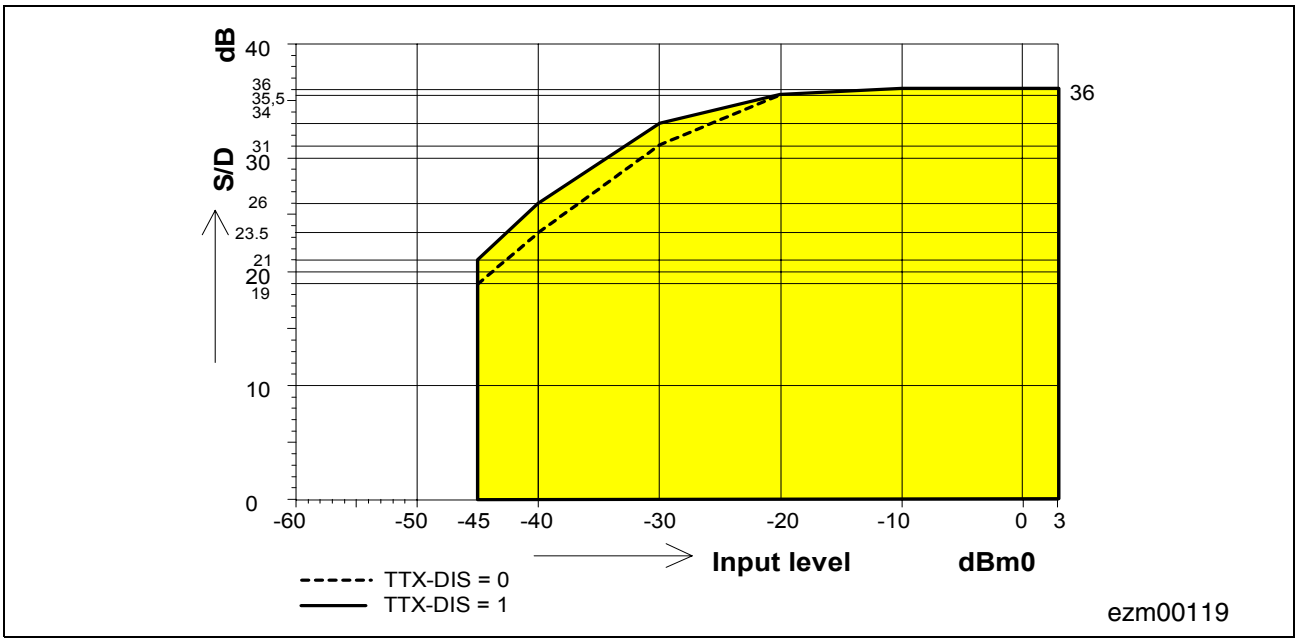


Figure 81 Total Distortion Receive (L_R = –7 dBr)

Measured with a sine wave of f = 1014 Hz (C message-weighted for µ-Law, psophometrically weighted for A-Law)

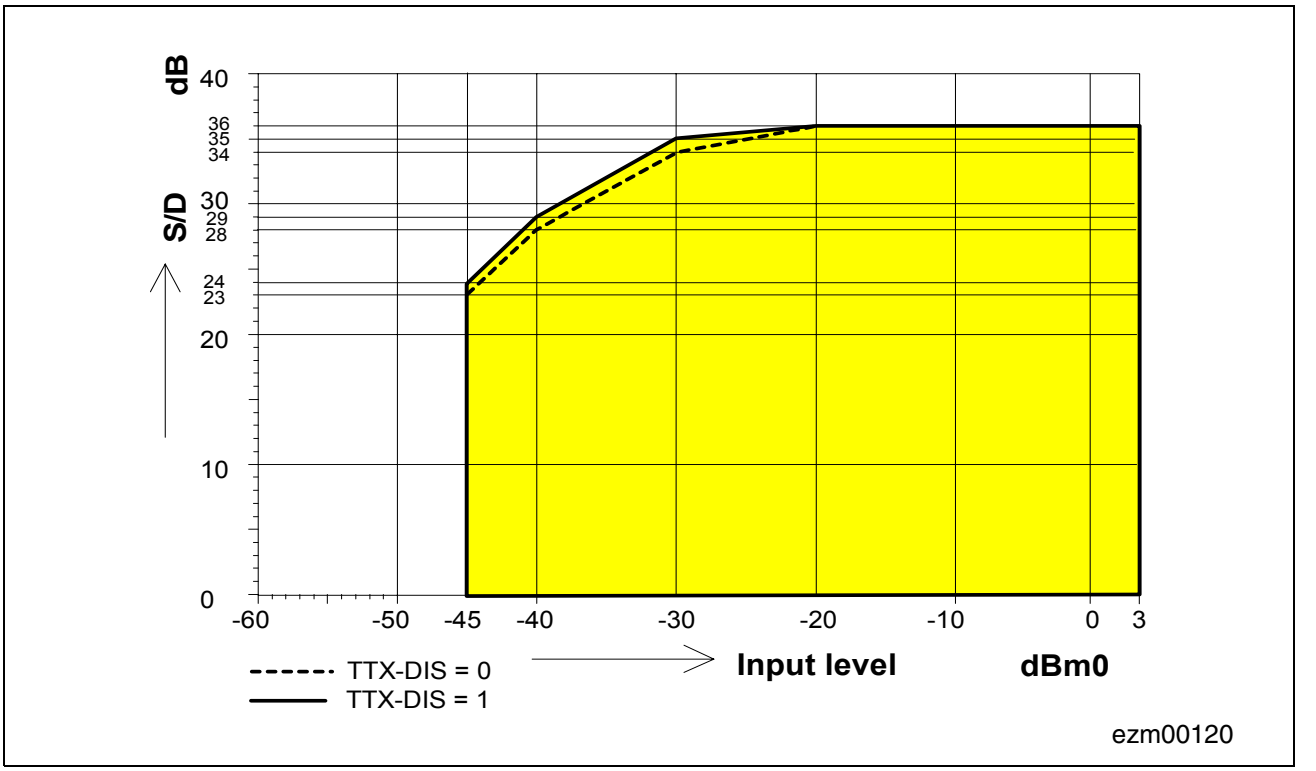


Figure 82 Total Distortion Receive (L_R = 0 dBr)

Measured with a sine wave of f = 1014 Hz (C message-weighted for µ-Law, psophometrically weighted for A-Law)

6.2 DC Characteristics

T_A = –40 °C to 85 °C, unless otherwise stated.

Table 78 DC Characteristics

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Line Termination Tip, Ring						
Sinusoidal Ringing						
Max. ringing voltage	V_{RNG0}	$V_{HR} - V_{BATH}$ = 150 V, V_{DC} = 20 V for ring trip (DuSLIC-E/-E2)	85	–	–	Vrms
		$-V_{BATR}$ = 150 V, V_{DC} = 20 V for ring trip (DuSLIC-P)	85	–	–	Vrms
		$V_{HR} - V_{BATH}$ = 90 V, V_{DC} = 20 V for ring trip (DuSLIC-S/-S2)	45	–	–	Vrms
Output impedance	R_{OUT}	SLIC output buffer and R_{STAB}	–	61	–	Ω
Harmonic distortion	THD	–	–	–	5	%
Output current limit	$\|I_{R, max.}\|$, $\|I_{T, max.}\|$	Modes: Active		–		
		SLIC-E/-E2/-S/-S2:	80	105	130	mA
		SLIC-P:	70	90	110	mA
Loop current gain accuracy	–	–	–	–	3	%
Loop current offset error[1)]	–	–	–0.75	–	0.75	mA
Loop open resistance TIP to BGND	R_{TG}	Modes: Power Down I_T = 2 mA, T_A = 25 °C	–	5	–	kΩ
Loop open resistance RING to V_{BAT}	R_{BG}	Modes: Power Down I_R = 2 mA, T_A = 25 °C	–	5	–	kΩ
Ring trip function	–	–	–	–	–	–
Ring trip DC voltage	–	SLIC-E/-E2/-S/-S2:	0	–	30	Vdc
		SLIC-P: balanced	0	–	30	Vdc
		SLIC-P: unbalanced	–	$V_{BATR}/2$	–	Vdc

Table 78 DC Characteristics (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Ring trip detection time delay	–	–	–	–	2	cycle
Ring off time delay	–	–	–	–	2	cycle

1) can be reduced with current offset error compensation described in **Chapter 3.8.2.8**

6.3 DuSLIC Power Up

For power up of SLICOFI-2/-2S and SLIC devices please refer to the instructions given in the device data sheets.

6.4 DuSLIC Timing Characteristics

T_A = –40 °C to 85 °C, unless otherwise stated.

6.4.1 Input/Output Waveform for AC Tests

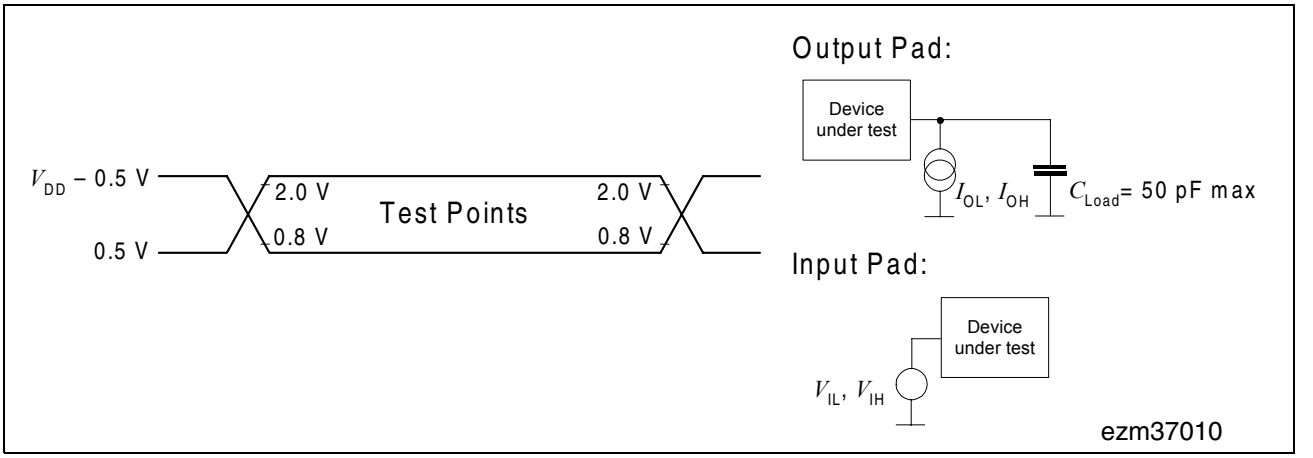


Figure 83 Waveform for AC Tests

During AC-Testing, the CMOS inputs are driven at a low level of 0.8 V and a high level of 2.0 V. The CMOS outputs are measured at 0.5 V and V_{DD} – 0.5 V respectively.

6.4.2 MCLK/FSC Timing

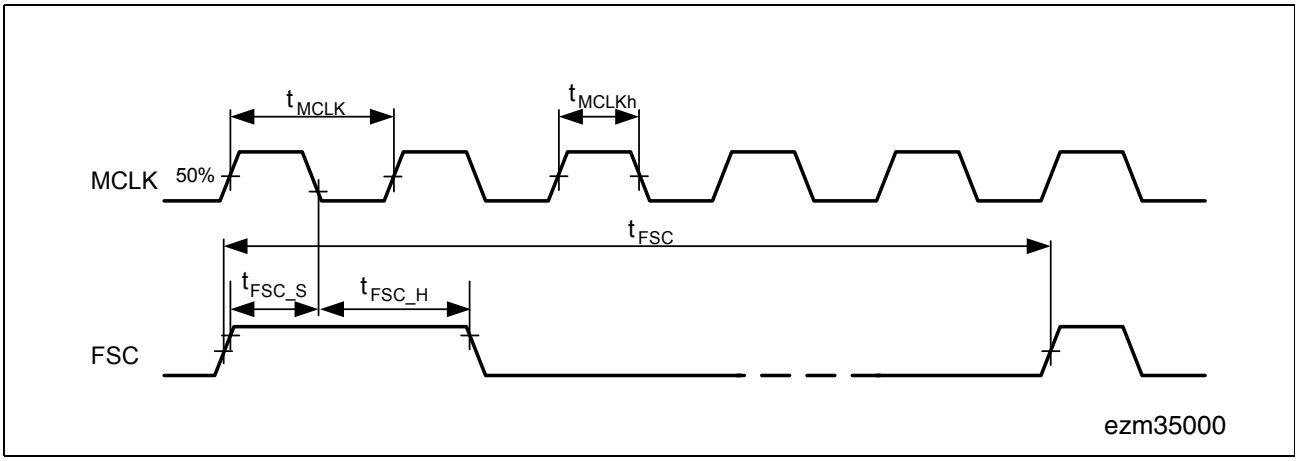


Figure 84 MCLK/FSC-Timing

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period MCLK[1)] 512 kHz ± 100 ppM 1536 kHz ± 100 ppM 2048 kHz ± 100 ppM 4096 kHz ± 100 ppM 7168 kHz ± 100 ppM 8192 kHz ± 100 ppM	t_{MCLK}	 1952.93 650.98 488.23 244.116 139.495 122.058	 1953.13 651.04 488.28 244.141 139.509 122.070	 1953.32 651.11 488.33 244.165 139.523 122.082	ns
MCLK high time	t_{MCLKh}	$0.4 \times t_{MCLK}$	$0.5 \times t_{MCLK}$	$0.6 \times t_{MCLK}$	µs
Period FSC[1)]	t_{FSC}	–	125	–	µs
FSC setup time	t_{FSC_s}	10	50	–	ns
FSC hold time	t_{FSC_h}	40	50	–	ns
FSC (or PCM) jitter time		$-0.2 \times t_{MCLK}$	–	$+0.2 \times t_{MCLK}$	ns

1) The MCLK frequency must be an integer multiple of the FSC frequency.

6.4.3 PCM Interface Timing

6.4.3.1 Single-Clocking Mode

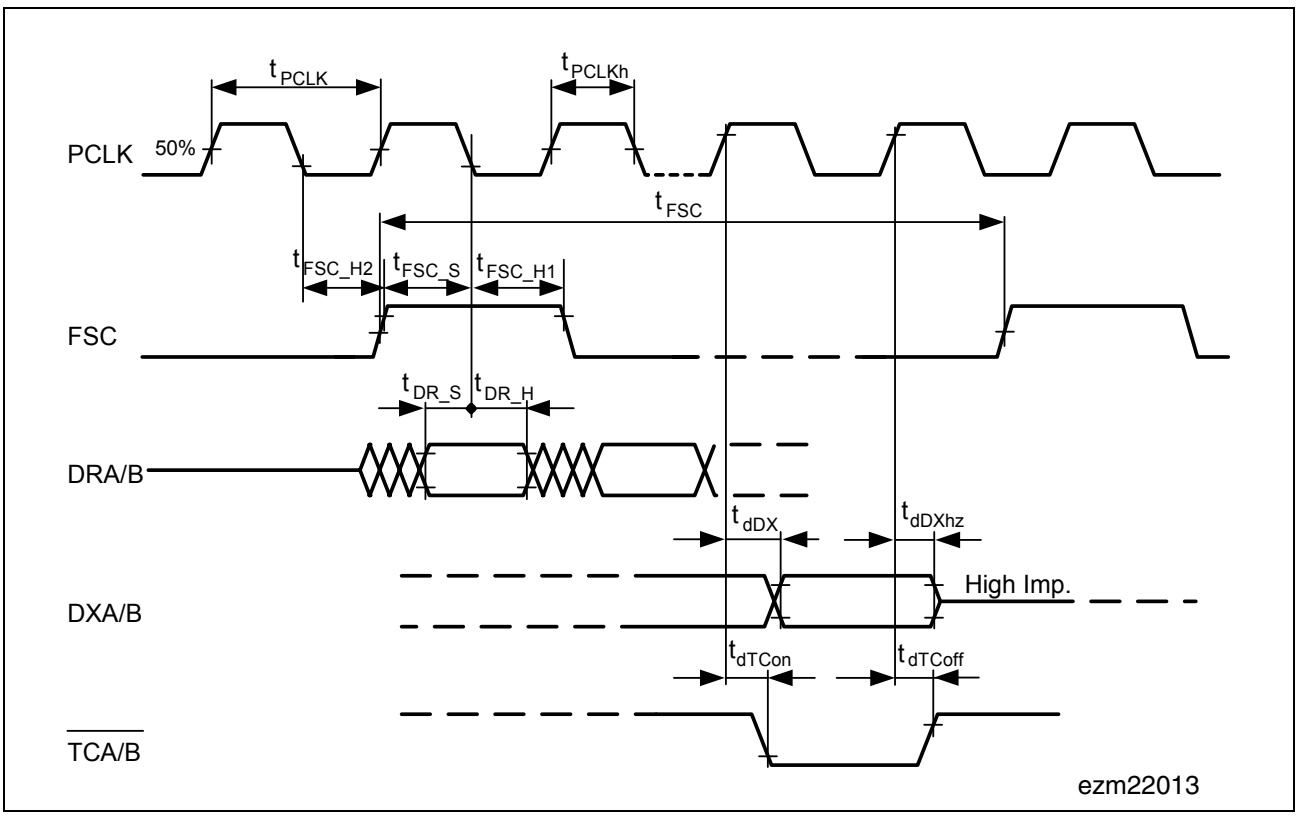


Figure 85 PCM Interface Timing – Single-Clocking Mode

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period PCLK[1)]	t_{PCLK}	1/8192	1/(n*64) with 2 ≤n ≤128	1/128	ms
PCLK high time	t_{PCLKh}	0.4 × t_{PCLK}	0.5 × t_{PCLK}	0.6 × t_{PCLK}	µs
Period FSC[1)]	t_{FSC}	–	125	–	µs
FSC setup time	t_{FSC_s}	10	50	–	ns
FSC hold time 1	t_{FSC_h1}	40	50	$t_{FSC} - t_{PCLK} - t_{FSC_s}$	ns
FSC hold time 2	t_{FSC_h2}	40	50	–	ns
DRA/B setup time	t_{DR_s}	10	50	–	ns
DRA/B hold time	t_{DR_h}	10	50	–	ns

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
DXA/B delay time[2)]	t_{dDX}	25	–	t_{dDX_min} + 0.4[ns/pF] × C_{Load}[pF]	ns
DXA/B delay time to high Z	t_{dDXhz}	25	–	50	ns
TCA/B delay time on	t_{dTCon}	25	–	t_{dTCon_min} + 0.4[ns/pF] × C_{Load}[pF]	ns
TCA/B delay time off	t_{dTCoff}	25	–	t_{dTCoff_min} + 2 × R_{Pullup}[kΩ] × C_{Load}[pF])	ns

1) The PCLK frequency must be an integer multiple of the FSC frequency.

2) All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load}, R_{Pullup} > 1.5 kΩ)

6.4.3.2 Double-Clocking Mode

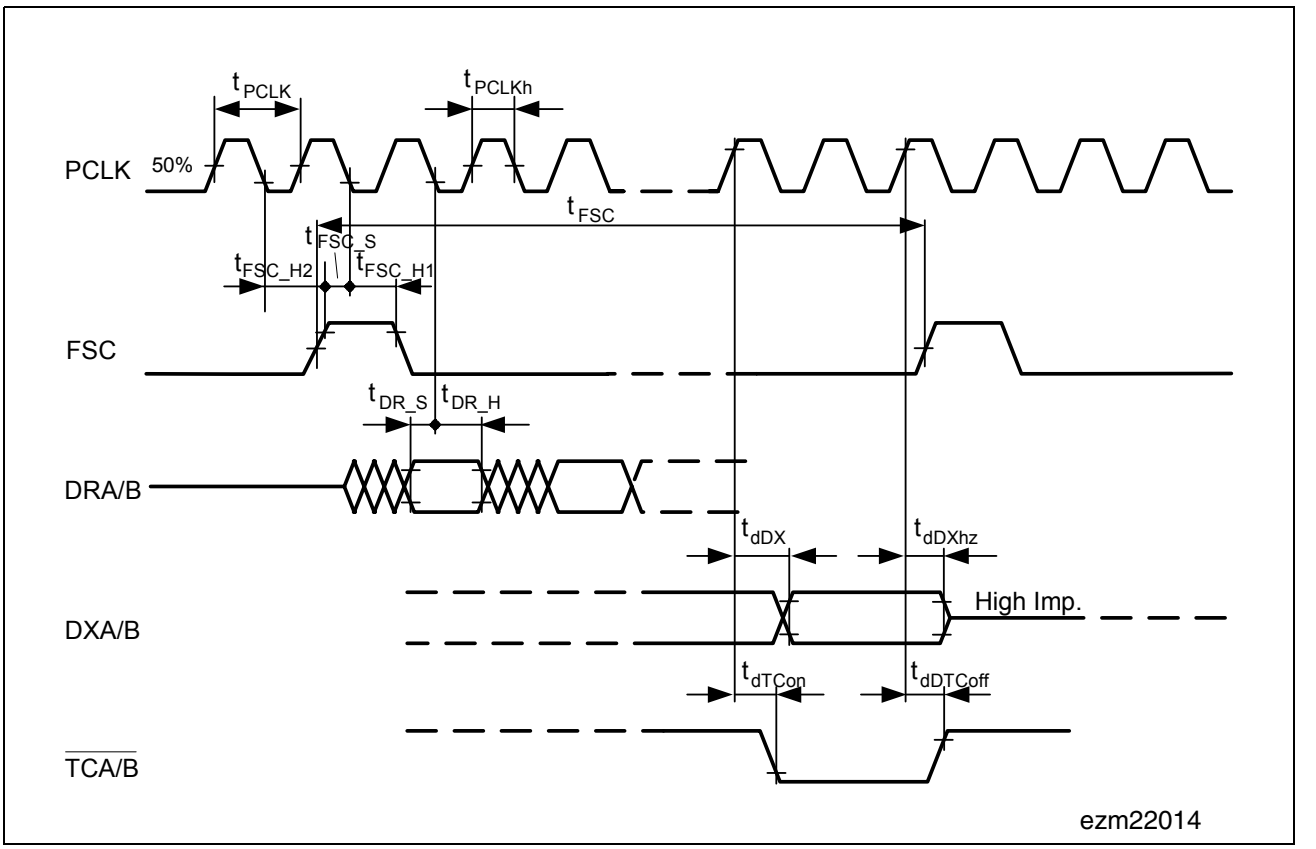


Figure 86 PCM Interface Timing – Double-Clocking Mode

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period PCLK[1]	t_{PCLK}	1/8192	1/(n*64) with 4 ≤n ≤128	1/256	ms
PCLK high time	t_{PCLKh}	0.4 × t_{PCLK}	0.5 × t_{PCLK}	0.6 × t_{PCLK}	µs
Period FSC[1]	t_{FSC}	–	125	–	µs
FSC setup time	t_{FSC_s}	10	50	–	ns
FSC hold time 1	t_{FSC_h1}	40	50	$t_{FSC} - t_{PCLK} - t_{FSC_s}$	ns
FSC hold time 2	t_{FSC_h2}	40	50	–	ns
DRA/B setup time	t_{DR_s}	10	50	–	ns
DRA/B hold time	t_{DR_h}	10	50	–	ns
DXA/B delay time[2]	t_{dDX}	25	–	t_{dDX_min} + 0.4[ns/pF] × C_{Load}[pF]	ns
DXA/B delay time to high Z	t_{dDXhz}	25	–	50	ns
TCA/B delay time on	t_{dTCon}	25	–	t_{dTCon_min} + 0.4[ns/pF] × C_{Load}[pF]	ns
TCA/B delay time off	t_{dTCoff}	25	–	t_{dTCoff_min} + 2 × R_{Pullup}[kΩ] × C_{Load}[pF])	ns

1) The PCLK frequency must be an integer multiple of the FSC frequency.

2) All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load}, R_{Pullup} > 1.5 kΩ)

6.4.4 Microcontroller Interface Timing

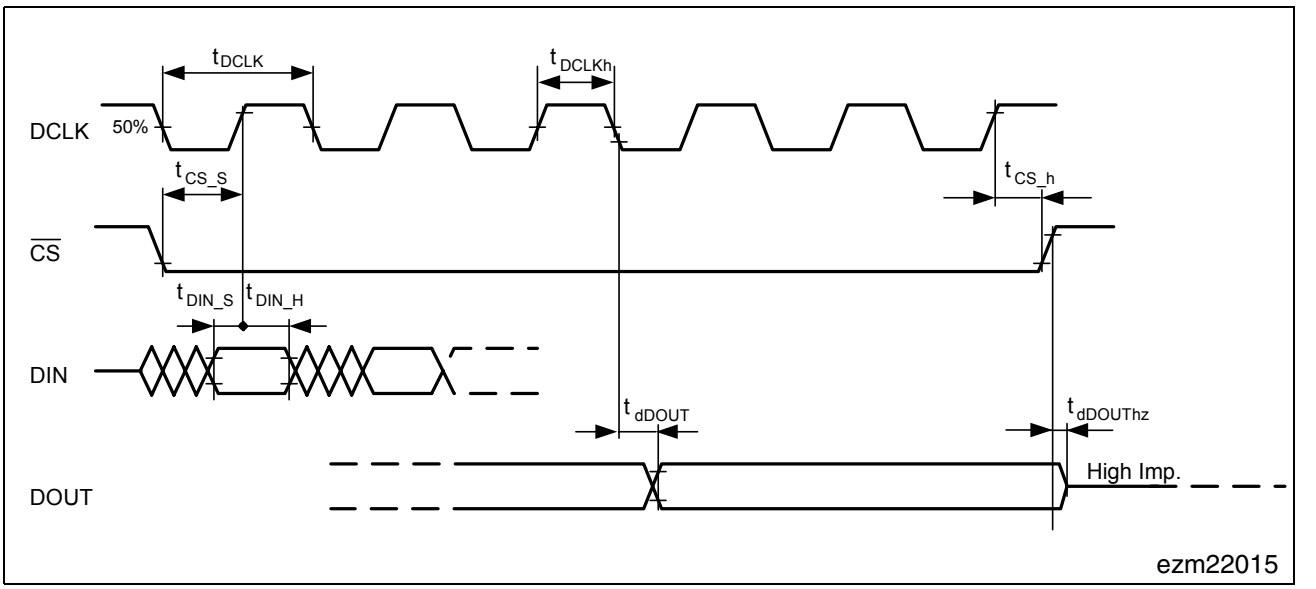


Figure 87 Microcontroller Interface Timing

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period DCLK	t_{DCLK}	1/8192	–	–	ms
DCLK high time	t_{DCLKh}	–	0.5 × t_{DCLK}	–	µs
CS setup time	t_{CS_s}	10	50	–	ns
CS hold time	t_{CS_h}	30	50	–	ns
DIN setup time	t_{DIN_s}	10	50	–	ns
DIN hold time	t_{DIN_h}	10	50	–	ns
DOUT delay time[1)]	t_{dDOUT}	30	–	t_{dDOUT_min} + 0.4[ns/pF] × C_{Load}[pF]	ns
DOUT delay time to high Z	$t_{dDOUThz}$	30	–	50	ns

1) All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load})

6.4.5 IOM-2 Interface Timing

6.4.5.1 Single-Clocking Mode

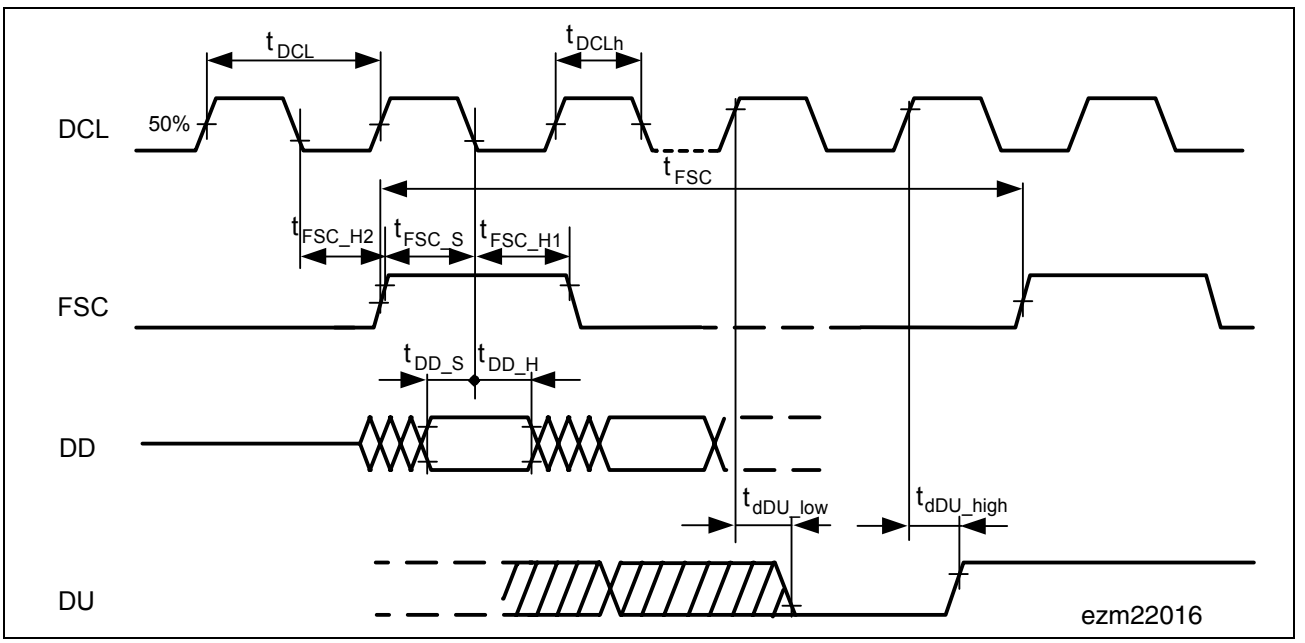


Figure 88 IOM-2 Interface Timing – Single-Clocking Mode

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period DCL[1)]	t_{DCL}	–	1/2048	–	ms
DCL high time	t_{DCLh}	0.4 × t_{DCL}	0.5 × t_{DCL}	0.6 × t_{DCL}	µs
Period FSC[1)]	t_{FSC}	–	125	–	µs
FSC setup time	t_{FSC_s}	10	50	–	ns
FSC hold time 1	t_{FSC_h1}	40	50	$t_{FSC} - t_{DCL} - t_{FSC_s}$	ns
FSC hold time 2	t_{FSC_h2}	40	50	–	ns
DD setup time	t_{DD_s}	10	50	–	ns
DD hold time	t_{DD_h}	10	50	–	ns
DU low time[2)]	t_{dDU_low}	25	–	$t_{dDU_low\ (min)}$ + 0.4[ns/pF] × C_{Load}[pF]	ns
DU high time[2)]	t_{dDU_high}	25	–	$t_{dDU_high\ (min)}$ + 2 × $R_{pull\text{-}up}$[kΩ] × C_{Load}[pF]	ns

1) The DCL frequency must be an integer multiple of the FSC frequency.

2) DU low and high times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load}, R_{Pullup} > 1.5 kΩ)

6.4.5.2 Double-Clocking Mode

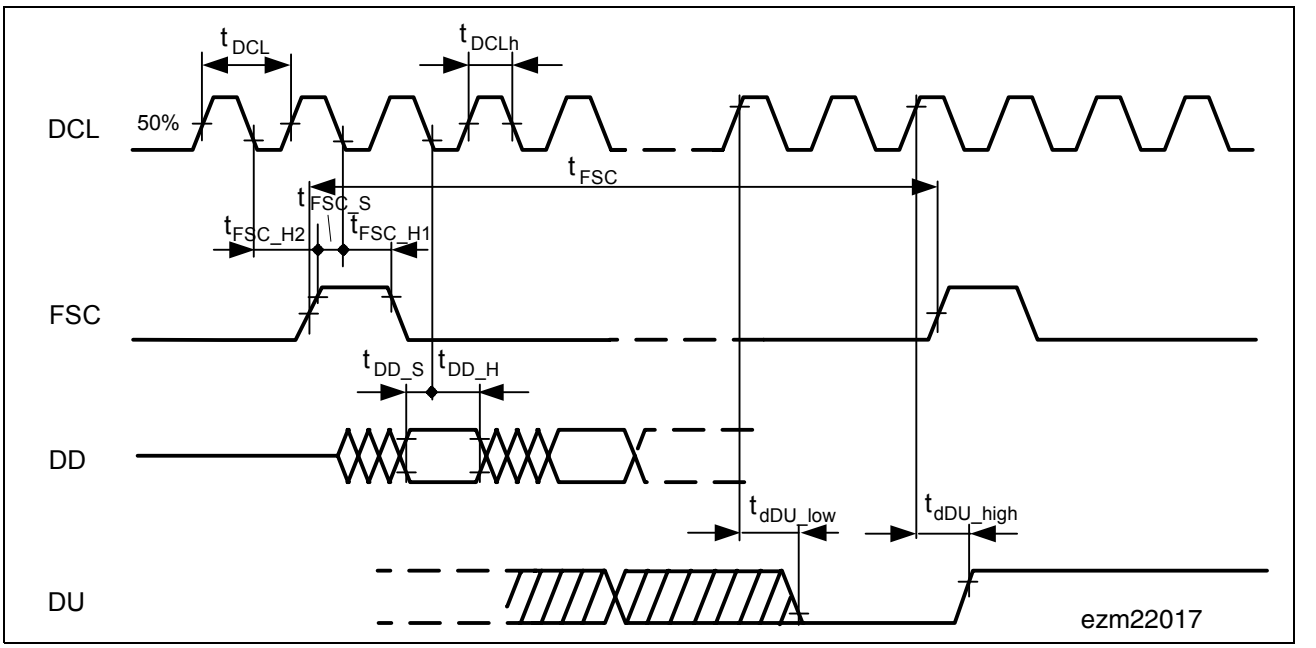


Figure 89 IOM-2 Interface Timing – Double-Clocking Mode

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period DCL[1)]	t_{DCL}	–	1/4096	–	ms
DCL high time	t_{DCLh}	0.4 × t_{DCL}	0.5 × t_{DCL}	0.6 × t_{DCL}	µs
Period FSC[1)]	t_{FSC}	–	125	–	µs
FSC setup time	t_{FSC_s}	10	50	–	ns
FSC hold time 1	t_{FSC_h1}	40	50	$t_{FSC} - t_{DCL} - t_{FSC_s}$	ns
FSC hold time 2	t_{FSC_h2}	40	50	–	ns
DD setup time	t_{DD_s}	10	50	–	ns
DD hold time	t_{DD_h}	10	50	–	ns
DU low time[2)]	t_{dDU_low}	25	–	$t_{dDU_low\ (min)}$ + 0.4[ns/pF] × C_{Load}[pF]	ns
DU high time[2)]	t_{dDU_high}	25	–	$t_{dDU_high\ (min)}$ + 2 × $R_{pull\text{-}up}$[kΩ] × C_{Load}[pF]	ns

1) The DCL frequency must be an integer multiple of the FSC frequency.

2) DU low and high times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load}, R_{Pullup} > 1.5 kΩ)

7 Application Circuits

Application circuits are shown for internal ringing with DuSLIC-E/-E2/-S/-P (balanced and unbalanced) and for external unbalanced ringing with DuSLIC-E/-E2/-S/-S2/-P for one line. Channel A and the SLIC must be duplicated in the circuit diagrams to show all necessary components for two channels.

7.1 Internal Ringing (Balanced/Unbalanced)

Internal balanced ringing is supported up to 85 Vrms for DuSLIC-E/-E2/-P and up to 45 Vrms for DuSLIC-S. Internal unbalanced ringing is supported for SLIC-P with ringing amplitudes up to 50 Vrms without any additional components. All DuSLIC chip sets incorporate internal off-hook- and ring trip detection.

7.1.1 Circuit Diagrams Internal Ringing (Balanced & Unbalanced)

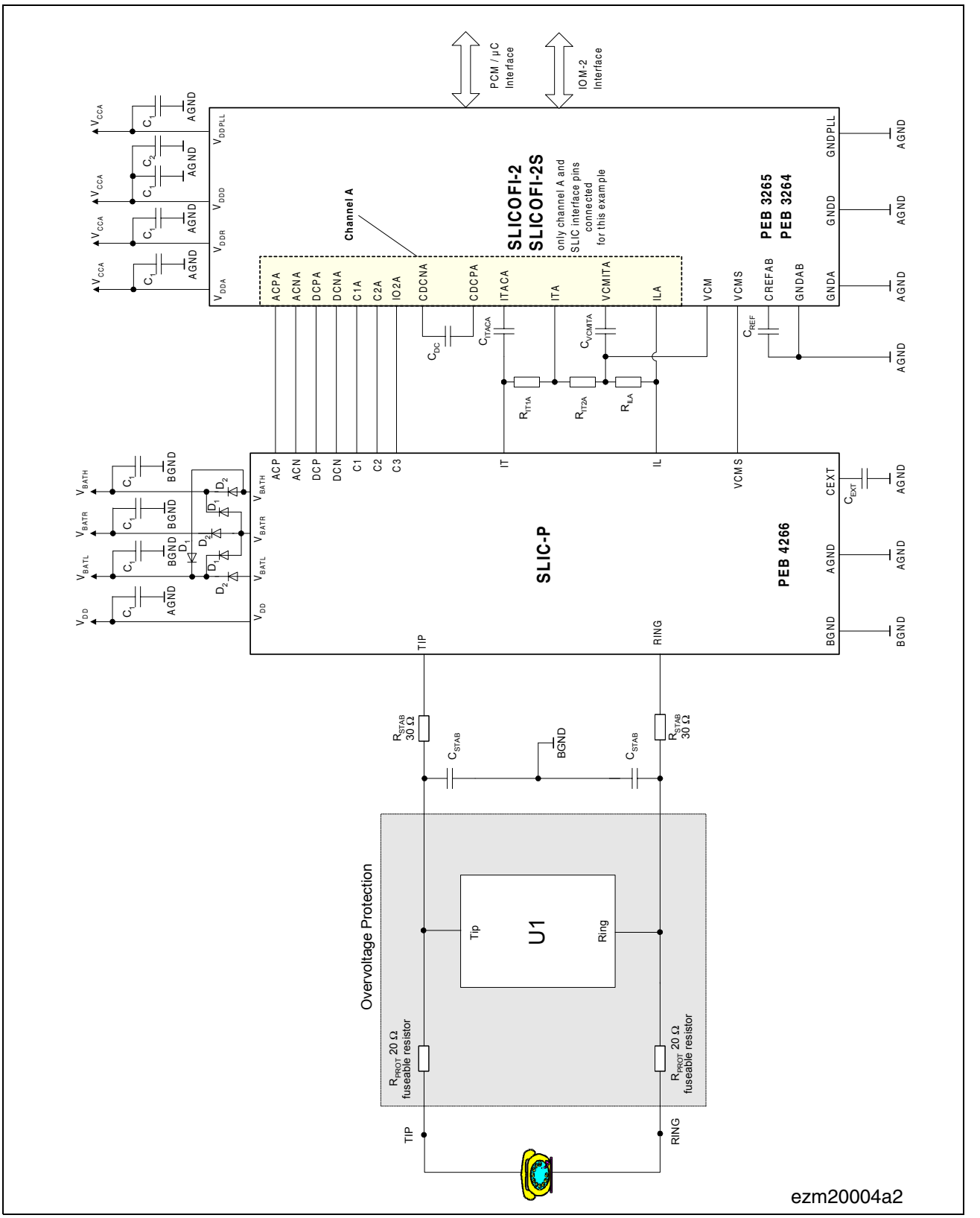


Figure 90 Internal (balanced and unbalanced) Ringing with SLIC-P

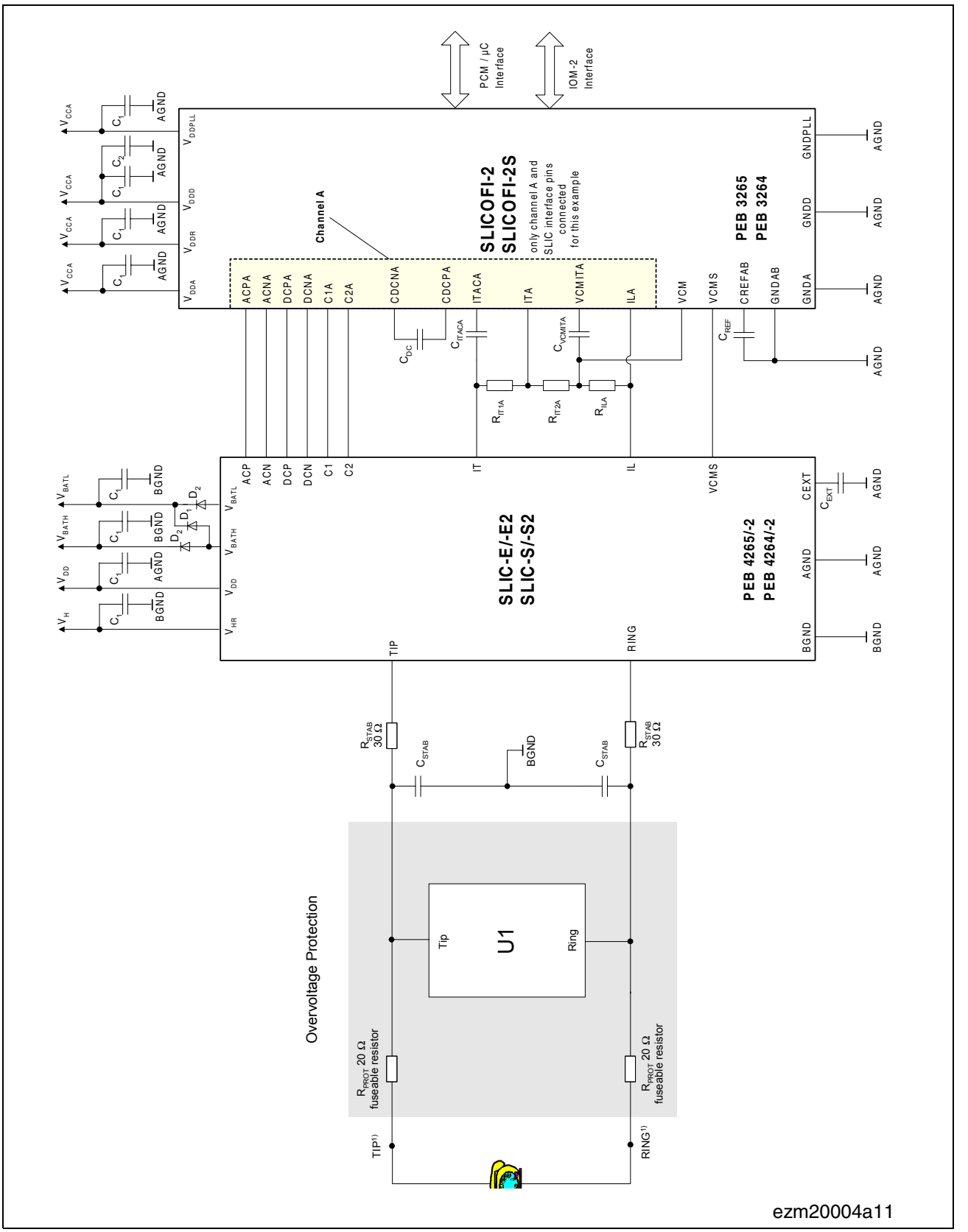


Figure 91 Internal (balanced) Ringing with SLIC-E/-E2 or SLIC-S/-S2

As **Figure 90** shows, balanced and unbalanced internal ringing use the same line circuit.

7.1.2 Bill of Materials

Table 79 shows the external passive components needed for a dual-channel solution consisting of one SLICOFI-2/-2S and two SLIC-E/-E2/-S/-S2/-P.

Table 79 External Components in Application Circuit DuSLIC-E/-E2/-S/-S2/-P

No.	Symbol	Value	Unit	Relat. Tol.	Rating
2	R_{IT1}	470	Ω	1 %	
2	R_{IT2}	680	Ω	1 %	
2	R_{IL}	1.6	kΩ	1 %	
4	R_{STAB}	30	Ω	1 %[1)]	
4	R_{PROT}[2)]	20	Ω	1 %[1)]	
4	C_{STAB}	15 (typ.)	nF	10 %	100 V
2	C_{DC}	120	nF	10 %	10 V
2	C_{ITAC}	680	nF	10 %	10 V
2	C_{VCMIT}	680	nF	10 %	10 V
1	C_{REF}	68	nF	20 %	10 V
2	C_{EXT}	470	nF	20 %	10 V
12	C_1	100 (typ.)	nF	10 %	
1	C_2[3)]	4.7	µF	20 %	10 V, Tantal
–	D_1[4)]	BAS21	–	–	–
4	D_2	BAS21	–	–	–
2	U_1[2)]	Overvoltage Protection Element	–	–	–

1) Matching tolerance dependent on longitudinal balance requirements (for details see the Application Note *External Components*).

2) See Application Note *Protection of DuSLIC / VINETIC Linecard Chip Sets against Overvoltages and Overcurrents*.

3) As close as possible connected to V_{DDD} and GNDD at SLICOFI-2

4) Optional; recommended only if power supply relation $V_{BATR} < V_{BATH} < V_{BATL}$ can not be guaranteed.

To handle higher electromagnetic compatibility (EMC) requirements, additional effort in the circuit design may be necessary, such as a current-compensated choke of 470 µH in the Tip/Ring lines. As well as the C_1 capacitors, one 22 µF capacitor per 8 Tip/Ring lines is recommended for buffering the supply voltages.

7.2 External Unbalanced Ringing with DuSLIC-E/-E2/-S/-S2/-P

External unbalanced ringing application circuits are shown for a standard solution (see **Figure 92** and **Figure 93**) and for a solution dedicated to higher loop lengths (see **Figure 94** and **Figure 95**).

*Note: Only the codec/SLIC combinations shown in **Table 3 "DuSLIC Chip Sets Presented in this Data Sheet" on Page 20** are possible.*

7.2.1 Circuit Diagrams External Unbalanced Ringing

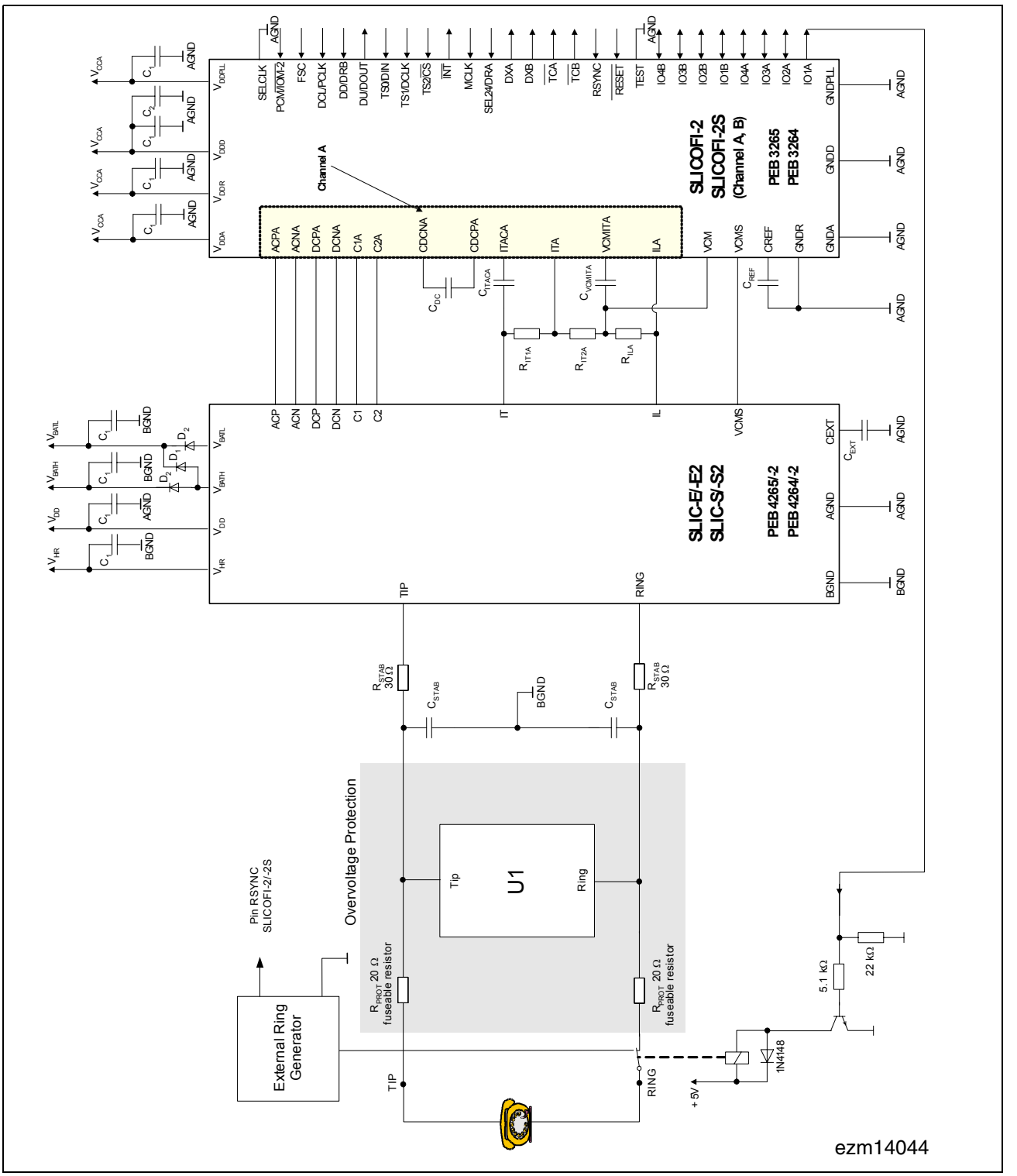


Figure 92 External Unbalanced Ringing with SLIC-E/-E2 or SLIC-S/-S2

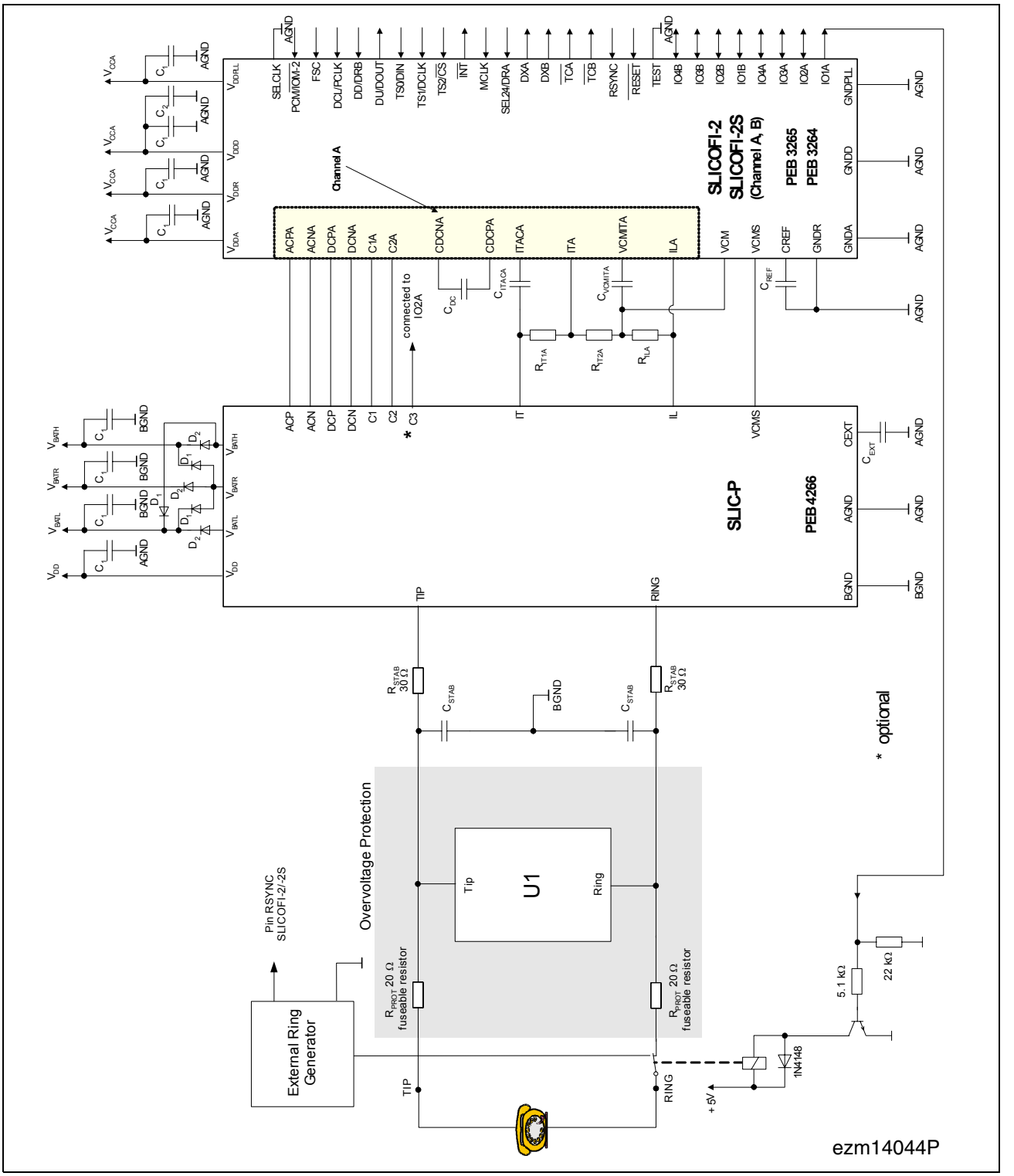


Figure 93 External Unbalanced Ringing with SLIC-P

In the circuits shown in **Figure 92** and **Figure 93** the ring current is sensed on only one line (Tip line). It is therefore restricted to applications with low longitudinal influence (short lines).

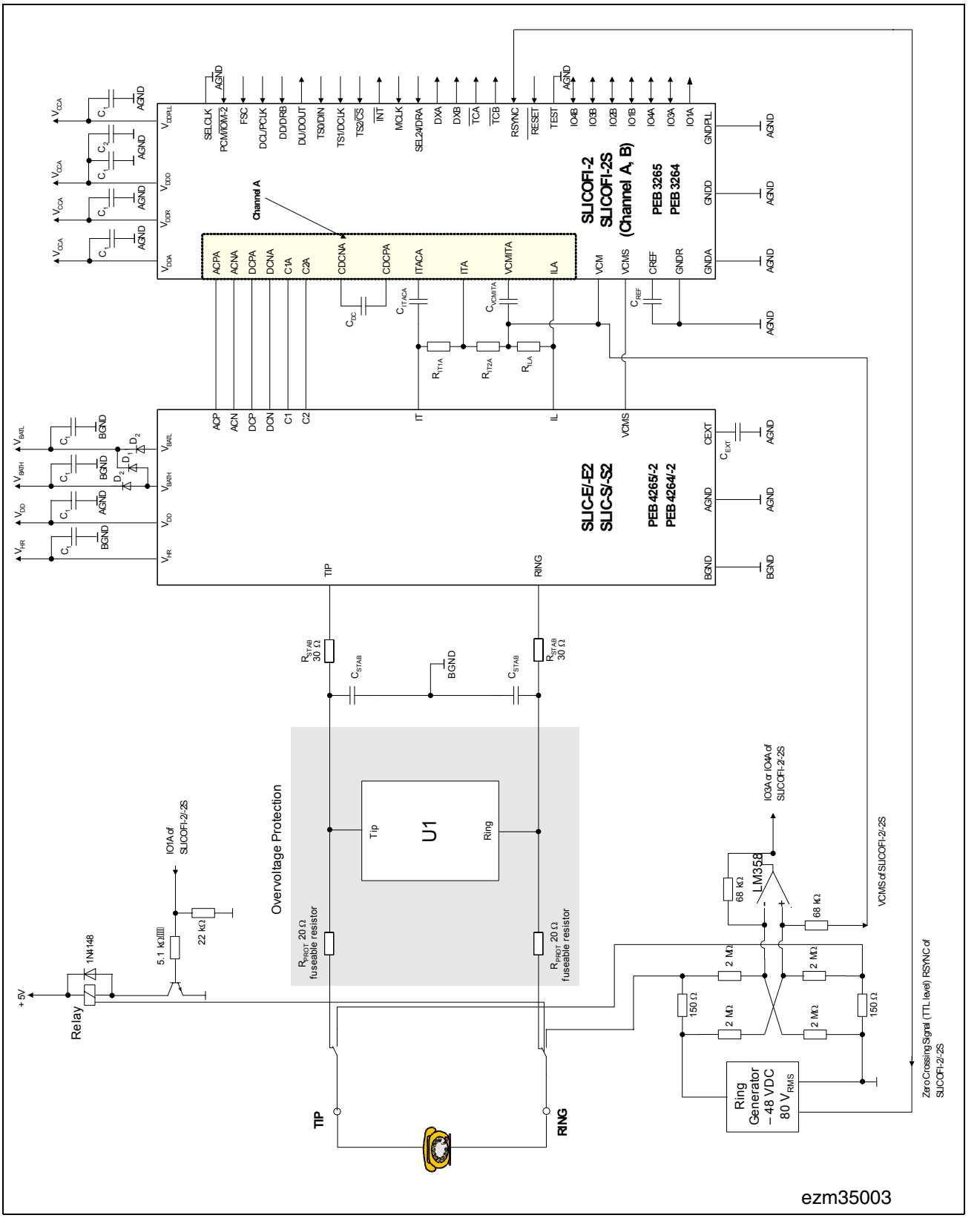


Figure 94 External Unb. Ringing (Long Loops) with SLIC-E/-E2 or SLIC-S/-S2

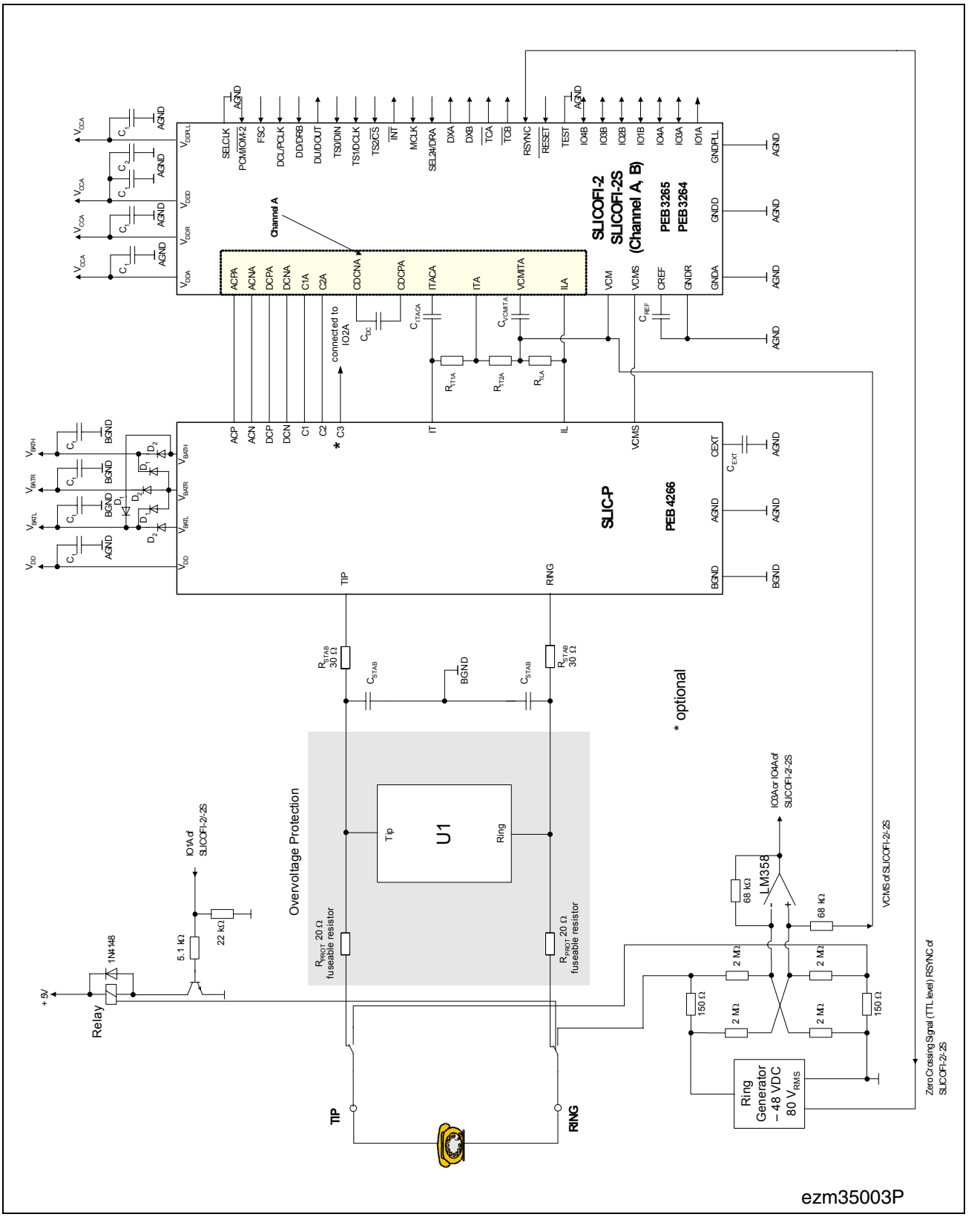


Figure 95 External Unbalanced Ringing (Long Loops) with SLIC-P

In the circuits shown in **Figure 94** and **Figure 95** the ring current is sensed in both Tip and Ring lines. Longitudinal influence is cancelled out. This circuit therefore is recommended for long line applications.

7.3 DuSLIC Layout Recommendations

- For each of the supply pins of *SLICOFI-2x* and SLIC, 100 nF capacitors should be used. These capacitors should be placed as close as possible to the supply pin of the associated ground/supply pins.
- *SLICOFI-2x* and SLIC should be placed as close to each other as possible.
- *SLICOFI-2x* and SLIC should be placed in such way that lines ACP, ACN, DCP, DCN, IT, ITAC are as short as possible.
- ACP/ACN lines should be placed in parallel and symmetrical; connections via holes should be avoided.
  ACP/ACN lines should be run above a GND plane;
- DCP/DCN lines should be placed in parallel and symmetrical; connections via holes should be avoided.
  DCP/DCN lines should be run above a GND plane
- VCMITA and VCM should be connected directly (VCMITA via C_{VCMITA}) at resistor R_{IT2A} (680 Ω).
- VCMITB and VCM should be connected directly (VCMITB via C_{VCMITB}) at resistor R_{IT2B} (680 Ω).
- Use separate traces for connecting VCM/VCMITA and VCM/VCMITB;
  these two VCM traces should be connected directly at the VCM pin of *SLICOFI-2x*
- In case of a multilayer board, it is recommended to use one common ground layer (AGND, BGND, GNDD, GNDA, GNDB, GNDPLL connected together and share one ground layer).
- In case of a two-layer board, a common ground should be used for AGND, BGND, GNDD, GNDA, GNDB and GNDPLL. Ground traces should be laid out as large as possible. Connections to and from ground pins should be as short as possible. Any unused area of the board should be filled with ground (copper pouring).
- The connection of GND, V_H and V_{BAT} to the protection devices should be low-impedance in order to avoid such issues as a GND shift due to the high impulse currents in case of an overvoltage strike.
- Tip/ring traces from the SLIC should be symmetrical.

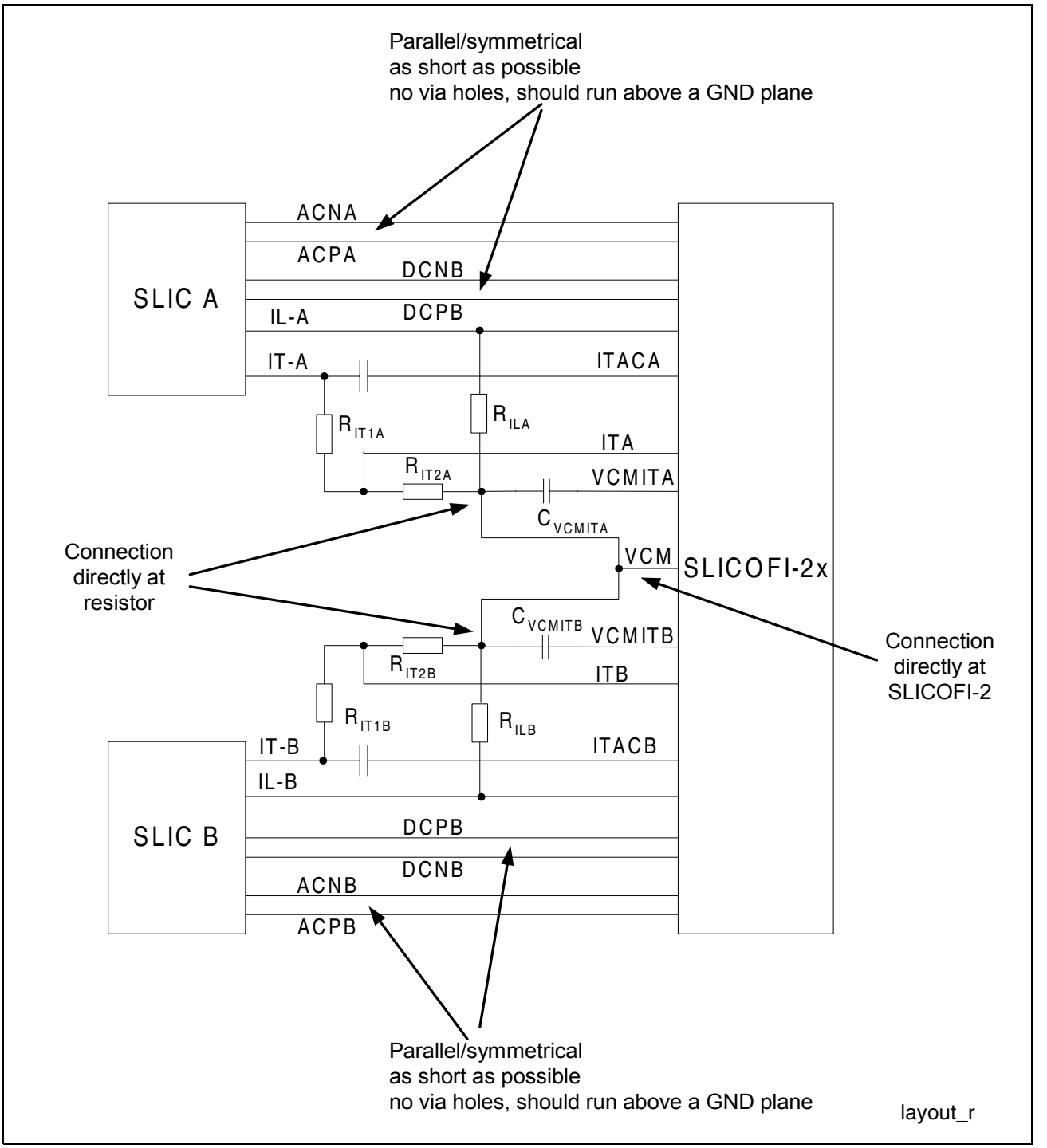
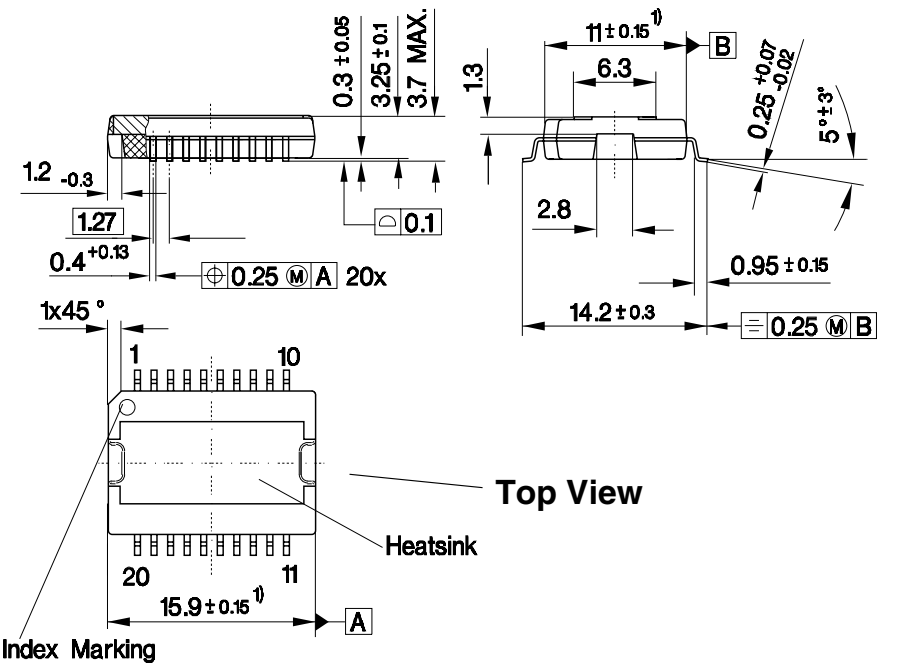


Figure 96 DuSLIC Layout Recommendation

8 Package Outlines

P-DSO-20-5
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side

Gps05755

Figure 97 SLIC-S/-S2, SLIC-E/-E2, SLIC-P (PEB 426x)

Note: The P-DSO-20-5 package is designed with heatsink on top. The pin counting for this package is clockwise (top view).

Attention: The heatsink is connected to V_{BATH} (V_{BATR}) via the chip substrate. Due to the high voltage of up to 150 V between VHR and V_{BATH} (B_{GND} and V_{BATR}), touching of the heatsink or any attached conducting part can be hazardous.

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

P-VQFN-48-4
(Very thin Profile Quad Flatpack No-lead)

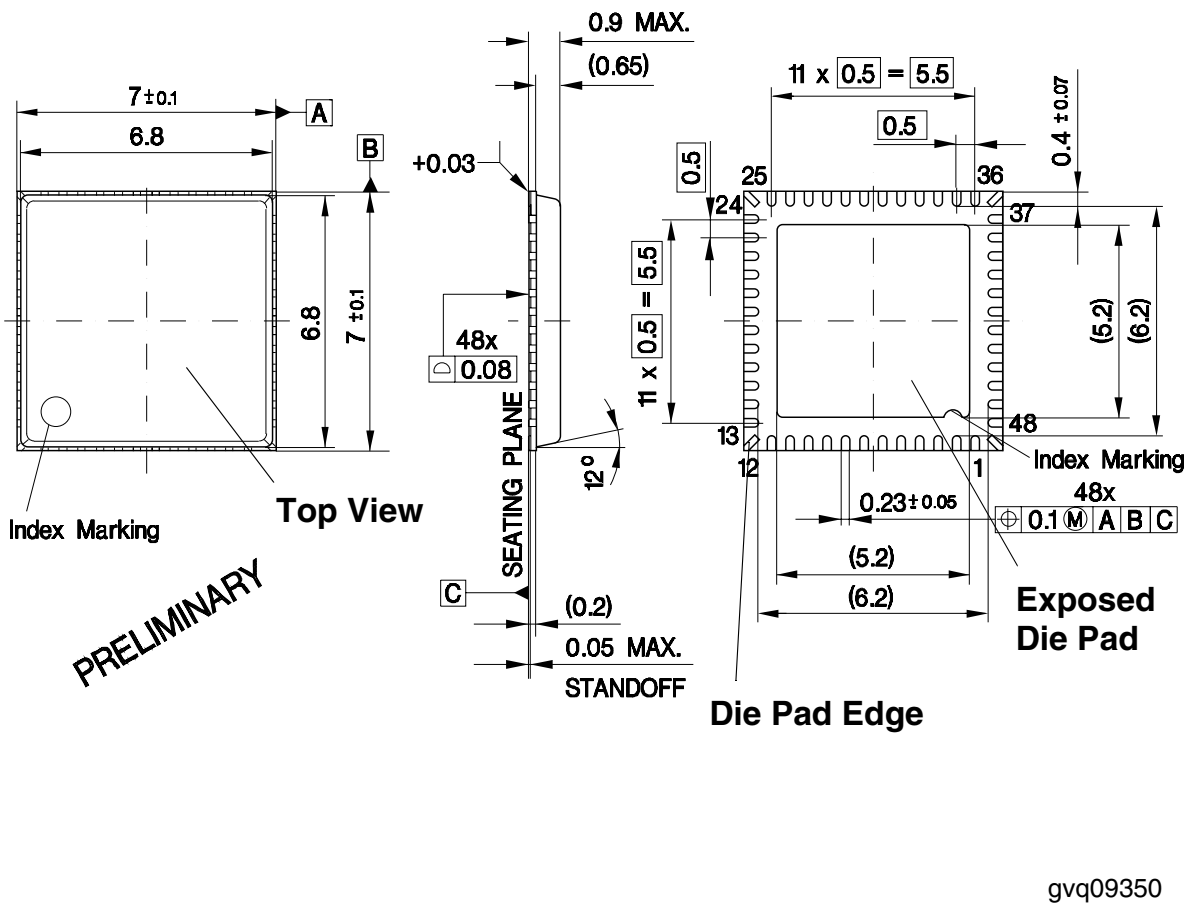


Figure 98 SLIC-S/-S2, SLIC-E/-E2, SLIC-P (PEB426x)

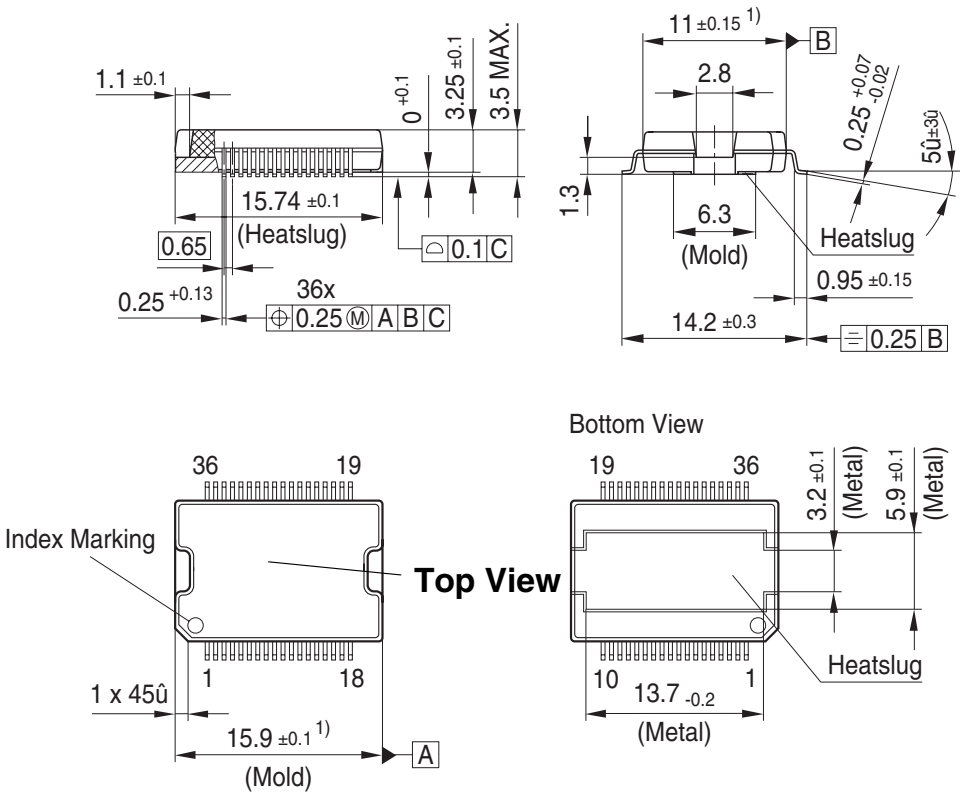
Attention: The exposed die pad and die pad edges are connected to V_{BATH} (V_{BATR}) via the chip substrate. Due to the high voltage of up to 150 V between V_{HR} and V_{BATH} (V_{BATR} and B_{GND}), touching of the die pad or any attached conducting part can be hazardous.

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

P-DSO-36-15
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side

gps09181

Figure 99 TSLIC-S (PEB 4364)

Attention: The heatslug is connected to V_{BATH} via the chip substrate. Due to the high voltages of up to 90 V between V_{HRA} (VHRB) and V_{BATH}, touching of the heatslug or any attached conducting part can be hazardous.

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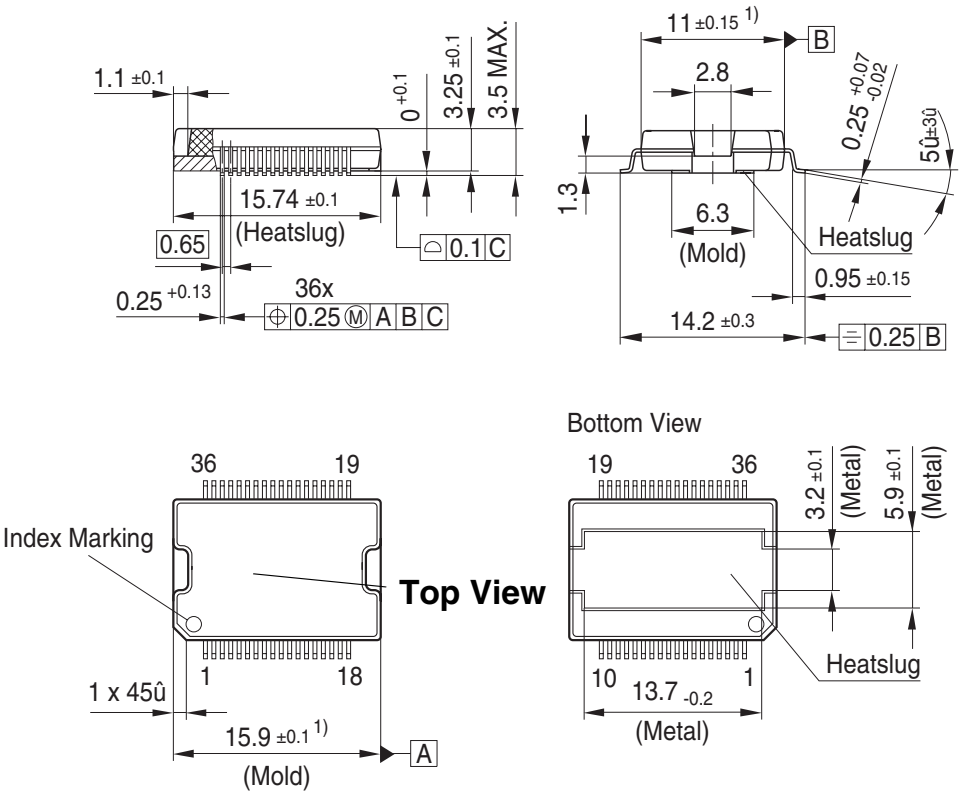
SMD = Surface Mounted Device

Dimensions in mm

P-DSO-36-10
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side

gps09181

Figure 100 TSLIC-E (PEB 4365)

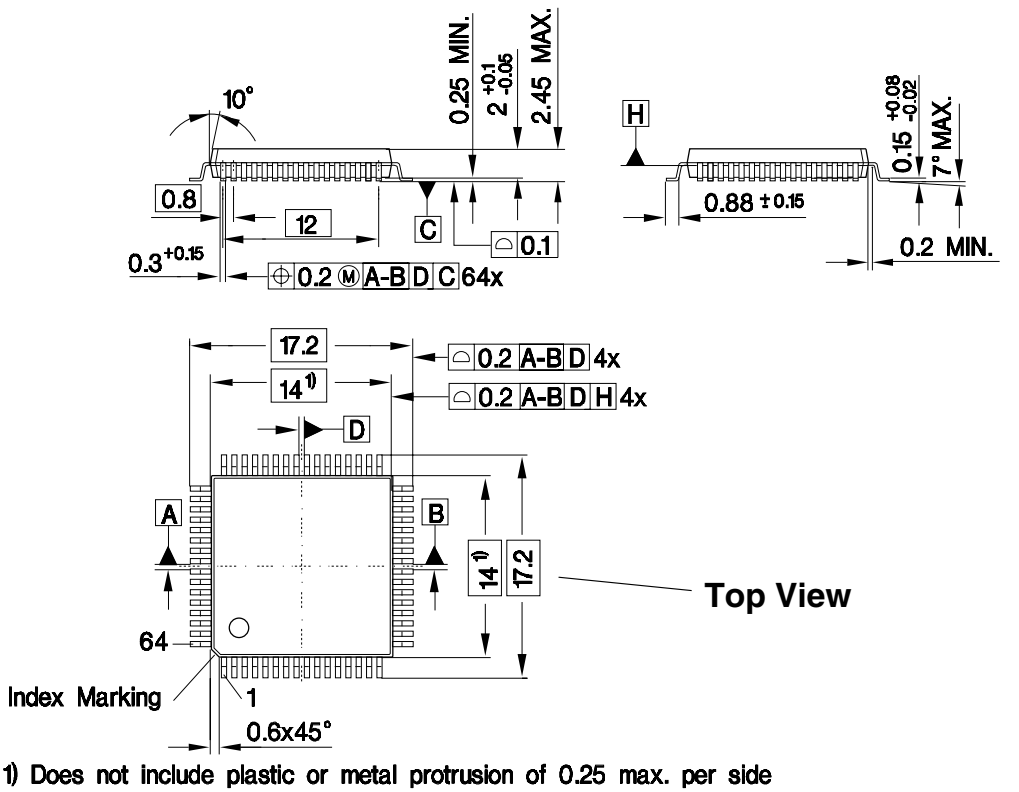
Attention: The heatslug is connected to V_{BATH} via the chip substrate. Due to the high voltages of up to 150 V between V_{HRA} (V_{HRB}) and V_{BATH}, touching of the heatslug or any attached conducting part can be hazardous.

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

P-MQFP-64-1
(Plastic Metric Quad Flat Package)



Gpm05250

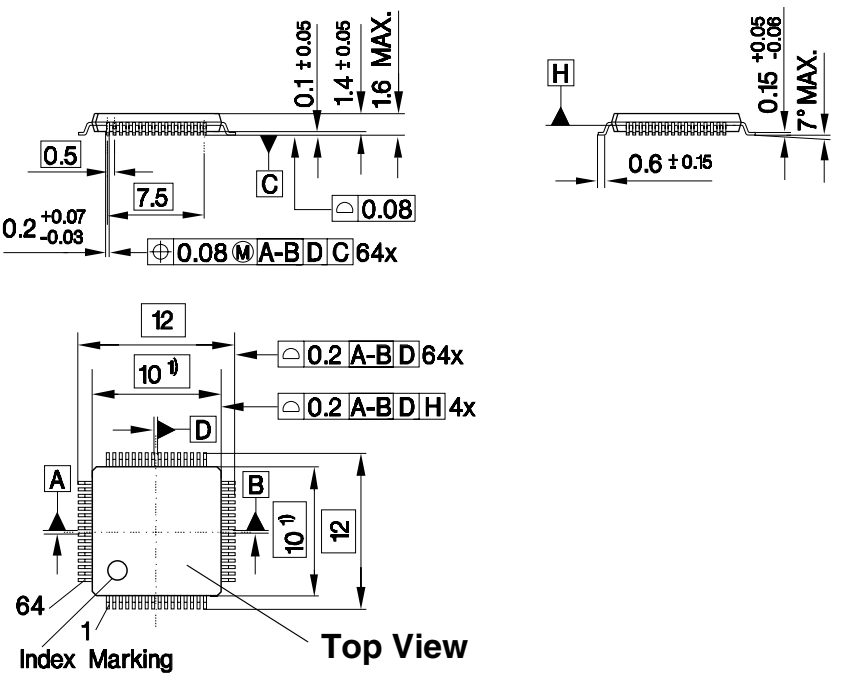
Figure 101 *SLICOFI-2x* (PEB 3265, PEB 3264)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

P-TQFP-64-1
(Plastic Thin Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Gpm05250

Figure 102 *SLICOFI-2x* (PEB 3265, PEB 3264)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

9 Terminology

A

ACTH	Active with V_{BATH}
ACTL	Active with V_{BATL}
ACTR	Active with V_{BATR} or V_{HR} and V_{BATH}
ADC	Analog Digital Converter
AR	Attenuation Receive
AX	Attenuation Transmit

B

BP	Band-pass

C

CMP	Compander
Codec	Coder Decoder
COP	Coefficient Operation
CRAM	Coefficient RAM

D

DAC	Digital Analog Converter
DSP	Digital Signal Processor
DUP	Data Upstream Persistence Counter
DuSLIC	Dual Channel Subscriber Line Interface Concept
DuSLICOS	Dual Channel Subscriber Line Interface Concept Coefficients Software

E

EXP	Expander

F

FRR	Frequency Response Receive Filter
FRX	Frequency Response Transmit Filter

L

LSSGR	Local area transport access Switching System Generic Requirements

P

PCM	Pulse Code Modulation

PDH	Power Down High Impedance
PDRHL	Power Down Load Resistive with V_{BATH} and BGND
PDRRL	Power Down Load Resisitve with V_{BATR} and BGND
PDRH	Power Down Resistive with V_{BATH} and BGND
PDRR	Power Down Resistive with V_{BATR} and BGND
POFI	Post Filter
PREFI	Antialiasing Pre Filter
R	
RECT	Rectifier (Testloops, Levelmetering)
S	
SLIC	Subscriber Line Interface Circuit (same for all versions)
SLIC-S/-S2	Subscriber Line Interface Circuit Standard Feature Set PEB 4264/-2
SLIC-E/-E2	Subscriber Line Interface Circuit Enhanced Feature Set PEB 4265/-2
SLIC-P	Subscriber Line Interface Circuit Enhanced Power Management PEB 4266
SLICOFI-2x	Dual Channel Subscriber Line Interface Codec Filter (same for all versions)
SLICOFI-2	Dual Channel Subscriber Line Interface Codec Filter PEB 3265
SLICOFI-2S	Dual Channel Subscriber Line Interface Codec Filter PEB 3264
SOP	Status Operation
T	
TG	Tone Generator
TH	Transhybrid Balancing
THFIX	Transhybrid Balancing Filter (fixed)
TS	Time Slot
TSLIC-S	Twin Subscriber Line Interface Circuit Standard Feature Set PEB 3264
TSLIC-E	Twin Subscriber Line Interface Circuit Standard Feature Set PEB 3265
TTX	Teletax

10 Index

Numerics

170V technology 45

A

Active 90
Active High 74, 76, 78, 80, 82
Active Low 74, 76, 78, 80, 82
Active Ring 74, 76, 78, 80, 83
Active State 52, 92
Active with HIR 74, 77, 79, 81, 83
Active with HIT 74, 77, 79, 81, 83
Active with Metering 75, 77, 141, 260, 320

B

Balanced ringing 46, 352
Battery feed 29

C

Caller ID 23, 30, 59, 66, 157
Central Office 24
Coding 29
Constant Current Zone 35
Constant Voltage Zone 37
COP-command 141, 142, 203, 315
CRAM coefficients 205, 318

D

DC characteristic 38
Digital Loop Carrier 24
DTMF 30, 66, 155, 177, 179, 295
DTMF decoder 30
DTMF generator 23, 30, 56
DuSLICOS 30, 203, 315

E

Enhanced Digital Signal Processor 56, 151, 157
MIPS Requirements 66
POP Commands 207
External Components
DuSLIC-P 355
External conference 71
External Ringing 48, 94, 170, 290

F

Fiber in the Loop 24
First Command Byte 140, 262, 263, 322, 323
Frequency response 29, 327
FSK 30

G

Ground key 152
Ground start 77

H

Hybrid 29
Hybrid balance 29

I

Impedance matching 29
Intelligent NT 24
Internal conference 71
IOM-2 interface 122, 129, 260, 263, 320, 323
ISDN Terminal Adapters 24

L

Layout Recommendation 361
Levelmeter
AC 105
DC 100
TTX 108
LIN mode 72
LIN16 mode 73
Line Echo Cancellation 30, 63, 66, 178
POP Commands 229
Line Resistance 113
Line Testing 94

M

Message waiting 23, 67

Metering 23, 54, 181, 183, 185, 297, 299, 301
Microcontroller interface 122, 127
Monitor Channel Operation 133
Monitor Receiver 136
Monitor Transfer Protocol 133
Monitor Transmitter 135

O

Operating Modes
- CIDD byte SLICOFI-2 260
- CIDD byte SLICOFI-2S 320
- CIOP byte 141
- DuSLIC 74
- DuSLIC-E/-E2 80
- DuSLIC-P 82
- DuSLIC-S/-S2 78
- Power Management 90

Overvoltage protection 29

P

PCM channel 126
PCM interface 43, 122, 150, 153, 272, 275, 344
PCM mode 72, 88, 189, 193, 305, 307
PCM/µC interface 72, 122, 173, 292
PCM16 mode 73
PCM-active 71
PCM-off 71
Polarity Reversal 23, 55
POP command 142, 207
Power Dissipation
- Operating Modes 90
- SLIC 91
- SLIC output stage 39
- SLICOFI-2 91

Power Down 90, 141, 167, 260, 320
Power Down High Impedance 74, 76, 141, 172, 260, 291, 320
Power Down Resistive 74, 76, 78, 80, 82
Power Down state 53, 71, 91, 197, 199, 309, 311
Power Management 20, 23, 76, 90
Private Branch Exchange 24

R

Ramp generator 68, 79, 81, 83
Read command 127
Receive gain 29
Receive path 43, 178, 197, 199, 201, 309, 311, 313
Register Description Example 142
Reset 84, 141
- Status 154, 276

Resistive Zone 36
Ring on Ring 77
Ring on Tip 77
Ring Pause 75, 77, 79, 81, 83
Ring Trip 45, 77, 341
Ringer Equivalence Number 45
Ringing 29, 45, 74, 77, 79, 81, 83, 90, 141, 260, 320

S

Second Command Byte 127, 142, 262, 263, 322, 323
Signaling 29, 52, 58, 263, 323
Sleep 74, 75, 80, 82, 141, 260, 320
Soft reversal 55, 170, 290
SOP-command 141, 144, 266
Supervision 29, 52

T

Teletax Metering 30
Test Loops 119
Three-party Conferencing 68, 173
Time Slot Assignment 43, 132
TIP/RING interface 122, 139
Transmit gain 29, 328
Transmit path 43, 178, 197, 199, 201, 309, 311, 313
TTX 29, 54, 77, 170, 199, 204, 311, 317

U

Unbalanced ringing 46, 90, 167, 287
Universal Tone Detection 30, 65, 66, 156

POP Commands 250
Universal Tone detection 177

V

Voice over Packet Network 24
Voltage reserve 34, 40

W

Wireless Local Loop 24
Write command 127

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