

EVALUATION KIT
AVAILABLE

7.5Msps, Ultra-Low-Power Analog Front-End

MAX19700

General Description

The MAX19700 is an ultra-low-power, mixed-signal analog front-end (AFE) designed for TD-SCDMA handsets and data cards. Optimized for high dynamic performance at ultra-low power, the MAX19700 integrates a dual 10-bit, 7.5Msps receive (Rx) ADC, dual 10-bit, 7.5Msps transmit (Tx) DAC with TD-SCDMA baseband filters, and three fast-settling 12-bit aux-DAC channels for ancillary RF front-end control. The typical operating power in Tx-Rx FAST mode is 36.3mW at a 5.12Msps clock frequency.

The Rx ADCs feature 54.9dB SINAD and 78dBc SFDR at a 1.87MHz input frequency with a 7.5Msps sample frequency. The analog I/Q input amplifiers are fully differential and accept 1.024V_{p-p} full-scale signals. Typical I/Q channel matching is $\pm 0.22^\circ$ phase and ± 0.02 dB gain.

The Tx DACs with TD-SCDMA lowpass filters feature -3dB cutoff frequency of 1.27MHz and >55dB stopband rejection at $f_{\text{IMAGE}} = 4.32$ MHz. The analog I/Q full-scale output voltage range is selectable at ± 410 mV or ± 500 mV. The output common-mode voltage is selectable from 0.9V to 1.4V and the I/Q channel offset is adjustable. The typical I/Q channel matching is ± 0.05 dB gain and $\pm 0.16^\circ$ phase.

The Rx ADC and Tx DAC share a single, 10-bit parallel, high-speed digital bus allowing half-duplex operation for time-division duplex (TDD) applications. A 3-wire serial interface controls power-management modes and the aux-DAC channels.

The MAX19700 operates on a single +2.7V to +3.3V analog supply and +1.8V to +3.3V digital I/O supply. The MAX19700 is specified for the extended (-40°C to +85°C) temperature range and is available in a 48-pin, thin QFN package.

Applications

TD-SCDMA Handsets
TD-SCDMA Data Cards
Portable Communication Equipment

Ordering Information

PART*	PIN-PACKAGE	PKG CODE
MAX19700ETM	48 Thin QFN-EP**	T4877-4
MAX19700ETM+	48 Thin QFN-EP**	T4877-4

*All devices are specified over the -40°C to +85°C operating range.

**EP = Exposed paddle.

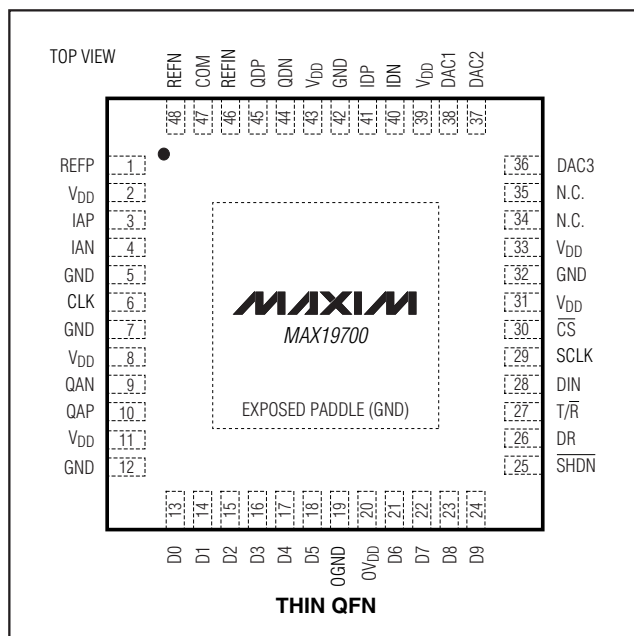
+Denotes lead-free package.

Functional Diagram appears at end of data sheet.

Features

- ◆ Dual 10-Bit Rx ADC and Dual 10-Bit Tx DAC
- ◆ Ultra-Low Power
 - 36.3mW at $f_{\text{CLK}} = 5.12$ Msps, Fast Mode
 - 19.8mW at $f_{\text{CLK}} = 5.12$ Msps, Slow Mode
 - Low Standby and Shutdown Current
- ◆ Integrated TD-SCDMA Filters with >55dB Stopband Rejection
- ◆ Excellent Dynamic Performance
 - SINAD = 54.9dB at $f_{\text{IN}} = 1.87$ MHz (Rx ADC)
 - SFDR = 76.5dBc at $f_{\text{OUT}} = 620$ kHz (Tx DAC)
- ◆ Excellent Gain/Phase Match
 - $\pm 0.22^\circ$ Phase, ± 0.02 dB Gain (Rx ADC) at $f_{\text{IN}} = 1.87$ MHz at -0.5dBFS
- ◆ Three 12-Bit, 1 μ s Aux-DACs
- ◆ Single-Supply Operation
- ◆ Multiplexed Parallel Digital I/O
- ◆ Serial-Interface Control
- ◆ Versatile Power-Control Circuits
 - Shutdown, Standby, Idle, Tx-Rx Disable
- ◆ Miniature 48-Pin Thin QFN Package (7mm x 7mm x 0.8mm)

Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND, OV_{DD} to OGND-0.3V to +3.4V
 GND to OGND-0.3V to +0.3V
 IAP, IAN, QAP, QAN, IDP, IDN, QDP,
 QDN, REFP, REFN, REFIN, COM,
 DAC1, DAC2, DAC3 to GND-0.3V to (V_{DD} + 0.3V)
 D0–D9, DR, T/R, SHDN, SCLK, DIN, CS,
 CLK to OGND-0.3V to (OV_{DD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
 48-Pin Thin QFN (derate 26.3mW/°C above +70°C)2.1W
 Thermal Resistance θ_{JA} 38°C/W
 Operating Temperature Range-40°C to +85°C
 Junction Temperature+150°C
 Storage Temperature Range-60°C to +150°C
 Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, CREFP = CREFN = CCOM = 0.33μF. Typical values are at T_A = +25°C, unless otherwise noted. C_L < 5pF on all aux-DAC outputs.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Analog Supply Voltage	V _{DD}		2.7	3.0	3.3	V
Output Supply Voltage	OV _{DD}		1.8		V _{DD}	V
V _{DD} Supply Current		Ext1-Tx, Ext3-Tx, and SPI2-Tx states; transmit DAC operating mode (Tx), f _{CLK} = 5.12MHz, f _{OUT} = 620kHz on both channels; aux-DACs ON and at midscale		10.3		mA
		Ext2-Tx, Ext4-Tx, and SPI4-Tx states; transmit DAC operating mode (Tx), f _{CLK} = 5.12MHz, f _{OUT} = 620kHz on both channels; aux-DACs ON and at midscale		12.4		
		Ext1-Rx, Ext4-Rx, and SPI3-Rx states; receive ADC operating mode (Rx), f _{CLK} = 5.12MHz, f _{IN} = 1.87MHz on both channels; aux-DACs ON and at midscale		12.1		
		Ext2-Rx, Ext3-Rx, and SPI1-Rx modes; receive ADC operating mode (Rx), f _{CLK} = 5.12MHz, f _{IN} = 1.87MHz on both channels; aux-DACs ON and at midscale		6.6		
		Ext2-Tx, Ext4-Tx, and SPI4-Tx modes; transmit DAC operating mode (Tx), f _{CLK} = 7.5MHz, f _{OUT} = 620kHz on both channels; aux-DACs ON and at midscale		13.1	16	
		Ext1-Tx, Ext3-Tx, and SPI2-Tx modes; transmit DAC operating mode (Tx), f _{CLK} = 7.5MHz, f _{OUT} = 620kHz on both channels; aux-DACs ON and at midscale		10.4		

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33μF. Typical values are at T_A = +25°C, unless otherwise noted. C_L < 5pF on all aux-DAC outputs.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V _{DD} Supply Current		Ext1-Rx, Ext4-Rx, and SPI3-Rx modes; receive ADC operating mode (Rx), f _{CLK} = 7.5MHz, f _{IN} = 1.87MHz on both channels; aux-DACs ON and at midscale		12.8	16	mA
		Ext2-Rx, Ext3-Rx, and SPI1-Rx modes; receive ADC operating mode (Rx), f _{CLK} = 7.5MHz, f _{IN} = 1.87MHz on both channels; aux-DACs ON and at midscale		7		
		Standby mode, CLK = 0 or OV _{DD} ; aux-DACs ON and at midscale		2.7	4	
		Idle mode, f _{CLK} = 7.5MHz; aux-DACs ON and at midscale		4.7	6	
		Shutdown mode, CLK = 0 or OV _{DD}		0.7		μA
OV _{DD} Supply Current		Ext1-Rx, Ext2-Rx, Ext3-Rx, Ext4-Rx, SPI1-Rx, SPI3-Rx modes; receive ADC operating mode (Rx), f _{CLK} = 7.5MHz, f _{IN} = 1.87MHz on both channels; aux-DACs ON and at midscale		1.38		mA
		Ext1-Tx, Ext2-Tx, Ext3-Tx, Ext4-Tx, SPI2-Tx, SPI4-Tx modes; transmit DAC operating mode (Tx), f _{CLK} = 7.5MHz, f _{OUT} = 620kHz; aux-DACs ON and at midscale		72.9		μA
		Idle mode, f _{CLK} = 7.5MHz; aux-DACs ON and at midscale		10.9		
		Shutdown mode, CLK = 0 or OV _{DD}		0.01		
		Standby mode, CLK = 0 or OV _{DD} ; aux-DACs ON and at midscale		0.03		
Rx ADC DC ACCURACY						
Resolution			10			Bits
Integral Nonlinearity	INL		±0.85			LSB
Differential Nonlinearity	DNL		±0.55			LSB
Offset Error		Residual DC offset error	±0.5		±5	%FS
Gain Error		Include reference error	±1.1		±5	%FS
DC Gain Matching			±0.01		±0.25	dB
Offset Matching			±4.5			LSB
Gain Temperature Coefficient			±15.7			ppm/°C
Power-Supply Rejection	PSRR	Offset error (V _{DD} ±5%)	±0.2			LSB
		Gain error (V _{DD} ±5%)	±0.04			%FS

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, CREFP = CREFN = CCOM = 0.33μF. Typical values are at T_A = +25°C, unless otherwise noted. C_L < 5pF on all aux-DAC outputs.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rx ADC ANALOG INPUT						
Input Differential Range	V _{ID}	Differential or single-ended inputs		±0.512		V
Input Common-Mode Voltage Range	V _{CM}			V _{DD} / 2		V
Input Impedance	R _{IN}	Switched capacitor load		720		kΩ
	C _{IN}			5		pF
Rx ADC CONVERSION RATE						
Maximum Clock Frequency	f _{CLK}	(Note 2)		7.5		MHz
Data Latency (Figure 3)		Channel I		5		Clock Cycles
		Channel Q		5.5		
Rx ADC DYNAMIC CHARACTERISTICS (Note 3)						
Signal-to-Noise Ratio	SNR	f _{IN} = 1.875MHz, f _{CLK} = 7.5MHz	53.7	55		dB
		f _{IN} = 3.5MHz, f _{CLK} = 7.5MHz		54.8		
Signal-to-Noise Plus Distortion	SINAD	f _{IN} = 1.875MHz, f _{CLK} = 7.5MHz	53.6	54.9		dB
		f _{IN} = 3.5MHz, f _{CLK} = 7.5MHz		54.7		
Spurious-Free Dynamic Range	SFDR	f _{IN} = 1.875MHz, f _{CLK} = 7.5MHz	66	78		dBc
		f _{IN} = 3.5MHz, f _{CLK} = 7.5MHz		70.1		
Third-Harmonic Distortion	HD3	f _{IN} = 1.875MHz, f _{CLK} = 7.5MHz		-84		dBc
		f _{IN} = 3.5MHz, f _{CLK} = 7.5MHz		-72.1		
Intermodulation Distortion	IMD	f ₁ = 1.8MHz, -7dBFS; f ₂ = 1MHz, -7dBFS		-75.6		dBc
Third-Order Intermodulation Distortion	IM3	f ₁ = 1.8MHz, -7dBFS; f ₂ = 1MHz, -7dBFS		-78		dBc
Total Harmonic Distortion	THD	f _{IN} = 1.875MHz, f _{CLK} = 7.5MHz		-77.9	-64	dBc
		f _{IN} = 3.5MHz, f _{CLK} = 7.5MHz		-71		
Aperture Delay				3.5		ns
Overdrive Recovery Time		1.5x full-scale input		2		ns
Rx ADC INTERCHANNEL CHARACTERISTICS						
Crosstalk Rejection		f _{INX,Y} = 1.875MHz at -0.5dBFS, f _{INX,Y} = 1MHz at -0.5dBFS (Note 4)		-85		dB
Amplitude Matching		f _{IN} = 1.875MHz at -0.5dBFS (Note 5)		±0.02		dB
Phase Matching		f _{IN} = 1.875MHz at -0.5dBFS (Note 5)		±0.22		Degrees

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33μF. Typical values are at T_A = +25°C, unless otherwise noted. C_L < 5pF on all aux-DAC outputs.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Tx DAC DC ACCURACY						
Resolution	N		10			Bits
Integral Nonlinearity	INL			±0.45		LSB
Differential Nonlinearity	DNL	Guaranteed monotonic (Note 6)		±0.26		LSB
Residual DC Offset	V _{OS}	T _A > +25°C	-4	±1	+4	mV
		T _A < +25°C	-6.5	±1	+6.5	
Full-Scale Gain Error		Include reference error (peak-to-peak error)	-50		+50	mV
TRANSMIT-PATH DYNAMIC PERFORMANCE						
Corner Frequency		3dB corner	1.1	1.27	1.5	MHz
Passband Ripple		DC to 640kHz (Note 6)		0.28	0.5	dB _{P-P}
Group Delay Variation in Passband		DC to 640kHz, guaranteed by design		50	100	ns
Error-Vector Magnitude	EVM	DC to 700kHz		2		%
Stopband Rejection		f _{IMAGE} = 4.32MHz, f _{OUT} = 800kHz, f _{CLK} = 5.12MHz	55			dBc
Baseband Attenuation		Spot relative to 100kHz	2MHz	20		dB
			4MHz	46.5		
			5MHz	54.7		
			10MHz	81		
			20MHz	88		
DAC Conversion Rate	f _{CLK}	(Note 2)			7.5	MHz
In-Band Noise Density	N _D	f _{OUT} = 620kHz, f _{CLK} = 5.12MHz, offset = 500kHz		-121.7		dBc/Hz
Third-Order Intermodulation Distortion	IM3	f ₁ = 620kHz, f ₂ = 640kHz		76		dBc
Glitch Impulse				10		pV•s
Spurious-Free Dynamic Range to Nyquist	SFDR	f _{CLK} = 7.5MHz, f _{OUT} = 620kHz	60	76.5		dBc
Total Harmonic Distortion to Nyquist	THD	f _{CLK} = 7.5MHz, f _{OUT} = 620kHz		-74.8	-59	dB
Signal-to-Noise Ratio to Nyquist	SNR	f _{CLK} = 7.5MHz, f _{OUT} = 620kHz		57.1		dB

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 3V$, $OV_{DD} = 1.8V$, internal reference (1.024V), $C_L \approx 10pF$ on all digital outputs, $f_{CLK} = 7.5MHz$ (50% duty cycle), ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, $C_{REFP} = C_{REFN} = C_{COM} = 0.33\mu F$. Typical values are at $T_A = +25^\circ C$, unless otherwise noted. $C_L < 5pF$ on all aux-DAC outputs.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMIT-PATH INTERCHANNEL CHARACTERISTICS						
I-to-Q Output Isolation		$f_{OUTx,Y} = 500\text{kHz}$, $f_{OUTx,Y} = 620\text{kHz}$	85			dB
Gain Mismatch Between DAC Outputs		Measured at DC	-0.3	± 0.05	+0.3	dB
Phase Mismatch Between DAC Outputs		$f_{OUT} = 620\text{kHz}$, $f_{CLK} = 7.5\text{MHz}$	± 0.16			Degrees
Differential Output Impedance			800			Ω
TRANSMIT-PATH ANALOG OUTPUT						
Full-Scale Output Voltage (Table 6)	V_{FS}	Bit E7 = 0 (default)	± 410			mV
		Bit E7 = 1	± 500			
Output Common-Mode Voltage (Table 8)		Bits CM1 = 0, CM0 = 0 (default)	1.32	1.4	1.48	V
		Bits CM1 = 0, CM0 = 1	1.25			
		Bits CM1 = 1, CM0 = 0	1.1			
		Bits CM1 = 1, CM0 = 1	0.9			
RECEIVE TRANSMIT-PATH INTERCHANNEL CHARACTERISTICS						
Receive Transmit Isolation		ADC $f_{INI} = f_{INQ} = 1.875\text{MHz}$, DAC $f_{OUTI} = f_{OUTQ} = 620\text{kHz}$, $f_{CLK} = 7.5\text{MHz}$	85			dB
AUXILIARY DACs (DAC1, DAC2, DAC3)						
Resolution		(Note 6)	12			Bits
Integral Nonlinearity	INL		± 1.25			LSB
Differential Nonlinearity	DNL	Guaranteed monotonic over codes 100 to 4000 (Note 6)	± 0.65			LSB
Gain Error	GE	$R_L > 200\text{k}\Omega$	± 0.7			%FS
Zero-Code Error			± 0.6			%FS
Output-Voltage Low	V_{OL}	$R_L > 200\text{k}\Omega$	0.1			V
Output-Voltage High	V_{OH}	$R_L > 200\text{k}\Omega$	2.56			V
DC Output Impedance		DC output at midscale	4			Ω
Settling Time		From 1/4 FS to 3/4 FS	1			μs
Glitch Impulse		From 0 to FS transition	24			nV•s
Rx ADC-Tx DAC TIMING CHARACTERISTICS						
CLK Rise to Channel-I Output Data Valid	t_{DOI}	Figure 3 (Note 6)	6.9 10			ns
CLK Fall to Channel-Q Output Data Valid	t_{DOQ}	Figure 3 (Note 6)	9.3 13			ns
CLK Rise/Fall to DR Rise/Fall Time	t_{DR}	Figure 3 (Note 6)	8.5 12			ns
I-DAC DATA to CLK Fall Setup Time	t_{DSI}	Figure 5 (Note 6)	10			ns

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, CREFP = CREFN = CCOM = 0.33μF. Typical values are at T_A = +25°C, unless otherwise noted. C_L < 5pF on all aux-DAC outputs.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Q-DAC DATA to CLK Rise Setup Time	t _{DSQ}	Figure 5 (Note 6)	10			ns
CLK Fall to I-DAC Data Hold Time	t _{DHI}	Figure 5 (Note 6)	0			ns
CLK Rise to Q-DAC Data Hold Time	t _{DHQ}	Figure 5 (Note 6)	0			ns
CLK Duty Cycle				50		%
CLK Duty-Cycle Variation				±15		%
Digital Output Rise/Fall Time		20% to 80%		2.3		ns
SERIAL-INTERFACE TIMING CHARACTERISTICS (Figure 6, Note 6)						
Falling Edge of $\overline{CS}$ to Rising Edge of First SCLK Time	t _{CSS}		10			ns
DIN to SCLK Setup Time	t _{DS}		10			ns
DIN to SCLK Hold Time	t _{DH}		0			ns
SCLK Pulse-Width High	t _{CH}		25			ns
SCLK Pulse-Width Low	t _{CL}		25			ns
SCLK Period	t _{CP}		50			ns
SCLK to $\overline{CS}$ Setup Time	t _{CS}		10			ns
$\overline{CS}$ High Pulse Width	t _{CSW}		80			ns
MODE-RECOVERY TIMING CHARACTERISTICS (Figure 7)						
Shutdown Wake-Up Time	t _{WAKE,SD}	From shutdown to Rx mode, ADC settles to within 1dB SINAD	75			μs
		From shutdown to Tx mode, DAC settles to within 10 LSB error	25			
Idle Wake-Up Time (With CLK)	t _{WAKE,ST0}	From idle to Rx mode with CLK present during idle, ADC settles to within 1dB SINAD	7.3			μs
		From idle to Tx mode with CLK present during idle, DAC settles to 10 LSB error	5			
Standby Wake-Up Time	t _{WAKE,ST1}	From standby to Rx mode, ADC settles to within 1dB SINAD	7.3			μs
		From standby to Tx mode, DAC settles to 10 LSB error	25			
Enable Time from Tx to Rx, (Ext2-Tx to Ext2-Rx, Ext4-Tx to Ext4-Rx, and SPI4-Tx to SPI3-Rx Modes)	t _{ENABLE, RX}	ADC settles to within 1dB SINAD	500			ns
Enable Time from Rx to Tx, (Ext1-Rx to Ext1-Tx, Ext4-Rx to Ext4-Tx, and SPI3-Rx to SPI4-Tx Modes)	t _{ENABLE, TX}	DAC settles to within 10 LSB error	1			μs

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 3V$, $OV_{DD} = 1.8V$, internal reference (1.024V), $C_L \approx 10pF$ on all digital outputs, $f_{CLK} = 7.5MHz$ (50% duty cycle), ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, $C_{REFP} = C_{REFN} = C_{COM} = 0.33\mu F$. Typical values are at $T_A = +25^\circ C$, unless otherwise noted. $C_L < 5pF$ on all aux-DAC outputs.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Enable Time from Tx to Rx, (Ext1-Tx to Ext1-Rx, Ext3-Tx to Ext3-Rx, and SPI2-Tx to SPI1-Rx Modes)	$t_{ENABLE, RX}$	ADC settles to within 1dB SINAD		7.3		μs
Enable Time from Rx to Tx, (Ext2-Rx to Ext2-Tx, Ext3-Rx to Ext3-Tx, and SPI1-Rx to SPI2-Tx Modes)	$t_{ENABLE, TX}$	DAC settles to within 10 LSB error		5		μs
INTERNAL REFERENCE (REFIN = V_{DD}; V_{REFP}, V_{REFN}, V_{COM} levels are generated internally)						
Positive Reference		$V_{REFP} - V_{COM}$		0.256		V
Negative Reference		$V_{REFN} - V_{COM}$		-0.256		V
Common-Mode Output Voltage	V_{COM}		$V_{DD} / 2 - 0.15$	$V_{DD} / 2$	$V_{DD} / 2 + 0.15$	V
Maximum REFP/REFN/COM Source Current	I_{SOURCE}			2		mA
Maximum REFP/REFN/COM Sink Current	I_{SINK}			2		mA
Differential Reference Output	V_{REF}	$V_{REFP} - V_{REFN}$	+0.490	+0.512	+0.534	V
Differential Reference Temperature Coefficient	$REFTC$			± 10		ppm/ $^\circ C$
BUFFERED EXTERNAL REFERENCE (external REFIN = 1.024V applied; V_{REFP}, V_{REFN}, V_{COM} levels are generated internally)						
Reference Input Voltage	V_{REFIN}			1.024		V
Differential Reference Output	V_{DIFF}	$V_{REFP} - V_{REFN}$		0.512		V
Common-Mode Output Voltage	V_{COM}			$V_{DD} / 2$		V
Maximum REFP/REFN/COM Source Current	I_{SOURCE}			2		mA
Maximum REFP/REFN/COM Sink Current	I_{SINK}			2		mA
REFIN Input Current				-0.7		μA
REFIN Input Resistance				500		$k\Omega$
DIGITAL INPUTS (CLK, SCLK, DIN, $\overline{CS}$, D0–D9, $\overline{T/R}$, $\overline{SHDN}$)						
Input High Threshold	V_{INH}	D0–D9, CLK, SCLK, DIN, $\overline{CS}$, $\overline{T/R}$, $\overline{SHDN}$		$0.7 \times OV_{DD}$		V
Input Low Threshold	V_{INL}	D0–D9, CLK, SCLK, DIN, $\overline{CS}$, $\overline{T/R}$, $\overline{SHDN}$			$0.3 \times OV_{DD}$	V
Input Leakage	D_{IIN}	D0–D9, CLK, SCLK, DIN, $\overline{CS}$, $\overline{T/R}$, $\overline{SHDN} = OGND$ or OV_{DD}	-1		+1	μA
Input Capacitance	DC_{IN}			5		pF

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ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS (D0–D9, DR)						
Output-Voltage Low	V_{OL}	$I_{SINK} = 200\mu A$			$0.2 \times OV_{DD}$	V
Output-Voltage High	V_{OH}	$I_{SOURCE} = 200\mu A$	$0.8 \times OV_{DD}$			V
Tri-State Leakage Current	I_{LEAK}		-1		+1	μA
Tri-State Output Capacitance	C_{OUT}			5		pF

Note 1: Specifications from $T_A = +25^\circ C$ to $+85^\circ C$ are guaranteed by production tests. Specifications from $T_A = +25^\circ C$ to $-40^\circ C$ are guaranteed by design and characterization.

Note 2: The minimum clock frequency for the MAX19700 is 2MHz.

Note 3: SNR, SINAD, SFDR, HD3, and THD are based on a differential analog input voltage of -0.5dBFS referenced to the amplitude of the digital outputs. SINAD and THD are calculated using HD2 through HD6.

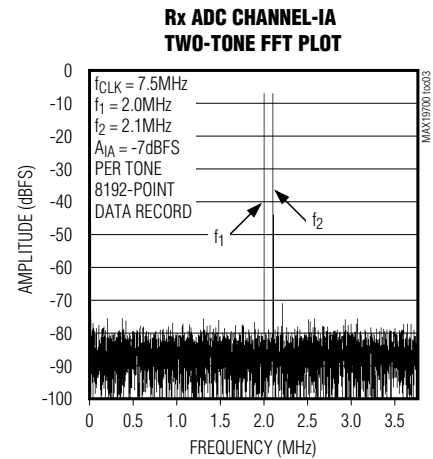
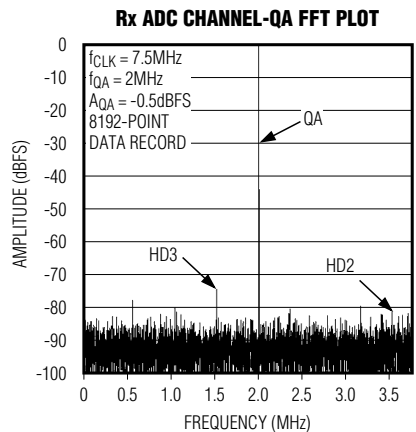
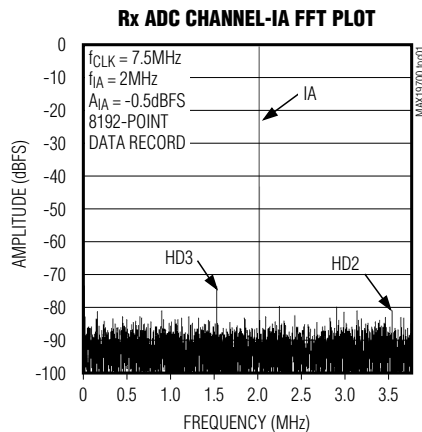
Note 4: Crosstalk rejection is measured by applying a high-frequency test tone to one channel and a low-frequency tone to the second channel. FFTs are performed on each channel. The parameter is specified as the power ratio of the first and second channel FFT test tone.

Note 5: Amplitude and phase matching is measured by applying the same signal to each channel, and comparing the two output signals using a sine-wave fit.

Note 6: Guaranteed by design and characterization.

Typical Operating Characteristics

($V_{DD} = 3V$, $OV_{DD} = 1.8V$, internal reference (1.024V), $C_L \approx 10pF$ on all digital outputs, $f_{CLK} = 7.5MHz$ 50% duty cycle, ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, $C_{REFP} = C_{REFN} = C_{COM} = 0.33\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)

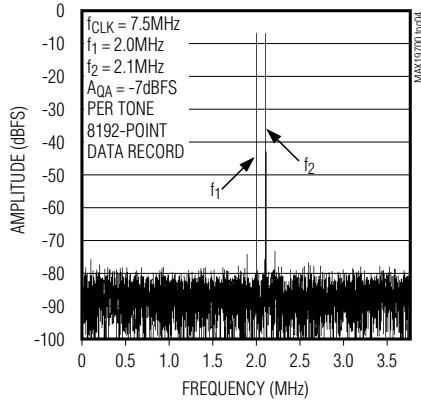


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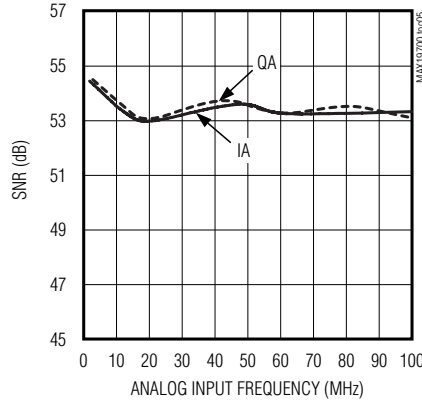
Typical Operating Characteristics (continued)

($V_{DD} = 3V$, $OV_{DD} = 1.8V$, internal reference (1.024V), $C_L \approx 10pF$ on all digital outputs, $f_{CLK} = 7.5MHz$ 50% duty cycle, ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, $C_{REFP} = C_{REFN} = C_{COM} = 0.33\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)

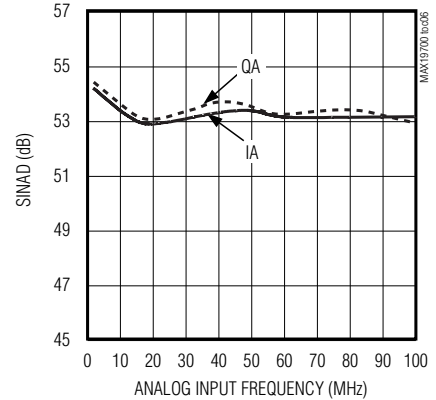
**Rx ADC CHANNEL-QA
TWO-TONE FFT PLOT**



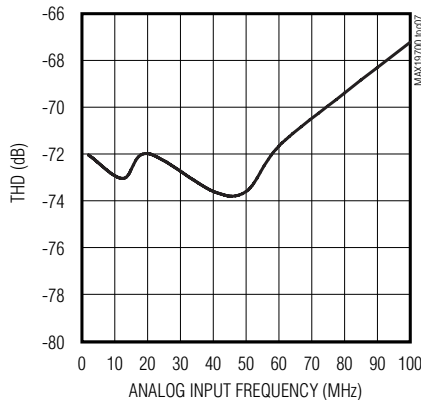
**Rx ADC SIGNAL-TO-NOISE RATIO
vs. ANALOG INPUT FREQUENCY**



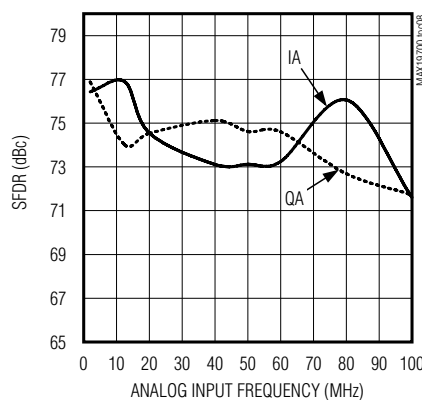
**Rx ADC SIGNAL-TO-NOISE AND DISTORTION
RATIO vs. ANALOG INPUT FREQUENCY**



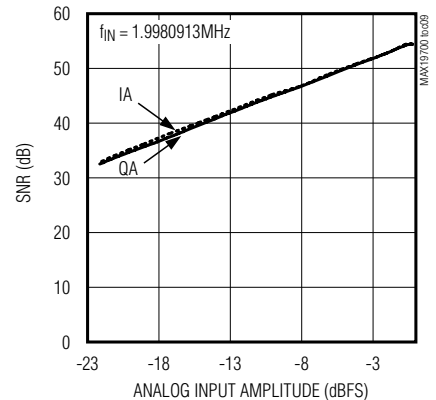
**Rx ADC TOTAL HARMONIC DISTORTION
vs. ANALOG INPUT FREQUENCY**



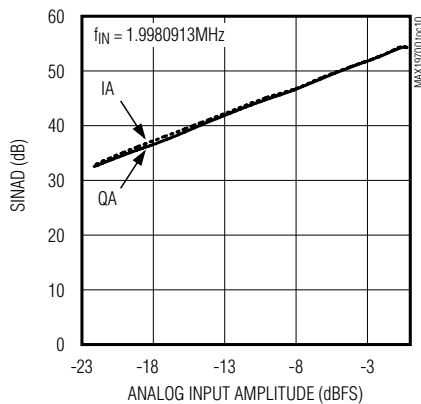
**Rx ADC SPURIOUS-FREE DYNAMIC RANGE
vs. ANALOG INPUT FREQUENCY**



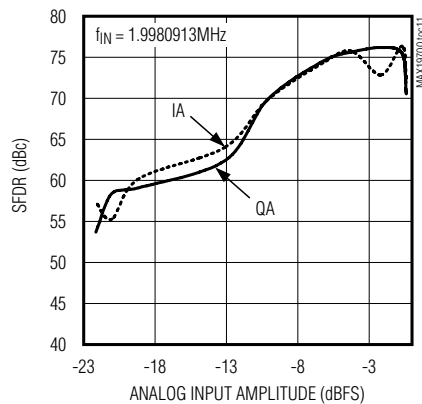
**Rx ADC SIGNAL-TO-NOISE RATIO
vs. ANALOG INPUT AMPLITUDE**



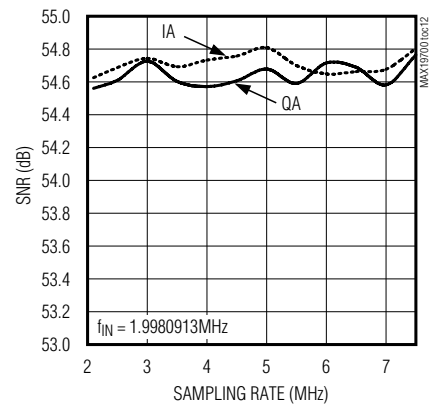
**Rx ADC SIGNAL-TO-NOISE AND DISTORTION
RATIO vs. ANALOG INPUT AMPLITUDE**



**Rx ADC SPURIOUS-FREE DYNAMIC RANGE
vs. ANALOG INPUT AMPLITUDE**



**Rx ADC SIGNAL-TO-NOISE RATIO
vs. SAMPLING RATE**



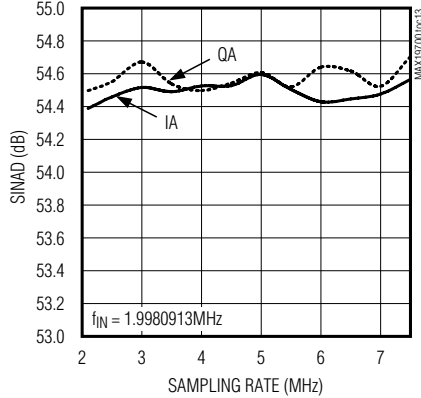
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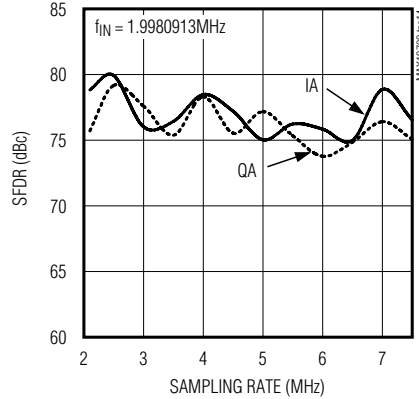
Typical Operating Characteristics (continued)

($V_{DD} = 3V$, $OV_{DD} = 1.8V$, internal reference (1.024V), $C_L \approx 10pF$ on all digital outputs, $f_{CLK} = 7.5MHz$ 50% duty cycle, ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, $C_{REFP} = C_{REFN} = C_{COM} = 0.33\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)

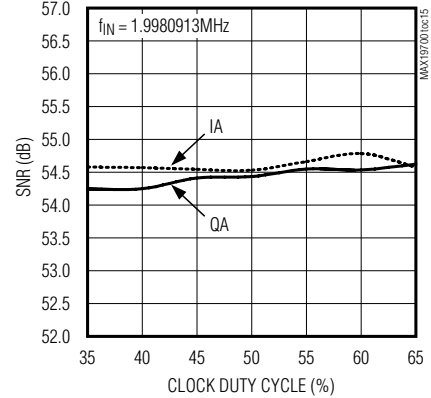
Rx ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. SAMPLING RATE



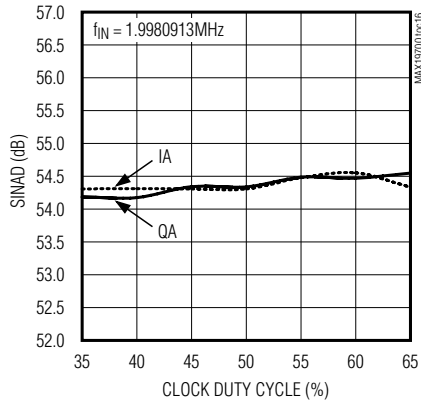
Rx ADC SPURIOUS-FREE DYNAMIC RANGE vs. SAMPLING RATE



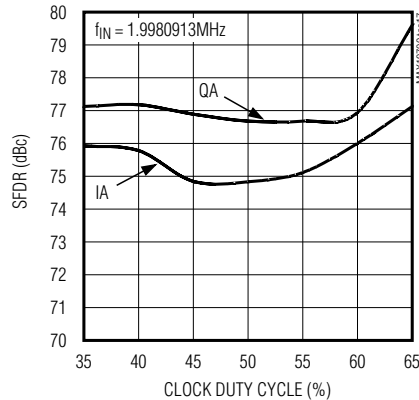
Rx ADC SIGNAL-TO-NOISE RATIO vs. CLOCK DUTY CYCLE



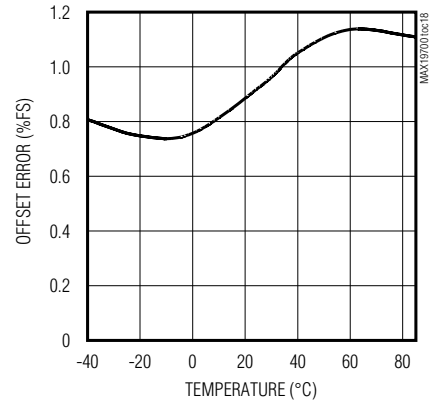
Rx ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. CLOCK DUTY CYCLE



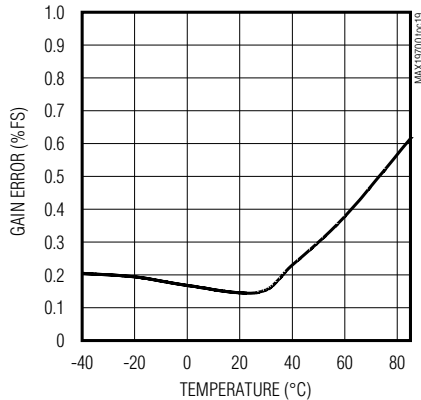
Rx ADC SPURIOUS-FREE DYNAMIC RANGE vs. CLOCK DUTY CYCLE



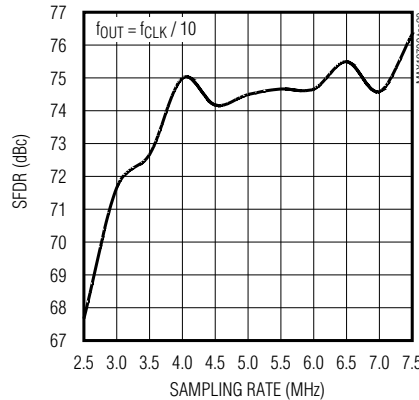
Rx ADC OFFSET ERROR vs. TEMPERATURE



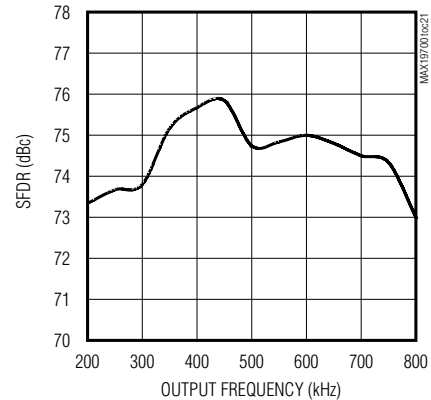
Rx ADC GAIN ERROR vs. TEMPERATURE



Tx PATH SPURIOUS-FREE DYNAMIC RANGE vs. SAMPLING RATE



Tx PATH SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY

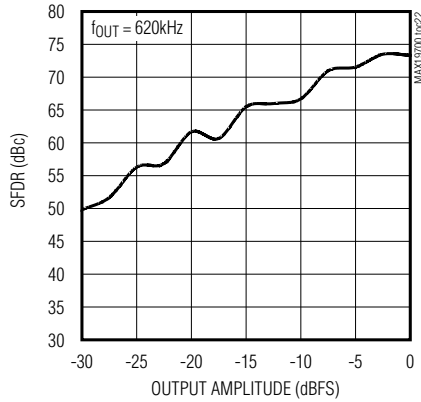


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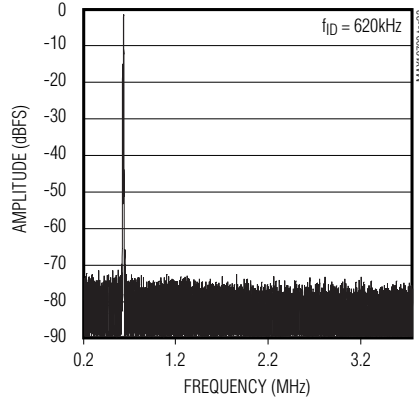
Typical Operating Characteristics (continued)

($V_{DD} = 3V$, $OV_{DD} = 1.8V$, internal reference (1.024V), $C_L \approx 10pF$ on all digital outputs, $f_{CLK} = 7.5MHz$ 50% duty cycle, ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, $C_{REFP} = C_{REFN} = C_{COM} = 0.33\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)

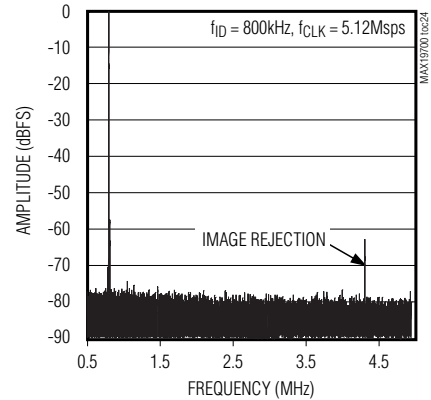
Tx PATH SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT AMPLITUDE



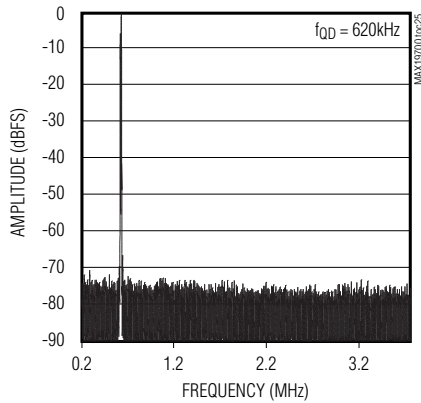
Tx PATH CHANNEL-ID SPECTRAL PLOT



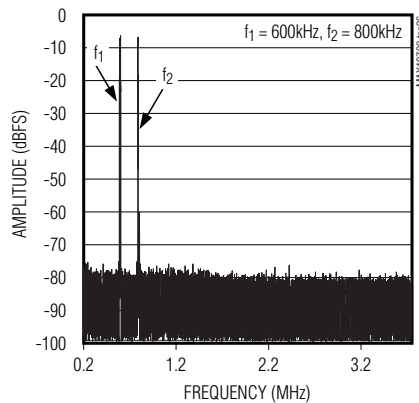
Tx PATH CHANNEL-ID SPECTRAL PLOT WITH IMAGE REJECTION



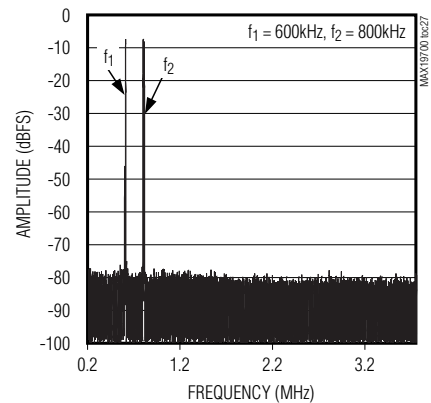
Tx PATH CHANNEL-QD SPECTRAL PLOT



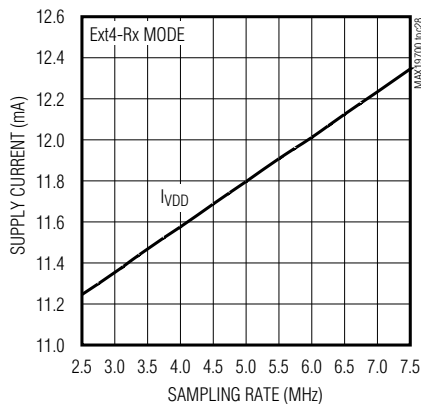
Tx PATH CHANNEL-ID TWO-TONE SPECTRAL PLOT



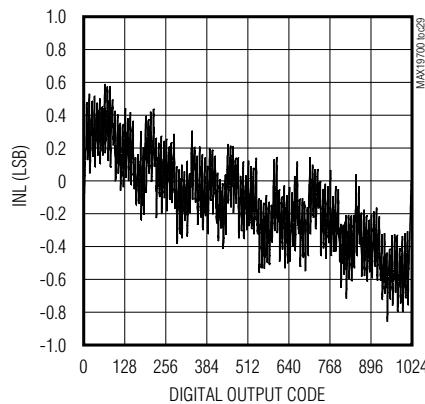
Tx PATH CHANNEL-QD TWO-TONE SPECTRAL PLOT



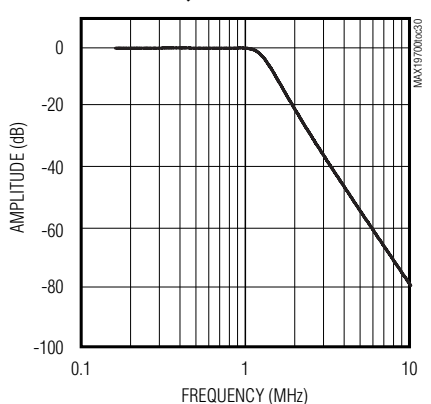
SUPPLY CURRENT vs. SAMPLING RATE



Rx ADC INTEGRAL NONLINEARITY



TRANSMIT FILTER FREQUENCY RESPONSE

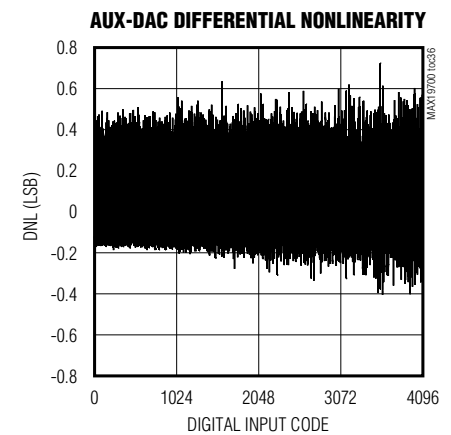
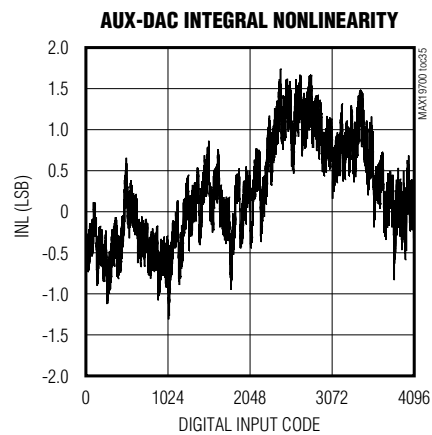
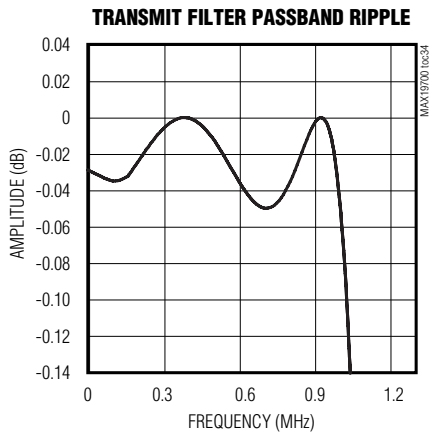
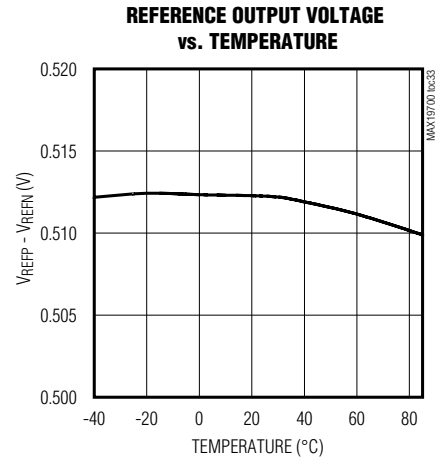
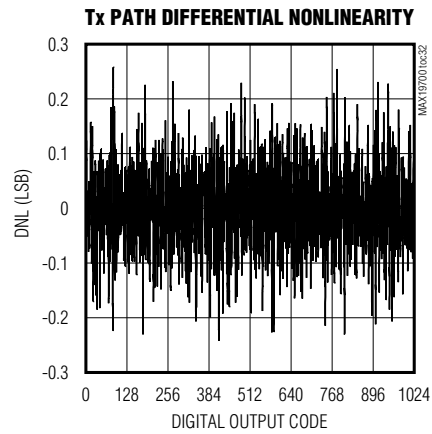
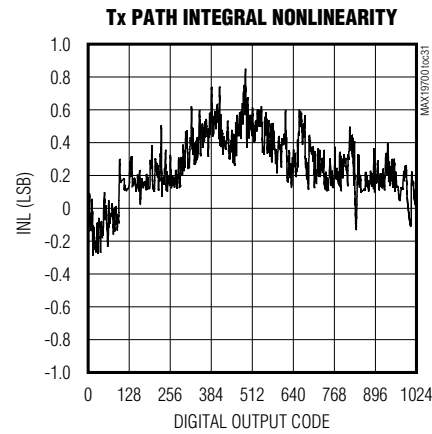


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Typical Operating Characteristics (continued)

($V_{DD} = 3V$, $OV_{DD} = 1.8V$, internal reference (1.024V), $C_L \approx 10pF$ on all digital outputs, $f_{CLK} = 7.5MHz$ 50% duty cycle, ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, $C_{REFP} = C_{REFN} = C_{COM} = 0.33\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)



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Pin Description

PIN	NAME	FUNCTION
1	REFP	Upper Reference Voltage. Bypass with a 0.33 μ F capacitor to GND as close to REFP as possible.
2, 8, 11, 31, 33, 39 43	V _{DD}	Analog Supply Voltage. Bypass V _{DD} to GND with a combination of a 2.2 μ F capacitor in parallel with a 0.1 μ F capacitor.
3	IAP	Channel IA Positive Analog Input. For single-ended operation, connect signal source to IAP.
4	IAN	Channel IA Negative Analog Input. For single-ended operation, connect IAN to COM.
5, 7, 12, 32, 42	GND	Analog Ground. Connect all GND pins to ground plane.
6	CLK	Conversion Clock Input. Clock signal for both receive ADCs and transmit DACs.
9	QAN	Channel QA Negative Analog Input. For single-ended operation, connect QAN to COM.
10	QAP	Channel QA Positive Analog Input. For single-ended operation, connect signal source to QAP.
13–18, 21–24	D0–D9	Digital I/O. Outputs for receive ADC in Rx mode. Inputs for transmit DAC in Tx mode. D9 is the most significant bit (MSB) and D0 is the least significant bit (LSB).
19	OGND	Output-Driver Ground
20	OV _{DD}	Output-Driver Power Supply. Supply range from +1.8V to V _{DD} to accommodate most logic levels. Bypass OV _{DD} to OGND with a combination of a 2.2 μ F capacitor in parallel with a 0.1 μ F capacitor.
25	$\overline{\text{SHDN}}$	Active-Low Shutdown Input. Apply logic-low to place the MAX19700 in shutdown.
26	DR	Data-Ready Indicator. This digital output indicates channel I data (DR = 1) or channel Q data (DR = 0) is present on the output.
27	T/ $\overline{\text{R}}$	Transmit- or Receive-Mode Select Input. T/ $\overline{\text{R}}$ logic-low input sets the device in receive mode. A logic-high input sets the device in transmit mode.
28	DIN	3-Wire Serial-Interface Data Input. Data is latched on the rising edge of the SCLK.
29	SCLK	3-Wire Serial-Interface Clock Input
30	$\overline{\text{CS}}$	3-Wire Serial-Interface Chip-Select Input. Logic-low enables the serial interface.
34, 35	N.C.	No Connection
36	DAC3	Analog Output for Auxiliary DAC3
37	DAC2	Analog Output for Auxiliary DAC2
38	DAC1	Analog Output for Auxiliary DAC1 (AFC DAC, V _{OUT} = 1.1V During Power-Up)
40, 41	IDN, IDP	DAC Channel-ID Differential Voltage Output
44, 45	QDN, QDP	DAC Channel-QD Differential Voltage Output
46	REFIN	Reference Input. Connect to V _{DD} for internal reference.
47	COM	Common-Mode Voltage I/O. Bypass COM to GND with a 0.33 μ F capacitor.
48	REFN	Negative Reference I/O. Conversion range is $\pm(\text{VREFP} - \text{VREFN})$. Bypass REFN to GND with a 0.33 μ F capacitor.
—	EP	Exposed Paddle. Exposed paddle is internally connected to GND. Connect EP to the GND plane.

Detailed Description

The MAX19700 integrates a dual 10-bit Rx ADC and a dual 10-bit Tx DAC with TD-SCDMA baseband filters while providing ultra-low power and high dynamic performance at a 7.5Msps conversion rate. The Rx ADC analog input amplifiers are fully differential and accept 1V_{p-p} full-scale signals. The Tx DAC analog outputs are fully differential with $\pm 410\text{mV}$ full-scale output, selectable common-mode range and offset adjust.

The MAX19700 includes a 3-wire serial interface to control operating modes and power management. The serial interface is SPI™ and MICROWIRE™ compatible. The MAX19700 serial interface selects shutdown, idle, standby, transmit (Tx), and receive (Rx) modes.

SPI is a trademark of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor Corp.

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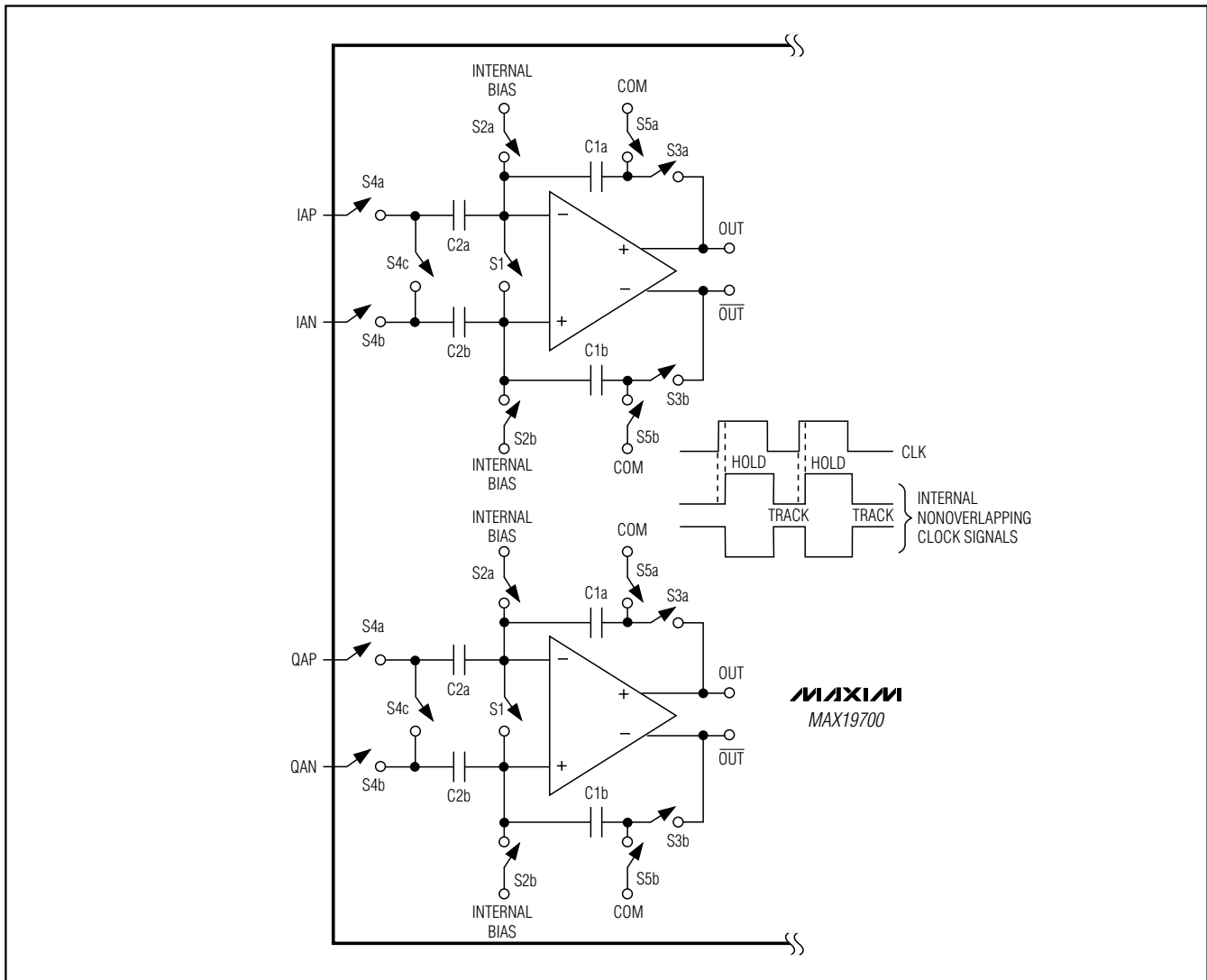


Figure 1. MAX19700 Rx ADC Internal T/H Circuits

To operate the device in TDD applications, configure the MAX19700 for Tx or Rx mode with the 3-wire serial interface. The Rx ADC and Tx DAC share a common digital bus to reduce the digital I/O to a single 10-bit parallel multiplexed bus.

Dual 10-Bit Rx ADC

The ADC uses a seven-stage, fully differential, pipelined architecture that allows for high-speed conversion while minimizing power consumption. Samples taken at the inputs move progressively through the pipeline stages every half clock cycle. Including the delay through the

output latch, the total clock-cycle latency is 5 clock cycles for channel IA and 5.5 clock cycles for channel QA. The ADC full-scale analog input range is $\pm V_{REF}$ with a $V_{DD} / 2 \pm 0.2V$ common-mode input range. V_{REF} is the difference between V_{REFP} and V_{REFN} . See the *Reference Configurations* section for details.

Input Track-and-Hold (T/H) Circuits

Figure 1 displays a simplified diagram of the Rx ADC input track-and-hold (T/H) circuitry. Both ADC inputs (IAP, QAP, IAN, and QAN) can be driven either differentially or single-ended. Match the impedance of IAP

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Table 1. Output Codes vs. Input Voltage

DIFFERENTIAL INPUT VOLTAGE	DIFFERENTIAL INPUT (LSB)	OFFSET BINARY (D0–D9)	OUTPUT DECIMAL CODE
$V_{REF} \times 512/512$	511 (+Full Scale – 1 LSB)	11 1111 1111	1023
$V_{REF} \times 511/512$	510 (+Full Scale – 2 LSB)	11 1111 1110	1022
$V_{REF} \times 1/512$	+1	10 0000 0001	513
$V_{REF} \times 0/512$	0 (Bipolar Zero)	10 0000 0000	512
$-V_{REF} \times 1/512$	-1	01 1111 1111	511
$-V_{REF} \times 511/512$	-511 (-Full Scale + 1 LSB)	00 0000 0001	1
$-V_{REF} \times 512/512$	-512 (-Full Scale)	00 0000 0000	0

and IAN, as well as QAP and QAN, and set the input signal common-mode voltage within the ADC range of $V_{DD}/2$ ($\pm 200\text{mV}$) for optimum performance.

ADC System Timing Requirements

Figure 3 shows the relationship between the clock, analog inputs, DR indicator, and the resulting output data. Channel I (CHI) and channel Q (CHQ) are sampled on the rising edge of the clock signal (CLK) and the resulting data is multiplexed at the D0–D9 outputs. CHI data is updated on the rising edge and CHQ data is updated on the falling edge of the CLK. The DR indicator follows CLK with a typical delay time of 8.5ns and remains high when CHI data is updated and low when CHQ data is updated. Including the delay through the output

latch, the total clock-cycle latency is 5 clock cycles for CHI and 5.5 clock cycles for CHQ.

Digital Input/Output Data (D0–D9)

D0–D9 are the Rx ADC digital logic outputs when the MAX19700 is in receive mode. This bus is shared with the Tx DAC digital logic inputs and operates in half-duplex mode. D0–D9 are the Tx DAC digital logic inputs when the MAX19700 is in transmit mode. The logic level is set by OV_{DD} from 1.8V to V_{DD} . The digital output coding is offset binary (Table 1). Keep the capacitive load on the digital outputs D0–D9 as low as possible ($<15\text{pF}$) to avoid large digital currents feeding back into the analog portion of the MAX19700 and degrading its dynamic performance. Buffers on the digital outputs isolate the outputs from heavy capacitive loads. Adding 100Ω resistors in series with the digital outputs close to the MAX19700 will help improve ADC performance. See the MAX19700EVKIT schematic for an example of the digital outputs driving a digital buffer through 100Ω series resistors.

During SHDN, IDLE, and STBY states, the pins D0–D9 are internally pulled up to prevent floating digital inputs. To ensure no current flows through D0–D9 I/O, the external bus needs to be either tri-stated or pulled up to OV_{DD} and should not be pulled to ground.

Dual 10-Bit Tx DAC and Transmit Path

The dual 10-bit digital-to-analog converters (Tx DAC) operate with clock speeds up to 7.5MHz. The Tx DAC digital inputs, D0–D9, are multiplexed on a single 10-bit bus. The voltage reference determines the Tx path full-scale output voltage. See the *Reference Configurations* section for details on setting the reference voltage. Each Tx path channel integrates a lowpass filter tuned to meet the TD-SCDMA spectral mask requirements. The TD-SCDMA filters are tuned for 1.27MHz cutoff frequency and $>55\text{dB}$ image rejection at $f_{\text{IMAGE}} = 4.32\text{MHz}$, $f_{\text{OUT}} = 800\text{kHz}$, and $f_{\text{CLK}} = 5.12\text{MHz}$. See Figure 4 for an illustration of the filter frequency response.

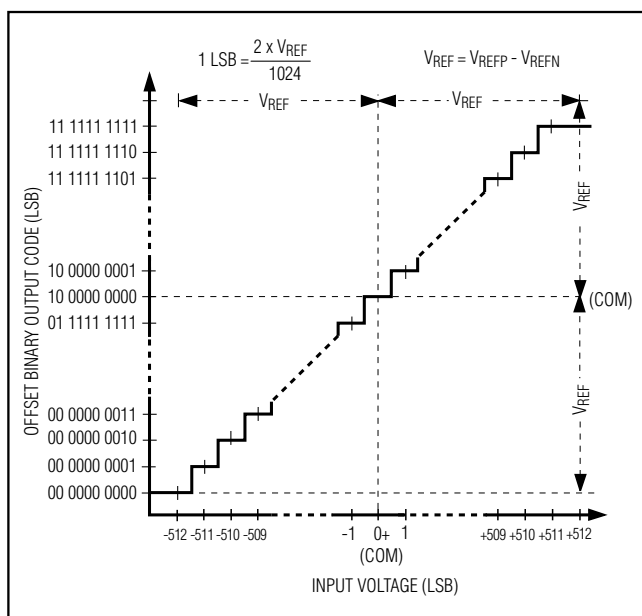


Figure 2. ADC Transfer Function

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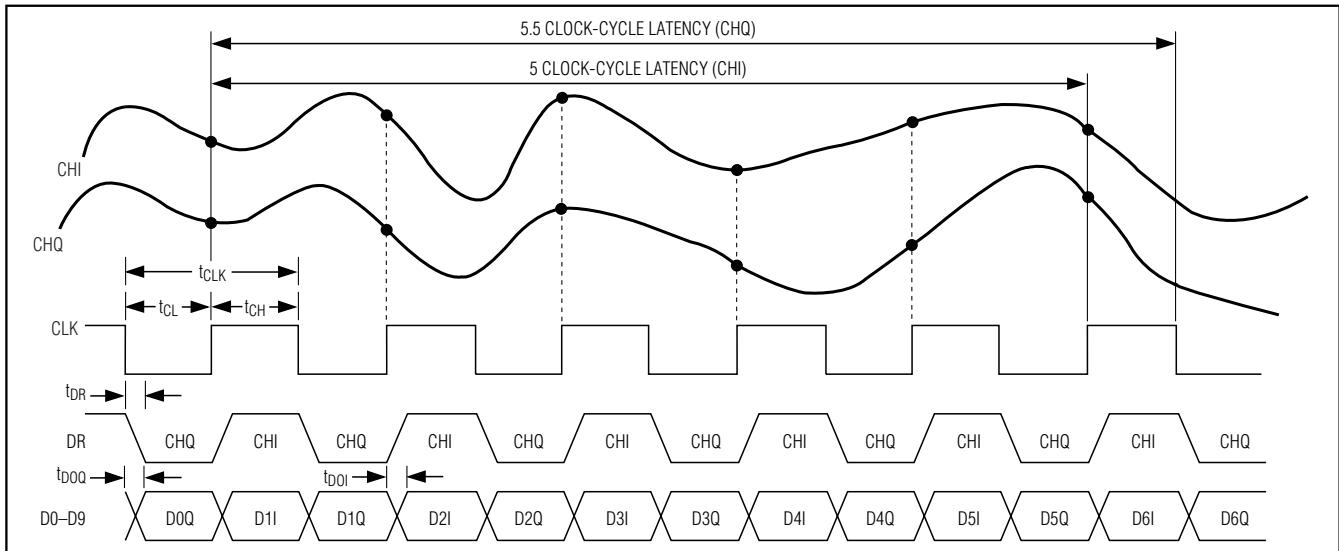


Figure 3. Rx ADC System Timing Diagram

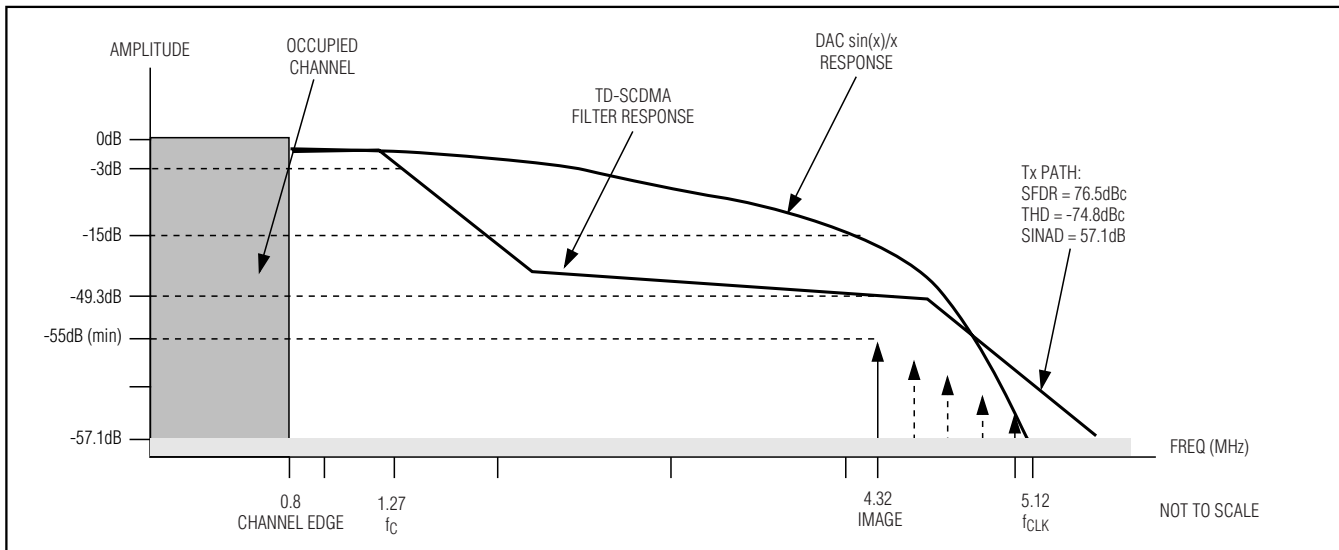


Figure 4. TD-SCDMA Filter Frequency Response

Buffer amplifiers follow the TD-SCDMA filters. The amplifier outputs are biased at an adjustable common-mode DC level and designed to drive a differential input stage with input impedance $\geq 70k\Omega$. This simplifies the analog interface between RF quadrature upconverters and the MAX19700. Many RF upconverters require a 0.9V to 1.5V common-mode bias. The SPI-controlled DC common-mode bias eliminates discrete level-setting resistors and code-generated level shifting while preserving the full dynamic range of each Tx DAC. Table 2

shows the Tx path output voltage vs. input codes. Table 10 shows the selection of DC common-mode levels.

The buffer amplifiers also feature a programmable full-scale output level of $\pm 410mV$ or $\pm 500mV$ and independent DC offset correction of each I/Q channel. Both features are configured through the SPI interface. The DC offset correction is used to optimize sideband and carrier suppression in the Tx signal path (see Tables 8 and 9).

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Table 2. Tx Path Output Voltage vs. Input Codes

(Internal Reference Mode $V_{REFDAC} = 1.024V$, External Reference Mode $V_{REFDAC} = V_{REFIN}$; $V_{FS} = 410mV$ for 820mVp-p Full Scale and $V_{FS} = 500mV$ for 1Vp-p Full Scale)

DIFFERENTIAL OUTPUT VOLTAGE (V)	OFFSET BINARY (D0–D9)	INPUT DECIMAL CODE
$(V_{FS}) \frac{V_{REFDAC}}{1024} \times \frac{1023}{1023}$	11 1111 1111	1023
$(V_{FS}) \frac{V_{REFDAC}}{1024} \times \frac{1021}{1023}$	11 1111 1110	1022
$(V_{FS}) \frac{V_{REFDAC}}{1024} \times \frac{3}{1023}$	10 0000 0001	513
$(V_{FS}) \frac{V_{REFDAC}}{1024} \times \frac{1}{1023}$	10 0000 0000	512
$(V_{FS}) \frac{-V_{REFDAC}}{1024} \times \frac{1}{1023}$	01 1111 1111	511
$(V_{FS}) \frac{-V_{REFDAC}}{1024} \times \frac{1021}{1023}$	00 0000 0001	1
$(V_{FS}) \frac{-V_{REFDAC}}{1024} \times \frac{1023}{1023}$	00 0000 0000	0

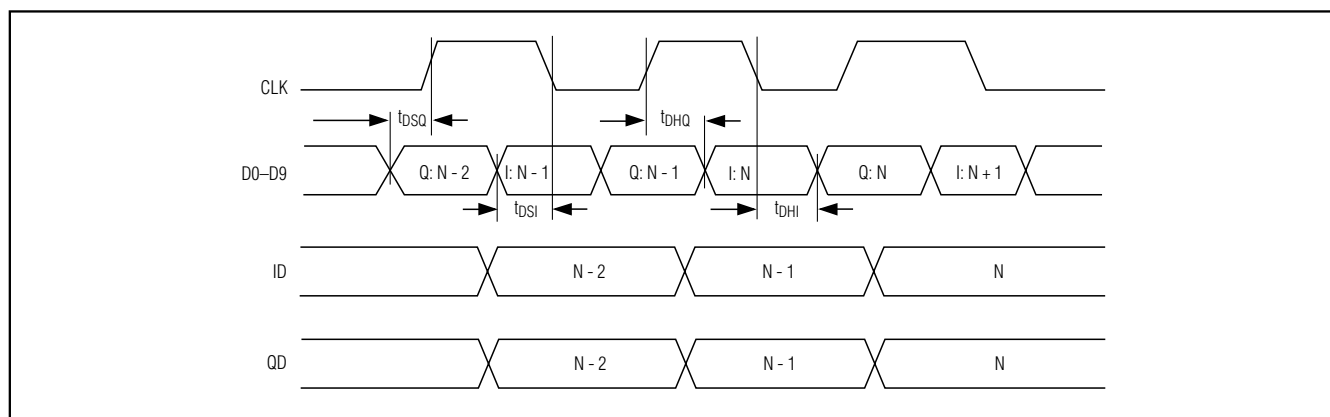


Figure 5. Tx DAC System Timing Diagram

Tx DAC Timing

Figure 5 shows the relationship between the clock, input data, and analog outputs. Data for the I-channel (ID) is latched on the falling edge of the clock signal, and Q-channel (QD) data is latched on the rising edge of the clock signal. Both I and Q outputs are simultaneously updated on the next rising edge of the clock signal.

3-Wire Serial Interface and Operation Modes

The 3-wire serial interface controls the MAX19700 operation modes as well as the three 12-bit aux-DACs. Upon power-up, program the MAX19700 to operate in the desired mode. Use the 3-wire serial interface to program the device for shutdown, idle, standby, Rx, Tx, or aux-DAC modes. A 16-bit data register sets the mode control. The 16-bit word is comprised of A3–A0 control bits and D11–D0 data bits. Tables 4, 5, and 6 show the MAX19700 operating modes and SPI commands. The serial interface remains active in all modes.

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SPI Register Description

The operating modes can be selected by programming the control bits, A3–A0, in the register as shown in Table 3. Modifying A3–A0 bits will select from ENABLE-16, Aux-DAC1, Aux-DAC2, Aux-DAC3, IOFFSET, QOFFSET, and COMSEL modes. ENABLE-16 is the default operating mode. This mode allows for shutdown, idle, and standby states as well as switching between FAST, SLOW, Rx, and Tx modes. Table 4 shows the MAX19700 power-management modes. Table 5 shows the T/R pin-controlled external Tx-Rx switching modes. Table 6 shows the SPI-controlled Tx-Rx switching modes.

In ENABLE-16 mode, the aux-DACs have independent control bits E6, E5, and E4, and the Tx-path full-scale output can be set with bit E7. Table 7 shows the auxiliary DAC enable codes and Table 8 shows the full-scale output selection. Bits E11 and E10 are reserved and need to be programmed to logic-low. Bits E9 and E8 are not used.

Modes Aux-DAC1, Aux-DAC2, and Aux-DAC3 select the aux-DAC channels named DAC1, DAC2, and DAC3 and hold the data inputs for each DAC. Bits $\overline{\text{D11}}$ – $\overline{\text{D0}}$ are the data inputs for each aux-DAC and can be programmed through SPI. The MAX19700 also includes two 6-bit registers that can be programmed to correct the offsets for the Tx-path I and Q channels independently (see Table 9). Use the COMSEL mode to select the output common-mode voltage with bits CM1 and CM0 (see Table 10).

Shutdown mode offers the most dramatic power savings by shutting down all the analog sections of the MAX19700 and placing the Rx ADC digital outputs in tri-state mode. When the Rx ADC outputs transition from tri-state to active, the last converted word is placed on the digital outputs. The Tx DAC previously stored data is lost when coming out of shutdown mode. The wake-up time from shutdown mode is dominated by the time required to charge the capacitors at REFP, REFN, and COM. In internal reference mode and buffered external reference mode, the wake-up time is typically 75 μ s to enter Rx mode and 25 μ s to enter Tx mode.

In idle mode, the reference and clock distribution circuits are powered, but all other functions are off. The Rx ADC outputs are forced to tri-state. The wake-up time is 7.3 μ s to enter Rx mode and 5 μ s to enter Tx mode. When the Rx ADC outputs transition from tri-state to active, the last converted word is placed on the digital outputs.

In standby mode, the reference is powered, but the rest of the device functions are off. The wake-up time from standby mode is 7.3 μ s to enter Rx mode and 25 μ s to enter Tx mode. When the Rx ADC outputs transition from tri-state to active, the last converted word is placed on the digital outputs.

FAST and SLOW Rx and Tx Modes

In addition to the external Tx-Rx control, the MAX19700 also features SLOW and FAST modes for switching between Rx and Tx operation. In FAST Tx mode, the Rx ADC core is powered on but the ADC core digital outputs are tri-stated on the D0–D9 bus; likewise, in FAST Rx mode the transmit path (DAC core and Tx filter) is powered on but the DAC core digital inputs are tri-stated on the D0–D9 bus. The switching time between Tx to Rx or Rx to Tx is FAST because the converters are on and do not have to recover from a power-down state. In FAST mode, the switching time between Rx to Tx and Tx to Rx is 1 μ s. However, power consumption is higher in this mode because both the Tx and Rx cores are always on. To prevent bus contention in these states, the Rx ADC output buffers are tri-stated during Tx and the Tx DAC input bus is tri-stated during Rx.

In SLOW mode, the Rx ADC core is off during Tx; likewise the Tx DAC and filters are turned off during Rx to yield lower power consumption in these modes. For example, the power in SLOW Tx mode is 31.2mW. The power consumption during Rx is 21mW compared to power consumption in FAST mode of 38.4mW. However, the recovery time between states is increased. The switching time in SLOW mode between Rx to Tx is 5 μ s and Tx to Rx is 7.3 μ s.

External T/R Switching Control vs. Serial-Interface Control

Bit E3 in the ENABLE-16 register determines whether the device Tx-Rx mode is controlled externally through the T/R input (E3 = low) or through the SPI command (E3 = high). By default, the MAX19700 is in the external Tx-Rx control mode. In the external control mode, use the T/R input (pin 27) to switch between Rx and Tx modes. Using the T/R pin provides faster switching between Rx and Tx modes. To override the external Tx-Rx control, program the MAX19700 through the serial interface. During SHDN, IDLE, or STBY modes, the T/R input is overridden. To restore external Tx-Rx control, program bit E3 low and exit the SHDN, IDLE, or STBY modes through the serial interface.

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SPI Timing

The serial digital interface is a standard 3-wire connection compatible with SPI/QSPI™/MICROWIRE/DSP interfaces. Set $\overline{CS}$ low to enable the serial data loading at DIN. Following a $\overline{CS}$ high-to-low transition, data is shifted synchronously, most significant bit first, on the rising edge of the serial clock (SCLK). After 16 bits are loaded into the serial input register, data is transferred to the latch when $\overline{CS}$ transitions high. $\overline{CS}$ must transition high for a minimum of 80ns before the next write sequence. The SCLK can idle either high or low between transitions. Figure 6 shows the detailed timing diagram of the 3-wire serial interface.

QSPI is a trademark of Motorola, Inc.

Mode-Recovery Timing

Figure 7 shows the mode-recovery timing diagram. t_{WAKE} is the wakeup time when exiting shutdown, idle, or standby mode and entering Rx or Tx mode. t_{ENABLE} is the recovery time when switching between either Rx or Tx mode. t_{WAKE} or t_{ENABLE} is the time for the Rx ADC to settle within 1dB of specified SINAD performance and Tx DAC settling to 10 LSB error. t_{WAKE} and t_{ENABLE} times are measured after either the 16-bit serial command is latched into the MAX19700 by a $\overline{CS}$ transition high (SPI controlled) or a $T/\overline{R}$ logic transition (external Tx-Rx control). In FAST mode, the recovery time is 1μs to switch between Tx or Rx modes.

Table 3. MAX19700 Mode Control

REGISTER NAME	D11 (MSB)	D10 15	D9 14	D8 13	D7 12	D6 11	D5 10	D4 9	D3 8	D2 7	D1 6	D0 5	A3 4	A2 3	A1 2	A0 1
ENABLE-16	E11 = 0 Reserved	E10 = 0 Reserved	—	—	E7	E6	E5	E4	E3	E2	E1	E0	0	0	0	0
Aux-DAC1	1D11	1D10	1D9	1D8	1D7	1D6	1D5	1D4	1D3	1D2	1D1	1D0	0	0	0	1
Aux-DAC2	2D11	2D10	2D9	2D8	2D7	2D6	2D5	2D4	2D3	2D2	2D1	2D0	0	0	1	0
Aux-DAC3	3D11	3D10	3D9	3D8	3D7	3D6	3D5	3D4	3D3	3D2	3D1	3D0	0	0	1	1
IOFFSET	—	—	—	—	—	—	IO5	IO4	IO3	IO2	IO1	IO0	0	1	0	0
QOFFSET	—	—	—	—	—	—	QO5	QO4	QO3	QO2	QO1	QO0	0	1	0	1
COMSEL	—	—	—	—	—	—	—	—	—	—	CM1	CM0	0	1	1	0

Table 4. Power-Management Modes

ADDRESS				DATA BITS				T/ $\overline{R}$	MODE	FUNCTION (POWER MANAGEMENT)	DESCRIPTION	COMMENT
A3	A2	A1	A0	E3	E2	E1	E0	PIN 27				
0000				X000				X	SHDN	SHUTDOWN	Rx ADC = OFF Tx DAC = OFF Aux-DAC = OFF REF = OFF	Device is in complete shutdown Overrides T/ $\overline{R}$ pin
				X001				X	IDLE	IDLE	Rx ADC = OFF Tx DAC = OFF Aux-DAC = Last State CLK = ON REF = ON	Fast turn-on time Moderate idle power Overrides T/ $\overline{R}$ pin
				X010				X	STBY	STANDBY	Rx ADC = OFF Tx DAC = OFF Aux-DAC = Last State CLK = OFF REF = ON	Slow turn-on time Low standby power Overrides T/ $\overline{R}$ pin

X = Don't care.

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Table 5. External Tx-Rx Control Using $\overline{T/R}$ Pin ($\overline{T/R} = 0 = \text{Rx Mode}$, $\overline{T/R} = 1 = \text{Tx Mode}$)

ADDRESS				DATA BITS				$\overline{T/R}$	STATE	FUNCTION Rx TO Tx-Tx TO Rx SWITCHING SPEED	DESCRIPTION	COMMENT
A3	A2	A1	A0	E3	E2	E1	E0	PIN 27				
0000				0011				0	Ext1-Rx	FAST-SLOW	Rx Mode Rx ADC = ON Tx DAC = ON Rx Bus = Enable	Moderate Power Fast Rx to Tx when $\overline{T/R}$ transitions 0 to 1
								1	Ext1-Tx		Tx Mode Rx ADC = OFF Tx DAC = ON Tx Bus = Enable	Low Power Slow Tx to Rx when $\overline{T/R}$ transitions 1 to 0
				0100				0	Ext2-Rx (Default)	SLOW-FAST	Rx Mode Rx ADC = ON Tx DAC = OFF Rx Bus = Enable	Low Power Slow Rx to Tx when $\overline{T/R}$ transitions 0 to 1
								1	Ext2-Tx		Tx Mode Rx ADC = ON Tx DAC = ON Tx Bus = Enable	Moderate Power Fast Tx to Rx when $\overline{T/R}$ transitions 1 to 0
				0101				0	Ext3-Rx	SLOW-SLOW	Rx Mode Rx ADC = ON Tx DAC = OFF Rx Bus = Enable	Low Power Slow Rx to Tx when $\overline{T/R}$ transitions 0 to 1
								1	Ext3-Tx		Tx Mode Rx ADC = OFF Tx DAC = ON Tx Bus = Enable	Low Power Slow Tx to Rx when $\overline{T/R}$ transitions 1 to 0
				0110				0	Ext4-Rx	FAST-FAST	Rx Mode Rx ADC = ON Tx DAC = ON Rx Bus = Enable	Moderate Power Fast Rx to Tx when $\overline{T/R}$ transitions 0 to 1
								1	Ext4-Tx		Tx Mode Rx ADC = ON Tx DAC = ON Tx Bus = Enable	Moderate Power Fast Tx to Rx when $\overline{T/R}$ transitions 1 to 0

System Clock Input (CLK)

Both the Rx ADC and Tx DAC share the CLK input. The CLK input accepts a CMOS-compatible signal level set by OV_{DD} from 1.8V to V_{DD} . Since the interstage conversion of the device depends on the repeatability of

the rising and falling edges of the external clock, use a clock with low jitter and fast rise and fall times ($<2\text{ns}$). Specifically, sampling occurs on the rising edge of the clock signal, requiring this edge to provide the lowest

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Table 6. Tx-Rx Control Using SPI Commands

ADDRESS				DATA BITS				T/R	MODE	FUNCTION (Tx-Rx SWITCHING SPEED)	DESCRIPTION	COMMENTS
A3	A2	A1	A0	E3	E2	E1	E0	PIN 27				
0000				1011				X	SPI1-Rx	SLOW	Rx Mode Rx ADC = ON Tx DAC = OFF Rx Bus = Enable	Low Power Slow Rx to Tx through SPI command
				1100				X	SPI2-Tx	SLOW	Tx Mode Rx ADC = OFF Tx DAC = ON Tx Bus = Enable	Low Power Slow Tx to Rx through SPI command
				1101				X	SPI3-Rx	FAST	Rx Mode Rx ADC = ON Tx DAC = ON Rx Bus = Enabled	Moderate Power Fast Rx to Tx through SPI command
				1110				X	SPI4-Tx	FAST	Tx Mode Rx ADC = ON Tx DAC = ON Tx Bus = Enabled	Moderate Power Fast Tx to Rx through SPI command

X = Don't care.

Table 7. Aux-DAC Enable Table
(ENABLE-16 Mode)

E6	E5	E4	Aux-DAC3	Aux-DAC2	Aux-DAC1
0	0	0	ON	ON	ON
0	0	1	ON	ON	OFF
0	1	0	ON	OFF	ON
0	1	1	ON	OFF	OFF
1	0	0	OFF	ON	ON
1	0	1	OFF	ON	OFF
1	1	0	OFF	OFF	ON
1	1	1	OFF	OFF	OFF

Table 8. Tx-Path Full-Scale Select
(ENABLE-16 Mode)

E7	Tx-PATH OUTPUT FULL SCALE
0 (Default)	820mVp-p
1	1Vp-p

possible jitter. Any significant clock jitter limits the SNR performance of the on-chip Rx ADC as follows:

$$\text{SNR} = 20 \times \log \left(\frac{1}{2 \times \pi \times f_{\text{IN}} \times t_{\text{AJ}}} \right)$$

where f_{IN} represents the analog input frequency and t_{AJ} is the time of the clock jitter.

Clock jitter is especially critical for undersampling applications. Consider the clock input as an analog input and route away from any analog input or other digital signal lines. The MAX19700 clock input operates with a $\text{OV}_{\text{DD}} / 2$ voltage threshold and accepts a 50% $\pm 15\%$ duty cycle.

12-Bit, Auxiliary Control DACs

The MAX19700 includes three 12-bit aux-DACs (DAC1, DAC2, DAC3) with 1 μ s settling time for controlling variable-gain amplifier (VGA), automatic gain-control (AGC), and automatic frequency-control (AFC) functions. The aux-DAC output range is 0.1V to 2.56V. During power-up, the VGA and AGC outputs (DAC2 and DAC3) are at zero. The AFC DAC (DAC1) is at 1.1V during power-up. The aux-DACs can be independently

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Table 9. Offset Control Bits for I and Q Channels (IOFFSET or QOFFSET Mode)

BITS IO5–IO0 WHEN IN IOFFSET MODE, BITS QO5–QO0 WHEN IN QOFFSET MODE						OFFSET 1 LSB = (VFS _{P-P} /1023)
IO5/QO5	IO4/QO4	IO3/QO3	IO2/QO2	IO1/QO1	IO0/QO0	
1	1	1	1	1	1	-31 LSB
1	1	1	1	1	0	-30 LSB
1	1	1	1	0	1	-29 LSB
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
1	0	0	0	1	0	-2 LSB
1	0	0	0	0	1	-1 LSB
1	0	0	0	0	0	0mV
0	0	0	0	0	0	0mV (Default)
0	0	0	0	0	1	1 LSB
0	0	0	0	1	0	2 LSB
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
0	1	1	1	0	1	29 LSB
0	1	1	1	1	0	30 LSB
0	1	1	1	1	1	31 LSB

Note: For transmit full-scale select of 820mV_{P-P}: 1 LSB = (820mV_{P-P}/1023) = 0.8016mV. For transmit full-scale select of 1V_{P-P}: 1 LSB = (1V_{P-P}/1023) = 0.9775mV.

Table 10. Common-Mode Select (COMSEL Mode)

CM1	CM0	Tx-PATH OUTPUT COMMON MODE (V)
0	0	1.4 (Default)
0	1	1.25
1	0	1.1
1	1	0.9

controlled through the SPI bus, except during SHDN mode where the aux-DACs are turned off completely and the output voltage is set to zero. In STBY and IDLE modes the aux-DACs maintain the last value. On wakeup from SHDN, the aux-DACs resume the last values.

Loading on the aux-DAC outputs should be carefully observed to achieve specified settling time and stability. The capacitive load must be kept to a maximum of 5pF including package and trace capacitance. The resistive load must be greater than 200kΩ. If capacitive loading exceeds 5pF, then add a 10kΩ resistor in series with the output. Adding the series resistor helps

drive larger load capacitance (<15pF) at the expense of slower settling time.

Reference Configurations

The MAX19700 features an internal precision 1.024V bandgap reference that is stable over the entire power-supply and temperature ranges. The REFIN input provides two modes of reference operation. The voltage at REFIN (V_{REFIN}) sets the reference operation mode (Table 11).

In internal reference mode, connect REFIN to V_{DD}. V_{REF} is an internally generated 0.512V ±4%. COM, REFP, and REFN are low-impedance outputs with V_{COM} = V_{DD} / 2, V_{REFP} = V_{DD} / 2 + V_{REF} / 2, and V_{REFN} = V_{DD} / 2 - V_{REF} / 2. Bypass REFP, REFN, and COM each with a 0.33μF capacitor. Bypass REFIN to GND with a 0.1μF capacitor.

In buffered external reference mode, apply 1.024V ±10% at REFIN. In this mode, COM, REFP, and REFN are low-impedance outputs with V_{COM} = V_{DD} / 2, V_{REFP} = V_{DD} / 2 + V_{REFIN} / 4, and V_{REFN} = V_{DD} / 2 - V_{REFIN} / 4. Bypass REFP, REFN, and COM each with a 0.33μF capacitor. Bypass REFIN to GND with a 0.1μF

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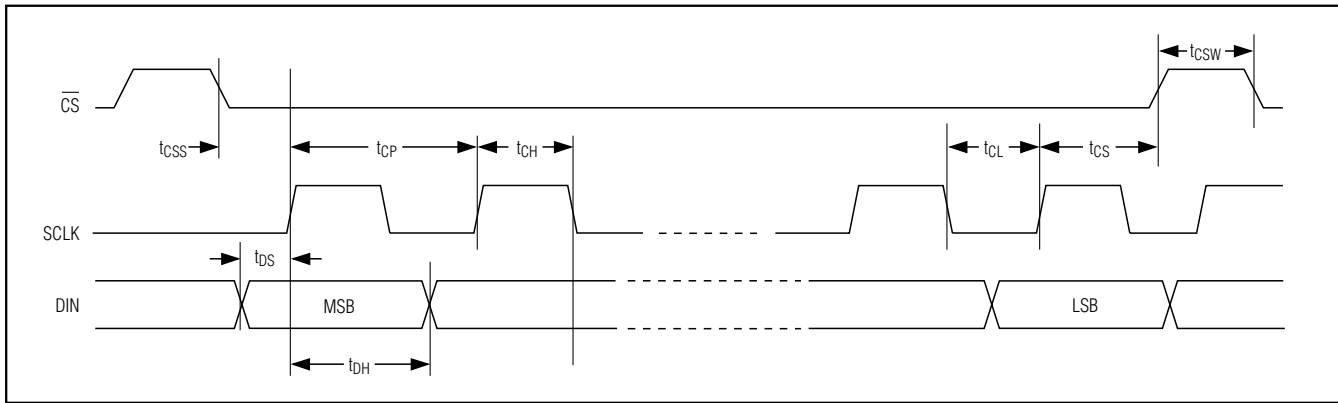


Figure 6. 3-Wire Serial-Interface Timing Diagram

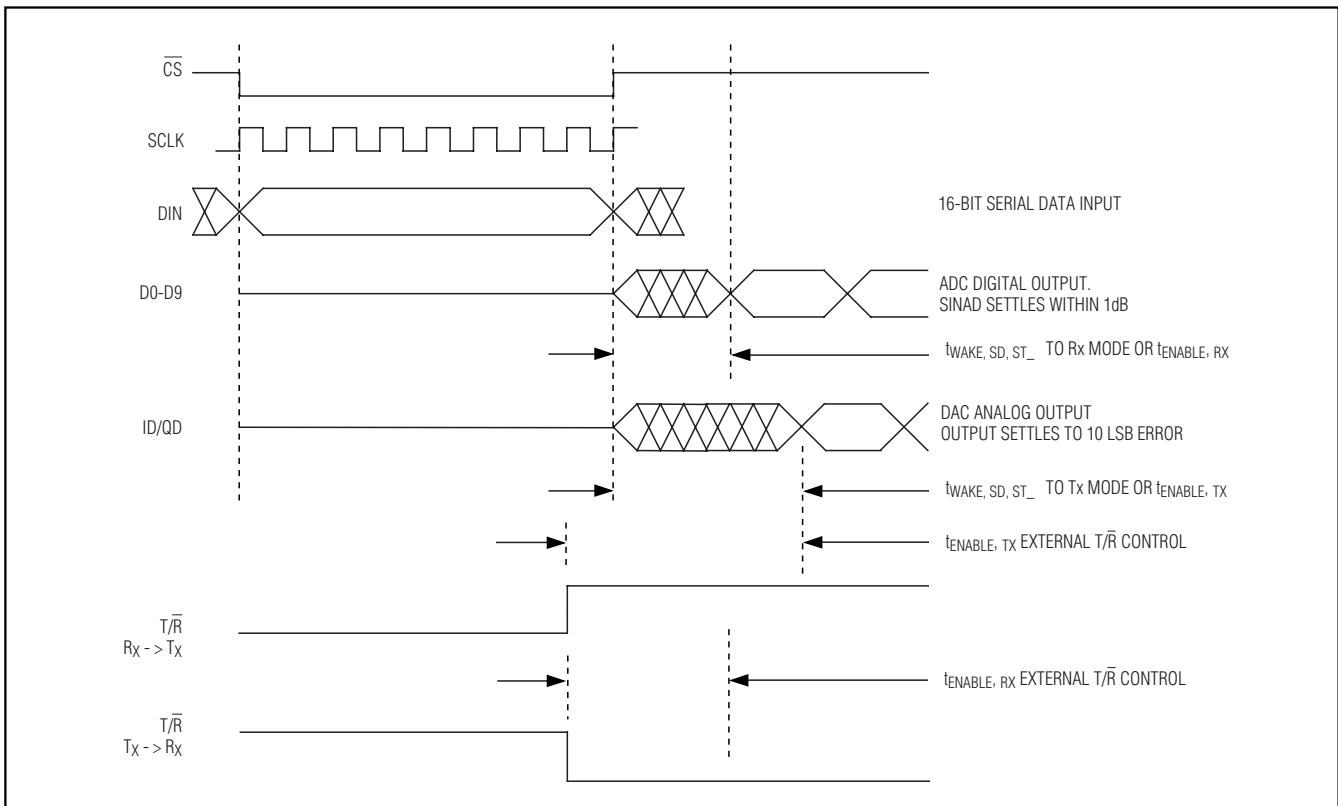


Figure 7. MAX19700 Mode-Recovery Timing Diagram

capacitor. In this mode, the Tx-path full-scale output is proportional to the external reference. For example, if the V_{REFIN} is increased by 10% (max), the Tx-path full-scale output is also increased by 10% or $\pm 451\text{mV}$.

Power-On Reset

The MAX19700 features a power-on-reset (POR) function that sets the device in a known state upon power-up. The default state is Ext2-Rx. The POR circuit is designed to accommodate power supplies that ramp

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Table 11. Reference Modes

V _{REFIN}	REFERENCE MODE
>0.8V × V _{DD}	Internal Reference Mode. V _{REF} is internally generated to be 0.512V. Bypass REFP, REFN, and COM each with a 0.33μF capacitor.
1.024V ±10%	Buffered External Reference Mode. An external 1.024V ±10% reference voltage is applied to REFIN. V _{REF} is internally generated to be V _{REFIN} / 2. Bypass REFP, REFN, and COM each with a 0.33μF capacitor. Bypass REFIN to GND with a 0.1μF capacitor.

from 0V to V_{DD} in less than or equal to 1ms. For power supplies that ramp from 0V to V_{DD} in greater than 1ms, program the MAX19700 to enter the desired state using the SPI interface.

Applications Information

Using Balun Transformer AC-Coupling

An RF transformer (Figure 8) provides an excellent solution to convert a single-ended signal source to a fully differential signal for optimum ADC performance. Connecting the center tap of the transformer to COM provides a V_{DD} / 2 DC level shift to the input. A 1:1 transformer can be used, or a step-up transformer can be selected to reduce the drive requirements. In general, the MAX19700 provides better SFDR and THD with fully differential input signals than single-ended signals, especially for high input frequencies. In differential mode, even-order harmonics are lower as both inputs (IAP, IAN, QAP, QAN) are balanced, and each of the Rx ADC inputs only requires half the signal swing compared to single-ended mode. Figure 9 shows an RF transformer converting the MAX19700 Tx DAC differential analog outputs to single-ended.

Using Op-Amp Coupling

Drive the MAX19700 Rx ADC with op amps when a balun transformer is not available. Figures 10 and 11 show the Rx ADC being driven by op amps for AC-coupled single-ended and DC-coupled differential applications. Amplifiers such as the MAX4454 and MAX4354 provide high speed, high bandwidth, low noise, and low distortion to maintain the input signal integrity. The op-amp circuit shown in Figure 11 can also be used to interface with the Tx DAC differential analog outputs to provide gain or buffering. The Tx DAC differential analog outputs cannot be used in single-ended mode because of the internally generated common-mode level. Also, the Tx DAC analog outputs are designed to drive a differential input stage with input impedance ≥70kΩ. If single-ended outputs are desired, use an amplifier to provide differential-to-single-ended conversion and select an amplifier with proper input common-mode voltage range.

TDD Mode

The MAX19700 is optimized to operate in TD-SCDMA applications. When FAST mode is selected, the MAX19700 can switch between Tx and Rx modes through the T/R pin in typically 1μs. The Rx ADC and Tx DAC operate independently. The Rx ADC and Tx DAC digital bus are shared forming a single 10-bit parallel bus. Using the 3-wire serial interface or external T/R pin, select between Rx mode to enable the Rx ADC or Tx mode to enable the Tx DAC. When operating in Rx mode, the Tx DAC bus is not enabled and in Tx mode the Rx ADC bus is tri-stated eliminating any unwanted

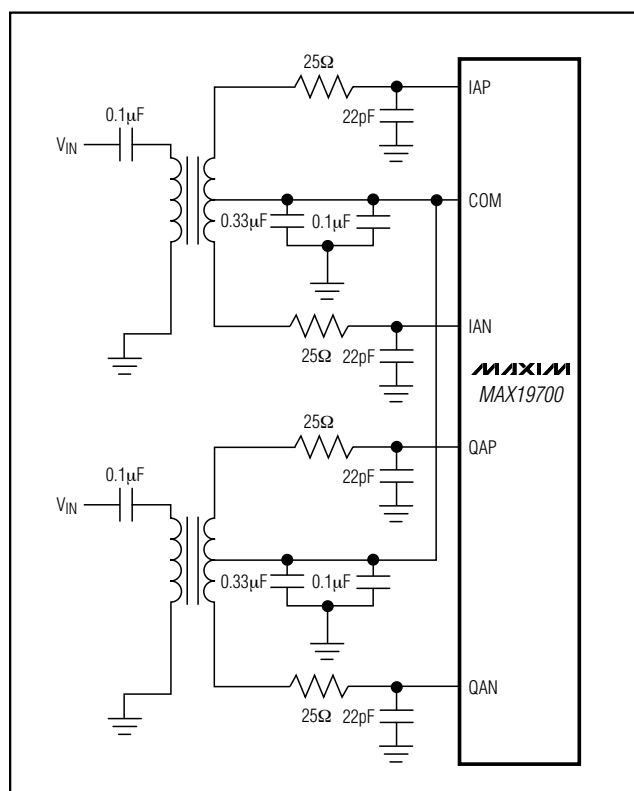


Figure 8. Balun Transformer-Coupled Single-Ended-to-Differential Input Drive for Rx ADC

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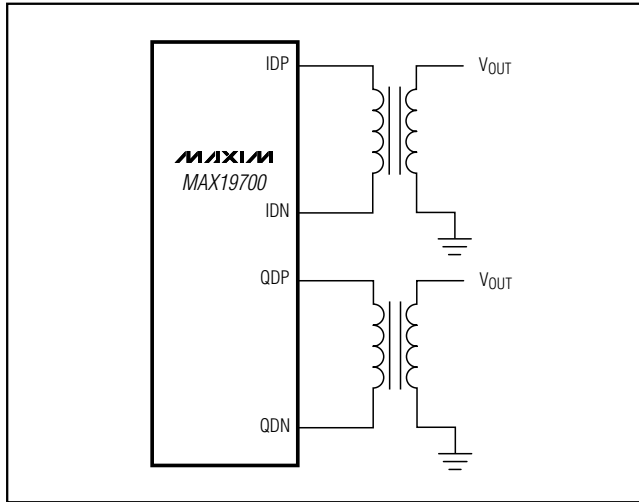


Figure 9. Balun Transformer-Coupled Differential-to-Single-Ended Output Drive for Tx DAC

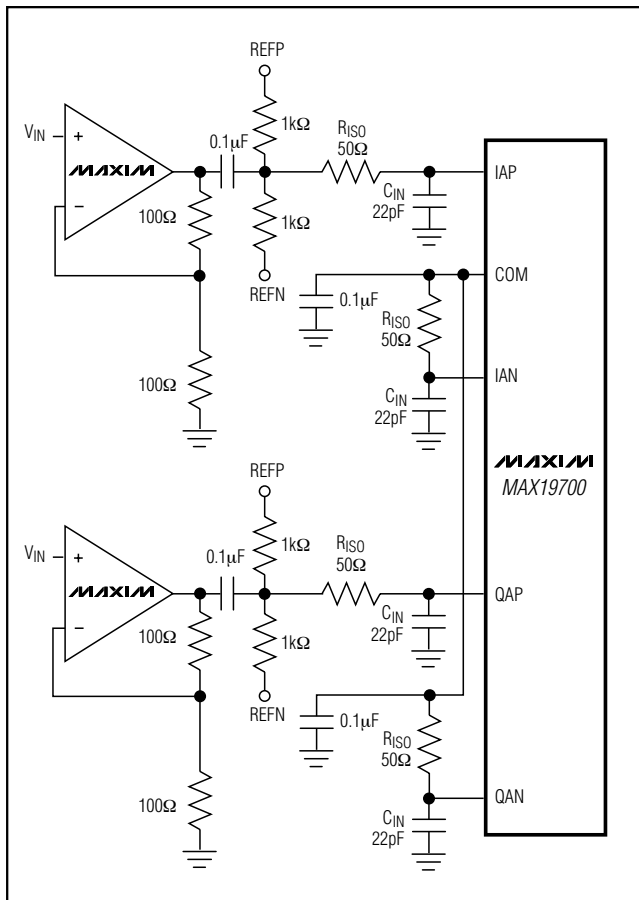


Figure 10. Single-Ended Drive for Rx ADC

spurious emissions and preventing bus contention. In TDD mode, the MAX19700 uses 38.4mW power in Rx mode at $f_{CLK} = 7.5\text{MHz}$, and 39.3mW in Tx mode.

TD-SCDMA Application

Figure 12 illustrates a typical TD-SCDMA application circuit. The MAX19700 is designed to interface directly with the MAX2507 and MAX2392 radio front-ends to provide a complete “RF-to-Bits” front-end solution. The MAX19700 provides several features that allow direct interface to the MAX2392 and MAX2507:

- Integrated Tx filters reduce component count, lower cost, and meet TD-SCDMA spectral mask requirements
- Programmable DC common-mode Tx output levels eliminate discrete DC level-shifting components while preserving Tx DAC full dynamic range
- Optimized Tx full-scale output level eliminates discrete amplifiers for I/Q gain control
- Tx-I/Q offset correction eliminates discrete trim DACs for offset trim to improve sideband/carrier suppression
- One microsecond settling time aux-DACs for VGA and AGC control allow fast, accurate Tx power and Rx gain control

Grounding, Bypassing, and Board Layout

The MAX19700 requires high-speed board layout design techniques. Refer to the MAX19700 EV kit data sheet for a board layout reference. Place all bypass capacitors as close to the device as possible, preferably on the same side of the board as the device, using surface-mount devices for minimum inductance. Bypass V_{DD} to GND with a $0.1\mu\text{F}$ ceramic capacitor in parallel with a $2.2\mu\text{F}$ capacitor. Bypass OV_{DD} to OGND with a $0.1\mu\text{F}$ ceramic capacitor in parallel with a $2.2\mu\text{F}$ capacitor. Bypass REF+, REF-, and COM each to GND with a $0.33\mu\text{F}$ ceramic capacitor. Bypass REFIN to GND with a $0.1\mu\text{F}$ capacitor.

Multilayer boards with separated ground and power planes yield the highest level of signal integrity. Use a split ground plane arranged to match the physical location of the analog ground (GND) and the digital output driver ground (OGND) on the device package. Connect the MAX19700 exposed backside paddle to GND plane. Join the two ground planes at a single point so the noisy digital ground currents do not interfere with the analog ground plane. The ideal location for this connection can be determined experimentally at a point along the gap between the two ground planes.

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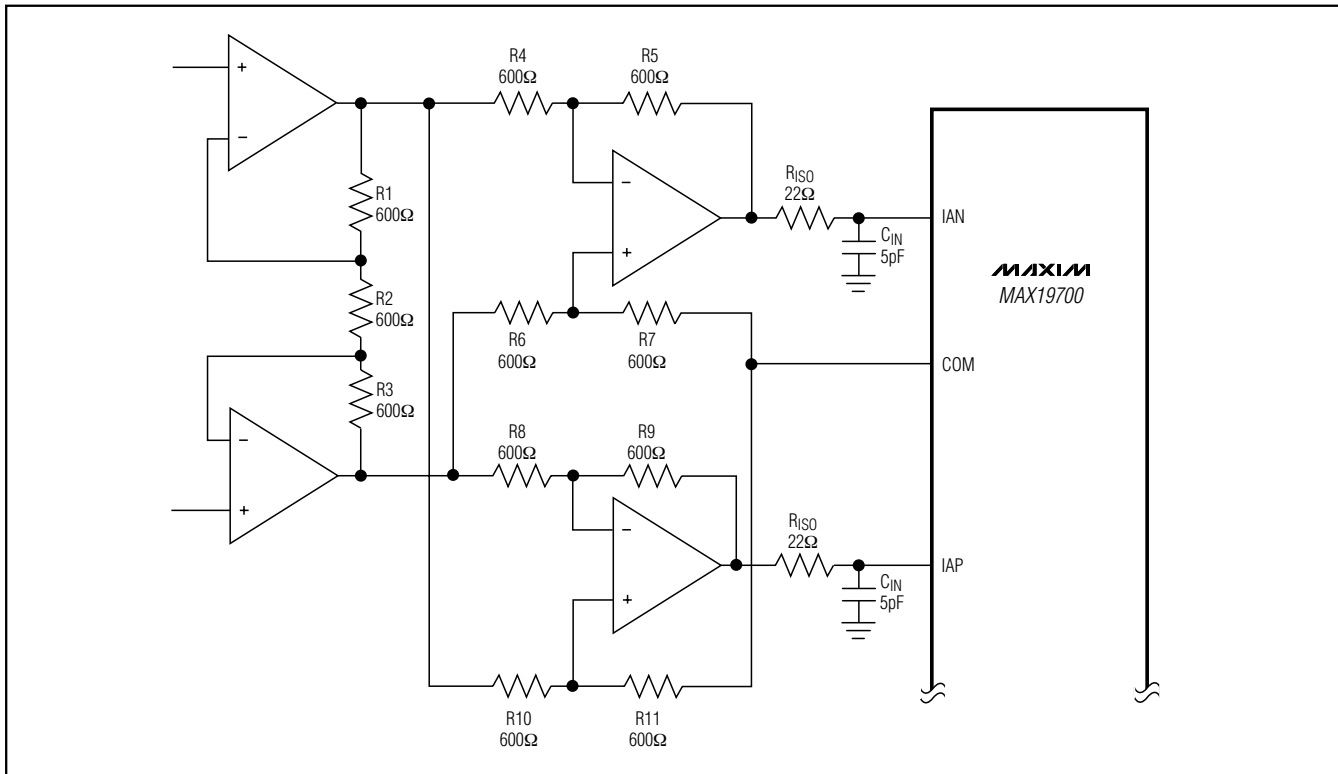


Figure 11. Rx ADC DC-Coupled Differential Drive

Make this connection with a low-value, surface-mount resistor (1Ω to 5Ω), a ferrite bead, or a direct short. Alternatively, all ground pins could share the same ground plane, if the ground plane is sufficiently isolated from any noisy digital system's ground plane (e.g., downstream output buffer or DSP ground plane).

Route high-speed digital signal traces away from sensitive analog traces. Make sure to isolate the analog input lines to each respective converter to minimize channel-to-channel crosstalk. Keep all signal lines short and free of 90° turns.

Dynamic Parameter Definitions

ADC and DAC Static Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. The static lin-

earity parameters for the device are measured using the best straight line fit (DAC Figure 13a).

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes (ADC) and a monotonic transfer function (ADC and DAC) (DAC Figure 13b).

ADC Offset Error

Ideally, the midscale transition occurs at 0.5 LSB above midscale. The offset error is the amount of deviation between the measured transition point and the ideal transition point.

DAC Offset Error

Offset error (Figure 13a) is the difference between the ideal and actual offset point. The offset point is the output value when the digital input is midscale. This error affects all codes by the same amount and usually can be compensated by trimming.

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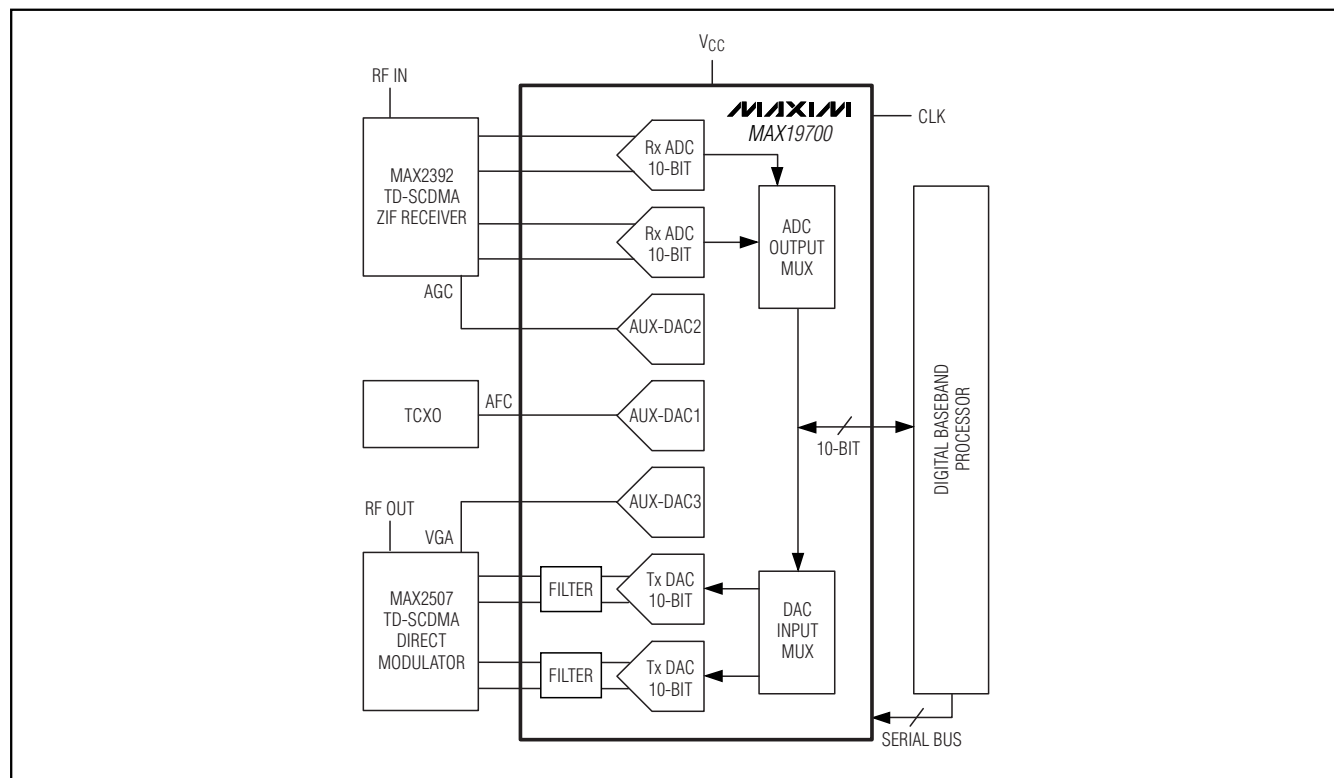


Figure 12. Typical Application Circuit for TD-SCDMA Radio

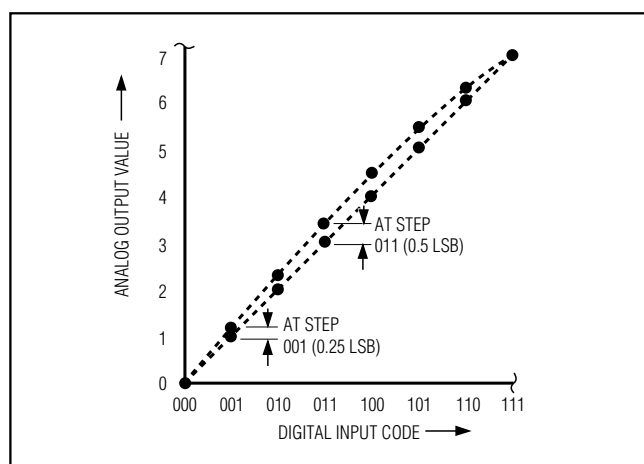


Figure 13a. Integral Nonlinearity

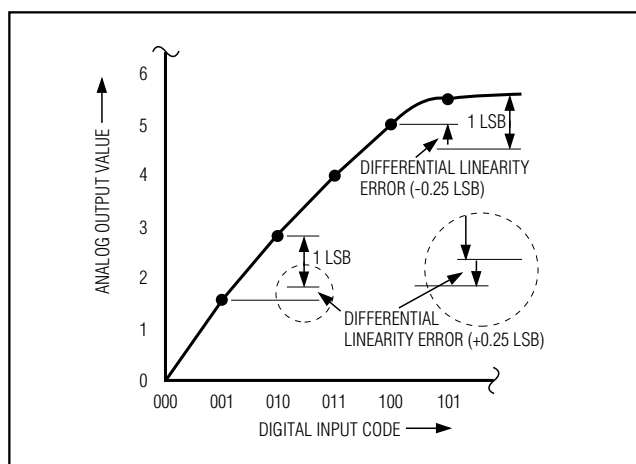


Figure 13b. Differential Nonlinearity

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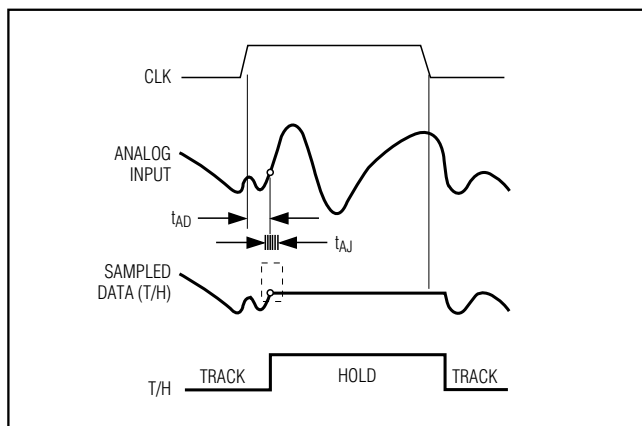


Figure 14. T/H Aperture Timing

ADC Gain Error

Ideally, the ADC full-scale transition occurs at 1.5 LSB below full scale. The gain error is the amount of deviation between the measured transition point and the ideal transition point with the offset error removed.

ADC Dynamic Parameter Definitions

Aperture Jitter

Figure 14 shows the aperture jitter (t_{AJ}), which is the sample-to-sample variation in the aperture delay.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the rising edge of the sampling clock and the instant when an actual sample is taken (Figure 14).

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error) and results directly from the ADC's resolution (N bits):

$$\text{SNR(max)} = 6.02\text{dB} \times N + 1.76\text{dB (in dB)}$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental and the DC offset.

Effective Number of Bits (ENOB)

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB for a full-scale sinusoidal input waveform is computed from:

$$\text{ENOB} = (\text{SINAD} - 1.76) / 6.02$$

Total Harmonic Distortion (THD)

THD is typically the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$\text{THD} = 20\log \left| \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1} \right|$$

where V_1 is the fundamental amplitude and V_2 – V_6 are the amplitudes of the 2nd- through 6th-order harmonics.

Third Harmonic Distortion (HD3)

HD3 is defined as the ratio of the RMS value of the third harmonic component to the fundamental input signal.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest spurious component, excluding DC offset.

Intermodulation Distortion (IMD)

IMD is the total power of the intermodulation products relative to the total input power when two tones, f_1 and f_2 , are present at the inputs. The intermodulation products are $(f_1 \pm f_2)$, $(2 \times f_1)$, $(2 \times f_2)$, $(2 \times f_1 \pm f_2)$, $(2 \times f_2 \pm f_1)$. The individual input tone levels are at -7dBFS.

3rd-Order Intermodulation (IM3)

IM3 is the power of the worst 3rd-order intermodulation product relative to the input power of either input tone when two tones, f_1 and f_2 , are present at the inputs. The 3rd-order intermodulation products are $(2 \times f_1 \pm f_2)$, $(2 \times f_2 \pm f_1)$. The individual input tone levels are at -7dBFS.

Power-Supply Rejection

Power-supply rejection is defined as the shift in offset and gain error when the power supply is changed $\pm 5\%$.

Small-Signal Bandwidth

A small -20dBFS analog input signal is applied to an ADC in such a way that the signal's slew rate does not limit the ADC's performance. The input frequency is then swept up to the point where the amplitude of the digitized conversion result has decreased by 3dB. Note that the T/H performance is usually the limiting factor for the small-signal input bandwidth.

7.5Msps, Ultra-Low-Power Analog Front-End

Full-Power Bandwidth

A large -0.5dBFS analog input signal is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by 3dB. This point is defined as the full-power bandwidth frequency.

DAC Dynamic Parameter Definitions

Total Harmonic Distortion

THD is the ratio of the RMS sum of the output harmonics up to the Nyquist frequency divided by the fundamental:

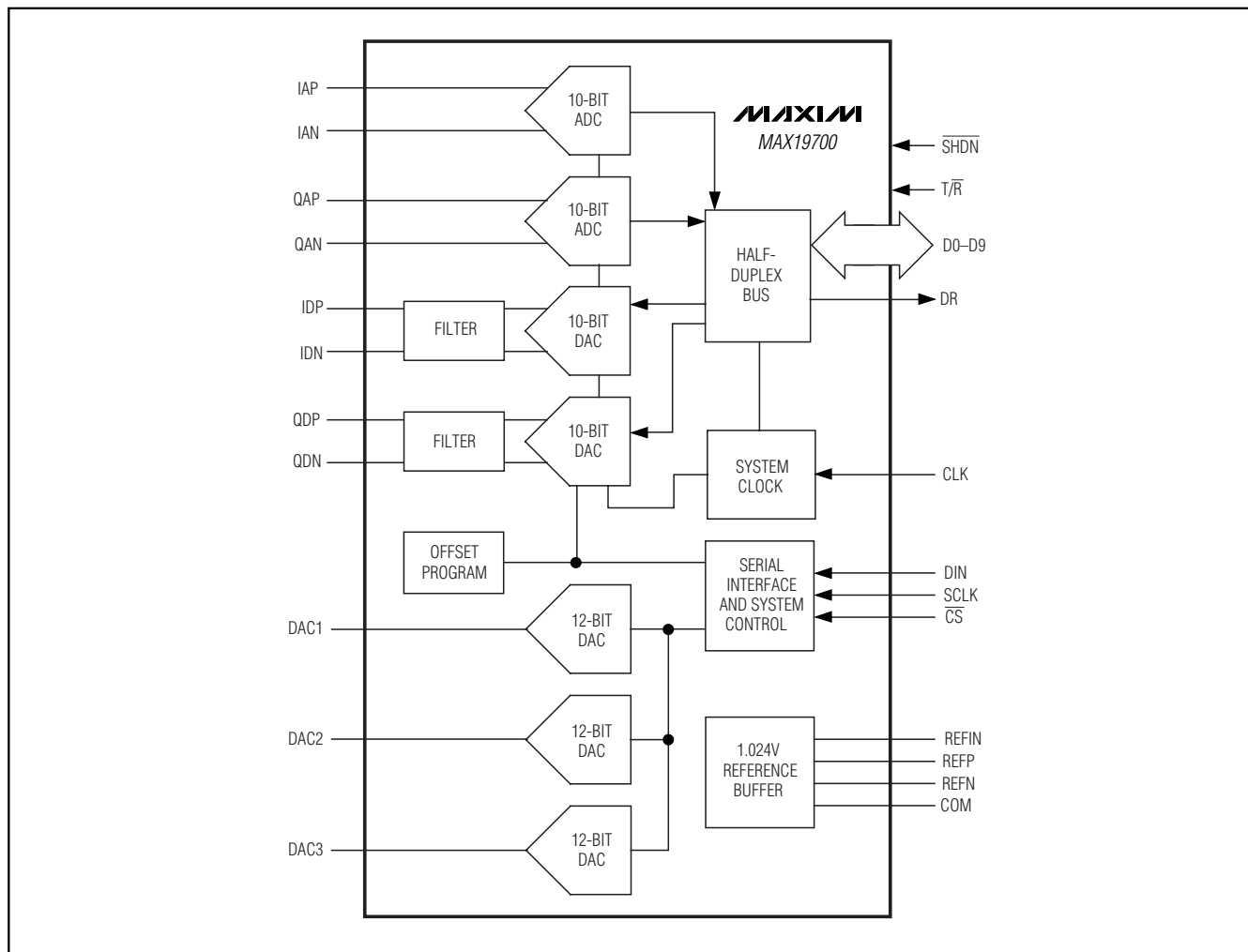
$$\text{THD} = 20\log \left[\frac{\sqrt{V_2^2 + V_3^2 + \dots + V_n^2}}{V_1} \right]$$

where V_1 is the fundamental amplitude and V_2 through V_n are the amplitudes of the 2nd through nth harmonic up to the Nyquist frequency.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest distortion component up to the Nyquist frequency excluding DC.

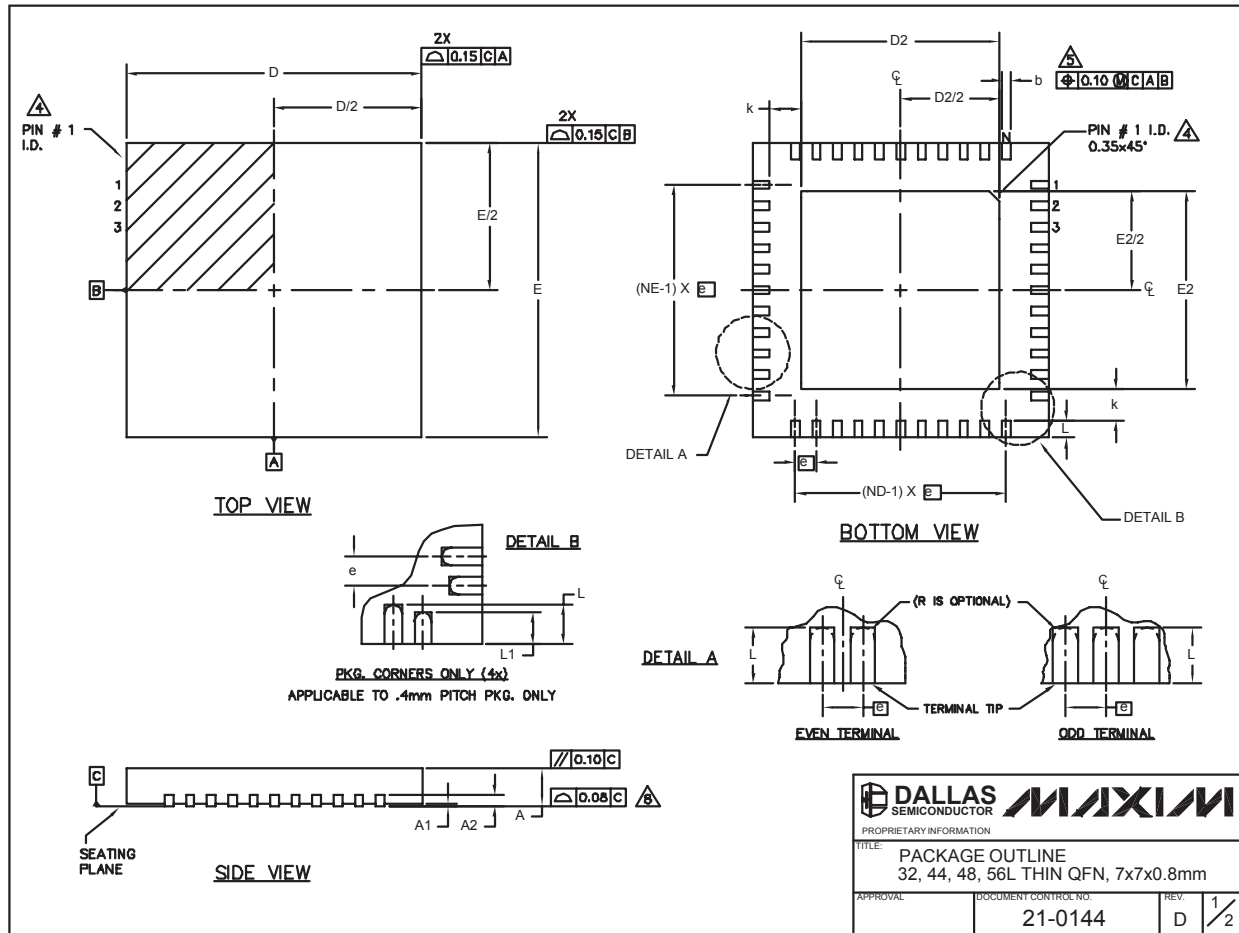
Functional Diagram



7.5Msps, Ultra-Low-Power Analog Front-End

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



32, 44, 48L QFN:EPS

MAX19700

7.5Mbps, Ultra-Low-Power Analog Front-End

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

COMMON DIMENSIONS															
PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7			56L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	—	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	0.35	0.45
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65	0.40	0.50	0.60
L1	—	—	—	—	—	—	—	—	—	—	—	—	0.30	0.40	0.50
N	32			44			48			44			56		
ND	8			11			12			10			14		
NE	8			11			12			12			14		

EXPOSED PAD VARIATIONS									
PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C	DOWN BONDS ALLOWED
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T3277-1	—	4.55	4.70	4.85	4.55	4.70	4.85	—	NO
T3277-2	—	4.55	4.70	4.85	4.55	4.70	4.85	—	YES
T4477-1	—	4.55	4.70	4.85	4.55	4.70	4.85	WKD-1	NO
T4477-2	—	4.55	4.70	4.85	4.55	4.70	4.85	WKD-1	YES
T4477-3	—	4.55	4.70	4.85	4.55	4.70	4.85	WKD-1	YES
T4877-1**	13,24,37,48	4.20	4.30	4.40	4.20	4.30	4.40	—	NO
T4877-2	—	5.45	5.60	5.63	5.45	5.60	5.63	—	NO
T4877-3	—	4.95	5.10	5.25	4.95	5.10	5.25	—	YES
T4877-4	—	5.45	5.60	5.63	5.45	5.60	5.63	—	YES
T4877-5	—	2.40	2.50	2.60	2.40	2.50	2.60	—	NO
T4877-6	—	5.45	5.60	5.63	5.45	5.60	5.63	—	NO
T5677-1	—	5.20	5.30	5.40	5.20	5.30	5.40	—	YES

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 EXCEPT THE EXPOSED PAD DIMENSIONS OF T3277-1; T4877-1/-2/-3/-4/-5/-6 & T5677-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

 DALLAS SEMICONDUCTOR			
PROPRIETARY INFORMATION			
TITLE: PACKAGE OUTLINE 32, 44, 48, 56L THIN QFN, 7x7x0.8mm			
APPROVAL	DOCUMENT CONTROL NO.		REV.
	21-0144		D 2/2

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