# RLDRAM II Controller MegaCore Function

May 2007, MegaCore Version 7.1 Errata Sheet

This document addresses known errata and documentation issues for the RLDRAM II Controller MegaCore® function version 7.1. Errata are functional defects or errors, which may cause the RLDRAM II Controller MegaCore function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Table 1 shows the issues that affect the RLDRAM II Controller MegaCore function v7.1.

*Table 1. RLDRAM II Controller MegaCore Function v7.1 Issues*


| Issue | Page |
|---|---|
| Error when Upgrading from v7.0 to v7.1 | 1 |
| NativeLink Fails with the ModelSim Simulator | 2 |
| Add an RLDRAM II Controller to a Project with Other Memory Controllers | 3 |
| Simulating with the NCSim Software | 4 |
| Simulating with the VCS Simulator | 4 |
| Multiple Instances of the auk_ddr_functions.vhd File | 5 |
| Gate-Level Simulation Filenames | 5 |
| Unpredictable Results for Gate-Level Simulations (HardCopy II Devices only) | 6 |
| Editing the Custom Variation (non-DQS Mode) | 7 |


For the most up-to-date errata for this release, refer to the errata sheet on the Altera® website:

**www.altera.com/literature/es/es_rldram_ii_71.pdf**

## RLDRAM II Controller MegaCore Function v7.1 Issues

This section describes the RLDRAM II Controller MegaCore function v7.1 issues.

### Error when Upgrading from v7.0 to v7.1

If you upgrade an existing custom variation of the RLDRAM II MegaCore function to v7.1, the following error occurs:

```
Error (10430): VHDL Primary Unit Declaration error at
auk_rldramii_functions.vhd(5): primary unit "auk_rldramii_functions"
already exists in library "work"
```

IP Toolbench adds files to your Quartus II project when you generate your custom variation. When you upgrade your MegaCore function from v7.0 to v7.1, the same files from the previous and current versions are present in the same Quartus II project, which causes a VHDL error.

### *Affected Configurations*

This issue affects all designs that were created in a previous version of the MegaCore function and then upgraded to v7.1

### *Workaround*

From your Quartus II project, remove the Device Design Files that were added by the earlier version of the MegaCore function. These files can be identified by the files' directory names.

### *Design Impact*

You cannot compile your Quartus II project until you remove the duplicate files.

### *Solution Status*

This issue will be fixed in a future version of the RLDRAM II controller.

## NativeLink Fails with the ModelSim Simulator

When using NativeLink to run VHDL gate-level simulations using the ModelSim software, the simulation fails with the following error message:

```
# ** Error: (vcom-19) Failed to access library 'altera' at "altera".
```

### *Affected Configurations*

The issue affects VHDL gate-level simulations.

### *Design Impact*

The design does not simulate.

### *Workaround*

The following lines need to be added to the NativeLink-generated gate-level simulation script:

```
vlib vhdl_libs/altera

vmap altera vhdl_libs/altera

vcom -work altera <Quartus installation
directory>/libraries/vhdl/altera/altera_europa_support_lib.vhd
```

### *Solution Status*

This issue will be fixed in a future version of the RLDRAM II controller.

## Add an RLDRAM II Controller to a Project with Other Memory Controllers

If you try to generate a new RLDRAM II controller in a project that already contains a DDR, DDR2, QDRII, or RLDRAM II controller, the example design gets corrupted and the compilation fails.

### *Affected Configurations*

This issue affects all configurations.

### *Design Impact*

The design does not compile.

### *Workaround*

To workaround this issue, follow these steps:

1. Generate the RLDRAM II controller in a new project and update the required project to instantiate the new RLDRAM II controller.
2. Copy the constraints from the new RLDRAM II project to the target project.
3. Copy the new RLDRAM II design files into the target project directory.

### *Solution Status*

This issue will be fixed in a future version of the RLDRAM II controller.

## Simulating with the NCSim Software

The RLDRAM II Controller MegaCore function v7.1 does not fully support the NCSim software.

### *Affected Configurations*

This issue affects all configurations.

### *Design Impact*

The design does not simulate.

### *Workaround*

Set the `-relax` switch for all calls to the VHDL or Verilog HDL analyzer.

### *Solution Status*

This issue will be fixed in a future version of the RLDRAM II controller.

## Simulating with the VCS Simulator

The RLDRAM II Controller MegaCore function v7.1 does not fully support the VCS simulator.

### *Affected Configurations*

This issue affects all configurations.

### *Design Impact*

The design does not simulate.

### *Workaround*

For VHDL simulations, in the <*variation name*>**_example_driver.vhd** file, change all `when` statements from:

```
when std_logic_vector'("<bit_pattern>")
```

to:

```
when "<bit_pattern>"
```

### *Solution Status*

This issue will be fixed in a future version of the RLDRAM II controller.

## Multiple Instances of the auk_ddr_functions.vhd File

When a project contains multiple memory MegaCore functions, the Quartus® II project has multiple instances of the **auk_ddr_functions.vhd** file (one per MegaCore function).

### *Affected Configurations*

This issue affects all configurations.

### *Design Impact*

The Quartus II project fails during compilation.

### *Workaround*

Remove the **auk_ddr_functions.vhd** file associated with the RLDRAM II controller from the list of files added to the Quartus II project, by choosing **Add/Remove Files from Project** (Project menu). Keep only the **auk_ddr_functions.vhd** file associated with the DDR or DDR2 SDRAM controller.

### *Solution Status*

This issue will be fixed in a future version of the RLDRAM II controller.

## Gate-Level Simulation Filenames

Various Quartus II software options may cause it to generate a netlist with a different filename to that expected by the gate-level simulation script. The simulation script expects <*project name*>**.vho** or **.vo** and <*project name*>**_v** or **_vhd.sdo** files to be present.

### *Affected Configurations*

This issue affects all configurations.

### *Design Impact*

You cannot run gate-level simulations.

### *Workaround*

For VHDL gate-level simulations, in the **simulation/modelsim** directory follow these steps:

1. Rename <*filename*>**.vho** file to <*project name*>**.vho.**
2. Rename <*filename*>**.sdo** file to <*project name*>**_vhd.sdo**.

For Verilog HDL gate-level simulations, in the **simulation/modelsim** directory follow these steps:

1. Rename the <*filename*>**.vo** file to <*project name*>**.vo.**
2. Rename the <*filename*>**.sdo** file to <*project name*>**_v.sdo**.
3. In the <*project name*>.**vo** file change the following line to point to the <*project name*>**_v.sdo** file:

```
initial $sdf_annotate("<project name>_v.sdo");
```

### *Solution Status*

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

## Unpredictable Results for Gate-Level Simulations (HardCopy II Devices only)

Gate-level simulations may not work as expected on HardCopy® II devices, because HardCopy II timing is preliminary in the Quartus II software version 5.1.

### *Affected Configurations*

This issue affects all configurations on HardCopy II devices.

### *Design Impact*

There is no design impact.

### *Workaround*

This issue has no workaround.

### *Solution Status*

This issue will be fixed in a future version of the Quartus II software.

## Editing the Custom Variation (non-DQS Mode)

When you generate a non-DQS mode custom variation with wide databus widths, you may encounter one of the following characteristics when you try to edit the custom variation:

- IP Toolbench does not reload
- IP Toolbench reloads, but the databus width and constraints are set to the default for the selected RLDRAM II device
- IP Toolbench reloads, but the databus width is set to the default value for the selected RLDRAM II device and the constraints floorplan shows no chosen byte groups

### *Affected Configurations*

This issue affects non-DQS mode designs only.

### *Design Impact*

There is no design impact, if you implement the workaround.

### *Workaround*

Use one of the following workarounds:

- If IP Toolbench does not reload, you must regenerate a new custom variation and re-enter your parameters
- If IP Toolbench reloads, but the databus width and constraints are set to the default, reselect the databus width and rechoose the byte groups in the constraints floorplan
- If IP Toolbench reloads, but the databus width is set to the default and the constraints floorplan shows no byte groups, reselect the databus width and rechoose the byte groups in the constraints floorplan

### *Solution Status*

This issue will be fixed in a future version of the RLDRAM II controller.

# Contact Information

For more information, contact Altera's mySupport website at **www.altera.com/mysupport** and click **Create New Service Request**. Choose the **Product Related Request** form.

## Revision History

Table 2 shows the revision history for the RLDRAM II Controller MegaCore function v7.1.

*Table 2. RLDRAM II Controller v7.1 Errata Sheet Revision History*

| Version | Date | Errata Summary |
|---|---|---|
| 1.0 | May 2007 | First release. |

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
www.altera.com
Applications Hotline:
(800) 800-EPLD
Literature Services:
literature@altera.com