

0.35-Ω Low-Voltage Dual SPDT Analog Switch

DESCRIPTION

The DG2535/DG2536 is a sub 1 Ω (0.35 Ω at 2.7 V) dual SPDT analog switches designed for low voltage applications. The DG2535/DG2536 has on-resistance matching (less than 0.05 Ω at 2.7 V) and flatness (less than 0.2 Ω at 2.7 V) that are guaranteed over the entire voltage range. Additionally, low logic thresholds make the DG2535/DG2536 an ideal interface to low voltage DSP control signals.

The DG2535/DG2536 has fast switching speed with break-before-make guaranteed. In the On condition, all switching elements conduct equally in both directions. Off-isolation and crosstalk is - 69 dB at 100 kHz.

The DG2535/DG2536 is built on Vishay Siliconix's high-density low voltage CMOS process. An epitaxial layer is built in to prevent latchup. The DG2535/DG2536 contains the additional benefit of 2,000 V ESD protection.

In space saving MSOP-10 and DFN-10 lead (Pb)-free packages, the DG2535/DG2536 are high performance, low r_{ON} switches for battery powered applications. No lead (Pb) is used in the manufacturing process either inside the device/package or on the external terminations. As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For analog switching products manufactured in DFN packages, the lead (Pb)-free "-E3/E4" suffix is being used as a designator. Lead (Pb)-free DFN products purchased at any time will have either a nickel-palladium-gold device termination or a 100 % matte tin device termination. The different lead (Pb)-free materials are interchangeable and meet all JEDEC standards for reflow and MSL rating.

FEATURES

- Low Voltage Operation
- Low On-Resistance - r_{ON} : 0.35 Ω at 2.7 V
- - 69 dB OIRR at 2.7 V, 100 kHz
- MSOP-10 and DFN-10 Packages
- ESD Protection > 2000 V
- Latch-Up Current > 300 mA (JESD 78)


RoHS
COMPLIANT

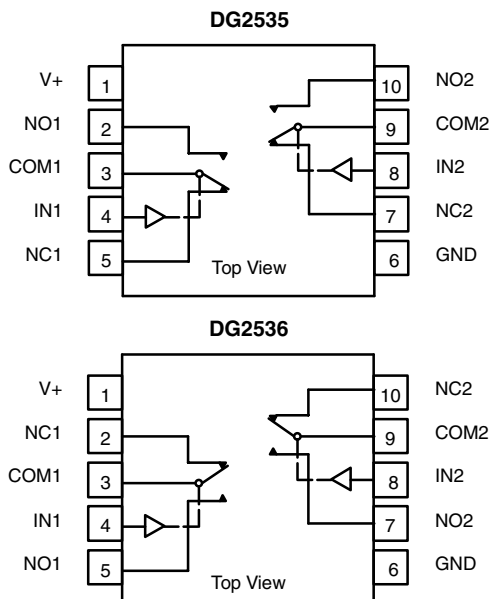
BENEFITS

- Reduced Power Consumption
- High Accuracy
- Reduce Board Space
- 1.8 V Logic Compatible
- High Bandwidth

APPLICATIONS

- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems
- Relay Replacement

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE

Logic	NC1 and NC2	NO1 and NO2
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION

Temp Range	Package	Part Number
- 40 to 85 °C	MSOP-10	DG2535DQ-T1-E3 DG2536DQ-T1-E3
	DFN-10	DG2535DN-T1-E4 DG2536DN-T1-E4

ABSOLUTE MAXIMUM RATINGS			
Parameter		Limit	Unit
Referenced V+ to GND		- 0.3 to + 6	V
IN, COM, NC, NO ^a		- 0.3 to (V+ + 0.3)	
Continuous Current (NO, NC, COM)		± 300	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 500	
Storage Temperature (D Suffix)		- 65 to 150	°C
ESD per Method 3015.7		> 2	kV
Power Dissipation (Packages) ^b	MSOP-10 ^c	320	mW
	DFN-10 ^d	1191	

Notes:

a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC Board.

c. Derate 4.0 mW/°C above 70 °C

d. Derate 14.9 mW/°C above 70 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V+ = 3 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, V _{IN} = 0.5 or 1.4 V ^e	Temp ^a	Limits - 40 to 85 °C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} V _{COM}		Full	0		V+	V
On-Resistance	r _{ON}	V+ = 2.7 V, V _{COM} = 0.6 V/1.5 V, I _{NO} , I _{NC} = 100 mA	Room Full		0.35	0.5 0.6	Ω
r _{ON} Flatness ^d	r _{ON} Flatness		Room		0.09	0.2	
On-Resistance Match Between Channels ^d	Δr _{DS(on)}		Room			0.05	
Switch Off Leakage Current	I _{NO(off)} I _{NC(off)}	V+ = 3.3 V V _{NO} , V _{NC} = 0.3 V/3 V, V _{COM} = 3 V/0.3 V	Room Full	- 1 - 10		1 10	nA
	I _{COM(off)}		Room Full	- 1 - 10		1 10	
Channel-On Leakage Current	I _{COM(on)}	V+ = 3.3 V, V _{NO} , V _{NC} = V _{COM} = 0.3 V/3 V	Room Full	- 1 - 10		1 10	
Digital Control							
Input High Voltage ^d	V _{INH}		Full	1.4			V
Input Low Voltage	V _{INL}		Full			0.5	
Input Capacitance	C _{in}		Full		10		pF
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	1		1	μA



SPECIFICATIONS (V+ = 3 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, VIN = 0.4 or 2.0 V ^e	Temp ^a	Limits - 40 to 85 °C			Unit
				Min ^b	Typ ^c	Max ^b	
Dynamic Characteristics							
Turn-On Time	t _{ON}	V _{NO} or V _{NC} = 2.0 V, R _L = 50 Ω, C _L = 35 pF	Room Full		52	82 90	ns
Turn-Off Time	t _{OFF}		Room Full		43	73 78	
Break-Before-Make Time	t _d		Full	1	6		
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{GEN} = 1.5 V, R _{GEN} = 0 Ω	Room		21		pC
Off-Isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 100 kHz	Room		- 69		dB
Crosstalk ^d	X _{TALK}		Room		- 69		
N _O , N _C Off Capacitance ^d	C _{NO(off)}	VIN = 0 or V+, f = 1 MHz	Room		145		pF
	C _{NC(off)}		Room		145		
Channel-On Capacitance ^d	C _{NO(on)}	VIN = 0 or V+, f = 1 MHz	Room		406		
	C _{NC(on)}		Room		406		
Power Supply							
Power Supply Current	I+	VIN = 0 or V+	Full			1.0	μA

Notes:

a. Room = 25 °C, Full = as determined by the operating suffix.

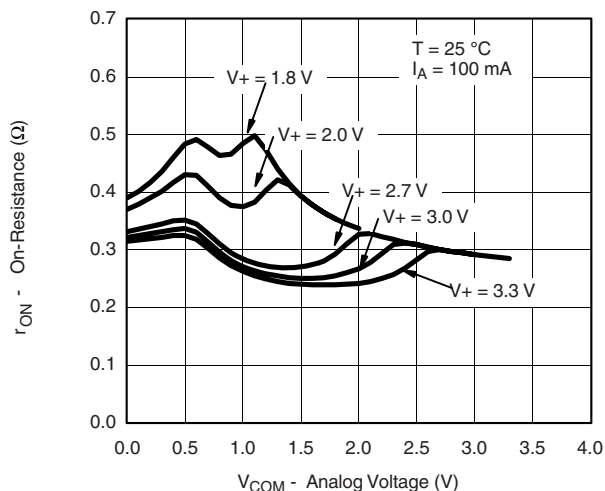
b. Typical values are for design aid only, not guaranteed nor subject to production testing.

c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

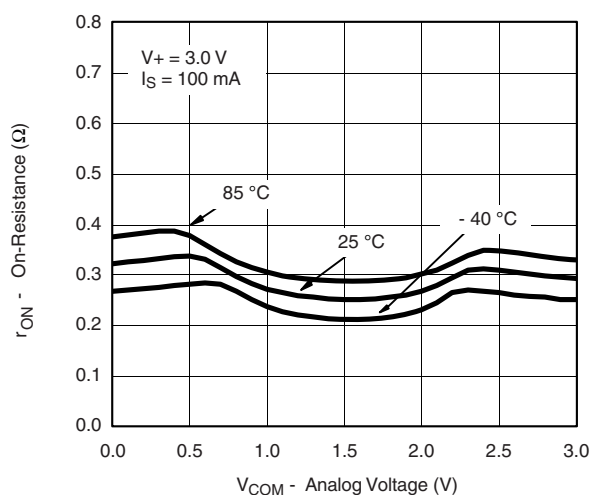
d. Guarantee by design, nor subjected to production test.

e. V_{IN} = input voltage to perform proper function.

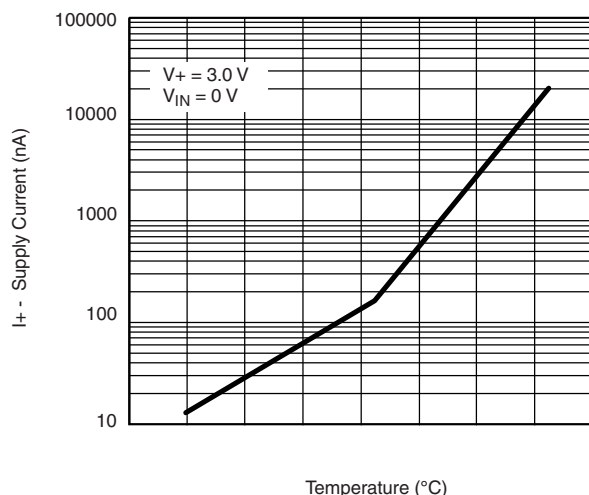
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



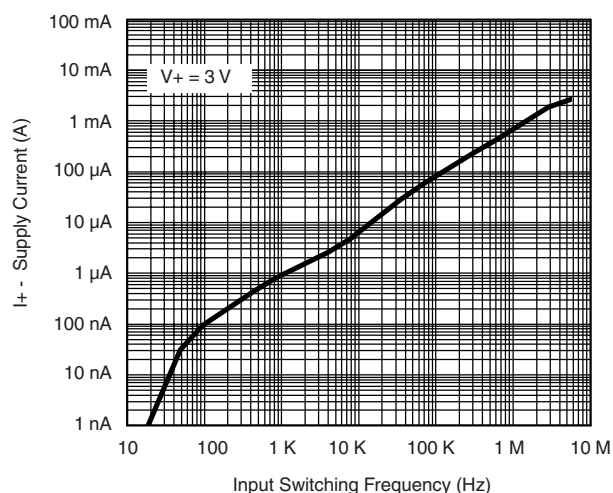
r_{ON} vs. V_{COM} and Supply Voltage



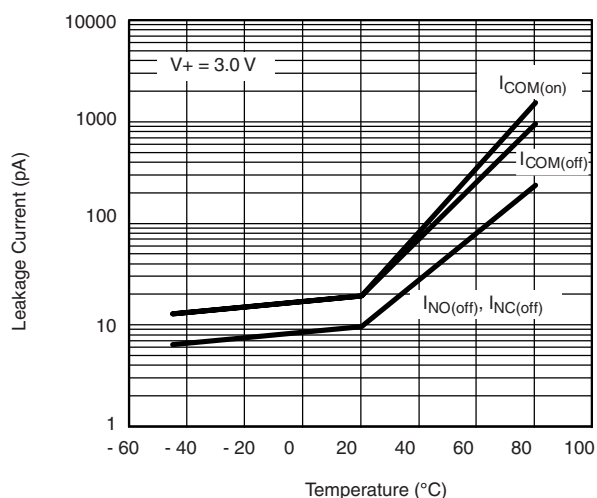
r_{ON} vs. Analog Voltage and Temperature (NC1)



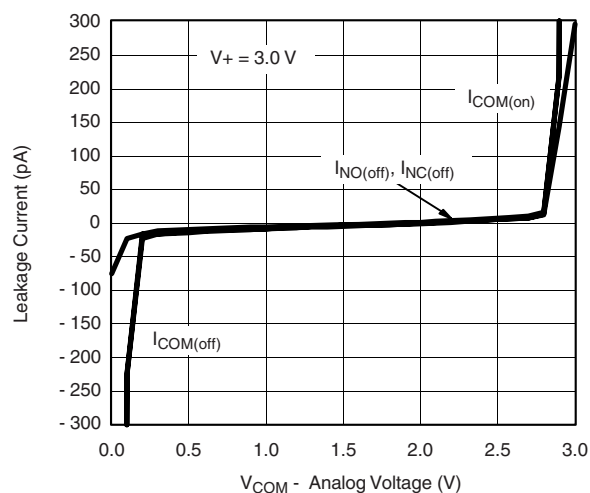
Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency



Leakage Current vs. Temperature



Leakage vs. Analog Voltage

A line graph showing the ratio of on-time to off-time (t_{ON} / t_{OFF}) in nanoseconds versus temperature in degrees Celsius for the 74VHC00. The y-axis ranges from 0 to 100 ns, and the x-axis ranges from -60 to 100 °C. Four curves are plotted for different supply voltages (V_{+}):

- $t_{ON} V_{+} = 2V$: The highest curve, starting at approximately 74 ns at -40 °C and rising to about 87 ns at 85 °C.
- $t_{ON} V_{+} = 3V$: The second curve from the top, starting at approximately 45 ns at -40 °C and rising to about 60 ns at 85 °C.
- $t_{OFF} V_{+} = 3V$: The third curve from the top, starting at approximately 44 ns at -40 °C and rising to about 56 ns at 85 °C.
- $t_{OFF} V_{+} = 2V$: The lowest curve, starting at approximately 35 ns at -40 °C and rising to about 48 ns at 85 °C.

An arrow points to the gap between the t_{ON} and t_{OFF} curves at $V_{+} = 2V$, indicating the difference between the two parameters.

Figure 1 is a line graph showing the frequency response of the OIRR and X_{TALK} . The x-axis represents Frequency (Hz) on a logarithmic scale from 100 K to 1 G. The y-axis represents Loss, OIRR, and X_{TALK} in dB, ranging from -90 to 10. Three curves are plotted: X_{TALK} (solid line), OIRR (dashed line), and Loss (dotted line). The X_{TALK} and OIRR curves start at -70 dB at 100 K Hz, rise to a peak of -5 dB at 100 M Hz, and then drop. The Loss curve is flat at -5 dB until 100 M Hz, then drops. Parameters: $V_+ = 3.0$ V, $R_L = 50 \Omega$.

The graph plots the switching threshold V_T against the supply voltage V_+ . The x-axis represents V_+ in Volts, ranging from 0 to 6. The y-axis represents V_T in Volts, ranging from 0.00 to 2.00. Two parallel lines are shown, with the region between them shaded in light gray. The lower line starts at approximately (1.8V, 0.65V) and ends at (5.0V, 1.22V). The upper line starts at approximately (1.8V, 0.90V) and ends at (5.0V, 1.60V).

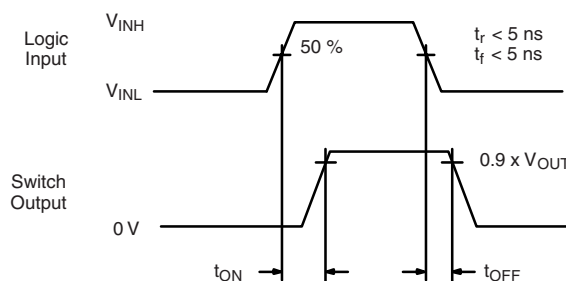
V_+ (V)	Lower V_T (V)	Upper V_T (V)
1.8	0.65	0.90
5.0	1.22	1.60

The graph shows the charge injection (Q) in pC as a function of the analog voltage (V_{COM}) in V. Two curves are plotted for different positive supply voltages (V_+): 2.0 V and 3.0 V. The y-axis ranges from -300 pC to 300 pC, and the x-axis ranges from 0.0 V to 3.0 V. The curve for $V_+ = 2.0$ V starts at approximately -190 pC at 0.0 V, crosses 0 pC at 1.0 V, peaks at about 130 pC at 1.5 V, and then decreases to approximately 80 pC at 3.0 V. The curve for $V_+ = 3.0$ V starts at approximately -240 pC at 0.0 V, crosses 0 pC at 1.0 V, peaks at about 150 pC at 2.0 V, and then decreases to approximately 80 pC at 3.0 V.

V_{COM} (V)	Q (pC) for $V_+ = 2.0$ V	Q (pC) for $V_+ = 3.0$ V
0.0	-190	-240
0.5	-100	-180
1.0	0	0
1.5	130	30
2.0	110	150
2.5	100	150
3.0	80	80

Charge Injection vs. Analog Voltage

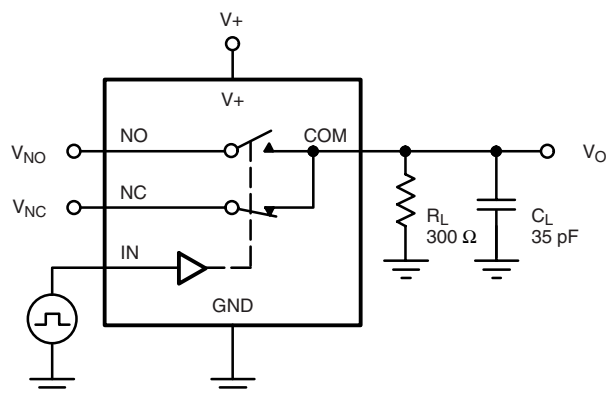
The diagram shows a 74VHC14 inverter. The input is connected to a switch labeled 'Switch Input'. The output is connected to a switch labeled 'Switch Output'. The output is also connected to a load resistor R_L (300 Ω) and a load capacitor C_L (35 pF). The input is also connected to a logic input signal. The output is connected to a 0 V ground.

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$


Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

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TEST CIRCUITS



C_L (includes fixture and stray capacitance)

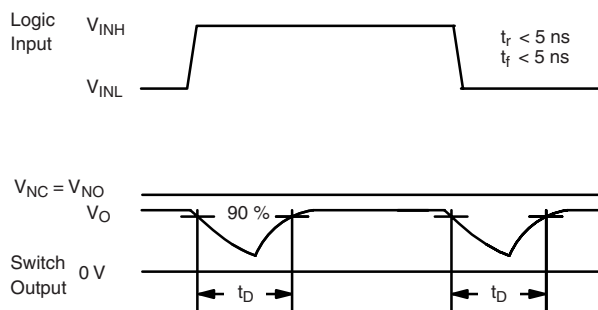
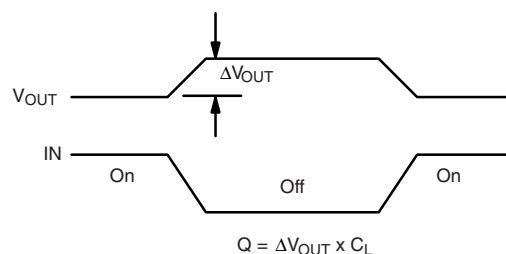
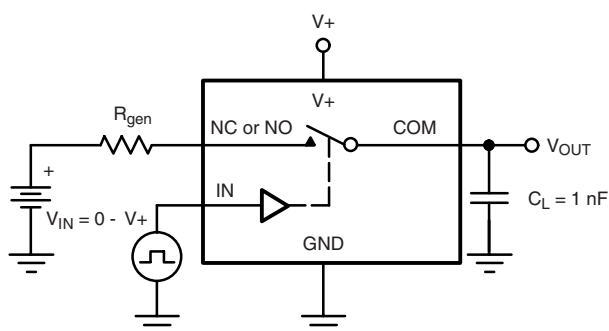


Figure 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

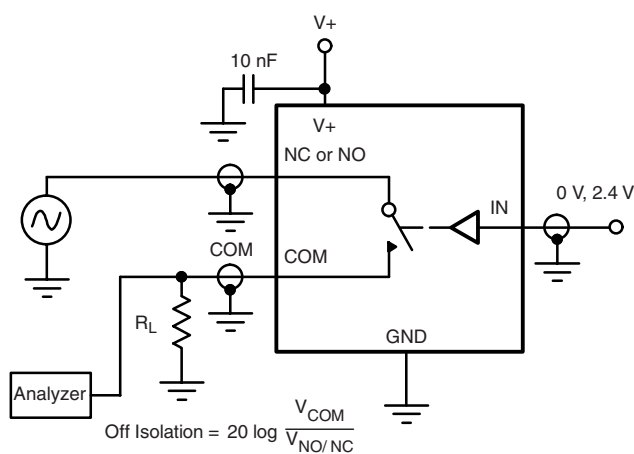


Figure 4. Off-Isolation

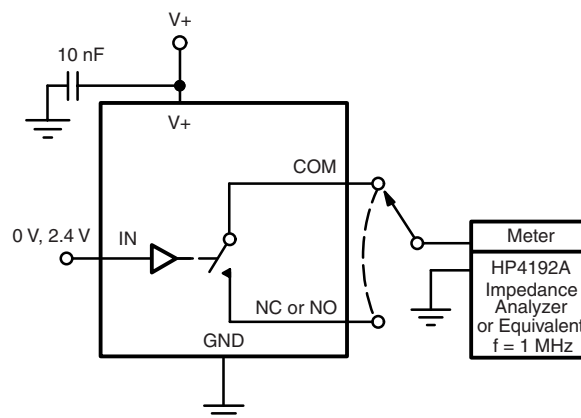


Figure 5. Channel Off/On Capacitance

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