Freescale Semiconductor
Data Sheet: Technical Data

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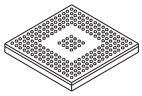
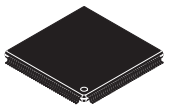
MPC5510



MAPBGA–208
17 mm x 17 mm



LQFP–144
20 mm x 20 mm

LQFP–176
24 mm x 24 mm

MPC5510 Microcontroller Family Data Sheet

MPC5510 Family Features

- Single issue, 32-bit CPU core complex (e200z1)
  - Compliant with the Power Architecture™ embedded category
  - Includes an instruction set enhancement allowing variable length encoding (VLE) for code size footprint reduction. With the optional encoding of mixed 16-bit and 32-bit instructions, it is possible to achieve significant code size footprint reduction.
- Up to 1.5-Mbyte on-chip flash with flash control unit (FCU)
- Up to 80 Kbytes on-chip SRAM
- Memory protection unit (MPU) with up to sixteen region descriptors and 32-byte region granularity
- Interrupt controller (INTC) capable of handling selectable-priority interrupt sources
- Frequency modulated Phase-locked loop (FMPLL)
- Crossbar switch architecture for concurrent access to peripherals, flash, or RAM from multiple bus masters
- 16-channel enhanced direct memory access controller (eDMA)
- Boot assist module (BAM) supports internal flash programming via a serial link (CAN or SCI)
- Timer supports input/output channels providing a range of 16-bit input capture, output compare, and pulse width modulation functions (eMIOS200)
- Up to 40-channel 12-bit analog-to-digital converter (ADC)
- Up to four serial peripheral interface (DSPI) modules
- Media Local Bus (MLB) emulation logic (works with two DSPIs, the e200z0, the eDMA, and system RAM to create a 3-pin or 5-pin 256Fs MLB protocol)
- Up to eight serial communication interface (eSCI) modules
- Up to six enhanced full CAN (FlexCAN) modules with configurable buffers
- One inter IC communication interface (I^2C) module
- Up to 144 configurable general purpose pins supporting input and output operations and 3.0V through 5.5V supply levels
- Real-time counter (RTC_API) with clock source from external 32-kHz crystal oscillator, internal 32-kHz or 16-MHz oscillator and supporting wake-up with selectable 1-second resolution and > 1-hour timeout, or 1-millisecond resolution with maximum timeout of one second
- Up to eight periodic interrupt timers (PIT) with 32-bit counter resolution
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 Class Two Plus standard
- Device/board test support per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator (VREG) for regulation of 5V input to 1.5V and 3.3V internal supply levels
- Optional e200z0, second Power Architecture based I/O processor with VLE instruction set
- Optional FlexRAY controller
- Optional external bus interface (EBI) module

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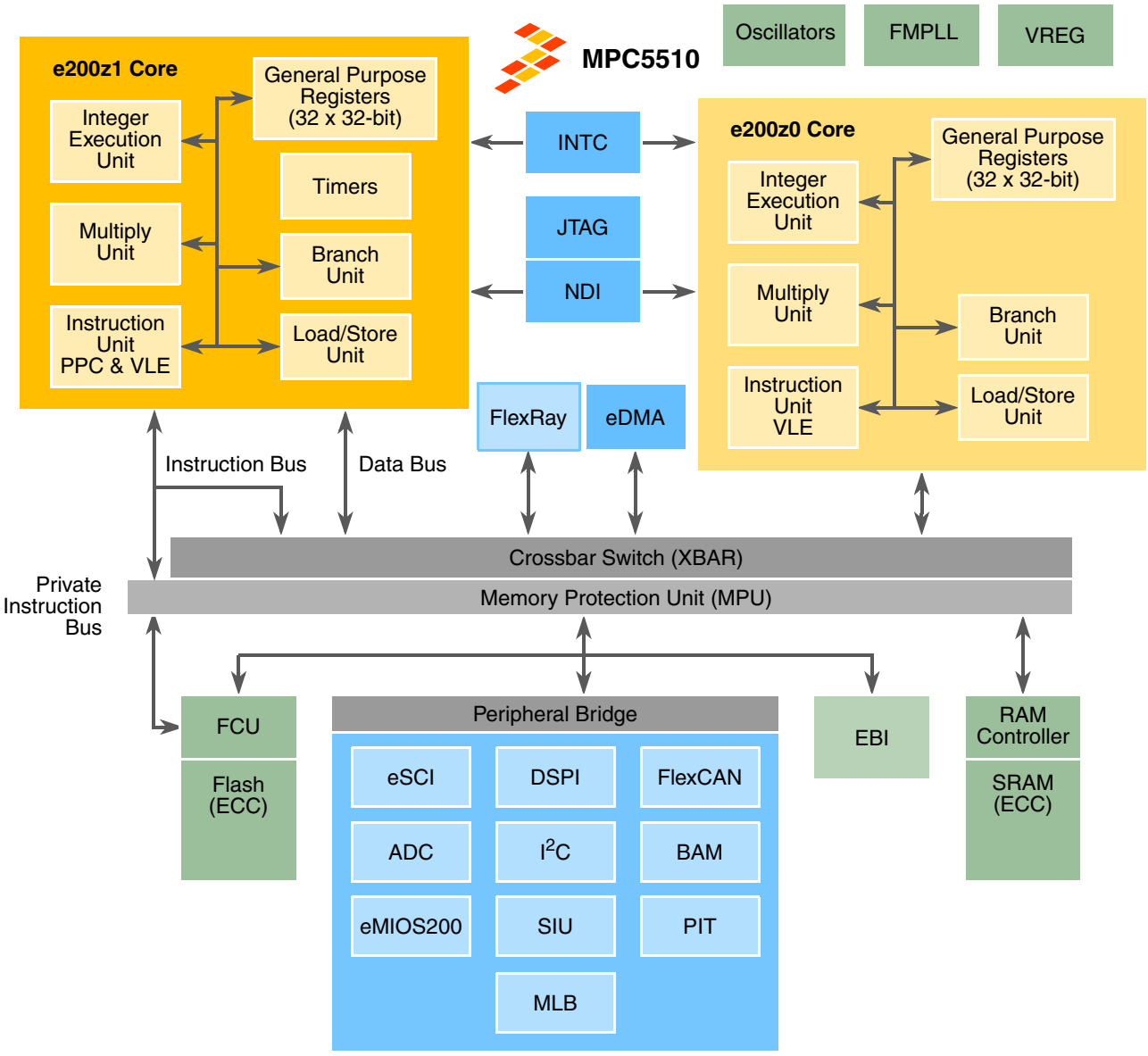

LEGEND

ADC	– Analog to Digital Converter modules	**FlexRay**	– Dual Channel FlexRay controller
BAM	– Boot Assist Module	**FMPLL**	– Frequency Modulated Phase Locked Loop module
EBI	– External Bus Interface module	**I^2C**	– Inter IC Controller modules
ECC	– Error Correction Code	**INTC**	– Interrupt Controller module
DSPI	– Serial Peripherals Interface controller module	**JTAG**	– Joint Test Action Group interface
eDMA	– enhanced Direct Memory Controller module	**MLB**	– Media Local Bus emulation logic
eMIOS200	– Timed Input Output module	**NDI**	– Nexus Debug Interface module
eSCI	– Serial Communications Interface modules	**PIT**	– Periodic Interrupt Timer module
FCU	– Flash Controller Unit	**SIU**	– System Integration module
FlexCAN	– Controller Area Network controller modules	**VREG**	– Voltage Regulator

Figure 1. MPC5510 Family Block Diagram

1 Pin Assignments and Reset States

1.1 Signal Properties and Multiplexing Summary

Table 1 shows the signal properties for each pin on the MPC5510. For all port pins, which have an associated pad configuration register (SIU_PCR*n* register) to control its pin properties, the "Supported Pin Functions" column lists the functions associated with the programming of the SIU_PCR*n*[PA] bit field in the following order: GPIO, Function1, Function2 and Function3. If fewer than three functions plus GPIO are supported by a given pin, then the unused functions begin with Function3, then Function2, then Function1. Note that the GPIO number is the same number as the corresponding pad configuration register (SIU_PCR*n*) number.

Table 1. MPC5510 Signal Properties

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
Port A (16)											
PA0	0	PA0 AN0	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	9	9	E3
PA1	1	PA1 AN1	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	8	8	E2
PA2	2	PA2 AN2	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	7	7	E1
PA3	3	PA3 AN3	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	6	6	D3
PA4	4	PA4 AN4	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	5	5	D2
PA5	5	PA5 AN5	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	4	4	D1
PA6	6	PA6 AN6	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	3	3	C2
PA7	7	PA7 AN7	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	2	2	C1
PA8	8	PA8 AN8/ANW	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	143	175	A3
PA9	9	PA9 AN9/ANX	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	142	174	C4
PA10	10	PA10 AN10/ANY	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	140	172	D5
PA11	11	PA11 AN11/ANZ	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	139	171	C5
PA12	12	PA12 AN12	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	138	170	B5
PA13	13	PA13 AN13	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	137	169	A5
PA14	14	PA14 AN14 EXTAL32[6]	GPI eQADC Analog Input 32 kHz Crystal Oscillator Input	I I I	V_{DDA}	AE + IH	—	—	136	167	D6

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PA15	15	PA15 AN15 XTAL32[6]	GPI eQADC Analog Input 32 kHz Crystal Oscillator Output	I I O	V_{DDA}	AE + IH	—	—	135	165	C6
Port B (16)											
PB0	16	PB0 AN28 eMIOS16 PCS_C5	GPIO eQADC Analog Input[7] eMIOS Channel DSPI_C Peripheral Chip Select	I/O I O O	V_{DDE1}	A + SH	—	—	134	162	C7
PB1	17	PB1 AN29 eMIOS17 PCS_C4	GPIO eQADC Analog Input[7] eMIOS Channel DSPI_C Peripheral Chip Select	I/O I O O	V_{DDE1}	A + SH	—	—	133	161	D7
PB2	18	PB2 AN30 eMIOS18 PCS_C3	GPIO eQADC Analog Input[7] eMIOS Channel DSPI_C Peripheral Chip Select	I/O I O O	V_{DDE1}	A + SH	—	—	132	160	A8
PB3	19	PB3 AN31 PCS_C2	GPIO eQADC Analog Input[7] DSPI_C Peripheral Chip Select	I/O I O	V_{DDE1}	A + SH	—	—	131	159	B8
PB4	20	PB4 AN32 PCS_C1	GPIO eQADC Analog Input[7] DSPI_C Peripheral Chip Select	I/O I O	V_{DDE1}	A + SH	—	—	130	158	C8
PB5	21	PB5 AN33 PCS_C0	GPIO eQADC Analog Input[7] DSPI_C Peripheral Chip Select	I/O I I/O	V_{DDE1}	A + SH	—	—	129	157	D8
PB6	22	PB6 AN34 SCK_C	GPIO eQADC Analog Input[7] DSPI_C Clock	I/O I I/O	V_{DDE1}	A + SH	—	—	128	156	A9
PB7	23	PB7 AN35 SOUT_C	GPIO eQADC Analog Input[7] DSPI_C Data Output	I/O I O	V_{DDE1}	A + SH	—	—	127	153	B9
PB8	24	PB8 AN36 SIN_C	GPIO eQADC Analog Input[7] DSPI_C Data Input	I/O I I	V_{DDE1}	A + SH	—	—	126	152	C9
PB9	25	PB9 AN37 CNTX_D PCS_B4	GPIO eQADC Analog Input[7] CAN_D Transmit DSPI_B Peripheral Chip Select	I/O I O O	V_{DDE1}	A + SH	—	—	125	151	D9
PB10	26	PB10 AN38 CNRX_D PCS_B3	GPIO eQADC Analog Input[7] CAN_D Receive DSPI_B Peripheral Chip Select	I/O I I O	V_{DDE1}	A + SH	—	—	124	150	A10
PB11	27	PB11 AN39 eMIOS19 PCS_B5	GPIO eQADC Analog Input[7] eMIOS Channel DSPI_B Peripheral Chip Select	I/O I O O	V_{DDE1}	A + SH	—	—	123	149	B10

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PB12	28	PB12 TXD_G PCS_B4	GPIO SCI_G Transmit DSPI_B Peripheral Chip Select	I/O O O	V_{DDE1}	SH	—	—	—	164	A7
PB13	29	PB13 RXD_G PCS_B3	GPIO SCI_G Receive DSPI_B Peripheral Chip Select	I/O I O	V_{DDE1}	SH	—	—	—	163	B7
PB14	30	PB14 TXD_H	GPIO SCI_H Transmit	I/O O	V_{DDE1}	SH	—	—	—	148	C10
PB15	31	PB15 RXD_H	GPIO SCI_H Receive	I/O I	V_{DDE1}	SH	—	—	—	147	A11
Port C (16)											
PC0	32	PC0 eMIOS0 FR_A_TX_EN AD24	GPIO eMIOS Channel FlexRay Channel A Transmit Enable EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	122	146	B11
PC1	33	PC1 eMIOS1 FR_A_TX AD16	GPIO eMIOS Channel FlexRay Channel A Transmit EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	121	145	C11
PC2	34	PC2 eMIOS2 FR_A_RX $\overline{TS}$	GPIO eMIOS Channel FlexRay Channel A Receive EBI Transfer Start	I/O I/O I I/O	V_{DDE1}	MH	—	—	120	144	D11
PC3	35	PC3 eMIOS3 FR_DBG0	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	MH	—	—	117	141	A12
PC4	36	PC4 eMIOS4 FR_DBG1	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	SH	—	—	116	140	B12
PC5	37	PC5 eMIOS5 FR_DBG2	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	SH	—	—	115	139	C12
PC6	38	PC6 eMIOS6 FR_DBG3	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	SH	—	—	114	138	D12
PC7	39	PC7 eMIOS7 FR_B_RX	GPIO eMIOS Channel FlexRay Channel B Receive	I/O I/O I	V_{DDE1}	SH	—	—	113	137	A13
PC8	40	PC8 eMIOS8 FR_B_TX AD15	GPIO eMIOS Channel FlexRay Channel B Transmit EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	112	136	B13
PC9	41	PC9 eMIOS9 FR_B_TX_EN AD14	GPIO eMIOS Channel FlexRay Channel B Transmit Enable EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	111	135	C13

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PC10	42	PC10 eMIOS10 PCS_C5 SCK_D	GPIO eMIOS Channel DSPI_C Peripheral Chip Select DSPI_D Clock	I/O I/O O I/O	V_{DDE1}	SH	—	—	110	134	A14
PC11	43	PC11 eMIOS11 PCS_C4 SOUT_D	GPIO eMIOS Channel DSPI_C Peripheral Chip Select DSPI_D Serial Out	I/O I/O O O	V_{DDE1}	SH	—	—	109	133	B14
PC12	44	PC12 eMIOS12 PSC_C3 SIN_D	GPIO eMIOS Channel DSPI_C Peripheral Chip Select DSPI_D Serial In	I/O I/O O I	V_{DDE1}	SH	—	—	108	132	B16
PC13	45	PC13 eMIOS13 PCS_A5 PCS_D0	GPIO eMIOS Channel DSPI_A Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDE1}	SH	—	—	107	131	C15
PC14	46	PC14 eMIOS14 PCS_A4 PCS_D1	GPIO eMIOS Channel DSPI_A Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDE1}	SH	—	—	106	130	C16
PC15	47	PC15 eMIOS15 PCS_A3 PCS_D2	GPIO eMIOS Channel DSPI_A Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDE1}	SH	—	—	105	129	D14
Port D (16)											
PD0	48	PD0 CNTX_A PCS_D3	GPIO CAN_A Transmit DSPI_D Peripheral Chip Select	I/O O O	V_{DDE1}	SH	—	—	104	128	D15
PD1	49	PD1 CNRX_A PCS_D4	GPIO CAN_A Receive DSPI_D Peripheral Chip Select	I/O I O	V_{DDE1}	SH	—	—	103	127	D16
PD2	50	PD2 CNRX_B eMIOS10 BOOTCFG PCS_D5	GPIO CAN_B Receive eMIOS Channel Boot Configuration DSPI_D Peripheral Chip Select	I/O I O I O	V_{DDE1}	SH	BOOTCFG (Pulldown)	GPI (Pulldown)	102	126	E14
PD3	51	PD3 CNTX_B eMIOS11	GPIO CAN_B Transmit eMIOS Channel	I/O O O	V_{DDE1}	SH	—	—	101	125	E15
PD4	52	PD4 CNTX_C eMIOS12	GPIO CAN_C Transmit eMIOS Channel	I/O O O	V_{DDE1}	SH	—	—	100	124	E16
PD5	53	PD5 CNRX_C eMIOS13	GPIO CAN_C Receive eMIOS Channel	I/O I O	V_{DDE1}	SH	—	—	99	123	F13

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PD6	54	PD6 TXD_A eMIOS14	GPIO SCI_A Transmit eMIOS Channel	I/O O O	V_{DDE1}	SH	—	—	98	122	F14
PD7	55	PD7 RXD_A eMIOS15	GPIO SCI_A Receive eMIOS Channel	I/O I O	V_{DDE1}	SH	—	—	97	121	F15
PD8	56	PD8 TXD_B SCL_A	GPIO SCI_B Transmit I^2C Serial Clock Line	I/O O I/O	V_{DDE1}	SH	—	—	94	118	G13
PD9	57	PD9 RXD_B SDA_A	GPIO SCI_B Receive I^2C Serial Data Line	I/O I I/O	V_{DDE1}	SH	—	—	93	117	F16
PD10	58	PD10 PCS_B2 CNTX_F NMI0	GPIO DSPI_B Peripheral Chip Select CAN_F Transmit NMI Input for Z1 Core	I/O O O I	V_{DDE1}	SH	—	—	92	116	G14
PD11	59	PD11 PCS_B1 CNRX_F NMI1	GPIO DSPI_B Peripheral Chip Select CAN_F Receive NMI Input for Z0 Core	I/O O I I	V_{DDE1}	SH	—	—	91	115	G15
PD12	60	PD12 PCS_B0 eMIOS9	GPIO DSPI_B Peripheral Chip Select eMIOS Channel	I/O I/O O	V_{DDE1}	SH	—	—	90	114	H14
PD13	61	PD13 SCK_B eMIOS8	GPIO DSPI_B Clock eMIOS Channel	I/O I/O O	V_{DDE1}	SH	—	—	89	113	H15
PD14	62	PD14 SOUT_B eMIOS7	GPIO DSPI_B Data Output eMIOS Channel	I/O O O	V_{DDE1}	SH	—	—	88	110	J14
PD15	63	PD15 SIN_B eMIOS6	GPIO DSPI_B Data Input eMIOS Channel	I/O I O	V_{DDE1}	SH	—	—	87	107	K14
Port E (16)											
PE0	64	PE0 PCS_A2 eMIOS5 MLBCLK	GPIO DSPI_A Peripheral Chip Select eMIOS Channel MLB Clock	I/O O O I	V_{DDE1}	SH	—	—	86	106	K16
PE1	65	PE1 PCS_A1 eMIOS4 MLBSI / MLBSIG	GPIO DSPI_A Peripheral Chip Select eMIOS Channel MLB Signal In (5-pin) / MLB Bi-directional Signal (3-pin)	I/O O O I I/O	V_{DDE1}	MH	—	—	85	103	L14
PE2	66	PE2 PCS_A0 eMIOS3 MLBDI / MLBDAT	GPIO DSPI_A Peripheral Chip Select eMIOS Channel MLB Data In (5-pin) / MLB Bi-directional Data (3-pin)	I/O I/O O I I/O	V_{DDE1}	MH	—	—	84	101	L15

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PE3	67	PE3 SCK_A eMIOS2 MLBSO / MLBSIG_BUFEN	GPIO DSPI_A Clock eMIOS Channel MLB Signal Out (5-pin) / MLB Signal Level Shifter Enable (3-pin)	I/O I/O O O O	V_{DDE1}	MH	—	—	83	100	M13
PE4	68	PE4 SOUT_A eMIOS1 MLBDO / MLBDAT_BUFEN	GPIO DSPI_A Data Out eMIOS Channel MLB Data Out (5-pin) / MLB Data Level Shifter Enable (3-pin)	I/O O O O O	V_{DDE1}	MH	—	—	82	98	N14
PE5	69	PE5 SIN_A eMIOS0 MLB_SLOT / MLB_SIGOBS / MLB_DATOBS	GPIO DSPI_A Data In eMIOS Channel MLB Slot Debug / MLB Clock Adjust Observe Signal / MLB Clock Adjust Observe Data	I/O I O O O O	V_{DDE1}	MH	—	—	81	97	M15
PE6	70	PE6 CLKOUT	GPIO System Clock Output	I/O O	V_{DDE3}	MH	—	—	67	83	P13
PE7	71	PE7	GPIO	I/O	V_{DDE1}	SH	—	—	—	—	H13
PE8	72	PE8	GPIO	I/O	V_{DDE1}	SH	—	—	—	—	H16
PE9	72	PE9	GPIO	I/O	V_{DDE1}	SH	—	—	—	—	J13
PE10	74	PE10	GPIO	I/O	V_{DDE1}	SH	—	—	—	112	J16
PE11	75	PE11	GPIO	I/O	V_{DDE1}	SH	—	—	—	111	J15
PE12	76	PE12	GPIO	I/O	V_{DDE1}	SH	—	—	—	109	K13
PE13	77	PE13	GPIO	I/O	V_{DDE1}	SH	—	—	—	108	L13
PE14	78	PE14	GPIO	I/O	V_{DDE1}	SH	—	—	—	102	L16
PE15	79	PE15	GPIO	I/O	V_{DDE1}	SH	—	—	—	99	M14
Port F (16)											
PF0	80	PF0 RD_$\overline{WR}$ EVTI[8]	GPIO EBI Read/Write Nexus Event In	I/O I/O I	V_{DDE3}	MH	—	—	66	82	N12
PF1	81	PF1 $\overline{TA}$ MLBCLK EVTO[8]	GPIO EBI Transfer Acknowledge MLB Clock Nexus Event Out	I/O I/O I O	V_{DDE3}	MH	—	—	65	81	P12
PF2	82	PF2 AD8 ADDR8 MLBSI / MLBSIG $\overline{MSEO}$[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Signal In (5-pin) / MLB Bi-Directional Signal (3-pin) Nexus Message Start/End Out	I/O I/O O I I/O O	V_{DDE3}	MH	—	—	64	80	R12

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PF3	83	PF3 AD9 ADDR9 MLBDI / MLBDAT MCKO[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Data In (5-pin) / MLB Bi-directional Data (3-pin) Nexus Message Clock Out	I/O I/O O I I/O O	V_{DDE3}	MH	—	—	63	79	T12
PF4	84	PF4 AD10 ADDR10 MLBSO / MLBSIG_BUFEN MDO0[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Signal Out (5-pin) / MLB Signal Level Shifter Enable (3-pin) Nexus Message Data Out	I/O I/O O O O O	V_{DDE3}	MH	—	—	59	74	T10
PF5	85	PF5 AD11 ADDR11 MLBDO / MLBDAT_BUFEN MDO1[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Data Out (5-pin) / MLB Data Level Shifter Enable (3-pin) Nexus Message Data Out	I/O I/O O O O O	V_{DDE3}	MH	—	—	58	72	R9
PF6	86	PF6 AD12 ADDR12 MLB_SLOT / MLB_SIGOBS / MLB_DATOBS MDO2[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Slot Debug / MLB Clock Adjust Observe Signal / MLB Clock Adjust Observe Data Nexus Message Data Out	I/O I/O O O O O O	V_{DDE3}	MH	—	—	57	68	T8
PF7	87	PF7 AD13 ADDR13 MDO3[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V_{DDE3}	MH	—	—	56	66	P8
PF8	88	PF8 AD14 ADDR14 MDO4[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V_{DDE2}	MH	—	—	55	65	N8
PF9	89	PF9 AD15 ADDR15 MDO5[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V_{DDE2}	MH	—	—	54	64	T7
PF10	90	PF10 $\overline{CS1}$ TXD_C MDO6[8]	GPIO EBI Chip Select SCI_C Transmit Nexus Message Data Out	I/O O O O	V_{DDE2}	MH	—	—	52	62	R7
PF11	91	PF11 $\overline{CS0}$ RXD_C MDO7[8]	GPIO EBI Chip Select SCI_C Receive Nexus Message Data Out	I/O O I O	V_{DDE2}	MH	—	—	51	61	P7
PF12	92	PF12 $\overline{TS}$ TXD_D ALE	GPIO EBI Transfer Start SCI_D Transmit EBI Address Latch Enable	I/O I/O O O	V_{DDE2}	MH	—	—	50	60	N7

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PF13	93	PF13 $\overline{OE}$ RXD_D	GPIO EBI Output Enable SCI_D Receive	I/O O I	V_{DDE2}	MH	—	—	49	59	R6
PF14	94	PF14 $\overline{WE0}$ $\overline{BDIP}$ CNTX_D	GPIO EBI Write Enable EBI Burst Data In Progress CAN_D Transmit	I/O O O O	V_{DDE2}	MH	—	—	45	55	P6
PF15	95	PF15 $\overline{WE1}$ $\overline{TEA}$ CNRX_D	GPIO EBI Write Enable EBI Transfer Error Acknowledge CAN_D Receive	I/O O I/O I	V_{DDE2}	MH	—	—	44	54	N6
Port G (16)											
PG0	96	PG0 AD16 eMIOS16	GPIO EBI Muxed Address/Data eMIOS Channel	I/O I/O I/O	V_{DDE2}	MH	—	—	43	51	P5
PG1	97	PG1 AD17 eMIOS17 SIN_C	GPIO EBI Muxed Address/Data eMIOS Channel DSPI_C Serial In	I/O I/O I/O I	V_{DDE2}	MH	—	—	42	50	T4
PG2	98	PG2 AD18 eMIOS18 SOUT_C	GPIO EBI Muxed Address/Data eMIOS Channel DSPI_C Serial Out	I/O I/O I/O O	V_{DDE2}	MH	—	—	41	49	R4
PG3	99	PG3 AD19 eMIOS19 SCK_C	GPIO EBI Muxed Address/Data eMIOS Channel DSPI_C Serial Clock	I/O I/O I/O I/O	V_{DDE2}	MH	—	—	40	48	P4
PG4	100	PG4 AD20 eMIOS20 PCS_C0	GPIO EBI Muxed Address/Data eMIOS Channel DSPI_C Peripheral Chip Select	I/O I/O I/O I/O	V_{DDE2}	MH	—	—	39	47	T3
PG5	101	PG5 AD21 eMIOS21	GPIO EBI Muxed Address/Data eMIOS Channel	I/O I/O I/O	V_{DDE2}	MH	—	—	38	46	R3
PG6	102	PG6 AD22 eMIOS22	GPIO EBI Muxed Address/Data eMIOS Channel	I/O I/O I/O	V_{DDE2}	MH	—	—	37	45	T2
PG7	103	PG7 AD23 eMIOS23 RXD_C	GPIO EBI Muxed Address/Data eMIOS Channel SCI_C Receive	I/O I/O I/O I	V_{DDE2}	MH	—	—	36	44	R1
PG8	104	PG8 AD24 PCS_A4	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O O	V_{DDE2}	MH	—	—	35	43	P2

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PG9	105	PG9 AD25 PCS_A3 TXD_C	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select SCI_C Transmit	I/O I/O O O	V_{DDE2}	MH	—	—	34	42	N3
PG10	106	PG10 AD26 PCS_A2	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O O	V_{DDE2}	MH	—	—	30	38	N2
PG11	107	PG11 AD27 PCS_A1	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O O	V_{DDE2}	MH	—	—	29	37	N1
PG12	108	PG12 AD28 PCS_A0	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O I/O	V_{DDE2}	MH	—	—	28	36	M4
PG13	109	PG13 AD29 SCK_A	GPIO EBI Muxed Address/Data DSPI_A Clock	I/O I/O I/O	V_{DDE2}	MH	—	—	27	35	M3
PG14	110	PG14 AD30 SOUT_A	GPIO EBI Muxed Address/Data DSPI_A Data Out	I/O I/O O	V_{DDE2}	MH	—	—	26	34	M2
PG15	111	PG15 AD31 SIN_A	GPIO EBI Muxed Address/Data DSPI_A Data In	I/O I/O I	V_{DDE2}	MH	—	—	25	33	M1
Port H (16)											
PH0	112	PH0 AN27 eMIOS20 SCL_A	GPIO eQADC Analog Input[7] eMIOS Channel I^2C_A Serial Clock	I/O I O I/O	V_{DDE2}	A + SH	—	—	24	32	L3
PH1	113	PH1 AN26 eMIOS21 SDA_A	GPIO eQADC Analog Input[7] eMIOS Channel I^2C_A Serial Data	I/O I O I/O	V_{DDE2}	A + SH	—	—	23	31	L2
PH2	114	PH2 AN25 eMIOS22 $\overline{CS3}$	GPIO eQADC Analog Input[7] eMIOS Channel EBI Chip Select	I/O I O O	V_{DDE2}	A + MH	—	—	22	30	L1
PH3	115	PH3 AN24 eMIOS23 $\overline{CS2}$	GPIO eQADC Analog Input[7] eMIOS Channel EBI Chip Select	I/O I O O	V_{DDE2}	A + MH	—	—	21	29	K4
PH4	116	PH4 AN23 TXD_E MA2	GPIO eQADC Analog Input[7] SCI_E Transmit eQADC External Mux Address	I/O I O O	V_{DDE2}	A + SH	—	—	20	28	K3
PH5	117	PH5 AN22 RXD_E MA1	GPIO eQADC Analog Input[7] SCI_E Receive eQADC External Mux Address	I/O I I O	V_{DDE2}	A + SH	—	—	19	24	J3

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PH6	118	PH6 AN21 TXD_F	GPIO eQADC Analog Input[7] SCI_F Transmit	I/O I O	V_{DDE2}	A + SH	—	—	18	23	J2
PH7	119	PH7 AN20 RXD_F	GPIO eQADC Analog Input[7] SCI_F Receive	I/O I I	V_{DDE2}	A + SH	—	—	17	22	J1
PH8	120	PH8 AN19 CNTX_E MA0	GPIO eQADC Analog Input[7] CAN_E Transmit eQADC External Mux Address	I/O I O O	V_{DDE2}	A + SH	—	—	14	17	H1
PH9	121	PH9 AN18/ANT CNRX_E	GPIO eQADC Analog Input[7] CAN_E Receive	I/O I I	V_{DDE2}	A + SH	—	—	13	14	G2
PH10	122	PH10 AN17/ANS CNRX_F	GPIO eQADC Analog Input[7] CAN_F Receive	I/O I I	V_{DDE2}	A + SH	—	—	12	12	F4
PH11	123	PH11 AN16/ANR CNTX_F	GPIO eQADC Analog Input[7] CAN_F Transmit	I/O I O	V_{DDE2}	A + SH	—	—	11	11	F3
PH12	124	PH12 PCS_D5	GPIO DSPI_D Peripheral Chip Select	I/O O	V_{DDE2}	SH	—	—	—	—	F2
PH13	125	PH13	GPIO	I/O	V_{DDE2}	SH	—	—	—	—	F1
PH14	126	PH14 $\overline{WE2}$	GPIO EBI Write Enable	I/O O	V_{DDE2}	MH	—	—	—	53	T5
PH15	127	PH15 $\overline{WE3}$	GPIO EBI Write Enable	I/O O	V_{DDE2}	MH	—	—	—	52	R5
Port J (16)											
PJ0	128	PJ0 AD0	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	—	N11
PJ1	129	PJ1 AD1	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	—	P11
PJ2	130	PJ2 AD2	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	—	N10
PJ3	131	PJ3 AD3	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	—	R10
PJ4	132	PJ4 AD4	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	75	P10
PJ5	133	PJ5 AD5	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	73	T9
PJ6	134	PJ6 AD6	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	69	P9
PJ7	135	PJ7 AD7	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	67	R8

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PJ8	136	PJ8 PCS_D4	GPIO DSPI_D Peripheral Chip Select	I/O I/O	V_{DDE2}	SH	—	—	—	27	K2
PJ9	137	PJ9 PCS_D3	GPIO DSPI_D Peripheral Chip Select	I/O I/O	V_{DDE2}	SH	—	—	—	26	K1
PJ10	138	PJ10 PCS_D2	GPIO DSPI_D Peripheral Chip Select	I/O I/O	V_{DDE2}	SH	—	—	—	25	J4
PJ11	139	PJ11 PCS_D1	GPIO DSPI_D Peripheral Chip Select	I/O I/O	V_{DDE2}	SH	—	—	—	19	H3
PJ12	140	PJ12 PCS_D0	GPIO DSPI_D Peripheral Chip Select	I/O I/O	V_{DDE2}	SH	—	—	—	18	H2
PJ13	141	PJ13 SCK_D	GPIO DSPI_D Clock	I/O I/O	V_{DDE2}	SH	—	—	—	16	G4
PJ14	142	PJ14 SOUT_D	GPIO DSPI_D Serial Out	I/O O	V_{DDE2}	SH	—	—	—	15	G3
PJ15	143	PJ15 SIN_D	GPIO DSPI_D Serial In	I/O I	V_{DDE2}	SH	—	—	—	13	G1
Port K (2)											
PK0	144	PK0 EXTAL32	GPIO 32 kHz Crystal Oscillator Input	I I	V_{DDA}	AE + IH	—	—	—	168	B6
PK1	145	PK1 XTAL32	GPIO 32 kHz Crystal Oscillator Output	I O	V_{DDA}	AE + IH	—	—	—	166	A6
Miscellaneous Pins (9)											
EXTAL	—	EXTAL EXTCLK	Main Crystal Oscillator Input External Clock Input	I I	V_{DDSYN}	AE	EXTAL		75	91	N16
XTAL	—	XTAL	Main Crystal Oscillator Output	O	V_{DDSYN}	AE	XTAL		74	90	P16
TMS	—	TMS	JTAG Test Mode Select Input	I	V_{DDE3}	SH	TMS (Pull Up)		72	88	T15
TCK	—	TCK	JTAG Test Clock Input	I	V_{DDE3}	IH	TCK (Pull Down)		71	87	R14
TDO	—	TDO	JTAG Test Data Output	O	V_{DDE3}	MH	TDO (Pull Up[9])		70	86	T14
TDI	—	TDI	JTAG Test Data Input	I	V_{DDE3}	IH	TDI (Pull Up)		69	85	R13
JCOMP	—	JCOMP	JTAG Compliancy	I	V_{DDE3}	IH	JCOMP (Pull Down)		68	84	T13
TEST[10]	—	TEST	Test Mode Select	I	V_{DDE3}	IH	TEST		62	78	R11
$\overline{\text{RESET}}$	—	$\overline{\text{RESET}}$	External Reset	I/O	V_{DDE2}	SH	$\overline{\text{RESET}}$ (Pull Up)		10	10	E4

1 The GPIO number is the same as the corresponding pad configuration register (SIU_PCR*n*) number.

2 This column lists the functions associated with the programming of the SIU_PCR*n*[PA] bit field in the following order: GPIO, function 1, function 2, and function 3. The unused functions by a given pin begin with function 3, then function 2, then function 1.

3 These are nominal voltages. Each segment provides the power and ground for the given set of I/O pins.

4 Pad types: SH - Bi-directional slow speed pad with input hysteresis; MH - Bi-directional medium speed pad with input hysteresis; IH - Input only pad with input hysteresis; AE/A - Analog pad.

5 A dash for the function in this column denotes the input and output buffer are turned off.

[6] Port A[14:15]—EXTAL32 and XTAL32 functions only apply on the 144LQFP. These functions are on PortK[0:1] for the 176LQFP and 208BGA. In the 176 LQFP and 208 BGA packages, activity on PA14 should be minimized if the 32kHz XTAL is enabled.

[7] This analog input pin has reduced analog-to-digital conversion accuracy compared to PA0–PA15. See eQADC spec #11 (Total Unadjusted Error for single ended conversions with calibration) for further notes on this.

[8] The NEXUS function is selected when the JTAG TAP controller is enabled via the JCOMP pin and the appropriate bits in the NP PCR register. The value of the PA field in the associated PCR register has no effect on the pin function when the NEXUS function is selected.

[9] Pullup is enabled only when JCOMP is negated.

[10] Always connect the TEST pin to Ground (Vss).

1.2 Power and Ground Supply Summary

Table 2. MPC5510 Power/Ground

Pin Name	Function Description	Voltage[1]	Package Pin Locations		
			144	176	208
V_{DDR}	Voltage Regulator Supply	5.0 V	46	56	T6
V_{DDA}	Analog Power	5.0 V	144	176	A2
V_{RH}[2]	eQADC Voltage Reference High	5.0 V			B3
V_{SSA}	Analog Ground	–	141	173	A4
V_{RL}[3]	eQADC Voltage Reference Low	–			B4
REFBYPC	eQADC Reference Bypass Capacitor	V_{SSA}	1	1	B1
V_{PP}[4]	Flash Program/Erase Power	5.0 V	78	94	P15
V_{DDSYN}[5]	Clock Synthesizer Power	3.3 V	73	89	R16
V_{SSSYN}	Clock Synthesizer Ground	–	76	92	M16
V_{DDE1}	External I/O Power	3.3 V – 5.0 V	96,119	105,120, 143,155	A15,D10,E13, G16,K15
V_{DDE2}			16,33,48	21,41,58	H4,L4,N5,P1
V_{DDE3}			61	71,77	N9,T11
V_{SSE1}	External I/O Ground	–	95,118	104,119, 142,154	Shorted to V_{SS} in the package
V_{SSE2}			15,32,47	20,40,57	Shorted to V_{SS} in the package
V_{SSE3}			60	70,76	Shorted to V_{SS} in the package
V_{DD33}[5]	3.3 V I/O Power	3.3 V	77	93	N15
V_{FLASH}[5, 6]	Flash Read Power				
V_{DD}[5]	Internal Logic Power	1.5 V	31,53,79	39,63,95	A1,A16,B2,B15, R2,R15,T1,T16
V_{DDF}[5]	Flash Internal Logic Power		79	95	Shorted to V_{DD} in the package
V_{SS}	Ground	–	80	96	C3,C14,D4,D13, G7-G10,H7-H10, J7-J10,K7-K10, N4,N13,P3,P14
V_{SSF}	Flash Internal Logic Ground				Shorted to V_{SS} in the package

[1] These are nominal voltages.

[2] V_{RH} is shorted to V_{DDA} in the 144LQFP and 176 LQFP packages.

3 V_{RL} is shorted to V_{SSA} in the 144LQFP and 176 LQFP packages.

4 V_{PP} requires 5V for program/erase operations, but may be 0-5V otherwise. V_{PP} should not go high or low when the device is in Sleep mode.

5 Voltage generated from internal voltage regulator and no external connection or load allowed except the required bypass capacitors.

6 V_{FLASH} is shorted to V_{DD33} in the package.

1.3 Pinout – 144 LQFP

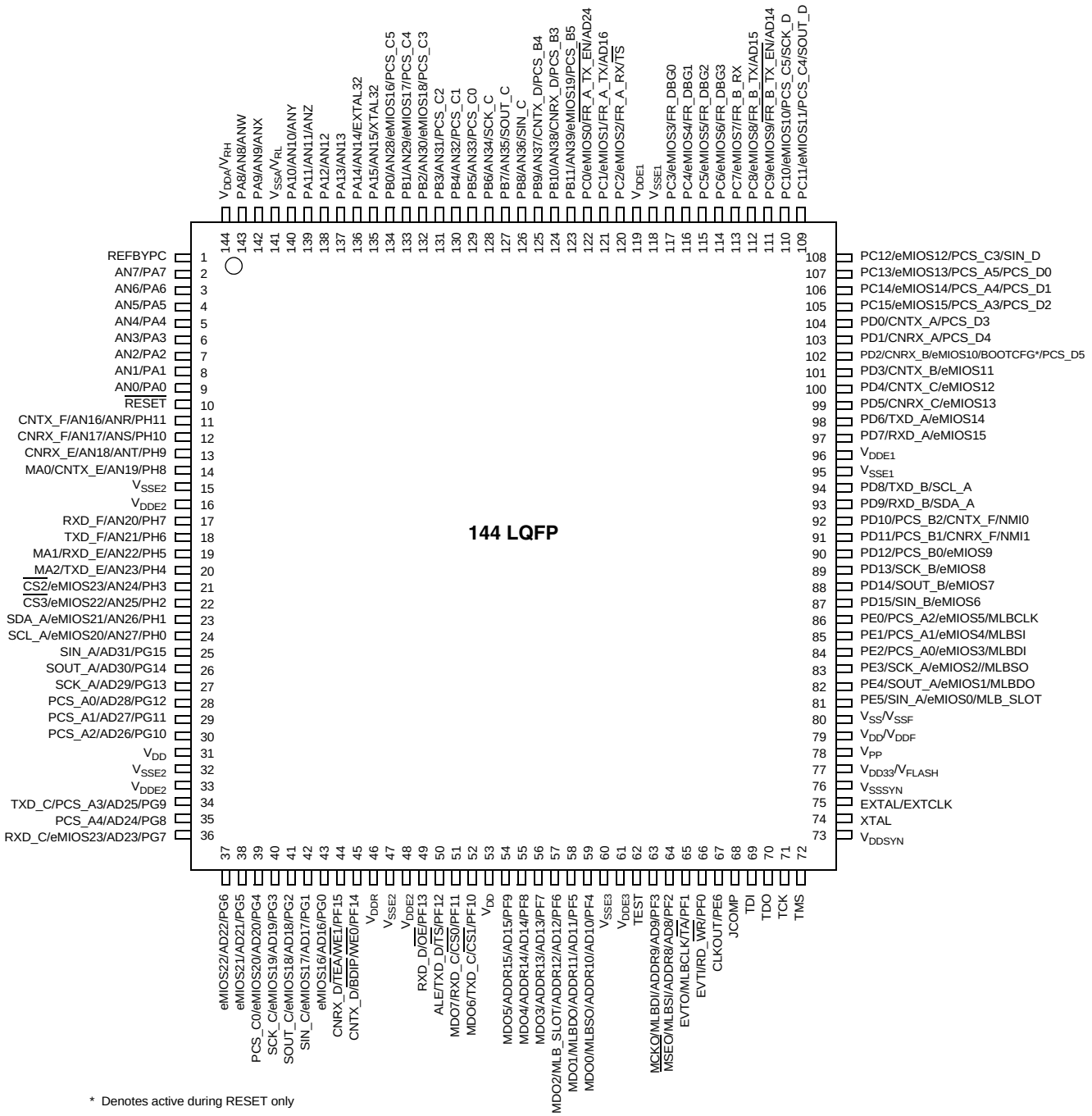

Figure 2. MPC5510 Pinout – 144 LQFP

1.4 Pinout – 176 LQFP

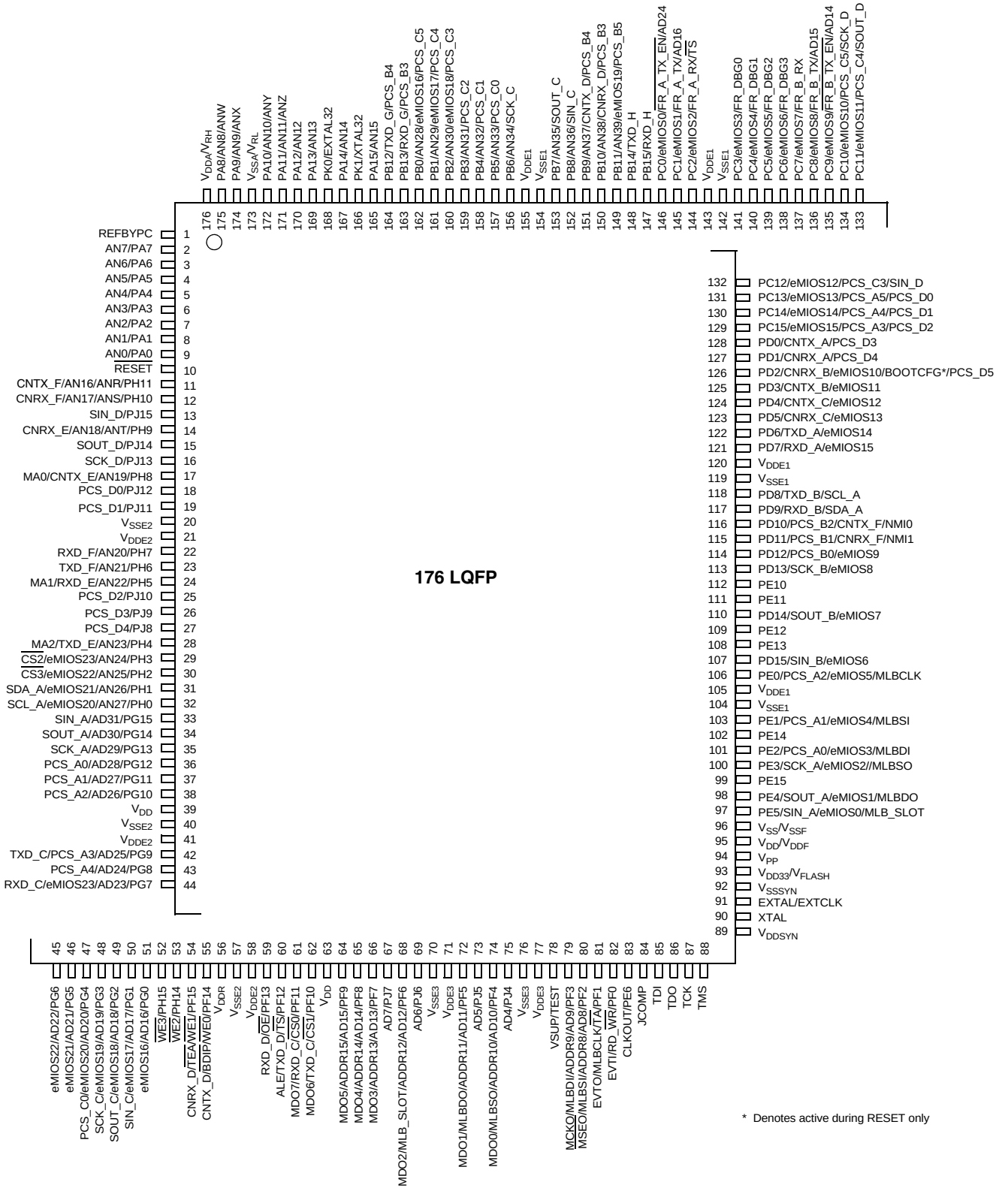

Figure 3. MPC5510 Pinout – 176 LQFP

1.5 Pinout – 208 PBGA

Figure 4. MPC5510 Pinout – 208 PBGA

2 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MCU.

2.1 Maximum Ratings

Table 3. Absolute Maximum Ratings[1]

Num	Characteristic	Symbol	Min	Max[2]	Unit
1	5.0V Voltage Regulator Reference Voltage	V_{DDR}	– 0.3	6.5	V
2	5.0V Analog Supply Voltage (reference to V_{SSA})	V_{DDA}	– 0.3	6.5	V
3	5.0V Flash Program/Erase Voltage	V_{PP}	– 0.3	6.5	V
4	3.3V – 5.0V External I/O Supply Voltage [3]	V_{DDE1}[4] V_{DDE2}[4] V_{DDE3}[4]	– 0.3 – 0.3 – 0.3	6.5 6.5 6.5	V
5	DC Input Voltage [5]	V_{IN}	–1.0[6]	6.5[7]	V
6	V_{REF} Differential Voltage	$V_{RH} - V_{RL}$	– 0.3	5.5	V
7	V_{RH} to V_{DDA} Differential Voltage	$V_{RH} - V_{DDA}$	– 5.5	5.5	V
8	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} - V_{SSA}$	– 0.3	0.3	V
9	V_{DDR} to V_{DDA} Differential Voltage	$V_{DDR} - V_{DDA}$	$- V_{DDA}$	0.3	V
10	Maximum DC Digital Input Current [8] (per pin, applies to all digital MH, SH, and IH pins)	I_{MAXD}	–2	2	mA
11	Maximum DC Analog Input Current [9] (per pin, applies to all analog AE and A pins)	I_{MAXA}	–3	3	mA
12	Storage Temperature Range	T_{STG}	– 55.0	150.0	°C
13	Maximum Solder Temperature [10]	T_{SDR}	—	260.0	°C
14	Moisture Sensitivity Level [11]	MSL	—	3	

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Absolute maximum voltages are currently maximum burn–in voltages. Absolute maximum specifications for device stress have not yet been determined.

3 All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE}.

4 V_{DDE1}, V_{DDE2}, and V_{DDE3} are separate power segments and may be powered independently with no differential voltage constraints between the power segments.

5 AC signal over and undershoot of the input voltages of up to +/– 2.0 volts is permitted for a cumulative duration of 60 hours over the complete lifetime of the device (injection current does not need to be limited for this duration).

6 Internal structures will hold the input voltage above -1.0 volt if the injection current limit of 2mA is met.

7 Internal structures hold the input voltage below this maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within Operating Voltage specifications.

8 Total injection current for all pins (including both digital and analog) must not exceed 25mA.

9 Total injection current for all analog input pins must not exceed 15mA.

10 Solder profile per CDF-AEC-Q100.

11 Moisture sensitivity per JEDEC test method A112.

2.2 Thermal Characteristics

Table 4. Thermal Characteristics

Num	Characteristic	Symbol	Unit	Value		
				208 MAPBGA	176 LQFP	144 LQFP
1	Junction to Ambient [1, 2] Natural Convection (Single layer board)	$R_{\theta JA}$	°C/W	44	38	43
2	Junction to Ambient [1, 3] Natural Convection (Four layer board 2s2p)	$R_{\theta JA}$	°C/W	27	31	34
3	Junction to Ambient [1, 3] (@200 ft./min., Single layer board)	$R_{\theta JMA}$	°C/W	35	30	34
4	Junction to Ambient [1, 3] (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	°C/W	24	25	28
5	Junction to Board [4]	$R_{\theta JB}$	°C/W	16	20	22
6	Junction to Case [5]	$R_{\theta JC}$	°C/W	8	6	7
7	Junction to Package Top [6] Natural Convection	Ψ_{JT}	°C/W	2	2	2

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

2.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textit{Eqn. 1}$$

where:

$$T_A = \text{ambient temperature for the package } (^oC) \quad \textit{Eqn. 2}$$

$$R_{\theta JA} = \text{junction to ambient thermal resistance } (^oC/W) \quad \textit{Eqn. 3}$$

$$P_D = \text{power dissipation in the package (W)} \quad \textit{Eqn. 4}$$

The supplied thermal resistances are provided based on JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined on the single-layer (1s) board and on the four-layer board with two signal layers and a power and a ground plane (2s2p) clearly demonstrate that the effective thermal resistance of

the component is not a constant. It depends on the construction of the application board (number of planes), the effective size of the board which cools the component, how well the component is thermally and electrically connected to the planes, and the power being dissipated by adjacent components.

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between through vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the application board has one oz (35 micron nominal thickness) internal planes, the components are well separated, and the overall power dissipation on the board is less than 0.02 W/cm^2.

The thermal performance of any component depends strongly on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D) \quad \textit{Eqn. 5}$$

where:

T_J = junction temperature (^oC) *Eqn. 6*

T_B = board temperature at the package perimeter ($^oC/W$) *Eqn. 7*

$R_{\theta JB}$ = junction to board thermal resistance ($^oC/W$) per JESD51-8 *Eqn. 8*

P_D = power dissipation in the package (W) *Eqn. 9*

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition, with the component soldered to a board with internal planes.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 10}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$) *Eqn. 11*

$R_{\theta JC}$ = junction to case thermal resistance ($^oC/W$) *Eqn. 12*

$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$) *Eqn. 13*

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the

device. This description is most useful for packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink will be used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for either hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 14}$$

where:

T_T = thermocouple temperature on top of the package (^oC) *Eqn. 15*

Ψ_{JT} = thermal characterization parameter ($^oC/W$) *Eqn. 16*

P_D = power dissipation in the package (W) *Eqn. 17*

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
805 East Middlefield Rd
Mountain View, CA 94043
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

2.3 ESD Characteristics

Table 5. ESD Ratings[1, 2]

Characteristic	Symbol	Value	Unit
ESD for Human Body Model (HBM)		2000	V
HBM Circuit Description	R1	1500	Ohm
	C	100	pF
ESD for Field Induced Charge Model (FDCM)		500 (all pins)	V
		750 (corner pins)	
Number of Pulses per pin: Positive Pulses (HBM) Negative Pulses (HBM)	 — —	 1 1	 — —
Interval of Pulses	—	1	second

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification

2.4 DC Electrical Specifications

Table 6. DC Electrical Specifications

Num	Characteristic	Symbol	Min	Max	Unit
1a	**C parts** Operating junction temperature range Operating ambient temperature range[1]	 T_J T_A	 – 40 – 40	 105 85	 °C °C
1b	**V parts** Operating junction temperature range Operating ambient temperature range[1]	 T_J T_A	 – 40 – 40	 120 105	 °C °C
1c	**M parts**[2] Operating junction temperature range Operating ambient temperature range[1]	 T_J T_A	 – 40 – 40	 145 125	 °C °C
2	5.0V Voltage Regulator Reference Voltage	V_{DDR}	4.5	5.25	V
3	5.0V Analog Supply Voltage	V_{DDA}	4.5	5.25	V
4	5.0V Flash Program/Erase Voltage [3]	V_{PP}	4.5	5.25	V
5	3.3V – 5.0V External I/O Supply Voltage	V_{DDE1}[4,5] V_{DDE2}[4] V_{DDE3}[4]	3.0 3.0 3.0	5.5 5.5 5.5	V
6	Pad (SH/MH/IH) Input High Voltage	V_{IH}	$0.65 \times V_{DDE}$	$V_{DDE} + 0.3$	V
7	Pad (SH/MH/IH) Input Low Voltage	V_{IL}	$V_{SS} - 0.3$	$0.35 \times V_{DDE}$	V
8	Pad (SH/MH/IH) Input Hysteresis	V_{HYS}	$0.1 \times V_{DDE}$	$0.2 \times V_{DDE}$	V
9	Analog (AE/A) Input Voltage	V_{INDC}	$V_{SSA} - 0.3$	$V_{DDA} + 0.3$ see note[5]	V
10	Slow/Medium I/O Output High Voltage I_{OH} = –1.0 mA I_{OH} = –0.2 mA	V_{OH}	 $0.80 \times V_{DDE}$ $0.95 \times V_{DDE}$	—	V
11	Slow/Medium I/O Output Low Voltage I_{OL} = 1.0 mA I_{OH} = 0.2 mA	V_{OL}	—	 $0.20 \times V_{DDE}$ $0.05 \times V_{DDE}$	V
12	Input Capacitance (Digital Pins: Pad type MH,SH, IH with no A or AE)	C_{IN}	—	7	pF
13	Input Capacitance (Analog Pins: Pad type A, AE, and AE+IH)	C_{IN_A}	—	10	pF
14	Input Capacitance (Shared digital and analog pins: A with SH or MH)	C_{IN_M}	—	12	pF
15	Slow/Medium I/O Weak Pull Up/Down Absolute Current [6]	I_{ACT}	10	170	µA
16	I/O Input Leakage Current [7]	I_{INACT_D}	– 1.5	1.5	µA
17	DC Injection Current (per pin)	I_{IC}	– 2.0	2.0	mA
18	Analog Input Current, Channel Off [8] (Analog pins AE and AE+IH)	I_{INACT_A}	– 200	200	nA
19	Analog Input Current (Shared digital and analog pins: A with SH or MH)	I_{INACT_AD}	–1.5	1.5	µA
20	V_{RH} to V_{DDA} Differential Voltage	$V_{RH} - V_{DDA}$	– 100	100	mV

Table 6. DC Electrical Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit
21	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} - V_{SSA}$	– 100	100	mV
22	V_{SS} to V_{SSA} Differential Voltage	$V_{SS} - V_{SSA}$	– 100	100	mV
23	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} - V_{SS}$	–50	50	mV
24	V_{DDR} to V_{DDA} Differential Voltage	$V_{DDR} - V_{DDA}$	– 100	100	mV
25	Slew rate on VDDA, VDDR, and VDDE power supply pins[9]	Vramp	1	100	V/ms
26	Capactive Supply Load VDD VDD33 VDDSYN	Vload	 800 200 200	 — —	nF

1 Please refer to Section 2.2.1, “General Notes for Specifications at Maximum Junction Temperature” for more details about the relation between ambient temperature T_A and device junction temperature T_J.

2 M parts can’t go above 66 MHz.

3 V_{PP} can drop to 0 volts during read-only operations and before entry to Sleep mode, to reduce power consumption.

4 V_{DDE1}, V_{DDE2}, and V_{DDE3} are separate power segments and may be powered independently with no differential voltage constraints between the power segments.

5 If V_{DDE1} is below V_{DDA} than the analog input limits (spec #9 (Analog (AE/A) Input Voltage) in Table 6) will be based on the V_{DDE1} voltage level.

6 Absolute value of current, measured at V_{IL} and V_{IH}.

7 Weak pull up/down inactive. Measured at V_{DDE} = 5.25 V. Applies to pad types: SH and MH.

8 Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 ^{o}C, in the ambient temperature range of 50 to 125 ^{o}C. Applies to pad types: A and AE.

9 This applies to the ramp up rate from 0.3 volts to 3.0 volts.

2.5 Operating Current Specifications

Table 7. Operating Currents

Num	Characteristic	Symbol	Typ[1] 25C Ambient	Typ[1] 70C Ambient	Max[1] -40–145C Junction	Unit
Equations	$I_{TOTAL} = I_{DDE} + I_{PP} + I_{DDA} + I_{DDR}$ $I_{DDE} = I_{DDE1} + I_{DDE2} + I_{DDE3}$					
1	$V_{DDE(1,2,3)}$ Current $V_{DDE(1,2,3)}$ @ 3.0V - 5.5V Static[2], or when in SLEEP or STOP Dynamic[3]	I_{DDE}	 1 Note [3]	 3 Note [3]	 30 Note [3]	 µA mA
2	V_{PP} Current V_{PP} @ 0V (All modes) V_{PP} @ 5.25V SLEEP mode STOP mode RUN mode	I_{PP}	 1 15 15 1	 1 20 20 1	 1 30 30 25	 µA µA µA mA
3	V_{DDA} Current V_{DDA} @ 4.5V - 5.25V RUN mode[4] SLEEP/STOP[5] mode with 32KIRC SLEEP/STOP[5] mode with 32KOSC SLEEP/STOP[5] mode with 16MIRC	I_{DDA}	 5 12 12 111	 5 16 16 165	 10 26 28 225	 mA µA µA µA
4	V_{DDR} Current V_{DDR} @ 4.5V - 5.25V SLEEP mode with XOSC[6] (additonal) with RTC/API (additonal) each 8K RAM block (additional) STOP mode with XOSC[6] (additonal) RUN mode (Using 16 MHz IRC) RUN mode (Maximum @ 48 MHz)[7] RUN mode (Maximum @ 66 MHz)[8] RUN mode (Maximum @ 80MHz)[9]	I_{DDR}	 20 500 1 0.8 170 500 30 50 105 120	 25 600 1 7 600 600 35 75 110 130	 360 900 3 45 1500 900 40 90 120 135	 µA µA µA µA µA µA mA mA mA mA

1 Typ - Nominal voltage levels and functional activity. Max - Maximum voltage levels and functional activity.

2 Static state of pins is when input pins are disabled or not being toggled and driven to a valid input level, output pins are not toggling or driving against any current loads, and internal pull devices are disabled or not pulling against any current loads.

3 Dynamic current from pins is application specific and depends on active pull devices, switching outputs, output capacitive and current loads, and switching inputs. Refer to Table 8 for more information.

4 RUN mode is a typical application with the ADC, 16MIRC, 32KIRC running.

5 SLEEP/STOP mode means that only the listed peripherals are on. All others are diabled.

6 XOSC: optionally enabled in SLEEP and STOP modes (oscillator remains running from crystal but XOSC clock output disabled).

7 RUN mode condition includes PLL selected as source of system clock, XOSC enabled with 40MHz crystal, all peripherals enabled, both cores running, and running a typical application using both SRAM and flash.

[8] RUN mode condition includes PLL selected as source of system clock, XOSC enabled with 40MHz crystal; all peripheral and cores enabled and running a typical application using both SRAM and flash. Be sure to calculate the junction temperature, as the maximum current at maximum ambient temperature can exceed the maximum junction temperature.

[9] RUN mode condition includes PLL selected as source of system clock, XOSC enabled with 40MHz crystal, all peripheral and cores enabled and running a typical application using both SRAM and flash. Only for 208 MAPBGA and only 120C junction or lower. Be sure to calculate the junction temperature, as the maximum current at maximum ambient temperature can exceed the maximum junction temperature

2.6 I/O Pad Current Specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from Table 8 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 8.

Table 8. I/O Pad Average DC Current[1]

Num	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	Voltage (V)	Slew Rate Control	Current (mA)
1	Slow (Pad Type SH)	I_{DRV_SH}	25	50	5.25	11	8.0
2			10	50	5.25	01	3.2
3			2	50	5.25	00	0.7
4			2	200	5.25	00	2.4
5	Medium (Pad Type MH)	I_{DRV_MH}	50	50	5.25	11	17.3
6			20	50	5.25	01	6.5
7			3.33	50	5.25	00	1.1
8			3.33	200	5.25	00	3.9

1 These values are estimated from simulation and are not tested. Currents apply to output pins only.

2 All loads are lumped.

2.7 Low Voltage Characteristics

Table 9. Low Voltage Monitors

Num	Characteristic	Symbol	Min	Typical	Max	Unit
1	Power-on-Reset Assert Level [1]	V_{POR}	—	0.70	—	V
2	Low Voltage Monitor 1.5V [1] Assert Level De-assert Level	 V_{LV15A} V_{LV15D}	 — —	 1.40 1.45	 — —	V
3	Low Voltage Monitor 3.3V [2] Assert Level De-assert Level	 V_{LV33A} V_{LV33D}	 — —	 3.05 3.10	 — —	V
4	Low Voltage Monitor Synthesizer [3] Assert Level De-assert Level	 V_{LVSYNA} V_{LVSYND}	 — —	 3.05 3.10	 — —	V
5	Low Voltage Monitor 5.0V Low Threshold [4] Assert Level De-assert Level	 V_{LV5LA} V_{LV5LD}	 3.30 3.35	 3.35 3.40	 3.40 3.45	V
6	Low Voltage Monitor 5.0V [4] Assert Level De-assert Level	 V_{LV5A} V_{LV5D}	 4.50 4.55	 4.55 4.60	 4.70 4.75	V
7	Low Voltage Monitor 5.0V High Threshold [4] Assert Level De-assert Level	 V_{LV5HA} V_{LV5HD}	 4.70 4.75	 4.75 4.80	 4.80 4.85	V

1 Monitors V_{DD}
2 Monitors V_{DD33}
3 Monitors V_{DDSYN}
4 Monitors V_{DDA}

2.8 Oscillators Electrical Characteristics

Table 10. 3.3V High Frequency External Oscillator

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	Frequency Range[1]	f_{ref}	4[2]	40	MHz
2	Duty Cycle of reference	t_{dc}	40	60	%
3	EXTAL Input High Voltage External crystal mode [3] External clock mode	V_{IHEXT}	 V_{XTAL} + 0.4 0.65 x V_{DDSYN}	 V_{DDSYN} + 0.3 V_{DDSYN} + 0.3	V
4	EXTAL Input Low Voltage External crystal mode [3] External clock mode	V_{ILEXT}	 V_{DDSYN} – 0.3 V_{DDSYN} – 0.3	 V_{XTAL} – 0.4 0.35 x V_{DDSYN}	V
5	XTAL Current [4]	I_{XTAL}	2	6	mA
6	Total On-chip stray capacitance on XTAL	C_{S_XTAL}	—	3	pF
7	Total On-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	3	pF
8	Crystal manufacturer's recommended capacitive load	C_L	See crystal specification	See crystal specification	pF
9	Discrete load capacitance to be connected to EXTAL	C_{L_EXTAL}	—	$2\times C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$[5]	pF
10	Discrete load capacitance to be connected to XTAL	C_{L_XTAL}	—	$2\times C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$[5]	pF
11	Startup Time	$t_{startup}$	—	10	ms

1 Since this is an amplitude controlled oscillator the use of overtone oscillators is not recommended. Only use fundamental frequency oscillators.

2 When PLL frequency modulation is active, reference frequencies less than 8MHz will distort the modulated waveform and the effects of this on emissions is not characterized.

3 This parameter is meant for those who do not use quartz crystals or resonators, but CAN osc, in crystal mode. In that case, $V_{extal} - V_{xtal} \geq 400mV$ criteria has to be met for oscillator's comparator to produce output clock.

4 I_{xtal} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

5 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively

Table 11. 5V Low Frequency (32 kHz) External Oscillator

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	Frequency Range	f_{ref32}	32	38	kHz
2	Duty Cycle of reference	t_{dc32}	40	60	%
3	XTAL32 Current [1]	I_{XTAL32}	0.5	3	µA
4	Crystal manufacturer's recommended capacitive load	C_{L32}	See crystal specification	See crystal specification	pF
5	Startup Time	$t_{startup}$	—	2	s

1 I_{xtal32} is the oscillator bias current out of the XTAL32 pin with both EXTAL32 and XTAL32 pins grounded.

Table 12. 5V High Frequency (16 MHz) Internal RC Oscillator

Num	Characteristic	Symbol	Min	Typ	Max	Unit
1	Frequency before trim[1]	F_{ut}	12.8	16	22.3	MHz
2	Frequency after loading factory trim[2]	F_t	15.1	16	16.9	MHz
3	Application trim resolution[3]	T_s	—	—	± 0.5	%
4	Application frequency trim step[3]	F_s	—	300	—	kHz
5	Start up time	S_t	—	—	500	ns

1 Across process, voltage, and temperature
2 Across voltage and temperature
3 Fixed voltage and temperature

Table 13. 5V Low Frequency (32 kHz) Internal RC Oscillator

Num	Characteristic	Symbol	Min	Typ	Max	Unit
1	Frequency before trim[1]	F_{ut32}	20.8	32.0	43.2	kHz
2	Frequency after loading factory trim[2]	F_{t32}	26	32.0	38	kHz
3	Application trim resolution[3]	T_{s32}	—	—	± 2	%
4	Application frequency trim step[3]	F_{s32}	—	1	—	kHz
5	Start up time	S_{t32}	—	—	100	µs

1 Across process, voltage, and temperature
2 Across voltage and temperature
3 Fixed voltage and temperature

2.9 FMPLL Electrical Characteristics

Table 14. FMPLL Electrical Specifications [1]

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	System frequency[2] -40 °C ≤ T_J ≤ 120 °C -40 °C ≤ T_J ≤ 145 °C	f_{sys}	 375 375	 80000 [3] 66000	kHz
2	PLL Reference Frequency (output of predivider)	f_{pllref}	4	10	MHz
3	VCO Frequency[4]	f_{vco}	250	500	MHz
4	PLL Frequency [5] -40 °C ≤ T_J ≤ 120 °C -40 °C ≤ T_J ≤ 145 °C	f_{pll}	 3 3	 80 [3] 66	MHz
5	Loss of Reference Frequency [6]	f_{LOR}	100	1000	kHz
6	Self Clocked Mode Frequency [7]	f_{SCM}	13	35	MHz
7	PLL Lock Time [8]	t_{lpll}	—	750	µs
8	Frequency un-LOCK Range	f_{UL}	– 4.0	4.0	% f_{sys}
9	Frequency LOCK Range	f_{LCK}	– 2.0	2.0	% f_{sys}
10	CLKOUT Cycle-to-cycle Jitter,[9, 10]	C_{jitter}	– 5	5	% f_{clkout}
10a	CLKOUT Jitter at 10 µs period [9,10, 11]	C_{jitter}	– 0.05	0.05	% f_{clkout}
11	Frequency Modulation Depth 1% Setting [12,13] (f_{sys}Max must not be exceeded)	C_{mod}	0.5	2	%f_{sys}
12	Frequency Modulation Depth 2% Setting [12,13] (f_{sys}Max must not be exceeded)	C_{mod}	1	3	%f_{sys}

1 V_{DDSYN} = 3.0V to 3.6 V, V_{SSSYN} = 0 V, TA = TL to TH

2 The maximum value is without frequency modulation turned on. If frequency modulation is turned on, the maximum value (average frequency) must be de-rated by the percentage of modulation enabled.

3 80 MHz is only available in the 208 pin package.

4 Optimum performance is achieved with the highest VCO frequency feasible based on the highest ERFD that results in the desired PLL frequency.

5 The VCO frequency range is higher than the maximum allowable PLL frequency. The synthesizer control register 2's enchanced reduced frequency divider (FMPLL_SYNCR2[ERFD]) in enhanced operation mode must be programmed to divide the VCO frequency within the PLL frequency range.

6 Loss of reference frequency is the reference frequency detected by the PLL which then transitions into self clocked mode.

7 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR}.

8 This specification applies to the period required for the PLL to relock after changing the enhanced multiplication factor divider (EMFD) bits in the synthesizer control register 1 (SYNCR1) in enhanced operation mode.

9 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the jitter percentage for a given interval. CLKOUT divider set to divide-by-2.

10 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{jitter} + C_{mod}.

11 The PLL % jitter reduces with more cycles. 10 µs was picked for a reference point for LIN (100 Kbits), slower speeds will have even less % jitter.

12 Modulation depth selected must not result in f_{sys} value greater than the f_{sys} maximum specified value.

13 These depth ranges are obtained by filtering the raw cycle-to-cycle clock frequency data to eliminate the presence of the the normal clock jitter riding on top of the FM waveform. The allowable modulation rates are 400 kHz to 1 MHz.

2.10 eQADC Electrical Characteristics

Table 15. eQADC Conversion Specifications (Operating)

Num	Characteristic	Symbol	Min	Max	Unit
1	ADC Clock (ADCLK) Frequency[1]	F_{ADCLK}	1	12	MHz
2	Conversion Cycles	CC	14+2 (or 16)	14+128 (or 142)	ADCLK cycles
3	Stop Mode Recovery Time[2]	T_{SR}	20	—	µs
4	Resolution	—	1.25	—	mV
5	INL: 12 MHz ADC Clock[3]	INL12	—	10	Counts
6	DNL: 12 MHz ADC Clock[3]	DNL12	—	10	Counts
7	Offset Error with Calibration[3]	OFFWC	—	10	Counts
8	Full Scale Gain Error with Calibration	GAINWC	—	10	Counts
9	Disruptive Input Injection Current [4, 5, 6, 7]	I_{INJ}	—	±1	mA
10	Incremental Error due to injection current. All channels have same 10kΩ < Rs <100kΩ [8] Channel under test has Rs=10kΩ, I_{INJ}=I_{INJMAX},I_{INJMIN}	E_{INJ}	—	±6	Counts
11	Total Unadjusted Error for single ended conversions with calibration[3, 9, 10, 11, 12]	TUE	—	±10	Counts
12	Source Impedance[13]	R_S	—	100k	Ohm

1 Conversion characteristics vary with F_{ADCLK} rate. Reduced conversion accuracy occurs at maximum F_{ADCLK} rate. The maximum value is based on 800KS/s and the minimum value is based on 20MHz oscillator clock frequency divided by a maximum 16 factor.

2 The specified value is for the case when the 100nF capacitor is not connected to the REFBYPC pin. When the capacitor is connected to the REFBPYC pin, the recovery time is 10ms.

3 At $V_{RH} - V_{RL}$ = 5.12 V, one lsb = 1.25 mV = one count.

4 Below disruptive current conditions, the channel being stressed has conversion values of 0x3FF for analog inputs greater than V_{RH} and 0x000 for values less than V_{RL}. This assumes that $V_{RH} \leq V_{DDA}$ and $V_{RL} \geq V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.

5 Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA}$ + 0.5V and $V_{NEGCLAMP}$ = – 0.3 V, then use the larger of the calculated values.

7 Condition applies to two adjacent pads on the internal pad.

8 At $V_{RH} - V_{RL}$ = 5.12 V, one lsb = 1.25 mV = one count. This count error is in addition to the TUE count error.

9 The TUE specification will always be better than the sum of the INL, DNL, offset, and gain errors due to canceling errors.

10 TUE includes all internal device error such as internal reference variation (75% Ref, 25% Ref)

11 Depending on the customer input impedance, the Analog Input Leakage current (DC Electrical specification) may affect the actual TUE measured on analog channels shared digital pins.

12 It is possible to see up to one additional count added for the 144 pin packages since the VRL and VRH functions are shared with the VSSA and VDDA, respectively. On Analog pins above PA15, the accuracy effects from adjacent digital port pin activity is application dependent because of frequency, level, noise, etc.

13 If R_S is greater than 1 k Ohm, be sure to calculate the affect of pin leakage and use the proper sampling time, to ensure that you get the accuracy required.

2.11 Flash Memory Electrical Characteristics

Table 16. Flash Program and Erase Specifications[1]

Num	Characteristic	Symbol	Min	Typ	Initial Max[2]	Max[3]	Unit
1	Double Word (64 bits) Program Time [4]	$T_{dwprogram}$	—	10	—	500	µs
2	Page (128 bits) Program Time [4]	$T_{pprogram}$	—	15	44	500	µs
3	16 Kbyte Block Pre-program and Erase Time	$T_{16kpperase}$	—	325	525	5000	ms
4	64 Kbyte Block Pre-program and Erase Time	$T_{64kpperase}$	—	525	675	5000	ms
5	128 Kbyte Block Pre-program and Erase Time	$T_{128kpperase}$	—	675	1800	7500	ms
6	Minimum operating frequency for program and erase operations	—	25	—	—	—	MHz
7	Wait States Relative to System Frequency PFCRPn[RWSC] = 0b000; PFCRPn[WWSC] = 0b01 PFCRPn[RWSC] = 0b001; PFCRPn[WWSC] = 0b01 PFCRPn[RWSC] = 0b010; PFCRPn[WWSC] = 0b01	T_{rwsc}	 — — —	 — — —	 — — —	 25 50 80	MHz
8	Recovery Time Stop mode exit or STOP bit negated Sleep mode exit (with CRP_RECPTR[FASTREC]=1) [5]	$T_{recover}$	 — —	 — —	 — —	 20 120	 µs µs

1 Typical program and erase times assume nominal supply values and operation at 25 °C.

2 Initial factory condition: < 100 program/erase cycles, nomial supply values and operation at 25 °C.

3 The maximum time is at worst case conditions after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4 This does not include software overhead.

5 If CRP_RECPTR[FASTREC]=0, then hardware will wait 2340 system clocks before exiting from Sleep mode to account for the flash recovery time. The default system clock source after Sleep is the 16MIRC. A nominal frequency of 16MHz equates to a hardware wait of 146µs.

Table 17. Flash EEPROM Module Life (Full Temperature Range)

Num	Characteristic	Symbol	Min	Typical[1]	Unit
1	Number of Program/Erase cycles per block over the operating temperature range (T_J) 16 Kbyte and 64 Kbyte blocks 128 Kbyte blocks	P/E	 100,000 1000	 — 100,000	cycles
2	Data retention Blocks with 0 – 1,000 P/E cycles Blocks with 1,001 – 100,000 P/E cycles	Retention	 20 5	—	years

1 Typical endurance is evaluated at 25C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of Typical Endurance, please refer to Engineering Bulletin EB619 “Typical Endurance for Nonvolatile Memory.”

2.12 Pad AC Specifications

Table 18. Pad AC Specifications (VDDE = 3.0V - 5.5V)[1]

Num	Pad Type	SRC	Out Delay[2, 3] (ns)	Rise/Fall[3, 4] (ns)	Load Drive (pF)
1	Slow (SH)	11	39	23	50
			120	87	200
		01	101	52	50
			188	111	200
		00	507	248	50
			597	312	200
2	Medium (MH)	11	23	12	50
			64	44	200
		01	50	22	50
			90	50	200
		00	261	123	50
			305	156	200
4	Pull Up/Down (3.6V max)	—	—	7500	50
5	Pull Up/Down (5.5V max)	—	—	9500	50

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at VDDE = 3.0V to 5.5V, T_A = TL to TH.

2 This parameter is supplied for reference and is not tested. Add a maximum of one system clock to the output delay for delay with respect to system clock.

3 Delay and rise/fall are measured to 20% or 80% of the respective signal.

4 This parameter is guaranteed by characterization before qualification rather than 100% tested.

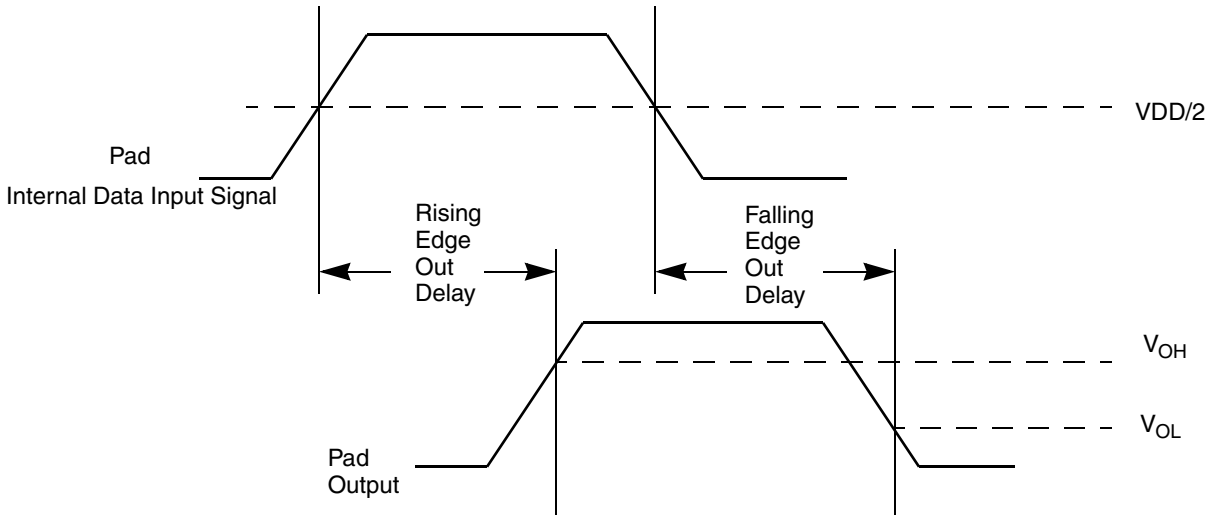

Figure 5. Pad Output Delay

2.13 AC Timing

2.13.1 Reset and Boot Configuration Pins

Table 19. Reset and Boot Configuration Timing

Num	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	150	—	ns
2	BOOTCFG Setup Time after $\overline{\text{RESET}}$ Valid	t_{RCSU}	—	100	µs
3	BOOTCFG Hold Time from $\overline{\text{RESET}}$ Valid	t_{RCH}	0	—	µs

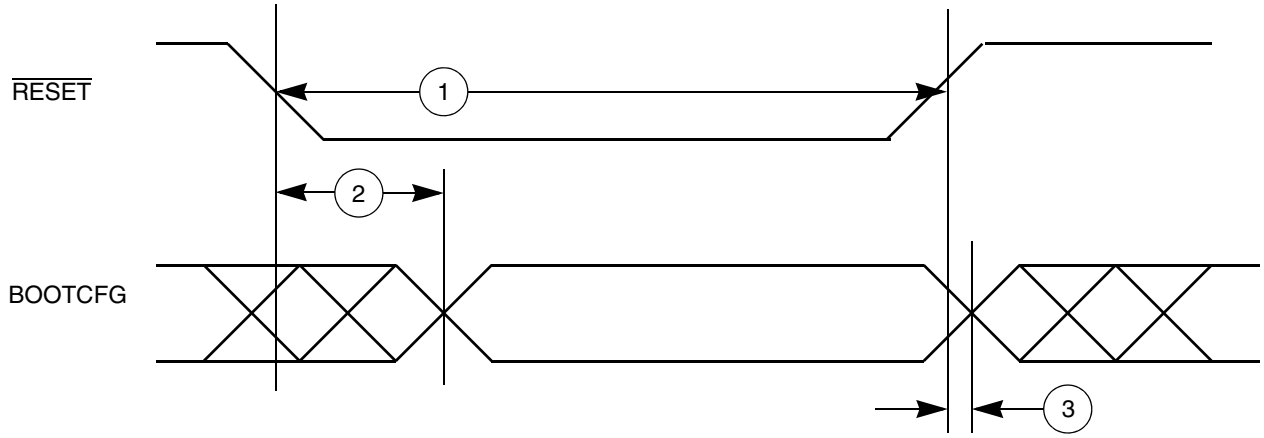

Figure 6. Reset and Boot Configuration Timing

2.13.2 External Interrupt (IRQ) and Non-Maskable Interrupt (NMI) Pins

Table 20. IRQ/NMI Timing

Num	Characteristic	Symbol	Min	Max	Unit
1	IRQ/NMI Pulse Width Low	t_{IPWL}	3	—	t_{SYS}
2	IRQ/NMI Pulse Width High	T_{IPWH}	3	—	t_{SYS}
3	IRQ/NMI Edge to Edge Time[1]	t_{ICYC}	6	—	t_{SYS}

[1] Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.

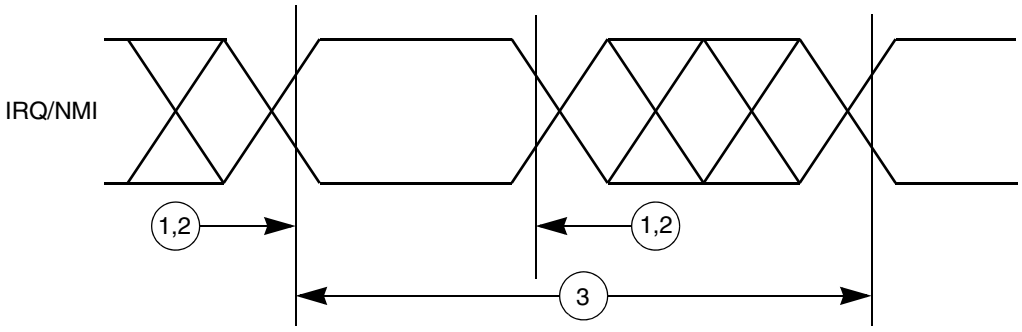

Figure 7. IRQ and NMI Timing

2.13.3 JTAG (IEEE 1149.1) Interface

Table 21. JTAG Interface Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	TCK Cycle Time	t_{JCYC}	100	—	ns
2	TCK Clock Pulse Width (Measured at VDDE/2)	t_{JDC}	40	60	ns
3	TCK Rise and Fall Times (40% – 70%)	$t_{TCKRISE}$	—	3	ns
4	TMS, TDI Data Setup Time	t_{TMSS}, t_{TDIS}	5	—	ns
5	TMS, TDI Data Hold Time	t_{TMSH}, t_{TDIH}	25	—	ns
6	TCK Low to TDO Data Valid	t_{TDOV}	—	20	ns
7	TCK Low to TDO Data Invalid	t_{TDOI}	0	—	ns
8	TCK Low to TDO High Impedance	t_{TDOHZ}	—	20	ns
9	JCOMP Assertion Time	t_{JCMPPW}	100	—	ns
10	JCOMP Setup Time to TCK Low	t_{JCMPS}	40	—	ns
11	TCK Falling Edge to Output Valid	t_{BSDV}	—	50	ns
12	TCK Falling Edge to Output Valid out of High Impedance	t_{BSDVZ}	—	50	ns
13	TCK Falling Edge to Output High Impedance	t_{BSDHZ}	—	50	ns
14	Boundary Scan Input Valid to TCK Rising Edge	t_{BSDST}	50	—	ns
15	TCK Rising Edge to Boundary Scan Input Invalid	t_{BSDHT}	50	—	ns

[1] These specifications apply to JTAG boundary scan only. JTAG timing specified at VDDE = 3.0V to 5.5V, T_A = TL to TH, and CL = 30pF with SRC = 0b11.

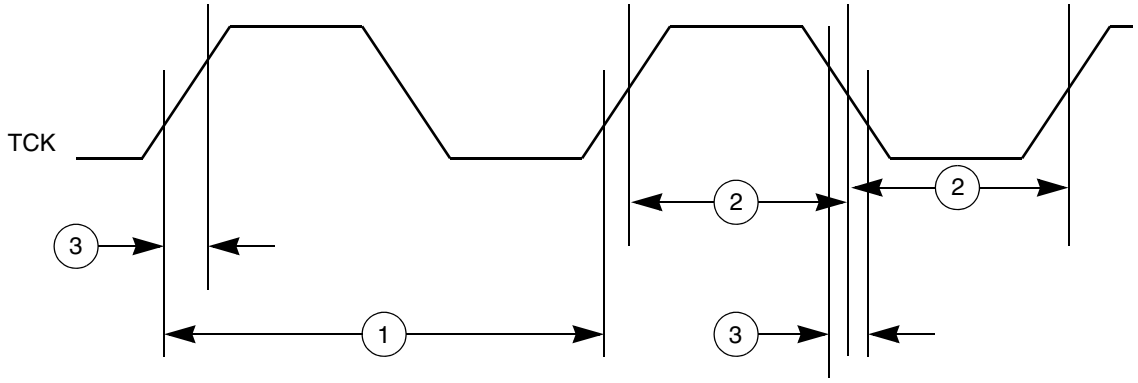

Figure 8. JTAG Test Clock Input Timing

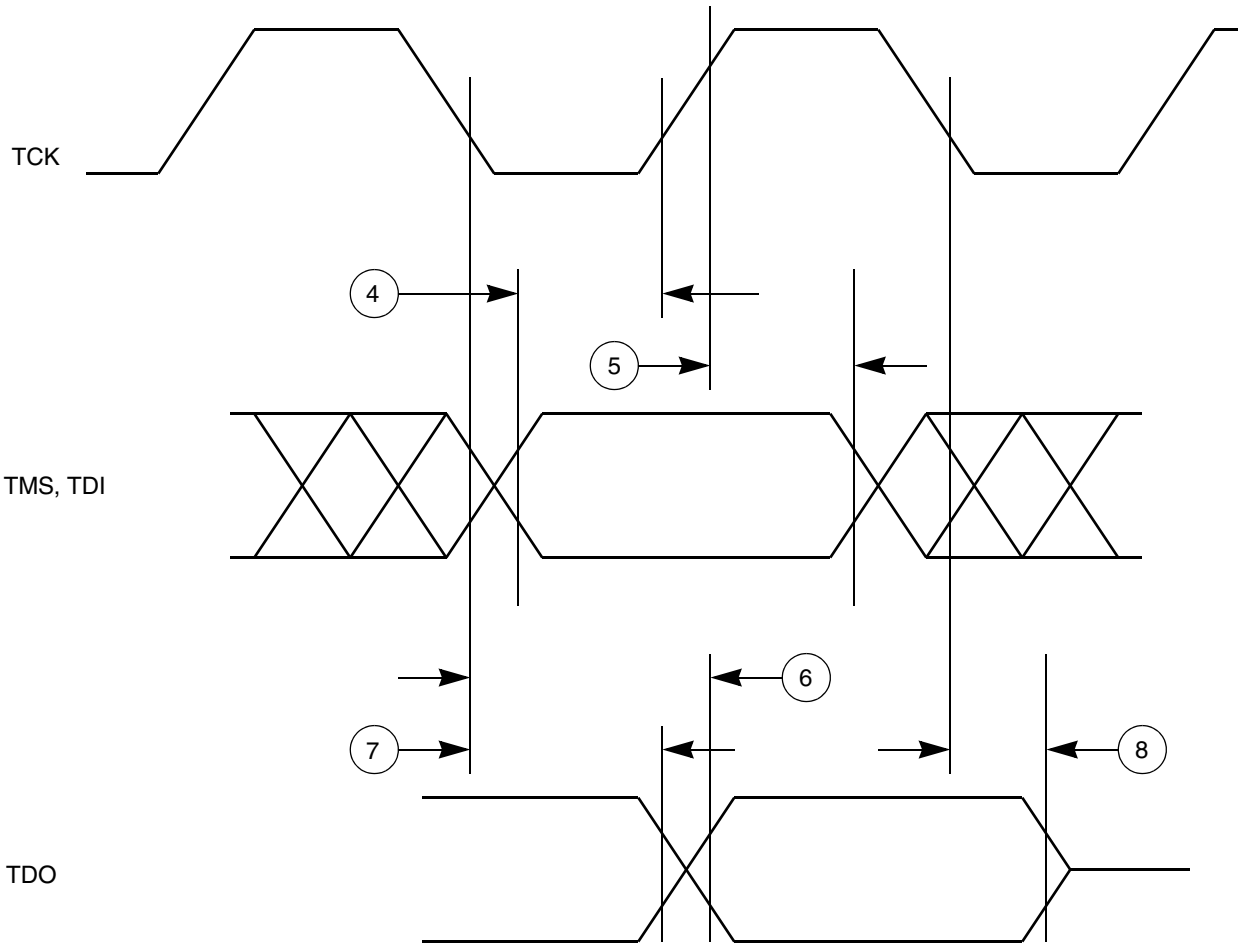

Figure 9. JTAG Test Access Port Timing

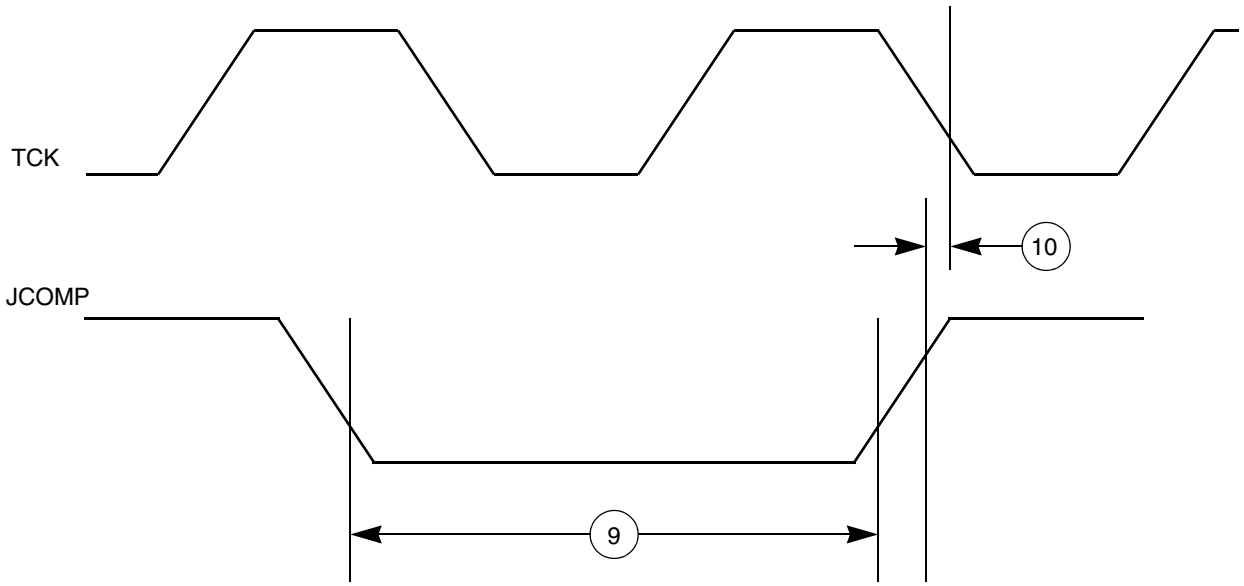

Figure 10. JTAG JCOMP Timing

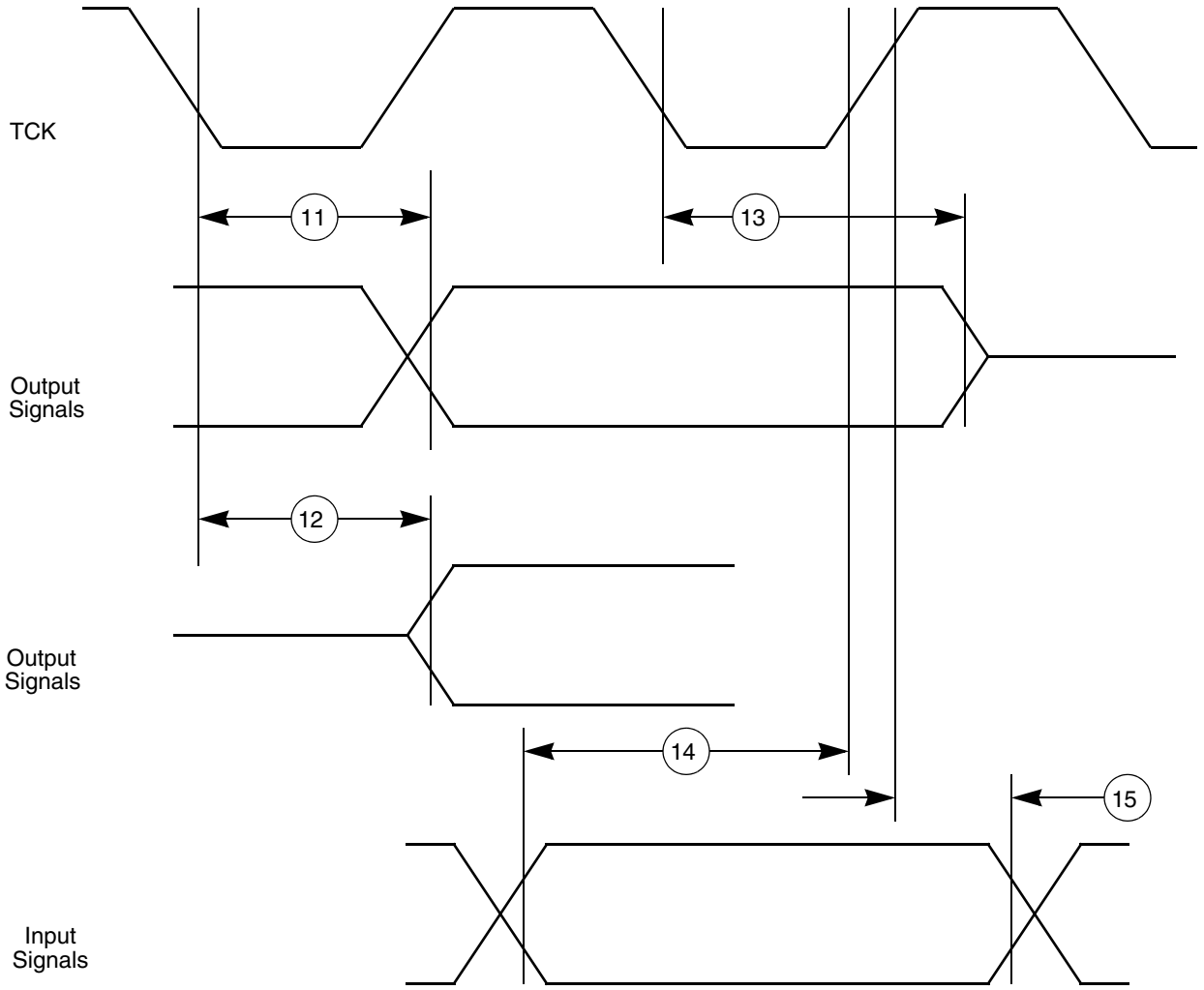

Figure 11. JTAG Boundary Scan Timing

2.13.4 Nexus Debug Interface

Table 22. Nexus Debug Port Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	MCKO Cycle Time	t_{MCYC}	40	—	ns
2	MCKO Duty Cycle	t_{MDC}	40	60	%
3	MCKO Low to MDO Data Valid[2]	t_{MDOV}	–2	4.0	ns
4	MCKO Low to $\overline{\text{MSEO}}$ Data Valid[2]	t_{MSEOV}	–2	4.0	ns
5	MCKO Low to $\overline{\text{EVTO}}$ Data Valid[2]	t_{EVTOV}	–2	4.0	ns
6	$\overline{\text{EVTI}}$ Pulse Width	t_{EVTIPW}	4.0	—	t_{TCYC}
7	$\overline{\text{EVTO}}$ Pulse Width	t_{EVTOPW}	1		t_{MCYC}
8	TCK Cycle Time[3]	t_{TCYC}	40	—	ns
9	TCK Duty Cycle	t_{TDC}	40	60	%
10	TDI, TMS Data Setup Time	t_{NTDIS}, t_{NTMSS}	8	—	ns
11	TDI, TMS Data Hold Time	t_{NTDIH}, t_{NTMSH}	4	—	ns
12	TCK Low to TDO Data Valid	t_{JOV}	0	8	ns

1 JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at VDDE = 3.0V to 5.5V, T_A = TL to TH, and CL = 30pF with SRC = 0b11.

2 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

3 The system clock frequency needs to be three times faster that the TCK frequency.

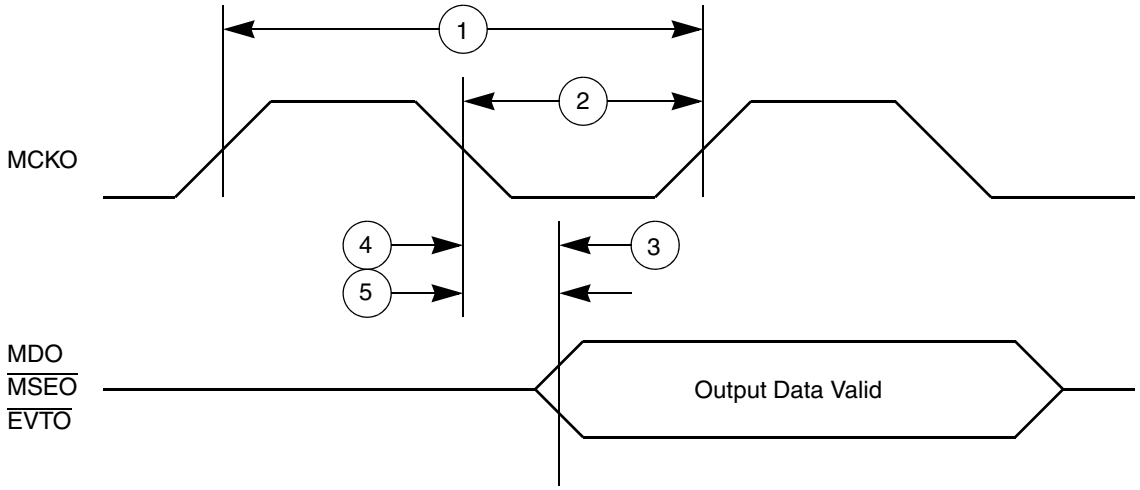

Figure 12. Nexus Output Timing

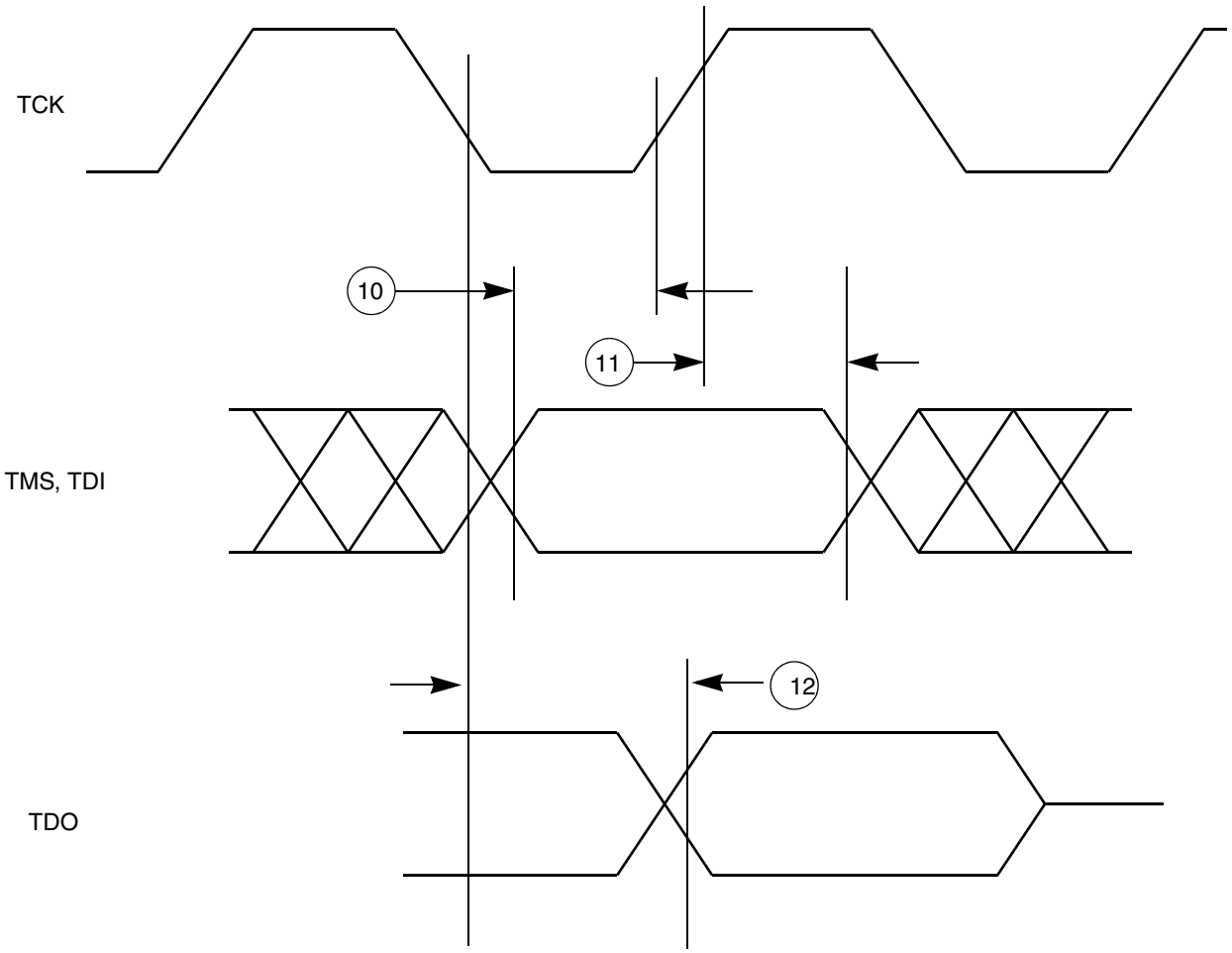

Figure 13. Nexus TDI, TMS, TDO Timing

2.13.5 External Bus Interface (EBI)

Table 23. External Bus Operation Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	CLKOUT Period[2]	T_C	40.0	—	ns
2	CLKOUT duty cycle	t_{CDC}	45%	55%	T_C
3	CLKOUT rise time	t_{CRT}	—	—[3]	ns
4	CLKOUT fall time	t_{CFT}	—	—[3]	ns
5	CLKOUT Positive Edge to Output Signal Invalid or High Z (Hold Time)	t_{COH}	2.0	—	ns
6	CLKOUT Positive Edge to Output Signal Valid (Output Delay)	t_{COV}	—	10.0	ns
7	Input Signal Valid to CLKOUT Posedge (Setup Time)	t_{CIS}	20.0	—	ns
8	CLKOUT Posedge to Input Signal Invalid (Hold Time)	t_{CIH}	0	—	ns
9	ALE Pulse Width High Time	t_{ALEPWH}	20	—	ns
10	ALE Fall to AD Invalid	t_{ALEAD}	2	—	ns

1 EBI timing specified at VDDE = 3.0V to 5.5V, T_A = TL to TH, and CL = 50pF with SIU_PCR*n*[SRC] = 0b11.

2 Initialize SIU_ECCR[EBDF] to meet maximum external bus frequency.

3 Refer to Medium High Voltage (MH) pad AC specification in Table 18.

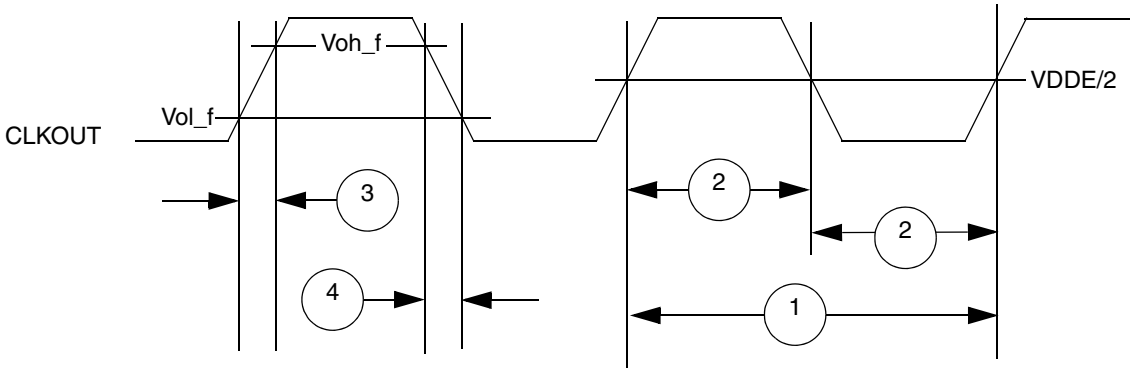

Figure 14. CLKOUT Timing

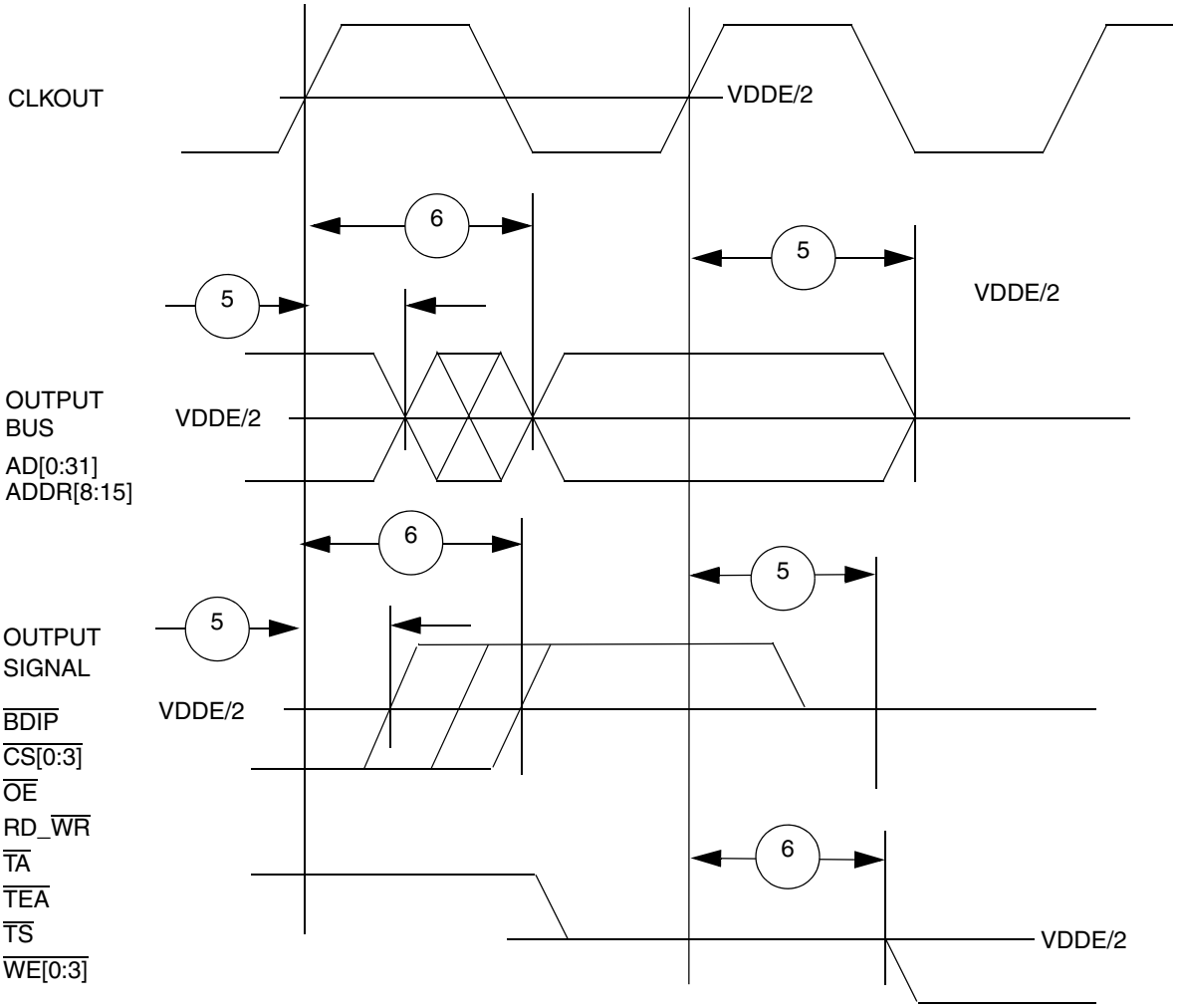

Figure 15. Synchronous Output Timing

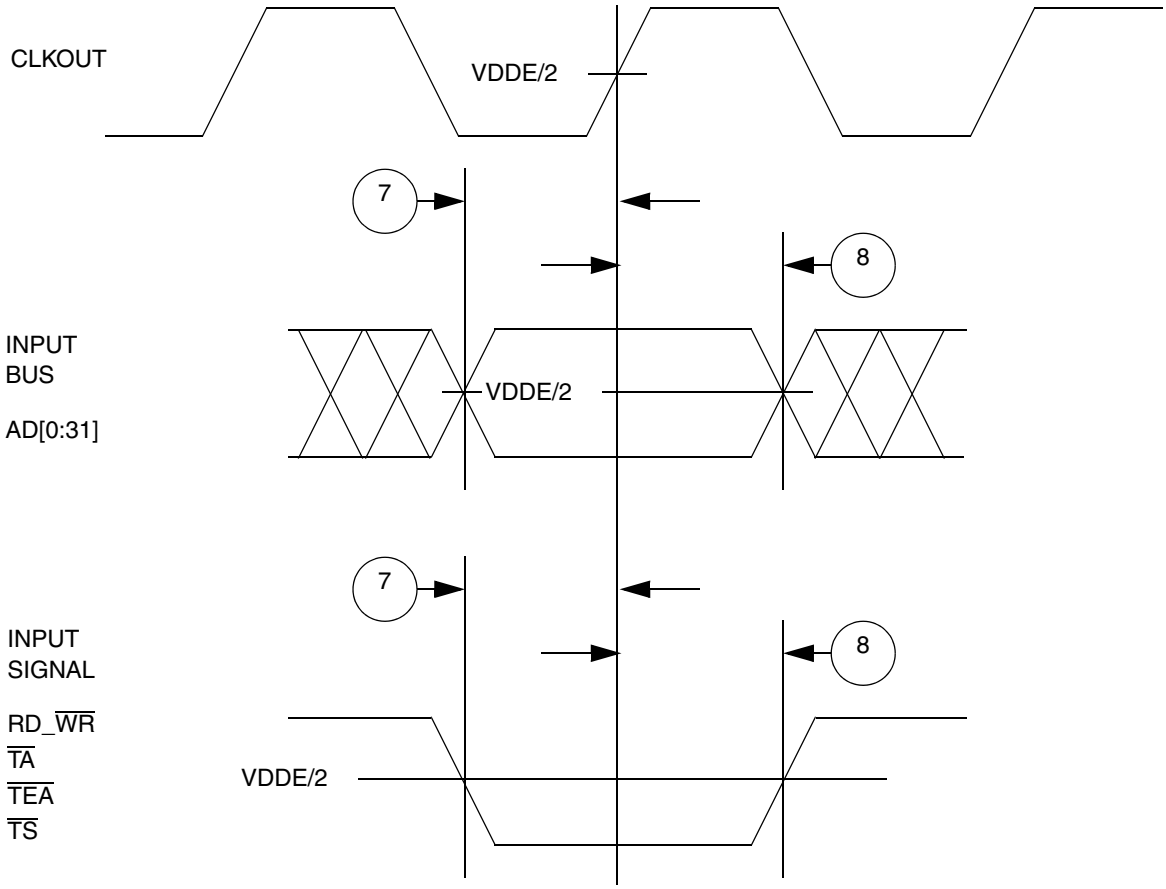

Figure 16. Synchronous Input Timing

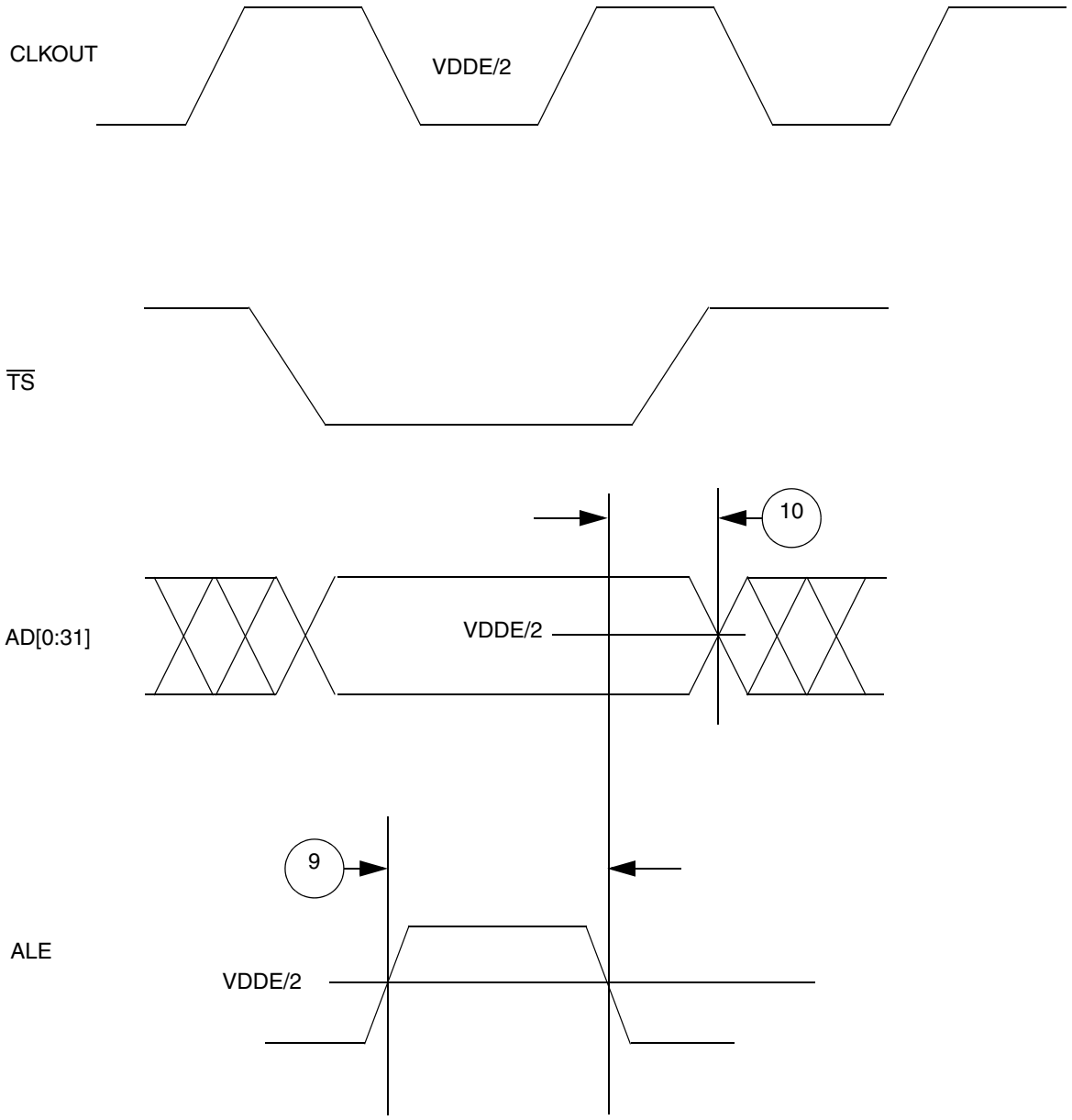

Figure 17. Address Latch Enable (ALE) Timing

2.13.6 Enhanced Modular I/O Subsystem (eMIOS)

Table 24. eMIOS Timing

Num	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{CYC}
2	eMIOS Output Pulse Width	t_{MOPW}	1	—	t_{CYC}

2.13.7 Deserial Serial Peripheral Interface (DSPI)

Table 25. DSPI Timing[1]

Num	Characteristic	Symbol	66 MHz		Unit
			Min	Max	
1	SCK Cycle TIme[2,3]	t_{SCK}	60	—	ns
2	PCS to SCK Delay[4]	t_{CSC}	20	—	ns
3	After SCK Delay[5]	t_{ASC}	20	—	ns
4	SCK Duty Cycle	t_{SDC}	$t_{SCK}/2$ –2ns	$t_{SCK}/2$ + 2ns	ns
5	Slave Access Time ($\overline{SS}$ active to SOUT driven)	t_A	—	25	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	—	25	ns
7	PCSx to $\overline{PCSS}$ time	t_{PCSC}	4	—	ns
8	$\overline{PCSS}$ to PCSx time	t_{PASC}	5	—	ns
9	Data Setup Time for Inputs	t_{SUI}			
	Master (MTFE = 0)		35	—	ns
	Slave		5	—	ns
	Master (MTFE = 1, CPHA = 0)[6]		5	—	ns
	Master (MTFE = 1, CPHA = 1)		35	—	ns
10	Data Hold Time for Inputs	t_{HI}			
	Master (MTFE = 0)		–4	—	ns
	Slave		10	—	ns
	Master (MTFE = 1, CPHA = 0)[6]		26	—	ns
	Master (MTFE = 1, CPHA = 1)		–4	—	ns
11	Data Valid (after SCK edge)	t_{SUO}			
	Master (MTFE = 0)		—	15	ns
	Slave		—	35	ns
	Master (MTFE = 1, CPHA=0)		—	30	ns
	Master (MTFE = 1, CPHA=1)		—	15	ns
12	Data Hold Time for Outputs	t_{HO}			
	Master (MTFE = 0)		–15	—	ns
	Slave		5.5	—	ns
	Master (MTFE = 1, CPHA = 0)		0	—	ns
	Master (MTFE = 1, CPHA = 1)		–15	—	ns

1 DSPI timing specified at VDDE = 3.0V to 5.5V, T_A = TL to TH, and CL = 50pF with SRC = 0b11.

2 The minimum SCK Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two MPC55xx devices communicating over a DSPI link.

3 The actual minimum SCK Cycle Time is limited by pad performance.

4 The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]

5 The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC]

6 This number is calculated assuming the SMPL_PT bit field in DSPI_MCR is set to 0b10.

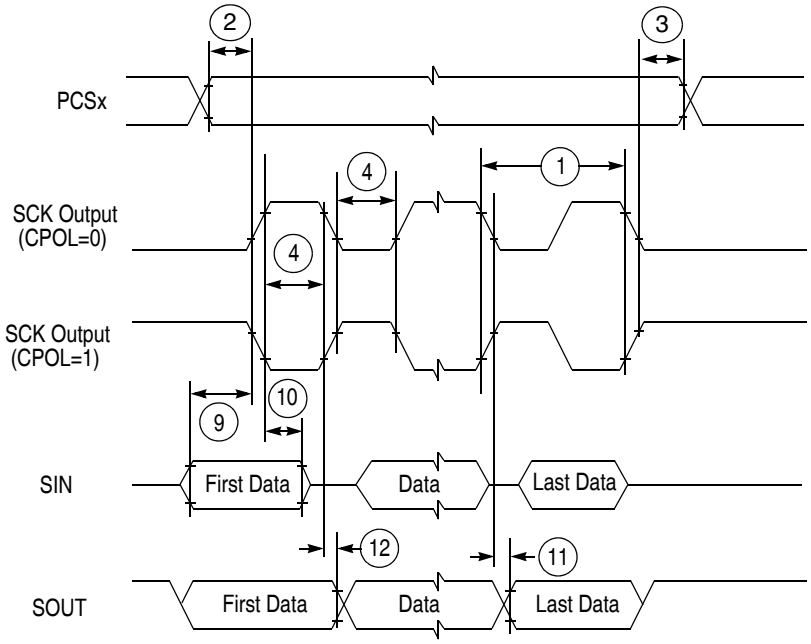

Figure 18. DSPI Classic SPI Timing — Master, CPHA = 0

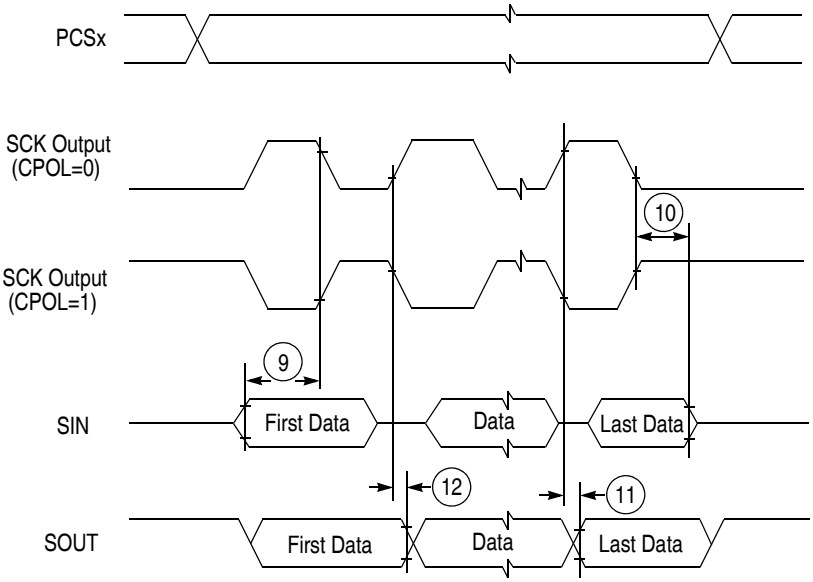

Figure 19. DSPI Classic SPI Timing — Master, CPHA = 1

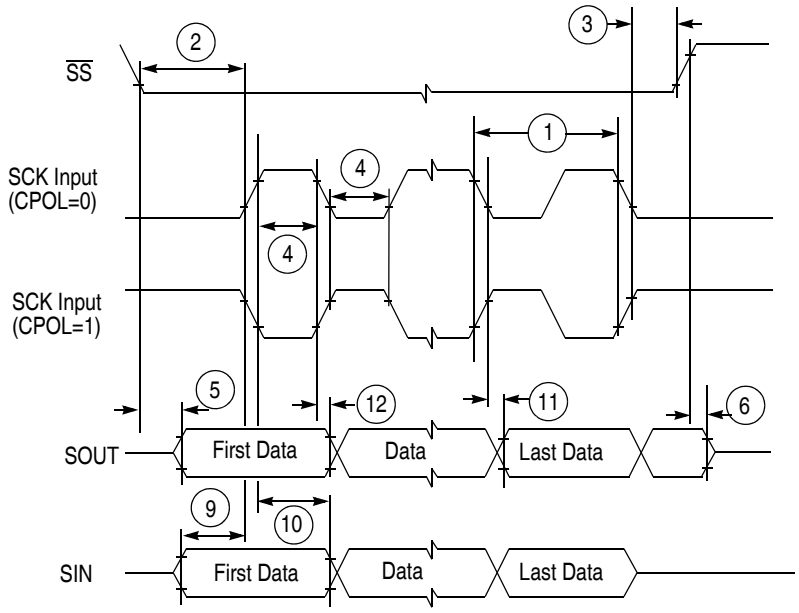

Figure 20. DSPI Classic SPI Timing — Slave, CPHA = 0

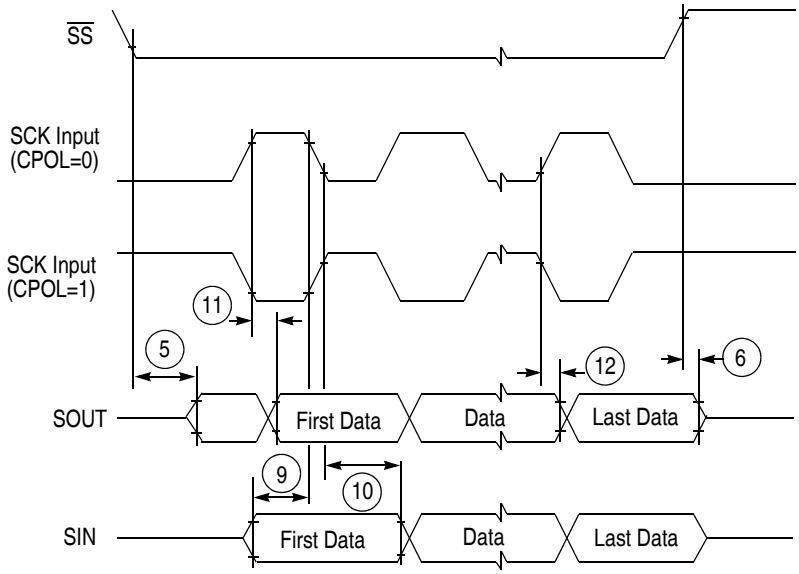

Figure 21. DSPI Classic SPI Timing — Slave, CPHA = 1

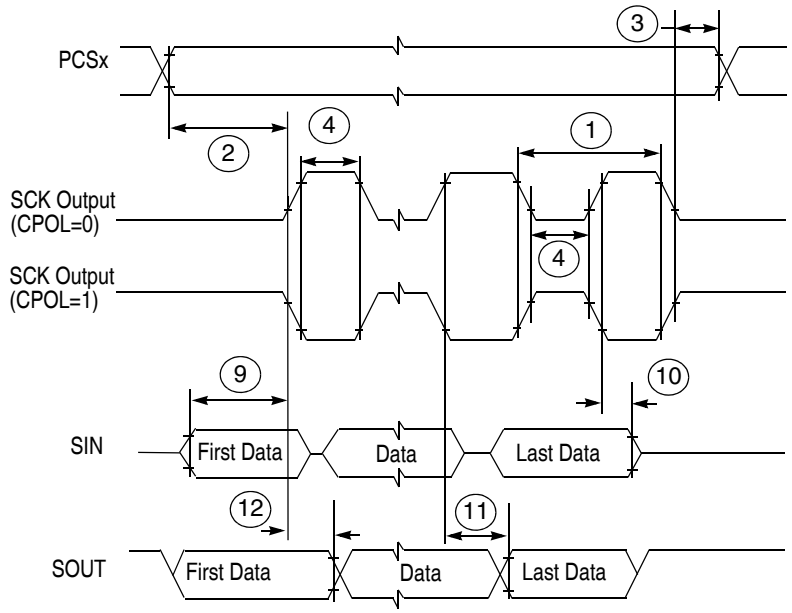

Figure 22. DSPI Modified Transfer Format Timing — Master, CPHA = 0

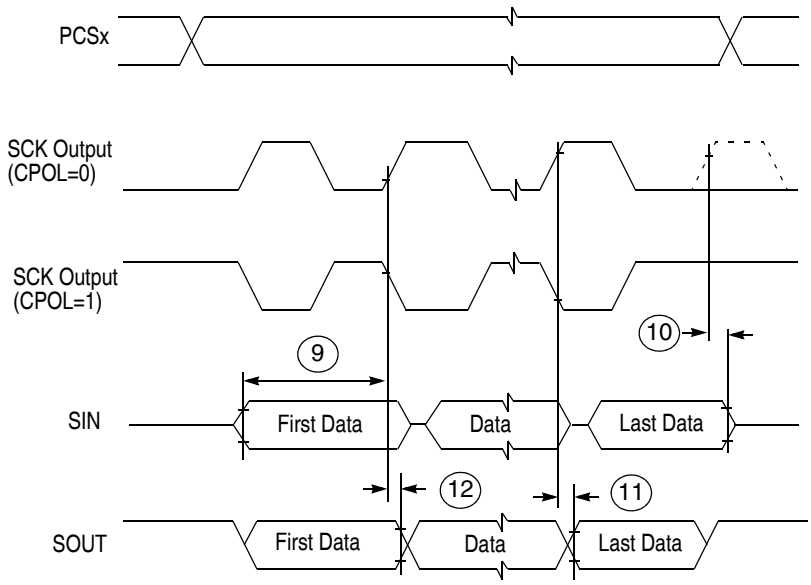

Figure 23. DSPI Modified Transfer Format Timing — Master, CPHA = 1

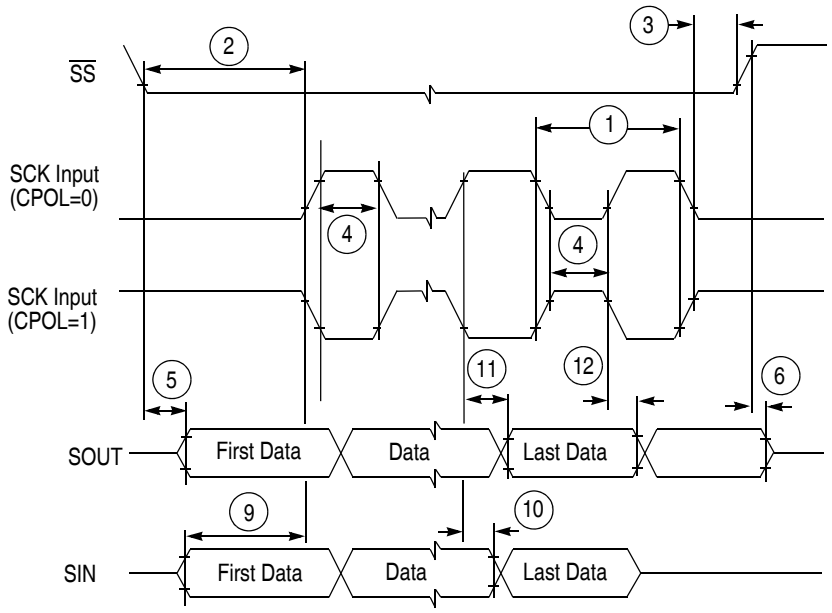

Figure 24. DSPI Modified Transfer Format Timing — Slave, CPHA = 0

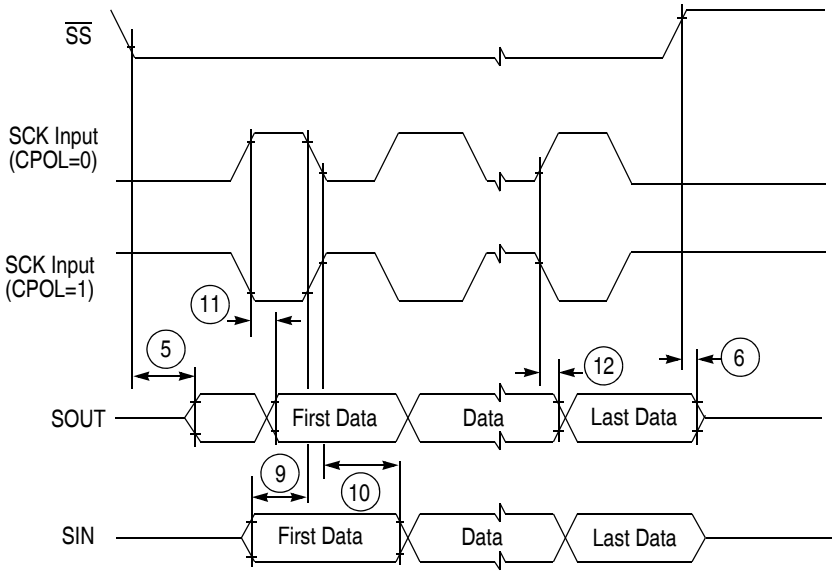

Figure 25. DSPI Modified Transfer Format Timing — Slave, CPHA = 1

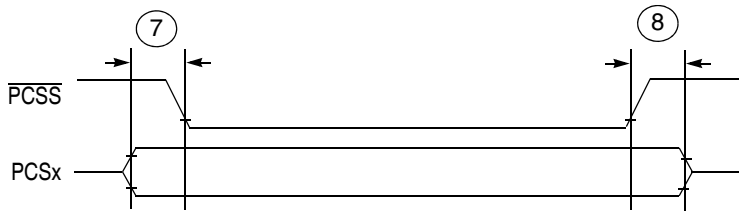

Figure 26. DSPI PCS Strobe ($\overline{\text{PCSS}}$) Timing

3 Package Information

The latest package outline drawings are available on the product summary pages on our web site: http://www.freescale.com/powerpc. The following table lists the package case number per device. Use these numbers in the web page's "keyword" search engine to find the latest package outline drawings.

Table 26. Package Information

Package	Package Case Number
144 LQFP	98ASS23177W
176 LQFP	98ASS23479W
208 MAPBGA	98ARS23882W

4 Product Documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at http://www.freescale.com/powerpc.

4.1 Revision History

Table 27 summarizes revisions to this document.

Table 27. Revision History of MPC5510 Data Sheet

Revision	Date	Substantive Changes
Rev. 0	9/2007	Initial Release. Preliminary content.
Rev. 1	6/2008	(Note: Change descriptions refer to locations in Rev. 0.) Changed MPC5516 to MPC5510 Family where appropriate. Modified Figure 1. MPC5510 Family Block Diagram. Deleted Table 1. MPC5510 Family Comparison, Maximum Feature Set Deleted Table 2. MPC5510 Peripheral Multiplexing Examples Corrected PK0 and PK1 pin assignments on 208 MAPBGA (Table 3 and Figure 4). Modified Table 4, footnote 4. Modified Table 8. DC Electrical Specifications and table footnotes. Modified Table 9. Operating Currents and table footnotes. Modified Table 12. 3.3V High Frequency External Oscillator, row 5. Modified Table 14. 5V High Frequency (16 MHz) Internal RC Oscillator, row 2. Modified Table 16. FMPLL Electrical Specifications, row 4. Modified Table 17. eQADC Conversion Specifications (Operating) and table footnotes. Modified Table 18. Flash Program and EraseSpecifications, row 5. Modified Table 19. Flash EEPROM Module Life (Full Temperature Range), row 1 Modified Table 28. Package Information.
Rev. 2	12/2008	(Note: Change descriptions refer to locations in Rev. 1.) Modified Table 1. MPC5510 Signal Properties: added note to TEST signal. Modified Table 6. DC Electrical Specifications: rows 1b, 5, 8, 9, 10, 11, 16, 19, 25, and footnotes. Modified Table 7. Operating Currents: Max column header, rows 1, 2, 3, 4, and footnotes. Modified Table 9. Low Voltage Monitors: rows 2, 3, 4, 6. Modified Table 10. 3.3V High Frequence External Oscillator: row 1 added footnote, removed duplicate footnote #3. Modified Table 11. 5V Low Frequency (32 kHz) External Oscillator: row 1. Modified Table 12. 5V High Frequency (16 MHz) Internal RC Oscillator: row 2. Modified Table 13. 5V Low Frequency (32 kHz) Internal RC Oscillator: row 2. Modified Table 14. FMPLL Electrical Specifications: rows 1 and 4; added two new rows. Modified Table 15. eQADC Conversion Specifications (Operating): rows 5, 6, 7, 8, 10, 11, and footnotes. Modified Figure 5. Pad Output Delay: moved the dashed horizontal line up so that it crosses the signal midway between top and bottom.
Rev. 3	3/2009	(Note: Change descriptions refer to locations in Rev. 2.) Modified Table 4. Thermal Characteristics: all values in 208 MAPBGA column. Modified Table 6. DC Electrical Specifications: spec #1c, added footnote; spec #25, added footnote. Modified Table 7. Operating Currents; spec #5. Modified Table 9. Low Voltage Monitors; spec #1. Modified Table 14. FMPLL Electrical Specifications: updated footnote 3; added spec #10a. Modified Table 15. eQADC Conversion Specifications (Operating): added another footnote. Modified Table 16: Flash Program and Erase Specifications: updated spec #7. Modified Figure 5: Pad Output Delay: adjusted lower timing diagram. Modified Figure 8: JTAG Test Clock Input Timing; updated so that it matches the spec definitions.
Rev. 4	7/2014	Updated the VCO Min. value from 192 to 250 MHz in Table 14., “FMPLL Electrical Specifications.

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Rev. 4
7/2014