



74ALVCH162827

20-bit buffer/line driver; non-inverting; with 30 Ohm termination resistors; 3-state

Rev. 3 — 28 June 2024

Product data sheet

1. General description

The 74ALVCH162827 is a 20-bit buffer/line driver with bus hold inputs, 30 Ω termination resistors and 3-state outputs. The device can be used as two 10-bit buffers or one 20-bit buffer. The device features output enable ($\overline{\text{nOE1}}$ and $\overline{\text{nOE2}}$) inputs, each controlling 10-bits. A HIGH on either $\overline{\text{nOE1}}$ or $\overline{\text{nOE2}}$ causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

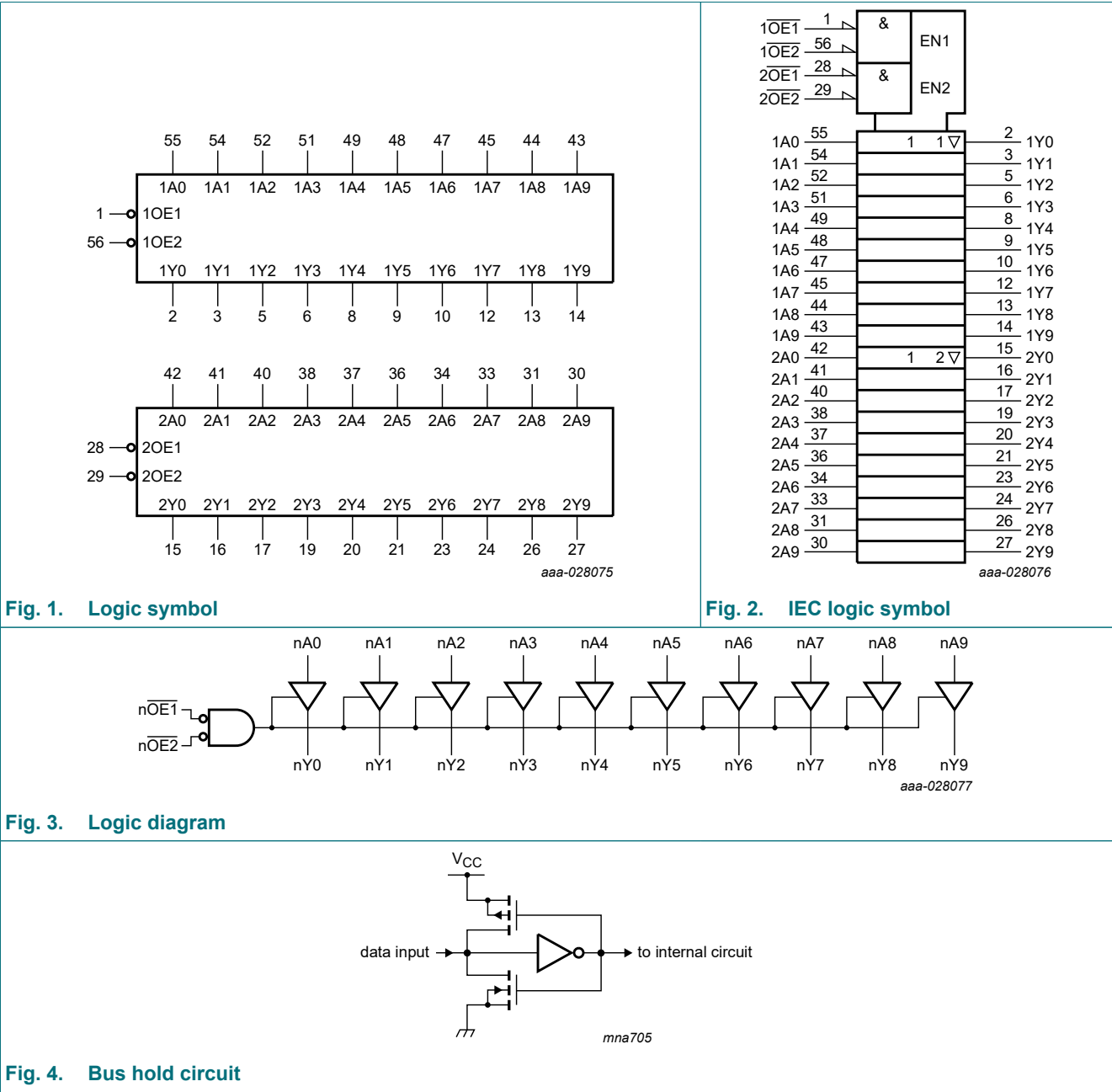
- CMOS low power dissipation
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Bus hold on data inputs
- Current drive ± 12 mA at 3.0 V
- Integrated 30 Ω termination resistors
- Complies with JEDEC standards:
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

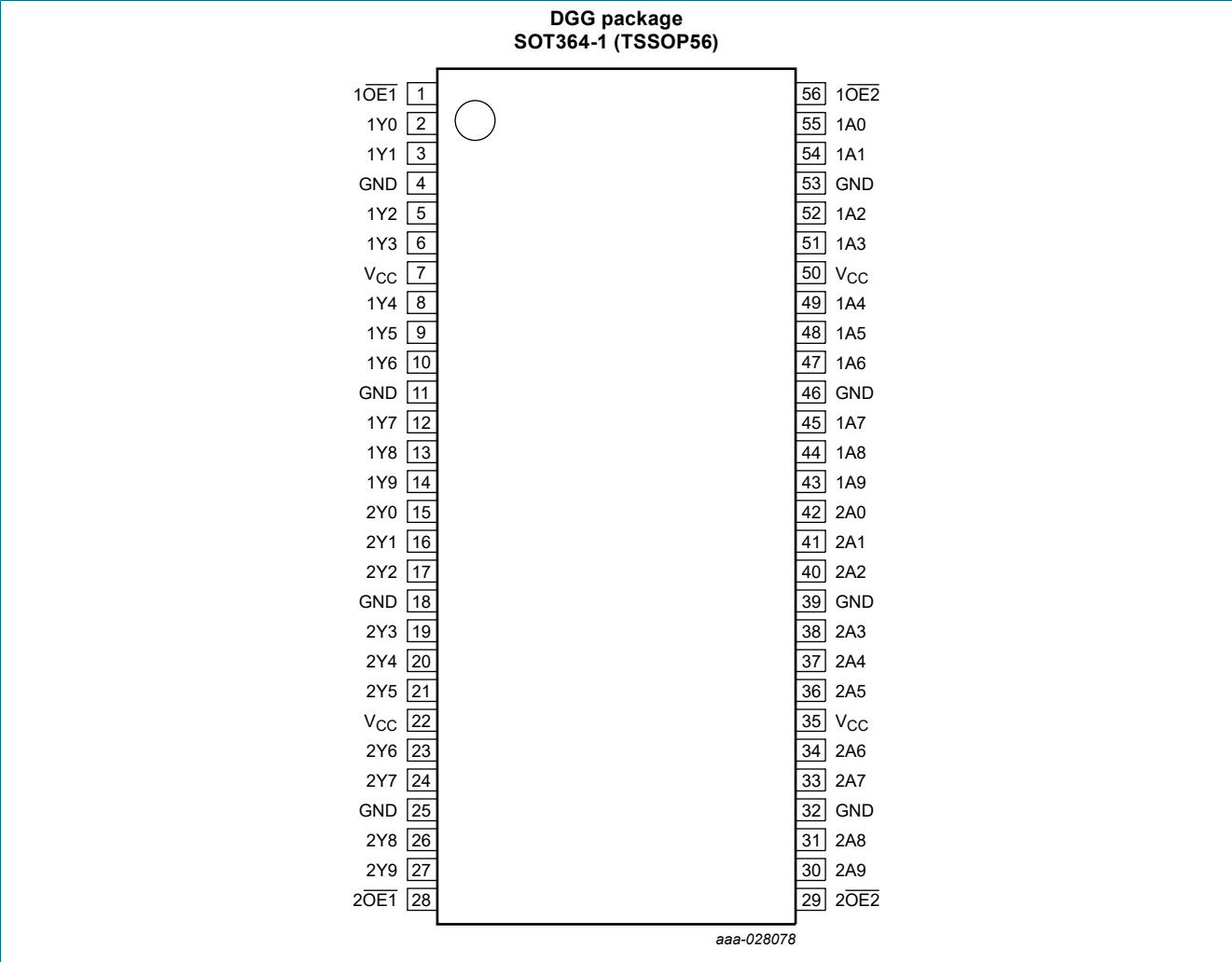
Type number	Package			
	Temperature range	Name	Description	Version
74ALVCH162827DGG	-40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7, 1A8, 1A9	55, 54, 52, 51, 49, 48, 47, 45, 44, 43	data input
2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7, 2A8, 2A9	42, 41, 40, 38, 37, 36, 34, 33, 31, 30	data input
1Y0, 1Y1, 1Y2, 1Y3, 1Y4, 1Y5, 1Y6, 1Y7, 1Y8, 1Y9	2, 3, 5, 6, 8, 9, 10, 12, 13, 14	data output
2Y0, 2Y1, 2Y2, 2Y3, 2Y4, 2Y5, 2Y6, 2Y7, 2Y8, 2Y9	15, 16, 17, 19, 20, 21, 23, 24, 26, 27	data output
1OE1, 1OE2, 2OE1, 2OE2	1, 56, 28, 29	output enable input (active-LOW)
GND	4, 11, 18, 25, 32, 39, 46, 53	ground (0 V)
VCC	7, 22, 35, 50	positive voltage supply

6. Functional description

Table 3. Function table

X = don't care; Z = High-impedance OFF-state; H = HIGH voltage level; L = LOW voltage level.

Operating mode	Input		Output
	nOEn	nAn	nYn
transparent	L	L	L
transparent	L	H	H
High-impedance	H	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		−0.5	+4.6	V
V _I	input voltage	[1]	−0.5	+4.6	V
V _O	output voltage	[1]	−0.5	V _{CC} + 0.5	V
I _{IK}	input clamping current	V _I < 0 V	−50	-	mA
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		−100	-	mA
T _{stg}	storage temperature		−65	+150	°C
P _{tot}	total power dissipation	T _{amb} = −40 °C to +85 °C	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage	For maximum speed performance at C _L = 30 pF	2.3	2.7	V
		For maximum speed performance at C _L = 50 pF	3.0	3.6	V
V _I	input voltage		0	V _{CC}	V
V _O	output voltage		0	V _{CC}	V
T _{amb}	ambient temperature	in free air	−40	+85	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.3 V to 3.0 V	0	20	ns/V
		V _{CC} = 3.0 V to 3.6 V	0	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 2.3 to 2.7 V	1.7	1.2	-	V
		V _{CC} = 2.7 to 3.6 V	2.0	1.5	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.3 to 2.7 V	-	1.2	0.7	V
		V _{CC} = 2.7 to 3.6 V	-	1.5	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -100 µA; V _{CC} = 2.3 V to 3.6 V	V _{CC} - 0.2	V _{CC}	-	V
		I _O = -4 mA; V _{CC} = 2.3 V	V _{CC} - 0.4	V _{CC} - 0.11	-	V
		I _O = -6 mA; V _{CC} = 2.3 V	V _{CC} - 0.6	V _{CC} - 0.17	-	V
		I _O = -4 mA; V _{CC} = 2.7 V	V _{CC} - 0.5	V _{CC} - 0.09	-	V
		I _O = -8 mA; V _{CC} = 2.7 V	V _{CC} - 0.7	V _{CC} - 0.19	-	V
		I _O = -6 mA; V _{CC} = 3.0 V	V _{CC} - 0.6	V _{CC} - 0.13	-	V
		I _O = -12 mA; V _{CC} = 3.0 V	V _{CC} - 1.0	V _{CC} - 0.27	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 µA; V _{CC} = 2.3 V to 3.6 V	-	GND	0.20	V
		I _O = 4 mA; V _{CC} = 2.3 V	-	0.07	0.40	V
		I _O = 6 mA; V _{CC} = 2.3 V	-	0.11	0.55	V
		I _O = 4 mA; V _{CC} = 2.7 V	-	0.06	0.40	V
		I _O = 8 mA; V _{CC} = 2.7 V	-	0.13	0.60	V
		I _O = 6 mA; V _{CC} = 3.0 V	-	0.09	0.55	V
		I _O = 12 mA; V _{CC} = 3.0 V	-	0.19	0.80	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 2.3 V to 3.6 V	-	0.1	5	µA
I _{BHL}	bus hold LOW current	V _{CC} = 2.3 V; V _I = 0.7 V	45	-	-	µA
I _{BHH}	bus hold HIGH current	V _{CC} = 2.3 V; V _I = 1.7 V	-45	-	-	µA
		V _{CC} = 3.0 V; V _I = 2.0 V	-75	-175	-	µA
I _{BHLO}	bus hold LOW overdrive current	V _{CC} = 3.6 V	500	-	-	µA
I _{BHHO}	bus hold HIGH overdrive current	V _{CC} = 3.6 V	-500	-	-	µA
I _{OZ}	OFF-state output current	V _{CC} = 2.3 V to 3.6 V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	-	0.1	10	µA
I _{CC}	supply current	V _{CC} = 2.3 to 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.2	40	µA
ΔI _{CC}	additional supply current	V _{CC} = 2.3 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	150	750	µA
C _I	input capacitance		-	5.0	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

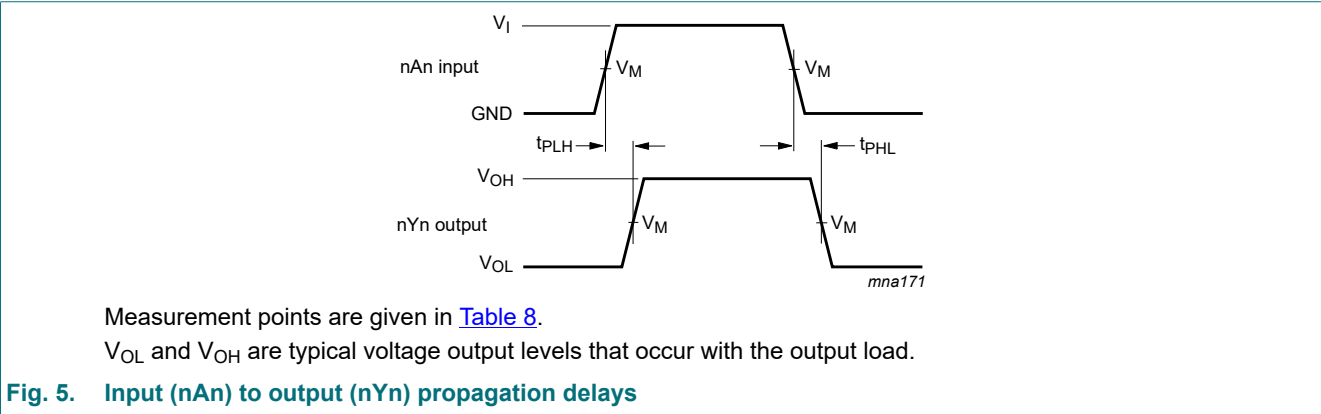
10. Dynamic characteristics

Table 7. Dynamic characteristics
 Voltages are referenced to GND (ground = 0 V). For test circuit, see Fig. 7 .

Symbol	Parameter	Conditions	−40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
t _{pd}	propagation delay	nAn to nYn; see Fig. 5 [2]				
		V _{CC} = 2.3 V to 2.7 V	1.0	2.9	4.6	ns
		V _{CC} = 2.7 V	-	3.1	4.7	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	2.9	4.2	ns
t _{en}	enable time	n $\overline{\text{OEn}}$ to nYn; see Fig. 6 [2]				
		V _{CC} = 2.3 V to 2.7 V	1.4	3.9	6.4	ns
		V _{CC} = 2.7 V	-	4.4	6.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.6	3.7	5.4	ns
t _{dis}	disable time	n $\overline{\text{OEn}}$ to nYn; see Fig. 6 [2]				
		V _{CC} = 2.3 V to 2.7 V	1.7	2.2	5.9	ns
		V _{CC} = 2.7 V	-	3.2	5.2	ns
		V _{CC} = 3.0 V to 3.6 V	1.8	3.0	4.7	ns
C _{PD}	power dissipation capacitance	per latch; V _I = GND to V _{CC} [3]				
		output enabled	-	14	-	pF
		output disabled	-	3	-	pF

- [1] Typical values are measured at T_{amb} = 25 °C
 Typical values for V_{CC} = 2.3 V to 2.7 V are measured at V_{CC} = 2.5 V
 Typical values for V_{CC} = 3.0 V to 3.6 V are measured at V_{CC} = 3.3 V
- [2] t_{pd} is the same as t_{PHL} and t_{PLH};
 t_{en} is the same as t_{PZH} and t_{PZL};
 t_{dis} is the same as t_{PHZ} and t_{PLZ}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



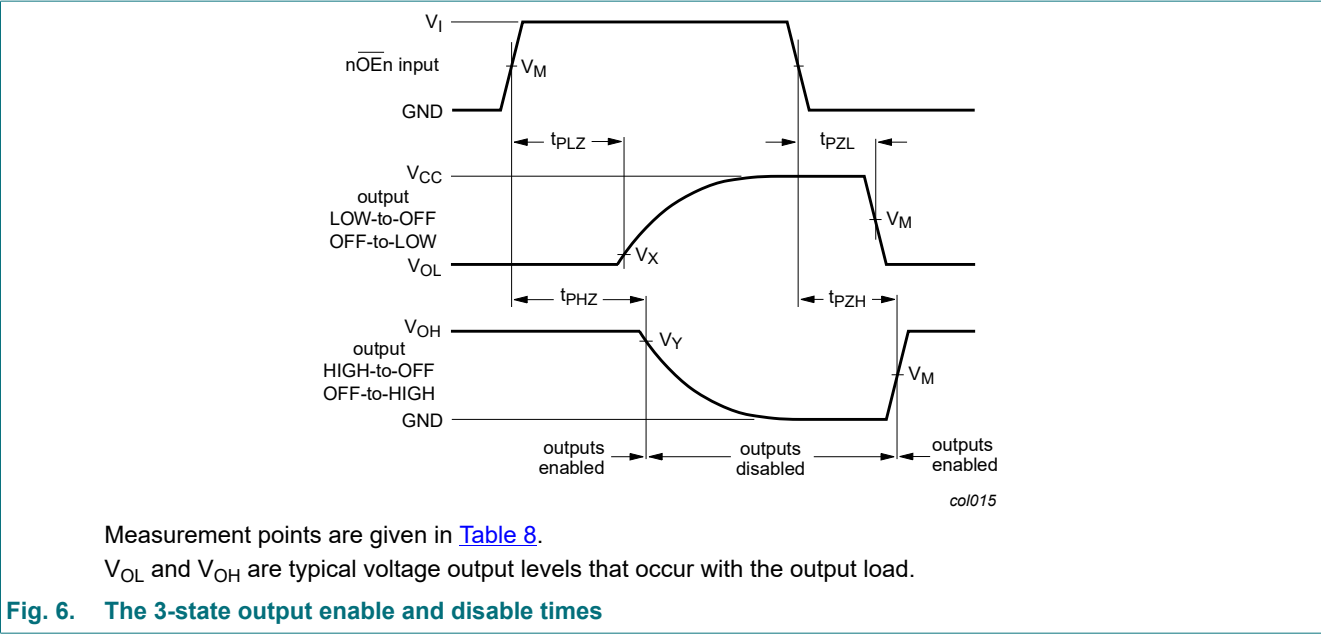


Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$

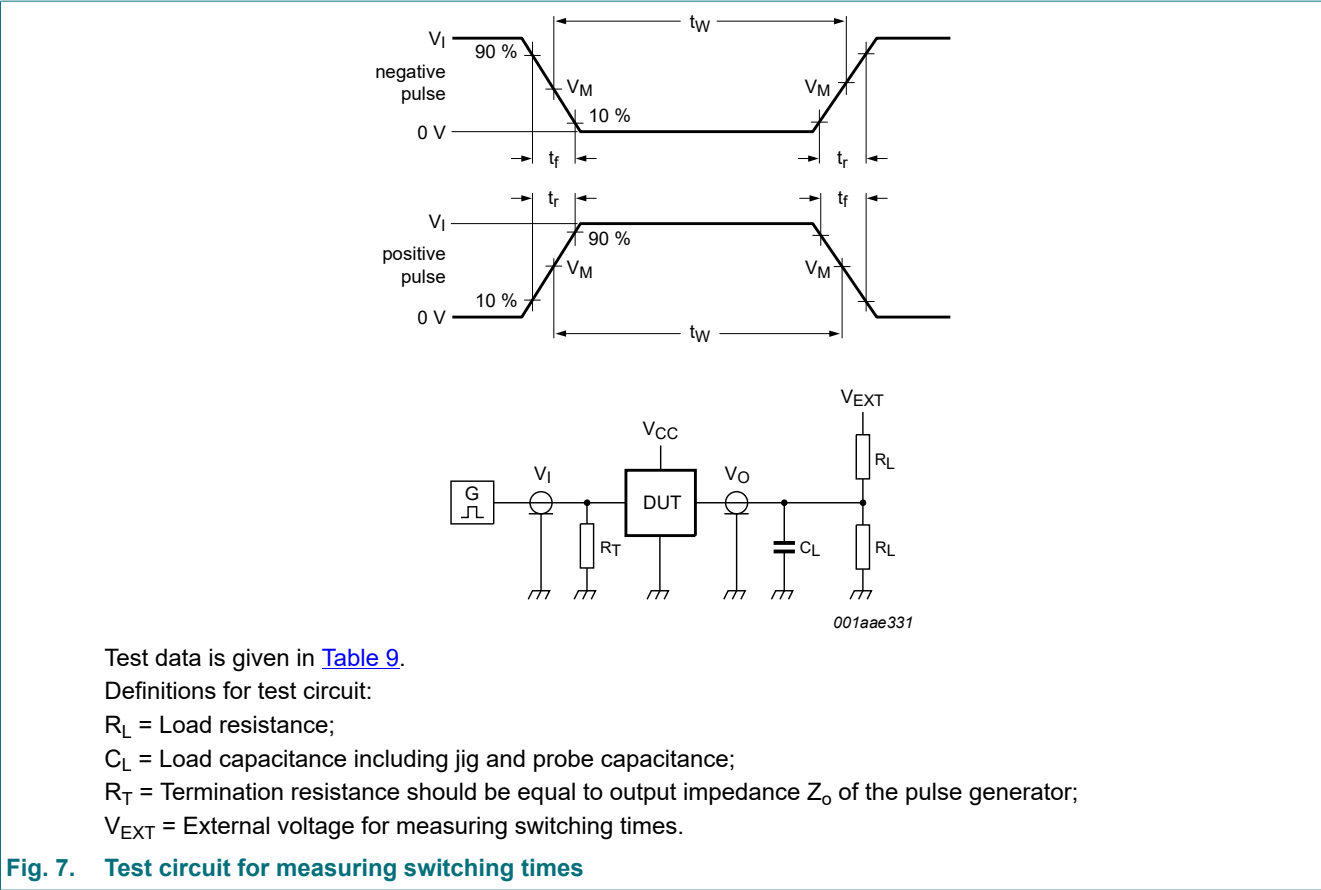


Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

11. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

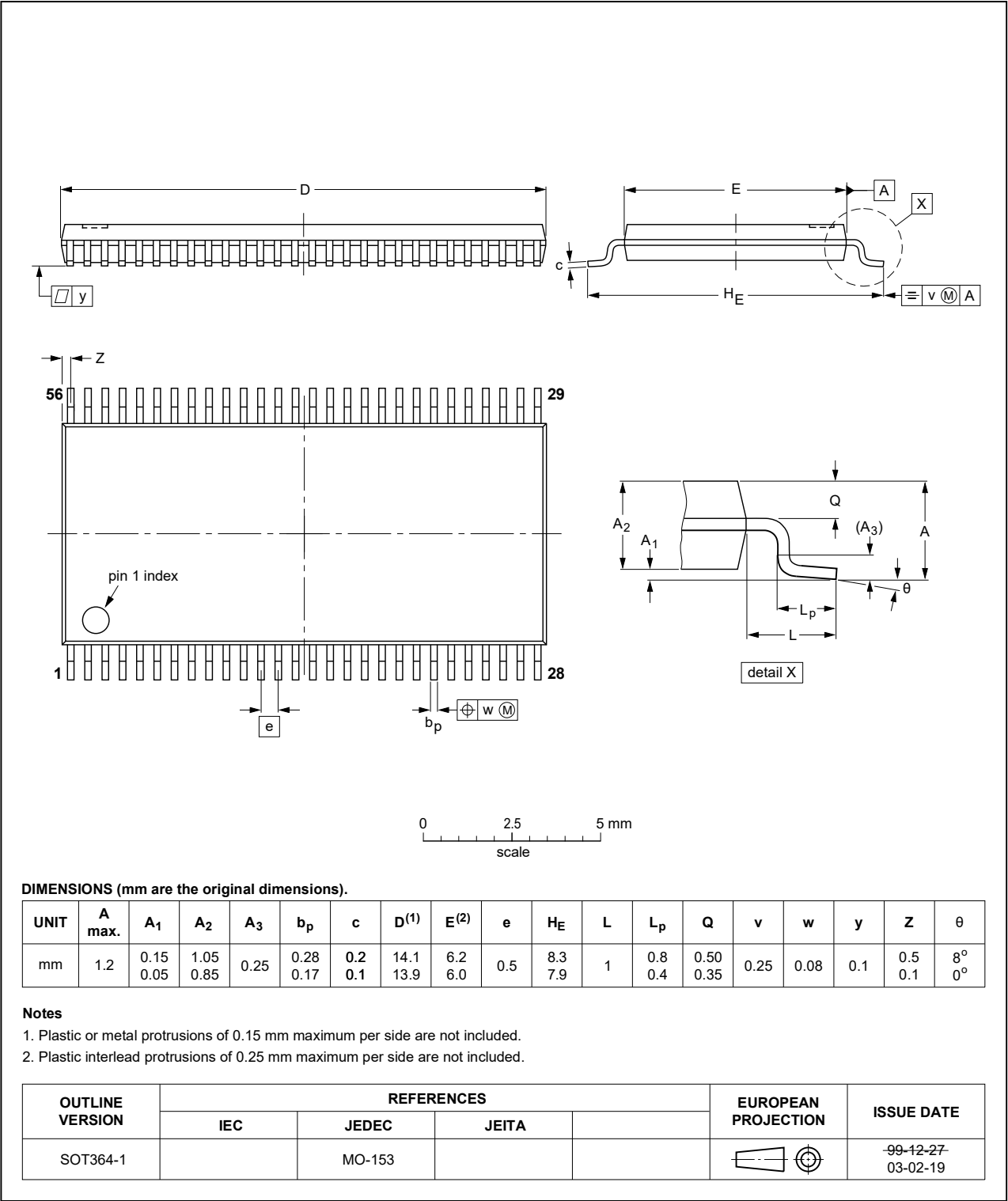


Fig. 8. Package outline SOT364-1 (TSSOP56)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH162827 v.3	20240628	Product data sheet	-	74ALVCH162827 v.2
Modifications:	• Section 1 updated. • Section 2: ESD specification updated according to the latest JEDEC standard. • Table 4: P_{tot} total power dissipation updated.			
74ALVCH162827 v.2	20180119	Product data sheet	-	74ALVCH162827 v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74ALVCH162827 v.1	19980929	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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