

Diagnostic Scan Register

Features

- Function, pinout and drive compatible with FCT, F Logic and AM29818
- FCT-C speed at 6.0 ns max. (Com'l)
FCT-B speed at 7.5 ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- Sink current 64 mA (Com'l),
20 mA (Mil)
- Source current 32 mA (Com'l),
3 mA (Mil)
- 8-Bit pipeline and shadow register
- ESD > 2000V

Functional Description

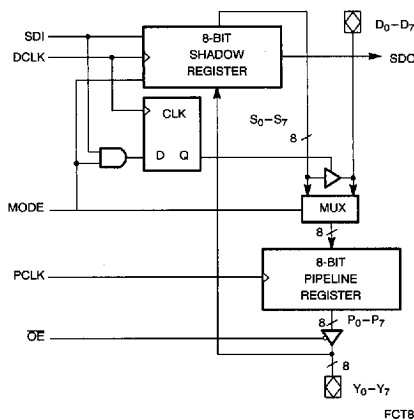
The FCT818T contains a high-speed 8-bit general-purpose data pipeline register and a high-speed 8-bit shadow register. The general-purpose register can be used in an 8-bit wide data path for a normal system application. The shadow register is designed for applications, such as diagnostics in sequential circuits, where it is desirable to load known data at a specific location in the circuit and to read the data at that location.

The shadow registers can load data from the output of the FCT818T, and can be used as a right-shift register with bit-serial input SDI and output SDO, using DCLK. The data register input is multiplexed to enable loading from the shadow register or from the data input pins using PCLK. Note that data can be loaded simultaneously from the shadow register to the pipeline register, and from the pipeline register to the shadow register provided set-up and hold time requirements are satisfied with respect to the two independent clock inputs.

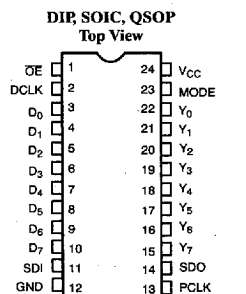
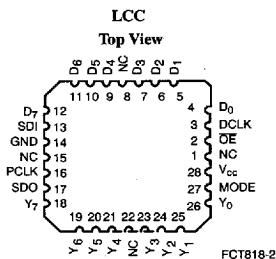
In a typical application, the general-purpose register in the FCT818T replaces an 8-bit data register in the normal data path of a system. The shadow register is placed in an auxiliary bit-serial loop which is used for diagnostics. During diagnostic operation, data is shifted serially into the shadow register, then transferred to the general purpose register to load a known value into the data path. To read the contents at that point in the data path, the data is transferred from the data register into the shadow register, then shifted serially in the auxiliary diagnostic loop to make it accessible to the diagnostics controller. This data is then compared with the expected value to diagnose faulty operation of the sequential circuit.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram



Pin Configurations



Function Table^[1]

Inputs			Inputs		Shadow Register	Pipeline Register	Operation
MODE	SDI	DCLK	PCLK	SDO			
L	X	┐	X	S ₇	S ₀ ← SDI S _i ← S _{i-1} NA	NA	Serial Shift; D ₇ –D ₀ Output Disabled
L	X	X	┐	S ₇	NA	P _i ← D _i	Load Pipeline Register from Data Input
H	L	┐	X	L	S _i ← Y _i	NA	Load Shadow Register from Y Output
H	H	┐	X	H	Hold	NA	Hold Shadow Register; D ₇ –D ₀ Output Enabled
H	X	X	┐	SDI	NA	P _i ← S _i	Load Pipeline Register from Shadow Register

Maximum Ratings^[2,3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–65°C to +135°C
Supply Voltage to Ground Potential	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Voltage	–0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	120 mA
Power Dissipation	0.5W

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT, BT	–40°C to +85°C	5V ± 5%
Military ^[4]	All	–55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. ^[5]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =–32 mA	Com'l	2.0			V
		V _{CC} =Min., I _{OH} =–15 mA	Com'l	2.4	3.3		V
		V _{CC} =Min., I _{OH} =–3 mA	Mil	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =20 mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage			2.0			V
V _{IL}	Input LOW Voltage					0.8	V
V _H	Hysteresis ^[6]	All inputs			0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =–18 mA			–0.7	–1.2	V
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}				5	μA
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V				±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V				±1	μA
I _{OZH}	Off State HIGH-Level Output Current	V _{CC} =Max., V _{OUT} =2.7V				10	μA
I _{OZL}	Off State LOW-Level Output Current	V _{CC} =Max., V _{OUT} =0.5V				–10	μA
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V		–60	–120	–225	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V				±1	μA

Notes:

1. NA = Not Applicable
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameters tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance^[6]

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance		5	10	pF
C _{OUT}	Output Capacitance		9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max., V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V	0.2	1.5	mA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V _{CC} =Max., V _{IN} =3.4V, ^[8] f ₁ =0, Outputs Open	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ^[9]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, OE=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V		0.25	mA/ MHz
I _C	Total Power Supply Current ^[10]	V _{CC} =Max., f ₀ =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =5 MHz, OE=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V		5.3	mA
		V _{CC} =Max., f ₀ =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =5 MHz, OE=GND, V _{IN} =3.4V or V _{IN} =GND		7.3	mA
		V _{CC} =Max., f ₀ =10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits and Four Controls Toggling, f ₁ =5 MHz, OE=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V		17.8 ^[11]	mA
		V _{CC} =Max., f ₀ =10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits and Four Controls Toggling, f ₁ =5 MHz, OE=GND, V _{IN} =3.4V or V _{IN} =GND		30.8 ^[11]	mA

Note:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC}D_HN_T + I_{CCD}(f₀/2 + f₁N₁)
I_{CC} = Quiescent Current with CMOS input levels
ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
D_H = Duty Cycle for TTL inputs HIGH

- N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
f₀ = Clock frequency for registered devices, otherwise zero
f₁ = Input signal frequency
N₁ = Number of inputs changing at f₁
All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range^[12]

Parameter	Description	FCT818T				FCT818AT				Unit	Fig. No. ^[14]
		Military		Commercial		Military		Commercial			
		Min. ^[13]	Max.	Min. ^[13]	Max.	Min. ^[13]	Max.	Min. ^[13]	Max.		
t _{PD}	Propagation Delay PCLK to Y MODE to SDO SDI to SDO DCLK to SDO		18 18 18 30		13 16 16 25		12 18 18 30		9 16 15 25	ns ns ns ns	5 6 3 5
t _S	Set-Up Time D to PCLK MODE to PCLK Y to DCLK MODE to DCLK SDI to DCLK DCLK to PCLK PCLK to DCLK	10 15 5 12 10 15 45		8 15 5 12 10 15 40		6 15 5 12 10 15 45		4 15 5 12 10 15 40		ns ns ns ns ns ns ns	4
t _H	Hold Time D to PCLK MODE to PCLK Y to DCLK MODE to DCLK SDI to DCLK	2 0 5 5 0		2 0 5 2 0		2 0 5 5 0		2 0 5 2 0		ns ns ns ns ns	4
t _{PLZ}	Output Disable Time LOW OE to Y DCLK to D		20 45		15 45		20 45		15 45	ns ns	7 5
t _{PHZ}	Output Disable Time HIGH OE to Y DCLK to D		30 90		25 85		30 90		25 80	ns ns	8 5
t _{PZL}	Output Enable Time LOW OE to Y DCLK to D		20 35		15 30		20 35		15 25	ns ns	7 5
t _{PZH}	Output Enable Time HIGH OE to Y DCLK to D		20 30		15 25		20 30		15 25	ns ns	8 5
t _W	Pulse Width PCLK (HIGH and LOW) DCLK (HIGH and LOW)	15 25		15 25		15 25		10 15		ns ns	5 5

Notes:

12. AC Characteristics guaranteed with C_L = 50 pF as shown in Figure 1 of the "Parameter Measurement Information" in the General Information Section.

13. Minimum limits are guaranteed but not tested on Propagation Delays.

14. See "Parameter Measurement Information" in the General Information Section.

Switching Characteristics Over the Operating Range^[12] (continued)

Parameter	Description	FCT818BT				FCT818CT				Unit	Fig. No. ^[14]
		Military		Commercial		Military		Commercial			
		Min. ^[13]	Max.	Min. ^[13]	Max.	Min. ^[13]	Max.	Min. ^[13]	Max.		
t _{PD}	Propagation Delay										
	PCLK to Y		9.0		7.5		7.6		6.0	ns	5
	MODE to SDO		10.5		9.0		8.9		7.2	ns	6
	SDI to SDO		10.5		9.0		8.9		7.1	ns	3
	DCLK to SDO		10.5		9.0		8.9		7.2	ns	5
t _S	Set-Up Time										
	D to PCLK	4.5		3.0		3.0		2.0		ns	
	MODE to PCLK	6.5		5.0		5.0		3.5		ns	
	Y to DCLK	4.5		3.0		3.0		2.0		ns	
	MODE to DCLK	6.5		5.0		5.0		3.5		ns	4
	SDI to DCLK	6.5		5.0		5.0		3.5		ns	
	DCLK to PCLK	6.5		5.0		5.0		3.5		ns	
	PCLK to DCLK	12.5		11.0		11.0		8.5		ns	
t _H	Hold Time										
	D to PCLK	2.0		2.0		2.0		1.5		ns	
	MODE to PCLK	0		0		0		0		ns	
	Y to DCLK	3.0		2.0		3.0		1.5		ns	4
	MODE to DCLK	3.0		2.0		3.0		1.5		ns	
	SDI to DCLK	0		0		0		0		ns	
t _{PLZ}	Output Disable Time										
	LOW										
	OE to Y		8.5		7.0		7.0		5.5	ns	7
	DCLK to D		8.5		7.0		7.0		5.5	ns	5
t _{PHZ}	Output Disable Time										
	HIGH										
	OE to Y		10.5		9.0		9.0		8.0	ns	8
	DCLK to D		10.5		9.0		9.0		8.0	ns	5
t _{pZL}	Output Enable Time										
	LOW										
	OE to Y		11.5		10.0		10.0		8.0	ns	7
	DCLK to D		11.5		10.0		10.0		9.0	ns	5
t _{pZH}	Output Enable Time										
	HIGH										
	OE to Y		11.5		10.0		10.0		8.5	ns	8
	DCLK to D		12.5		11.0		11.0		9.0	ns	5
t _w	Pulse Width										
	PCLK (HIGH and	7.0		6.0		6.0		5.0		ns	5
	LOW)	7.0		6.0		6.0		5.0		ns	5
	DCLK (HIGH and										
	LOW)										

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.0	CY29FCT818CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT818CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT818CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.5	CY29FCT818BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT818BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT818BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.6	CY29FCT818CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT818CTLMB	L64	28-Square Leadless Chip Carrier	
9.0	CY29FCT818ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT818ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT818ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
	CY29FCT818BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT818BTLMB	L64	28-Square Leadless Chip Carrier	
12.0	CY29FCT818ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT818ATLMB	L64	28-Square Leadless Chip Carrier	
13.0	CY29FCT818TPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT818TQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT818TSOC	S13	24-Lead (300-Mil) Molded SOIC	
18.0	CY29FCT818TDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT818TLMB	L64	28-Square Leadless Chip Carrier	

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