

NC7SZ38

TinyLogic™ UHS 2-Input NAND Gate (Open Drain Output)

General Description

The NC7SZ38 is a single 2-Input NAND Gate with open drain output stage from Fairchild's Ultra High Speed Series of TinyLogic™. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.8V to 5.5V V_{CC} range. The inputs and output are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 6V independent of V_{CC} operating voltage. The open drain output stage will tolerate voltages up to 6V independent of V_{CC} when in the high impedance state.

Features

- Space saving SOT23 or SC70 5-lead surface mount package
- Open Drain output stage for OR tied applications
- Ultra High Speed; T_{PD} 2.4 ns Typ into 50 pF at 5V V_{CC}
- High Output Sink Drive; 24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range; 1.8V to 5.5V
- Matches the performance of LCX when operated at 3.3V V_{CC}
- Power down high impedance inputs/output
- Overvoltage Tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

Ordering Code:

Product Code	Package	Package Drawing	Package Top Mark	Supplied As
NC7SZ38M5	SOT23-5	MA05B	7Z38	250 Units on Tape and Reel
NC7SZ38M5X	SOT23-5	MA05B	7Z38	3k Units on Tape and Reel
NC7SZ38P5	SC70-5	MAA05A	Z38	250 Units on Tape and Reel
NC7SZ38P5X	SC70-5	MAA05A	Z38	3k Units on Tape and Reel

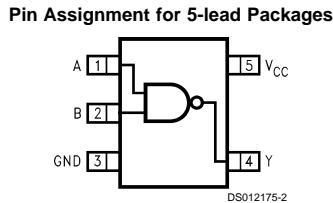
Logic Symbol



Pin Descriptions

Pin Names	Description
A, B	Inputs
Y	Output

Connection Diagram



(Top View)

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	*H
L	H	*H
H	L	*H
H	H	L

H = HIGH Logic Level

L = LOW Logic Level

*H = HIGH Impedance output state (Open Drain)

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Absolute Maximum Ratings (Note 1)			Negative Source Current (NIT)	-500 mA
			Positive Source Voltage (PVT)	+8V
Supply Voltage (V_{CC})		-0.5V to +6V		
DC Input Voltage (V_{IN})		-0.5V to +6V		
DC Output Voltage (V_{OUT})		-0.5V to +6V		
DC Input Diode Current (I_{IK})				
@ $V_{IN} < -0.5V$		-50 mA	Supply Voltage Operating (V_{CC})	1.8V to 5.5V
@ $V_{IN} > 6V$		+20 mA	Supply Voltage Data Retention (V_{CC})	1.5V to 5.5V
DC Output Diode Current (I_{OK})			Input Voltage (V_{IN})	0V to 5.5V
@ $V_{OUT} < -0.5V$		-50 mA	Output Voltage (V_{OUT})	0V to V_{CC}
@ $V_{OUT} > 6V, V_{CC} = GND$		+20 mA	Operating Temperature (T_A)	-40°C to +85°C
DC Output Current (I_{OUT})		+50 mA	Input Rise and Fall Time (t_r, t_f)	
DC V_{CC}/GND Current (I_{CC}/I_{GND})		±50 mA	$V_{CC} = 1.8V, 2.5V \pm 0.2V$	0 ns/V to 20 ns/V
Storage Temperature (T_{STG})		-65°C to +150°C	$V_{CC} = 3.3V \pm 0.3V$	0 ns/V to 10 ns/V
Junction Temperature under Bias (T_J)		150°C	$V_{CC} = 5.0V \pm 0.5V$	0 ns/V to 5 ns/V
Junction Lead Temp. (T_1); (Soldering, 10 sec)		260°C	Thermal Resistance (θ_{JA})	
Power Dissipation (P_D) @ +85°C			SOT23-5	300°C/W
SOT23-5		200 mW	SC70-5	425°C/W
SC70-5		150 mW		
ESD Tolerance (Human Body Model)				
MIL-STD-883D method 3015.7		1000V		
DC Latchup Tolerance (JEDEC Method 17)				

Recommended Operating Conditions

Supply Voltage Operating (V_{CC})	1.8V to 5.5V
Supply Voltage Data Retention (V_{CC})	1.5V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_A)	-40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
$V_{CC} = 1.8V, 2.5V \pm 0.2V$	0 ns/V to 20 ns/V
$V_{CC} = 3.3V \pm 0.3V$	0 ns/V to 10 ns/V
$V_{CC} = 5.0V \pm 0.5V$	0 ns/V to 5 ns/V
Thermal Resistance (θ_{JA})	
SOT23-5	300°C/W
SC70-5	425°C/W

Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

DC Electrical Characteristics

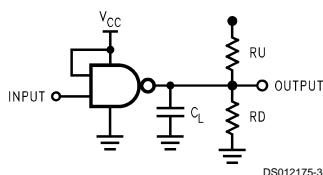
Symbol	Parameter	V_{CC} (V)	NC7SZ38			Units	Conditions		
			$T_A = +25^\circ C$						
			Min	Typ	Max				
V_{IH}	High Level Input Voltage	1.8 2.3 to 5.5	0.75 V_{CC} 0.7 V_{CC}		0.75 V_{CC} 0.7 V_{CC}	V			
V_{IL}	Low Level Input Voltage	1.8 2.3 to 5.5		0.25 V_{CC} 0.3 V_{CC}		V			
I_{LKG}	High Level Output Leakage	5.5		±5		µA	$V_{IN} = V_{IL}$ $V_{OUT} = V_{CC}$ or GND		
V_{OL}	Low Level Output Voltage	1.8	0.0	0.1	0.1	V	$V_{IN} = V_{IH}$		
		2.3	0.0	0.1	0.1		$I_{OL} = 100 \mu A$		
		3.0	0.0	0.1	0.1				
		4.5	0.0	0.1	0.1				
		2.3	0.10	0.3	0.3	V	$I_{OL} = 8 mA$		
		3.0	0.15	0.4	0.4		$I_{OL} = 16 mA$		
		3.0	0.22	0.55	0.55		$I_{OL} = 24 mA$		
		4.5	0.22	0.55	0.55		$I_{OL} = 32 mA$		
I_{IN}	Input Leakage Current	5.5		±1	±10	µA	$V_{IN} = 5.5V, GND$		
I_{OFF}	Power Off Leakage Current	0.0		1	10	µA	V_{IN} or $V_{OUT} = 5.5V$		
I_{CC}	Quiescent Supply Current	5.5		2.0	20	µA	$V_{IN} = 5.5V, GND$		

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	NC7SZ38			NC7SZ38			Units	Conditions	Fig. No.			
			T _A = +25°C			T _A = -40°C to +85°C								
			Min	Typ	Max	Min	Max							
t _{PZL}	Propagation Delay	1.8	1.5	5.4	10.5	1.5	11.0	ns	C _L = 50 pF RU = 500Ω RD = 500Ω V _{IN} = 2 x V _{CC}	Figure 1, Figure 3				
		2.5 ±0.2	0.8	3.5	7.0	0.8	7.5							
		3.3 ±0.3	0.8	2.8	5.0	0.8	5.2							
		5.0 ±0.5	0.5	2.2	4.3	0.5	4.5							
t _{PLZ}	Propagation Delay	1.8	1.5	4.6	10.5	1.5	11.0	ns	C _L = 50 pF RU = 500Ω RD = 500Ω V _{IN} = 2 x V _{CC}	Figure 1, Figure 3				
		2.5 ±0.2	0.8	3.0	7.0	0.8	7.5							
		3.3 ±0.3	0.8	2.1	5.0	0.8	5.2							
		5.0 ±0.5	0.5	1.3	4.3	0.5	4.5							
C _{IN} C _{OUT}	Input Capacitance Output Capacitance	0	4					pF						
C _{PD}	Power Dissipation Capacitance	3.3	5.1					pF	(Note 2)	Figure 2				
		5.0	7.3											

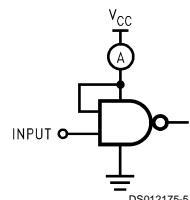
Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression:

$$I_{CCD} = (C_{PD}) (V_{CC}) (f_{IN}) + (I_{CC} \text{ static})$$



C_L includes load and stray capacitance
Input PRR = 1.0 MHz; t_w = 500 ns

FIGURE 1. AC Test Circuit



Input = AC Waveform; t_r = t_f = 1.8 ns
PRR = 10 MHz; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

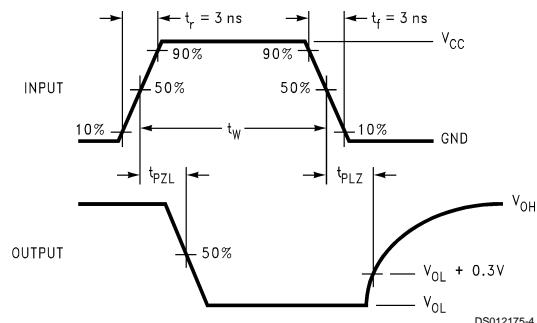
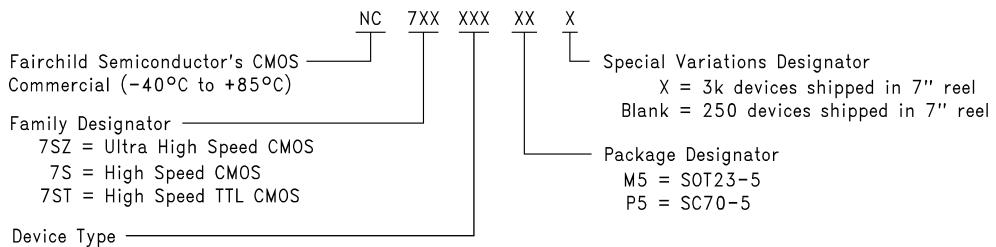


FIGURE 3. AC Waveforms

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



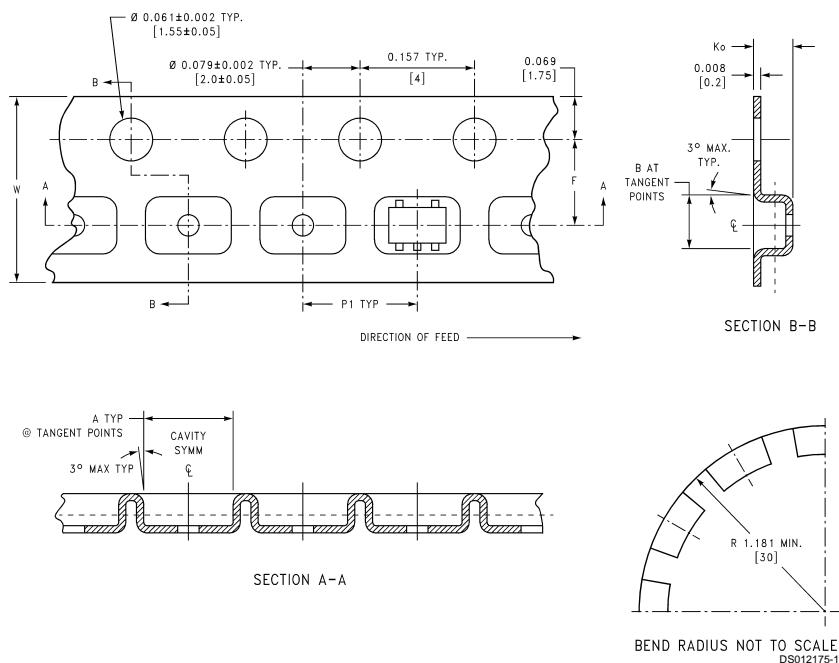
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Tape and Reel Specification

TAPE FORMAT

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
M5, P5	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	250	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed
M5X, P5X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)

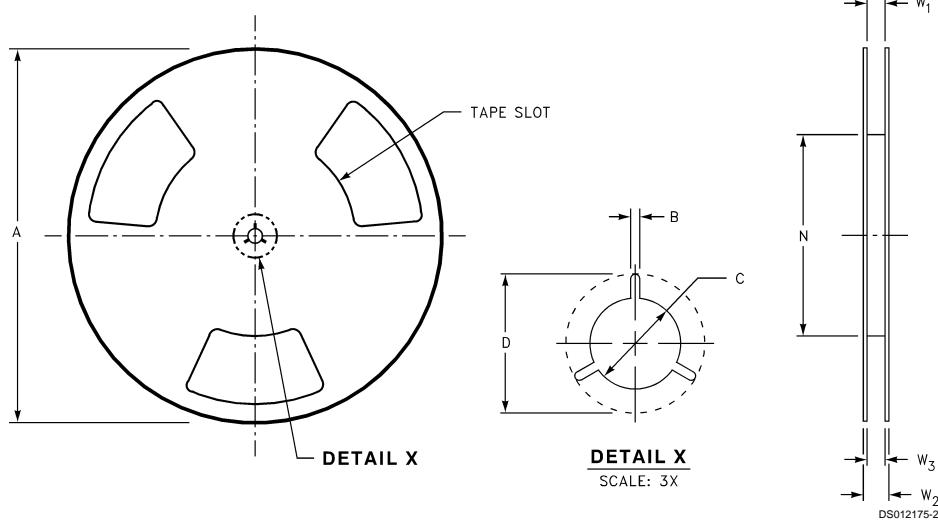


Pkg	Tape Size	DIM A	DIM B	DIM F	DIM K _o	DIM P1	DIM W
SC70-5	8 mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)
SOT23-5	8 mm	0.130 (3.3)	0.130 (3.3)	0.138 ± 0.002 (3.5 ± 0.05)	0.055 ± 0.004 (1.4 ± 0.11)	0.157 (4)	0.315 ± 0.012 (8 ± 0.3)

Tape and Reel Specification

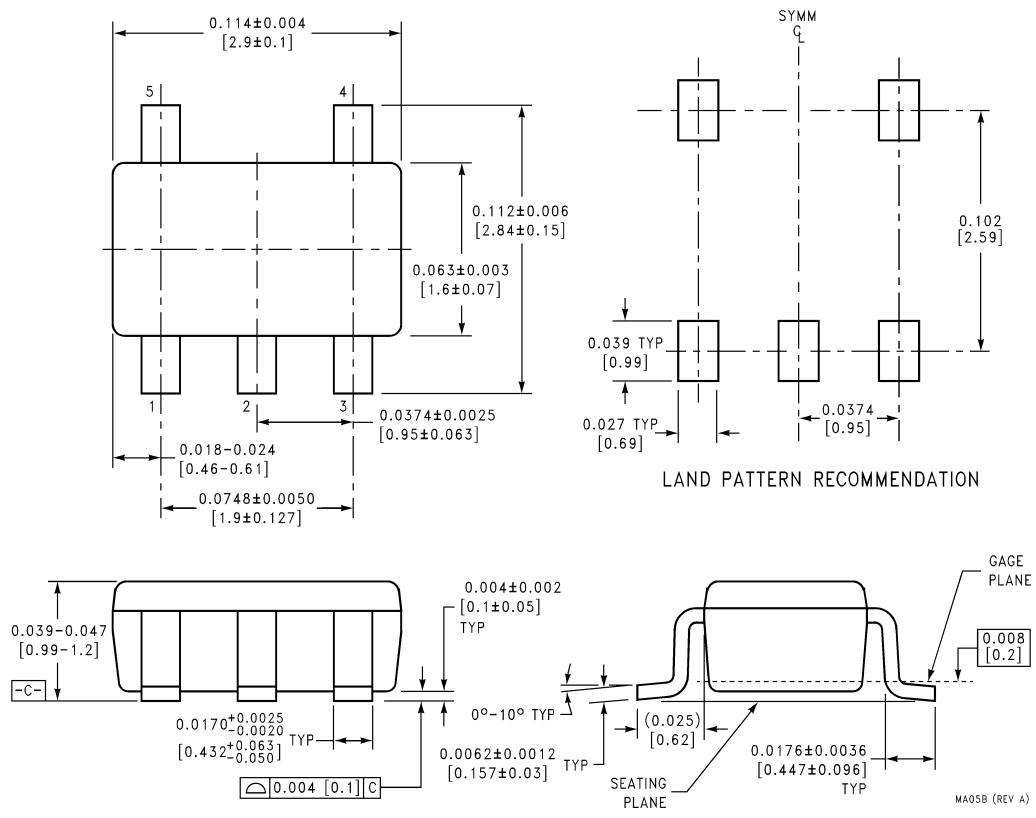
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REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 +0.059/-0.000 (8.40 +1.50/-0.00)	0.567 (14.40)	W1 +0.078/-0.039 (W1 +2.00/-1.00)

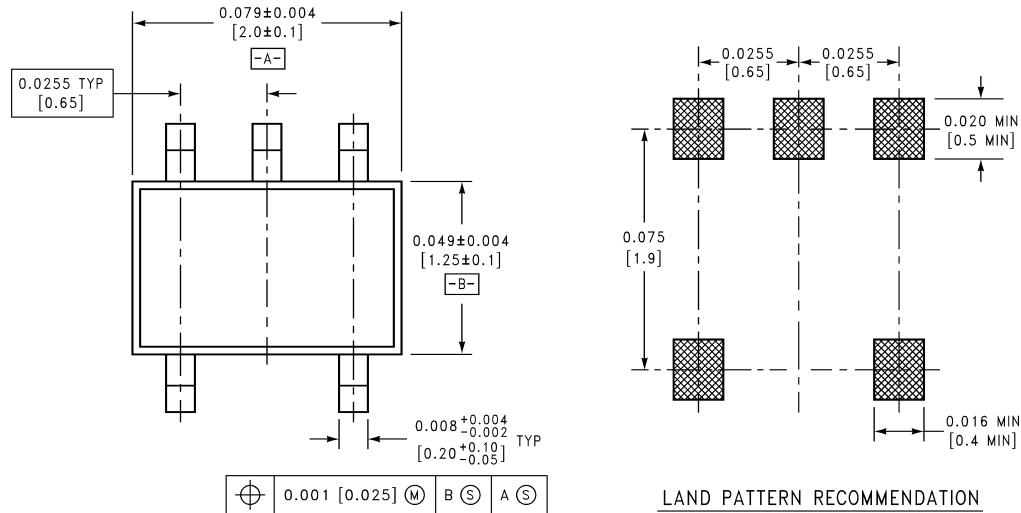
Physical Dimensions inches (millimeters) unless otherwise noted



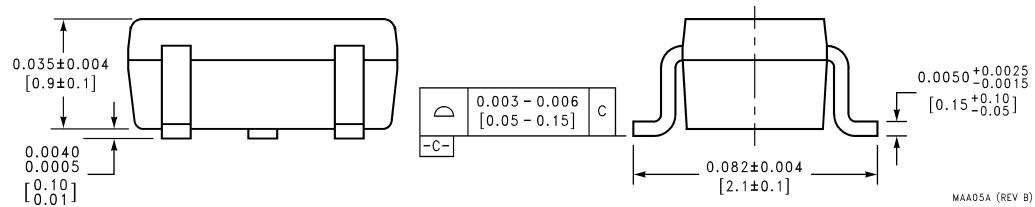
**5-Lead Molded SOT23, Enhanced Thermal
Package Number MA05B**

NC7SZ38 TinyLogic UHS 2-Input NAND Gate (Open Drain Output)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



5-Lead Molded SC70, Enhanced Thermal
Package Number MAA05A

MAA05A (REV B)

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Fairchild Semiconductor
Corporation
Americas
Customer Response Center
Tel: 1-888-522-5372

www.fairchildsemi.com

Fairchild Semiconductor
Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor
Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor
Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179