74LV541
Octal buffer/line driver; 3-state

Rev. 03 — 14 April 2009　　　　　　　　　　　　　　**Product data sheet**

1. General description

The 74LV541 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC541 and 74HCT541.

The 74LV541 has octal non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $\overline{OE}1$ and $\overline{OE}2$. A HIGH on $\overline{OE}n$ causes the outputs to assume a high-impedance OFF-state.

2. Features

■ Optimized for low voltage applications: 1.0 V to 3.6 V
■ Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
■ Typical output ground bounce < 0.8 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
■ Typical HIGH-level output voltage (V_{OH}) undershoot: > 2 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
■ ESD protection:
　◆ HBM JESD22-A114E exceeds 2000 V
　◆ MM JESD22-A115-A exceeds 200 V
■ Non-inverting outputs
■ Multiple package options
■ Specified from −40 °C to +85 °C and from −40 °C to +125 °C

3. Ordering information

Table 1.　Ordering information

Type number	Package				
	Temperature range	Name	Description		Version
74LV541N	−40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)		SOT146-1
74LV541D	−40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm		SOT163-1
74LV541DB	−40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm		SOT339-1
74LV541PW	−40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm		SOT360-1

NXP
founded by Philips

4. Functional diagram
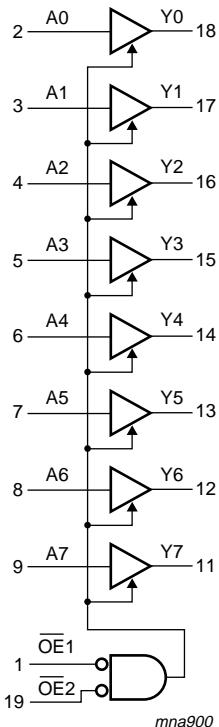
Fig 1. Logic symbol
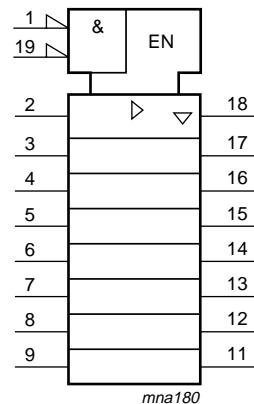
Fig 2. IEC logic symbol

5. Pinning information

5.1 Pinning
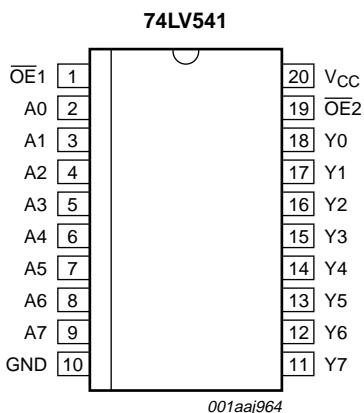
Fig 3. Pin configuration DIP20, SO20
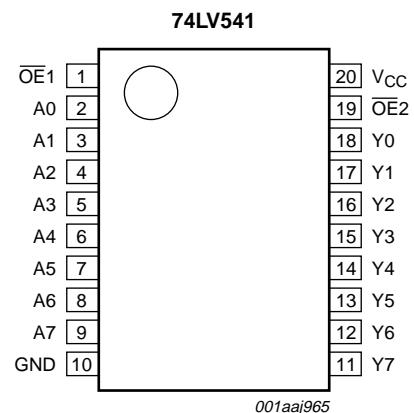
Fig 4. Pin configuration, (T)SSOP20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}1$	1	output enable input (active LOW)
A0 to A7	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
Y0 to Y7	18, 17, 16, 15, 14, 13, 12, 11	data output
$\overline{OE}2$	19	output enable input (active LOW)
V_{CC}	20	supply voltage

6. Functional description

Table 3. Functional table[1]

Control		Input	Output
$\overline{OE}1$	$\overline{OE}2$	An	Yn
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+4.6	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	50	mA
I_O	output current	$V_O = -0.5$ V to ($V_{CC} + 0.5$ V)		-	35	mA
I_{CC}	supply current			-	70	mA
I_{GND}	ground current			−70	-	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2]			
		DIP20		-	750	mW
		SO20, SSOP20, TSSOP20		-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP20 packages: above 70 °C the value of P_{tot} derates linearly with 12 mW/K.
     For SO20 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
     For (T)SSOP20 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage[1]		1.0	3.3	3.6	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		−40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.0 V to 2.0 V	-	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V	-	-	200	ns/V
		V_{CC} = 2.7 V to 3.6 V	-	-	100	ns/V

[1] The static characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 3.6 V, but LV devices are guaranteed to function down to V_{CC} = 1.0 V (with input levels GND or V_{CC}).

9. Static characteristics

Table 6. Static characteristics
At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V_{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V_{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		$I_O = -100$ μA; V_{CC} = 1.2 V	-	1.2	-	-	-	V
		$I_O = -100$ μA; V_{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		$I_O = -100$ μA; V_{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		$I_O = -100$ μA; V_{CC} = 3.0 V	2.8	3.0	-	2.8	-	V
		$I_O = -8$ mA; V_{CC} = 3.0 V	2.4	2.82	-	2.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		$I_O = 100$ μA; V_{CC} = 1.2 V	-	0	-	-	-	V
		$I_O = 100$ μA; V_{CC} = 2.0 V	-	0	0.2	-	0.2	V
		$I_O = 100$ μA; V_{CC} = 2.7 V	-	0	0.2	-	0.2	V
		$I_O = 100$ μA; V_{CC} = 3.0 V	-	0	0.2	-	0.2	V
		$I_O = 8$ mA; V_{CC} = 3.0 V	-	0.2	0.40	-	0.50	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 3.6 V	-	-	1.0	-	1.0	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; V_{CC} = 3.6 V	-	-	5	-	10	μA

74LV541_3

Product data sheet **Rev. 03 — 14 April 2009** 4 of 15

Table 6. **Static characteristics** *…continued*
At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 3.6 V	-	-	20	-	160	µA
ΔI_{CC}	additional supply current	per input; V_I = V_{CC} − 0.6 V; V_{CC} = 2.7 V to 3.6 V	-	-	500	-	850	µA
C_I	input capacitance		-	3.5	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. **Dynamic characteristics**
Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 7.

Symbol	Parameter	Conditions		−40 °C to +85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	An to Yn; see Figure 5	[2]						
		V_{CC} = 1.2 V		-	60	-	-	-	ns
		V_{CC} = 2.0 V		-	20	39	-	46	ns
		V_{CC} = 2.7 V		-	15	29	-	34	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	[3]	-	10	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	11	23	-	27	ns
t_{en}	enable time	$\overline{OE}$n to Yn; see Figure 6	[2]						
		V_{CC} = 1.2 V		-	100	-	-	-	ns
		V_{CC} = 2.0 V		-	34	65	-	77	ns
		V_{CC} = 2.7 V		-	25	48	-	56	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	19	38	-	45	ns
t_{dis}	disable time	$\overline{OE}$n to Yn; see Figure 6	[2]						
		V_{CC} = 1.2 V		-	100	-	-	-	ns
		V_{CC} = 2.0 V		-	36	66	-	78	ns
		V_{CC} = 2.7 V		-	27	48	-	58	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	21	39	-	47	ns

74LV541_3

Product data sheet **Rev. 03 — 14 April 2009** 5 of 15

Table 7.   Dynamic characteristics …continued

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 7.

| Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC} [4]	-	37	-	-	-	pF

[1]   All typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

  t_{en} is the same as t_{PZL} and t_{PZH}.

  t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3]   Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V).

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

  $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

  f_i = input frequency in MHz, f_o = output frequency in MHz

  C_L = output load capacitance in pF

  V_{CC} = supply voltage in Volts

  N = number of inputs switching

  $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11. Waveforms
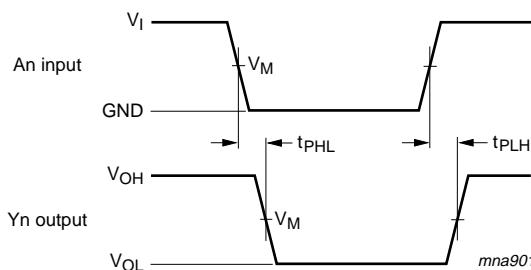
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

**Fig 5.   Propagation delay input (An) to output (Yn)**
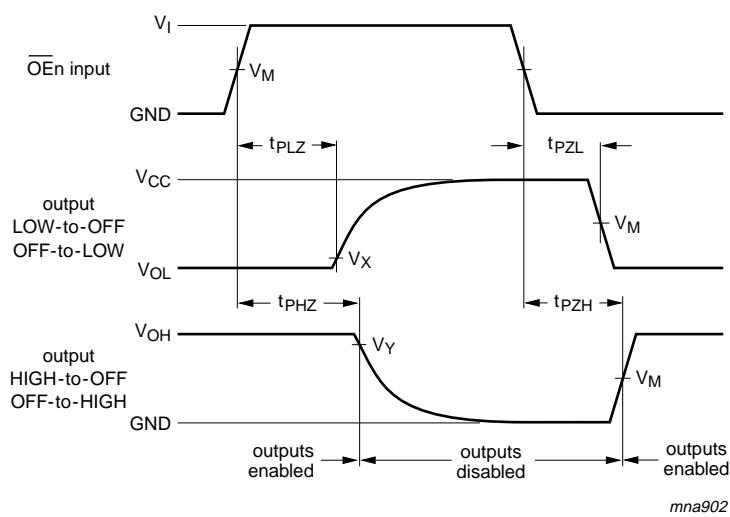
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6.   enable and disable times

Table 8.   Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
< 2.7 V	0.5V_{CC}	0.5V_{CC}	V_{OL} + 0.1V_{CC}	V_{OH} − 0.1V_{CC}
2.7 V to 3.6 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V
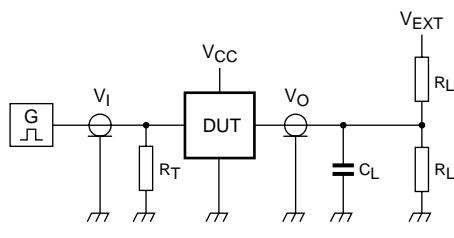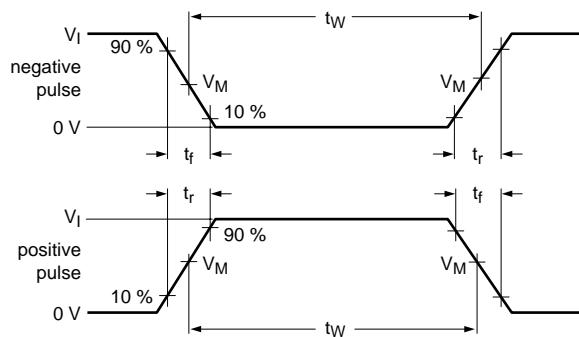
Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 7. **Test circuit for measuring switching times**

Table 9. **Test data**

Supply voltage	Input			Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}	
< 2.7 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	open	GND	$2V_{CC}$	
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns	15 pF, 50 pF	1 kΩ	open	GND	$2V_{CC}$	

12. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)   **SOT146-1**
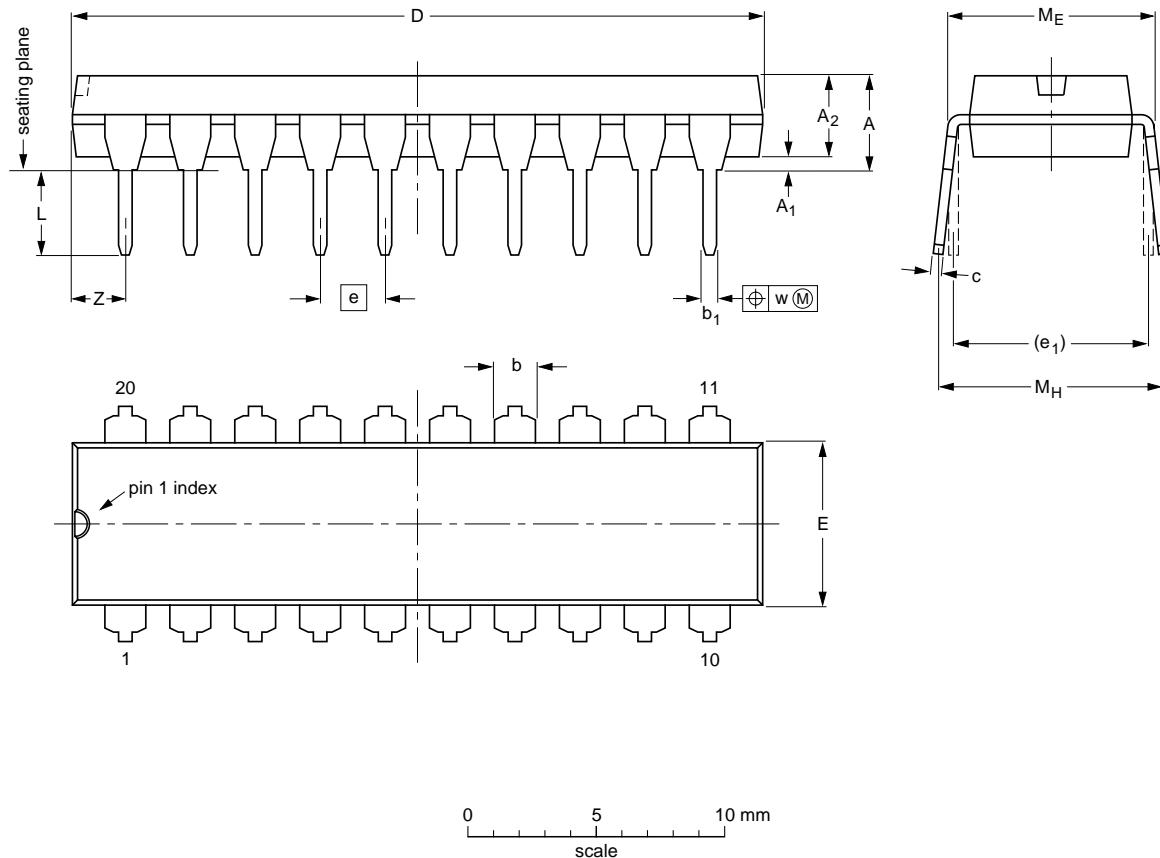
DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁ min.	A₂ max.	b	b₁	c	D [1]	E [1]	e	e₁	L	M_E	M_H	w	Z [1] max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT146-1		MS-001	SC-603			~~99-12-27~~ 03-02-13

Fig 8.   Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁	A₂	A₃	b_p	c	D⁽¹⁾	E⁽¹⁾	e	H_E	L	L_p	Q	v	w	y	Z⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT163-1 (SO20)

**SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm**   **SOT339-1**

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				~~99-12-27~~ 03-02-19
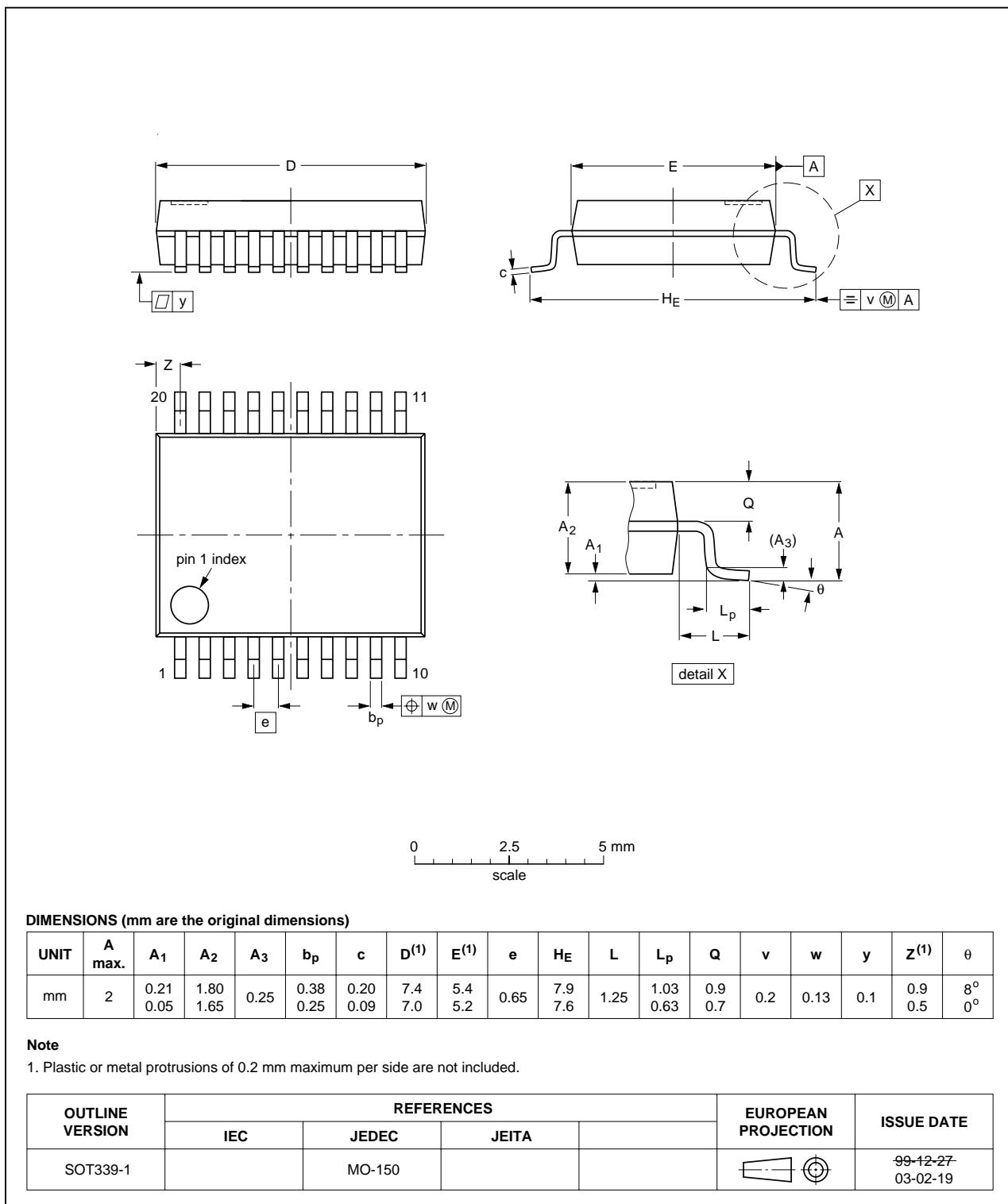
Fig 10. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A1	A2	A3	bp	c	D(1)	E(2)	e	HE	L	Lp	Q	v	w	y	Z(1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19
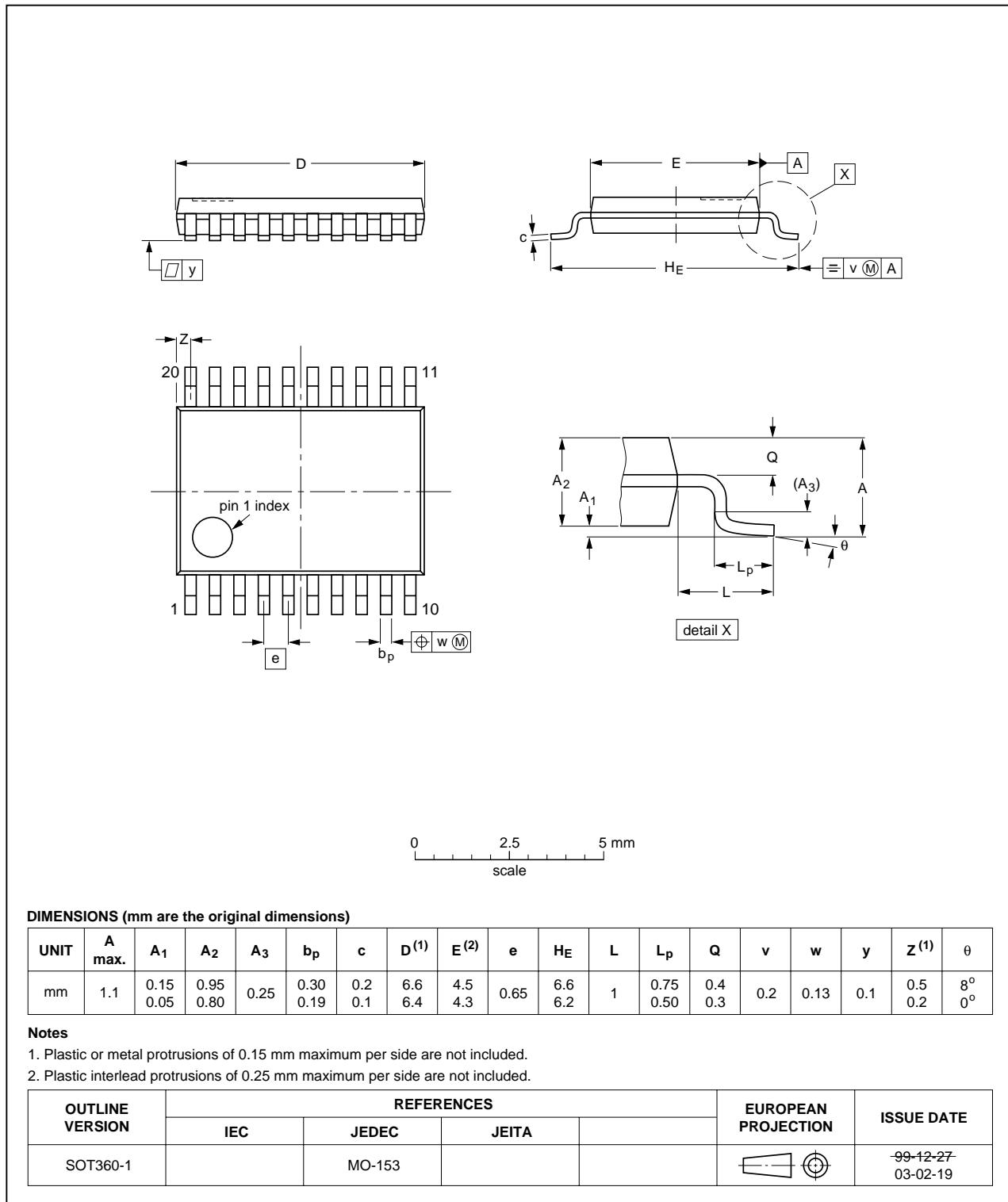
Fig 11. Package outline SOT360-1 (TSSOP20)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV541_3	20090414	Product data sheet	-	74LV541_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name when appropriate.			
74LV541_2	19980610	Product specification	-	74LV541_1
74LV541_1	19970304	Product specification	-	-

74LV541_3

Product data sheet **Rev. 03 — 14 April 2009** **13 of 15**

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

15.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

74LV541_3

Product data sheet **Rev. 03 — 14 April 2009** **14 of 15**

17. Contents

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information: