

3.125 Gbps 2x2 LVDS Crosspoint Switch with Transmit Pre-emphasis and Receive Equalization

DS25CP102 Evaluation Kit

USER MANUAL

Part Number: DS25CP102EVK NOPB

For the latest documents concerning these products and evaluation kit, visit lvds.national.com.
Schematics and gerber files are also available at lvds.national.com.

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Overview

The DS25CP102EVK is an evaluation kit designed for demonstrating performance of the DS25CP102, a 3.125 Gbps 2x2 LVDS Crosspoint Switch with transmit pre-emphasis and receive equalization. The evaluation kit is comprised of the DS25CP102 with its associated input and output SMA connectors and jumpers to manually configure the switch. In addition, the EVJ features three FR4 striplines (14 (~35), 28 (~75) and 42 (~105) inches (cm) in length) for exercising device's signal conditioning features (pre-emphasis and equalization).

The purpose of this document is to familiarize the user with the DS25CP102EVK, to suggest test setup procedures and instrumentation to test the device optimally, and to guide the user through some typical measurements that demonstrate the performance of the DS25CP102 in typical applications.

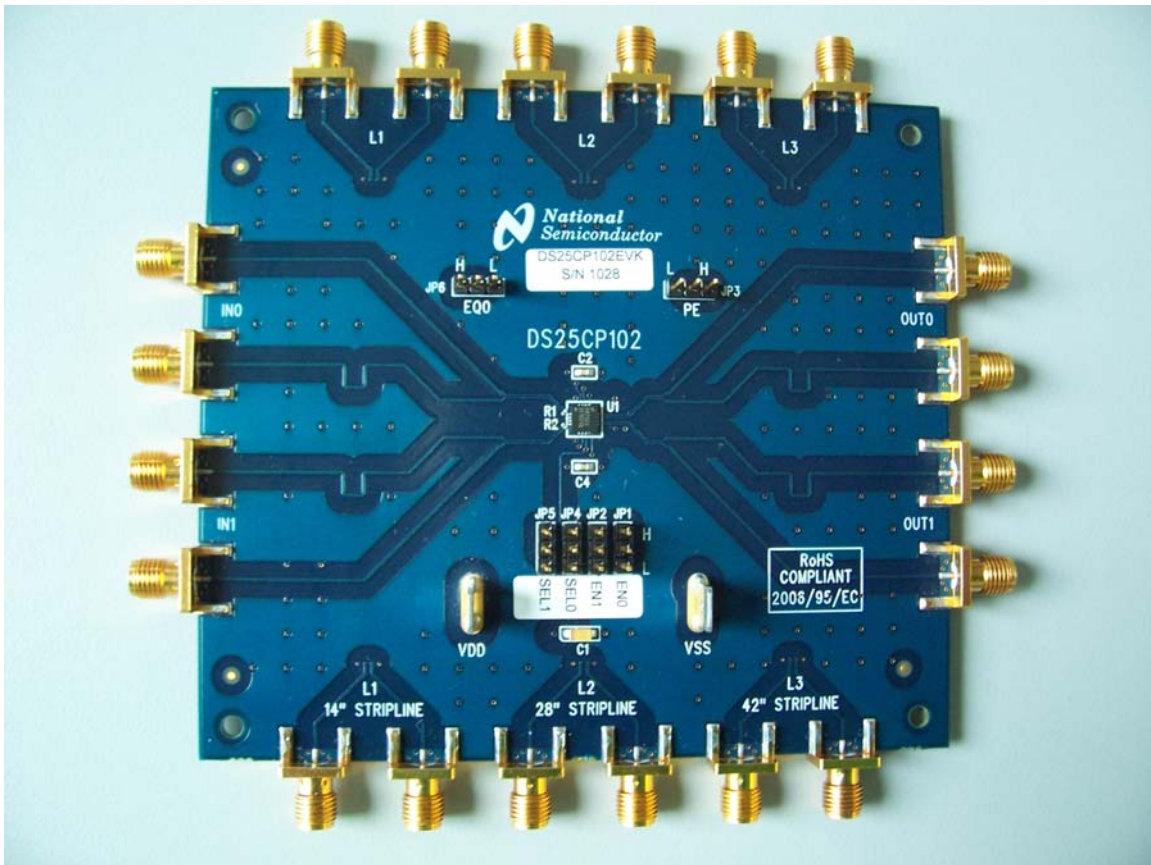


Figure 1. Photo of the DS25CP102EVK

Description

Figure 2 shows the top layer drawing of the PCB with the silkscreen annotations. The 4.5 by 4.0 inch, four-layer PCB is designed to evaluate the functions of the DS25CP102.

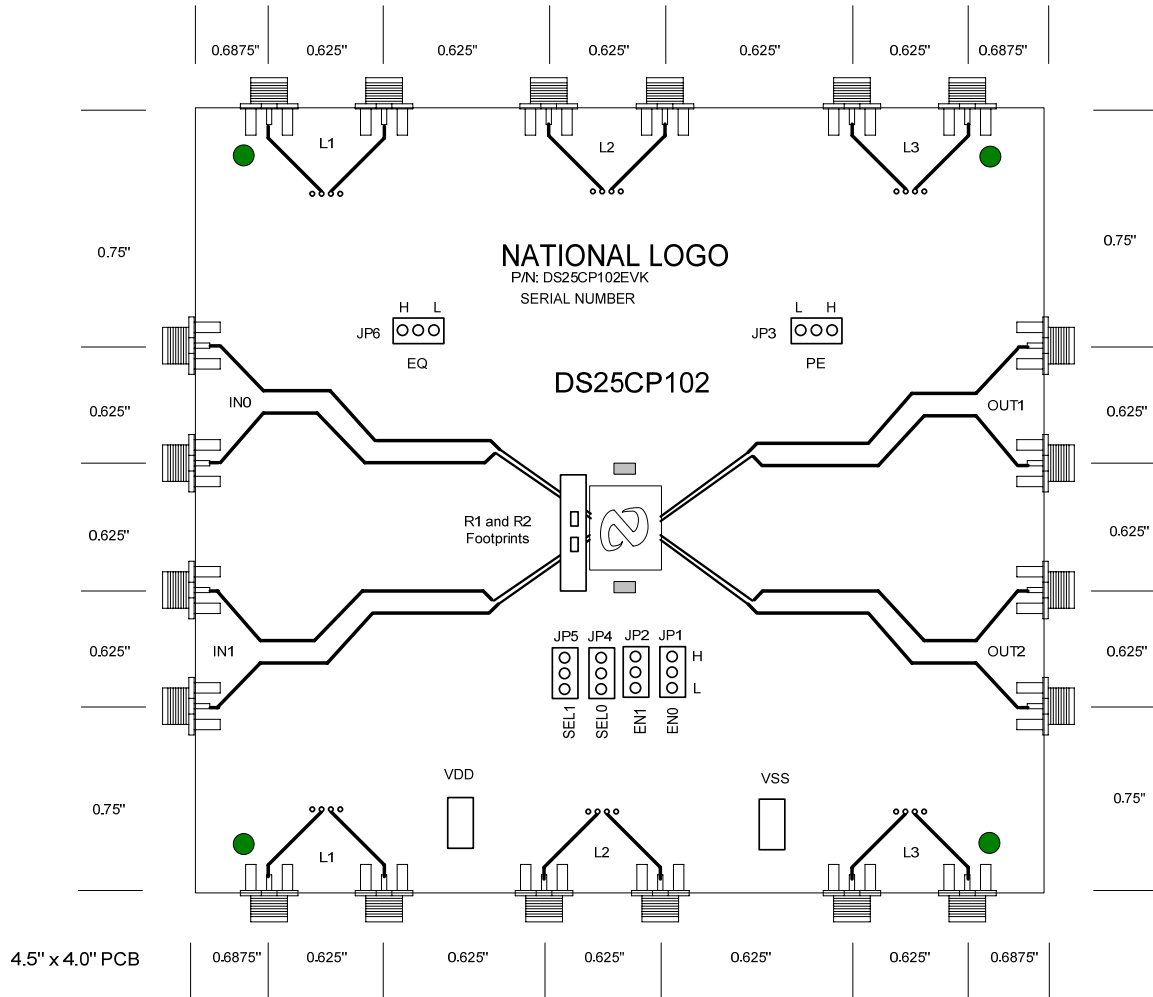


Figure 2. Top Layer DS25CP102EVK

Evaluation

This section provides recommended test setup procedure for the device evaluation. Figure 3 depicts a typical setup and instrumentation you may use for the device evaluation.

1. Configure the test setup as shown in Figure 3.
2. Set and enable the desired INn to OUTn drivers by selecting SEL0, SEL1, EN0 and EN1 according to Tables 1 – 2.
3. Apply + supply (3.3V typical) to the VDD and – supply (ground) to the VSS connectors.
4. Set desired pre-emphasis and/or equalization levels according to Tables 3 – 4.
5. Connect a signal source (signal generator, data source, or an LVDS driver) to the desired INn inputs on the board and adjust the signal parameters (VOH, VOL, VCM) so that they comply with the device input recommendations.
6. Connect an oscilloscope to the selected OUTn outputs and view the output signals with an oscilloscope with the analog bandwidth of at least 5 GHz.

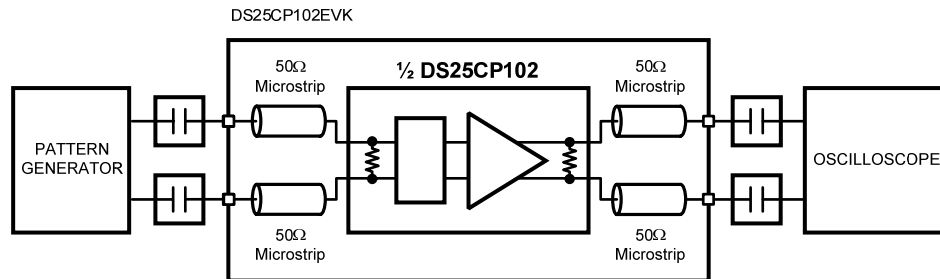


Figure 3. DS25CP102 Test Setup Example

Switch Configuration Truth Tables

SEL1	SEL0	OUT1	OUT0
0	0	IN0	IN0
0	1	IN0	IN1
1	0	IN1	IN0
1	1	IN1	IN1

Table 1. Switch Configuration Truth Table

EN1	EN0	OUT1	OUT0
0	0	Disabled	Disabled
0	1	Disabled	Enabled
1	0	Enabled	Disabled
1	1	Enabled	Enabled

Table 2. Output Enable Truth Table

OUTPUTS OUT0 and OUT1	
CONTROL Pin PE State	Pre-emphasis Level
0	OFF
1	ON

Table 3. Transmit Pre-emphasis Truth Table

OUTPUTS OUT0 and OUT1	
CONTROL Pin PE State	Pre-emphasis Level
0	OFF
1	ON

Table 4. Receive Equalization Truth Table

Typical Performance

This section of the User Manual shows a typical eye diagram you can expect to see when evaluating the DS25CP102EVK.

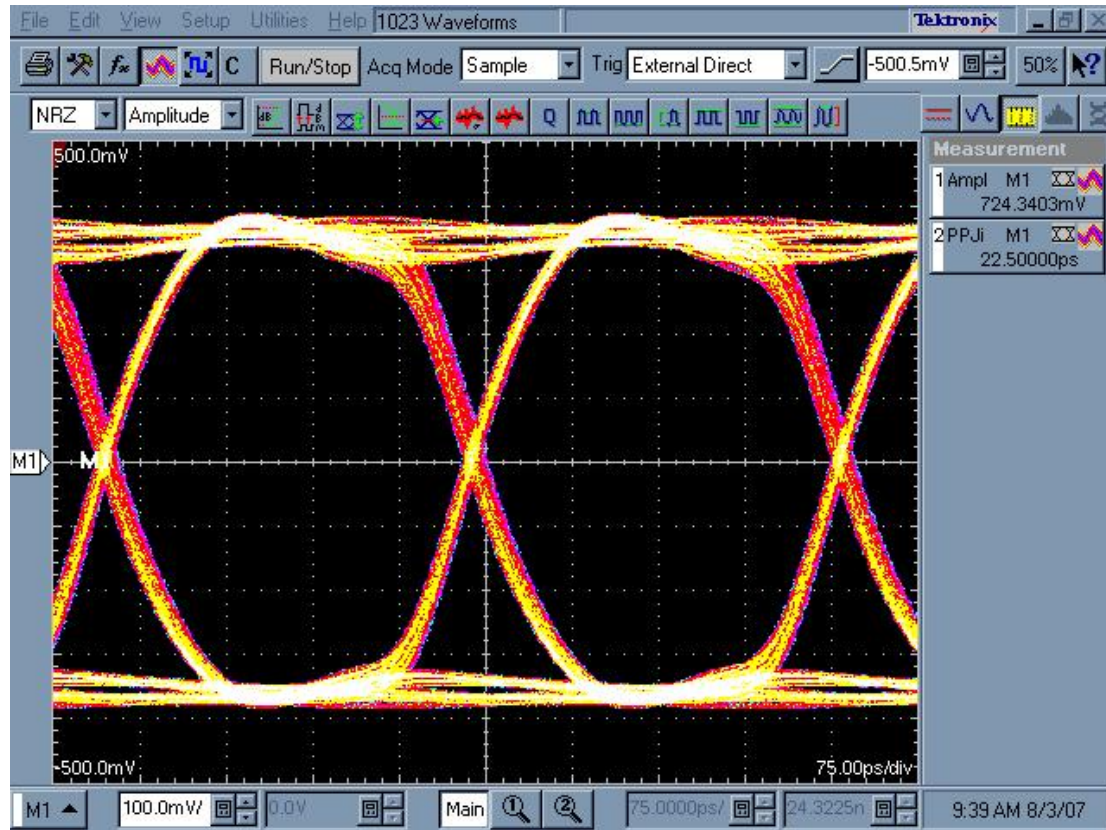
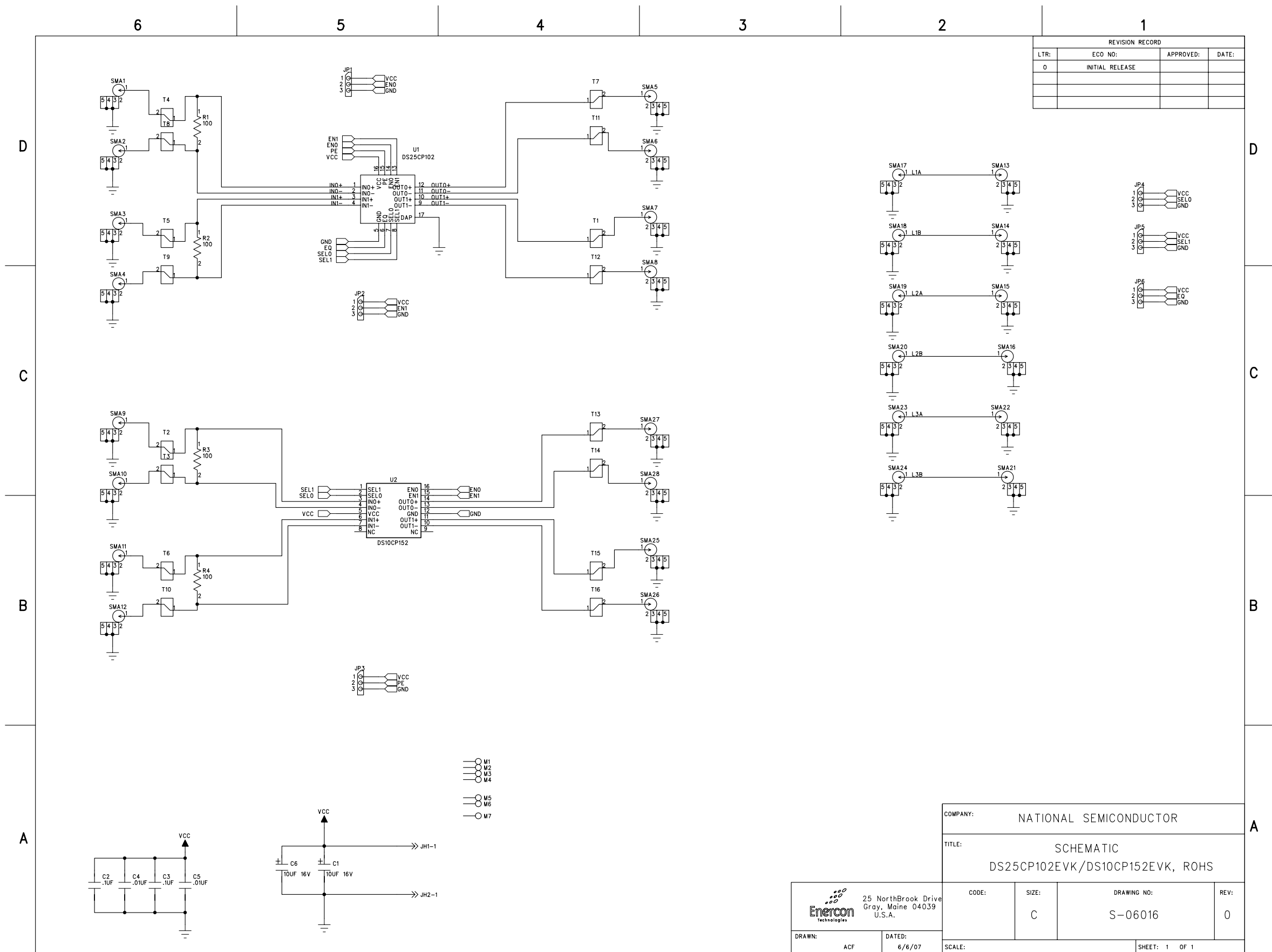


Figure 4. DS25CP102 3.125 Gbps NRZ PRBS-7 Output Eye Diagram



ENERCON - BILL OF MATERIALS

TITLE:

**NATIONAL SEMICONDUCTOR
PCBA, DS25CP102EVK, ROHS**PL Number: Z3102-01
Rev: 1
Rev By: AFRev Date:
10/9/2007PL Status:
ReleasedMain Product:
PCBA, DS25CP102EVK

Responsible Eng/Mgr:

Creator:

Arlene Fox

Creation Date:
6/7/2007

Item	Part Type	Part Number/Value	Mfg	NoSub	Description	Qty	SMT	Ref Des	Notes	Rev
1	PCB	P-06015R1	ENERCON		DS25CP102: 4.00x4.50x.060in, 8 layer	1			Bd: (101.60x 114.30mm) Panel: (4.50x 8.10in) (114.30x205.74mm) 2 bds/panel	1
2										
3	IC	DS25CP102TSQ	NAT		3.125 Gbps LVDS Crosspoint Switch, LLP16, Pb-Free	1	X	U1	Customer Supplied	0
4										
5	CAP	06035C103KAT	AVX		.01µF, 50V, ±10%, 0603, Ceramic, X7R, Pb-Free	1	X	C4		0
	<ALT>	C0603C103K5RAC	KEMET		.01µF, 50V, ±10%, 0603, Ceramic, X7R, Pb-Free					
	<ALT>	ECJ-1VB1H103K	PANA		.01µF, 50V, ±10%, 0603, Ceramic, X7R, Pb-Free					
6	CAP	0603YC104KAT	AVX		.1µF, 16V, ±10%, 0603, Ceramic, X7R, Pb- Free	1	X	C2		0
	<ALT>	C0603C104K4RAC	KEMET		.1µF, 16V, ±10%, 0603, Ceramic, X7R, Pb- Free					
	<ALT>	ECJ-1VB1C104K	PANA		.1µF, 16V, ±10%, 0603, Ceramic, X7R, Pb- Free					
7	CAP	TAJA106K016	AVX		10µF, 16V, ±10%, A-Case, Tantalum, Pb- Free	1	X	C1		0
	<ALT>	T491A106K016AT	KEMET		10µF, 16V, ±10%, A-Case, Tantalum, Pb- Free					
8										
9	CONN	1287	KEYSTONE		Faston, Male, .250", Pb-Free	2		JH1-2	VDD, VSS	0
10	CONN	142-0701-851	EMERSON		SMA, Jack Receptacle, 50 OHM, Pb-Free	20		SMA1-8,13-24		0
11	CONN	TSW-103-07-G-S	SAMTEC		Header, 3p, Male, .100"sp, Gold, Pb-Free	6		JP1-6		0
12										
13	STENCL	T-06019R0	ENERCON		STENCIL FABRICATION, TOP, DS25CP102/DS10CP152EVK	1				0
14										
15	REF	C-06017R1	ENERCON		FABRICATION DWG, DS25CP102/DS10CP152EVK					1

ENERCON - BILL OF MATERIALS		TITLE: NATIONAL SEMICONDUCTOR PCBA, DS25CP102EVK, ROHS	PL Number: Z3102-01		Rev: 1	Rev By: AF	Rev Date: 10/9/2007	PL Status: Released
Main Product: PCBA, DS25CP102EVK			Responsible Eng/Mgr:			Creator: Arlene Fox		Creation Date: 6/7/2007

Item	Part Type	Part Number/Value	Mfg	NoSub	Description	Qty	SMT	Ref Des	Notes	Rev
16	REF	C-06018R0	ENERCON		PALLET DWG, DS25CP102/DS10CP152EVK					0
17	REF	S-06016R0	ENERCON		SCHEMATIC, DS25CP102/DS10CP152EVK					0
18										
19										

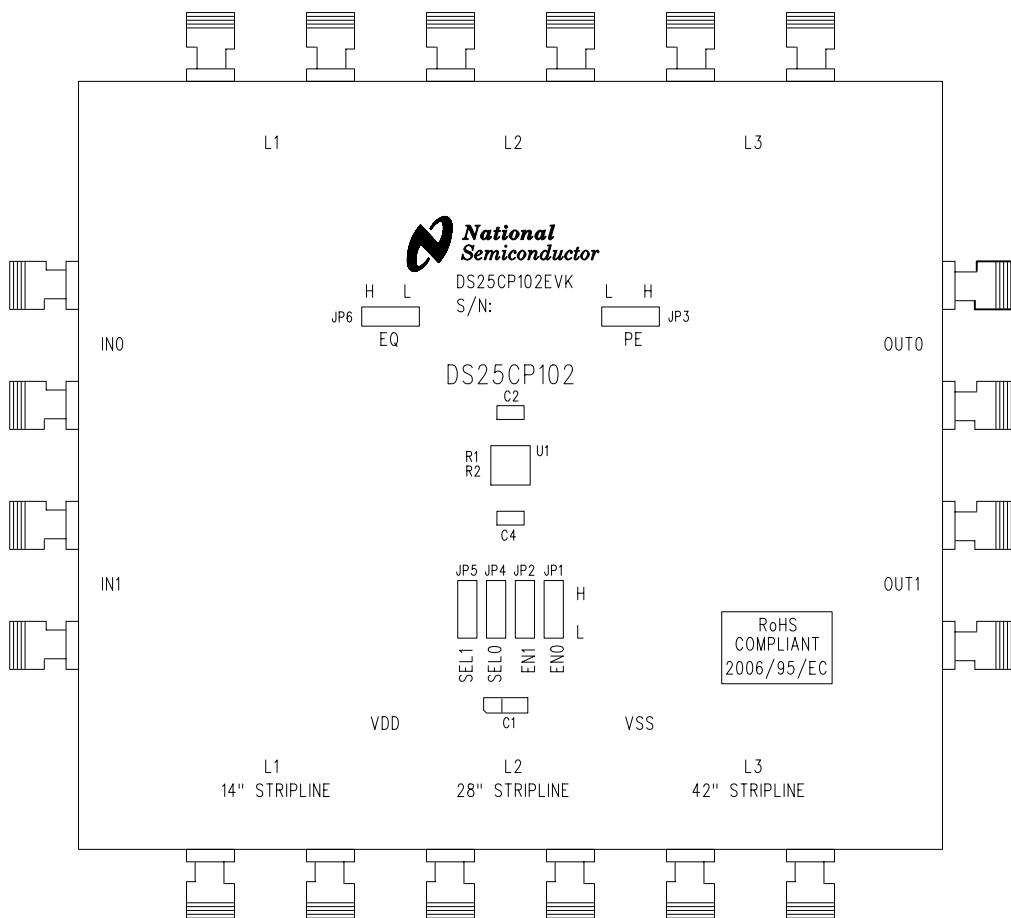
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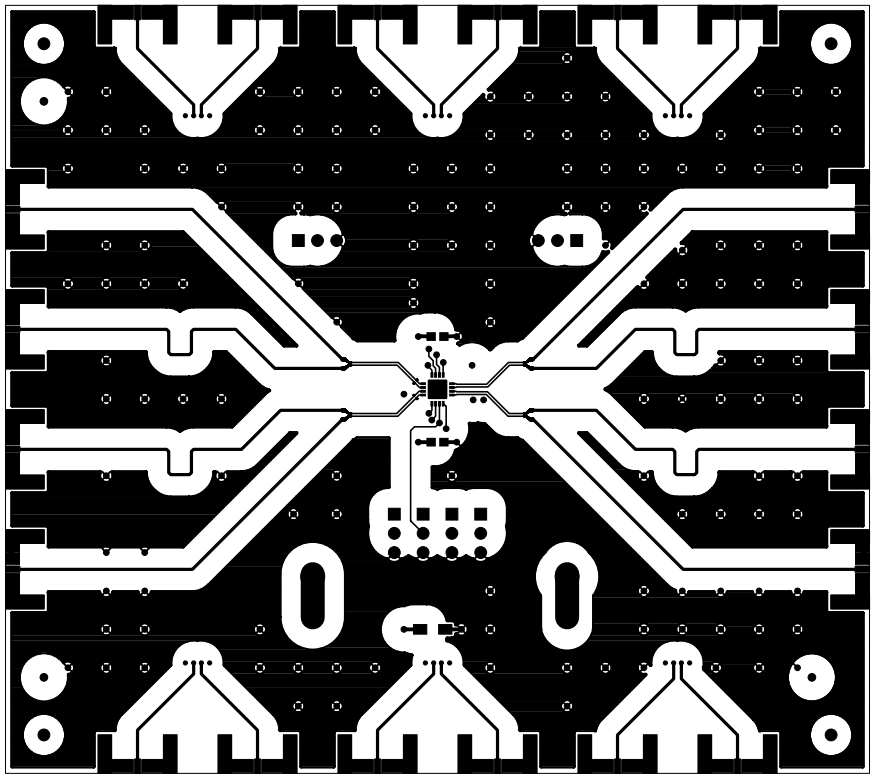
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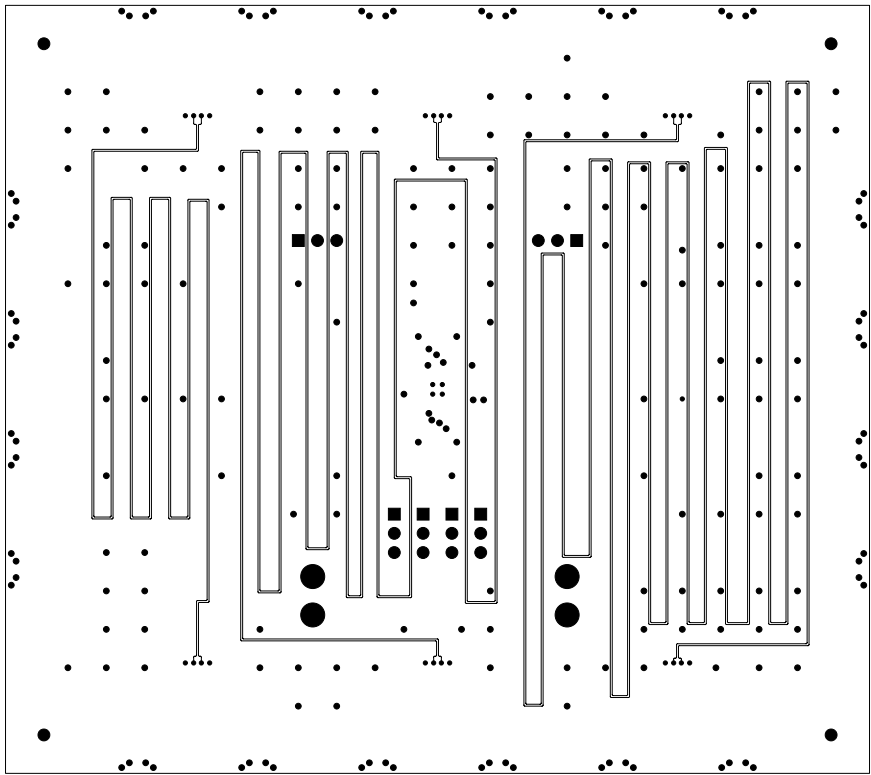
R1,2

C3,5,6

SMA9,10,11,12,25,26,27,28







LAYER 6 SIGNAL

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