HIGH VOLTAGE MONOLITHIC IC

ECN3290TF/PL/FN

8–Channel High Voltage Analog Switch IC

The ECN3290 is an 8-Channel High Voltage Analog Switching IC manufactured in a DI (Dielectric Isolation) process. DI technology delivers Latch-Up free operation.
High voltage and low ON-resistance MOS switches are used as output devices controlled by a 5V signal. The ECN3290 is most suited to Ultrasound Imaging applications.

Functions

- 8-Integrated High Voltage, Low ON-resistance Analog Switches
- Latch-Up Free CMOS built in a Dielectric Isolated Process
- DC to greater than 10MHz Analog Signal Bandwidth
- Superior Data Capture Timing
- Superior Data Clock Frequency (f_{CLK} : 10MHz max.)
- Superior Data Out Availability (t_{DO} : 85ns max.)

Features

- Small Signal ON-resistance (R_{ONS}): 20Ω typical (V_{PP}=100V, V_{NN}=-100V)
- Large Signal ON-resistance (R_{ONL}): 20Ω typical (V_{PP}=100V, V_{NN}=-100V)
- Extremely Low DC Offset Switch Voltage (DC_{OFF}/DC_{ON}:10mV typ.)
- Integrated 8-bit Shift Register controls 8-Output Analog Switches
- 28-lead PLCC, 48-lead TQFP and 28-QFN packages

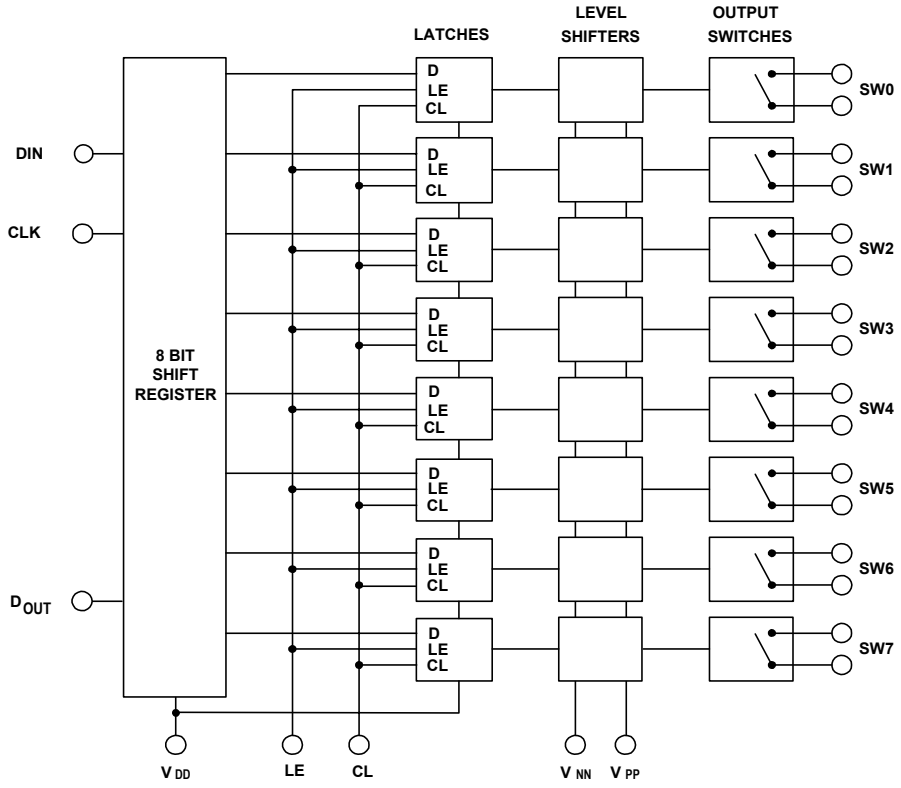

Fig.1 Logic / Block Diagram

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1. Absolute Maximum Ratings

No.	Item	Symbol	Terminal	Values	Unit	Note	
1	Logic power supply voltage	V_{DD}	V_{DD}	-0.5 to +7	V	Ta=25°C	
2	V_{PP}-V_{NN} supply voltage	—	V_{PP}, V_{NN}	220	V	Ta=25°C	
3	V_{PP} Positive high voltage supply	V_{PP}	V_{PP}	-0.5 to V_{NN}+200	V	Ta=25°C	
4	V_{NN} Negative high voltage supply	V_{NN}	V_{NN}	+0.5 to -200	V	Ta=25°C	
5	Logic input voltages	V_{DD}	DIN, CLK, CL, LE	-0.5 to V_{DD}+0.3	V	Ta=25°C	
6	Analog signal range	—	SW0 to SW7	V_{NN} to V_{PP}	V	Ta=25°C	
7	Operating junction temperature	Tjop	-	-20 to +125	°C		
8	Storage temperature	Tstg	-	-65 to +150	°C		
9	Power dissipation	Pw	-	1.0	W	TQFP48	Ta=70°C
				1.2	W	QFJ28, QFN28	

2. Recommended Operating Conditions

Note: Please operate within the limit of the following operating conditions.

No.	Items	Symbol	Recommended Value			Unit	Comment
			Min	Typ	Max		
1	Logic power supply voltage	V_{DD}	4.5	-	5.5	V	
2	Positive high voltage supply	V_{PP}	40	-	V_{NN} +200	V	
3	Negative high voltage supply	V_{NN}	-40	-	-160	V	
4	High-level input voltage	V_{IH}	V_{DD} -1.5	-	V_{DD}	V	
5	Low-level input voltage	V_{IL}	0	-	1.5	V	
6	Analog signal voltage peak to peak	V_{SIG}	V_{NN} +10	-	V_{PP} -10	V	
7	Operating Free-air Temperature	T_A	0	-	70	°C	
8	Switching frequency	fsw	-	-	50	KHz	Duty Cycle=50%
9	Set up time for LE	tSD	75	-	-	ns	
10	Pulse width of LE	tWLE	75	-	-	ns	
11	Time width of CL	tWCL	60	-	-	ns	
12	Set up time DATA to Clock	tSU	10	-	-	ns	
13	Hold time DATA from Clock	th	20	-	-	ns	
14	Maximum VSIG Slew Rate	dV/dt	-	-	30	V/ns	

Important:

1. Power supply ON sequence (Turn ON) should be V_{DD} ON, V_{PP} ON then V_{NN} ON.
2. Power OFF sequence (Turn OFF) should be V_{NN} OFF, V_{PP} OFF then V_{DD} OFF.

3. Electrical Characteristics

3.1 DC Characteristics (Ta = 25°C VDD = 5V)

No.	Item	Symbol	Specification			Unit	Test Conditions	
			Min	Typ	Max			
1	Small Signal Switch (ON) Resistance	R_{ONS}	-	26	38	Ω	I_{SIG} = 5mA	V_{PP} = 40V, V_{NN} = -160V
			-	22	27		I_{SIG} = 200mA	
			-	22	27		I_{SIG} = 5mA	V_{PP} = 100V, V_{NN} = -100V
			-	18	24		I_{SIG} = 200mA	
			-	20	25		I_{SIG} = 5mA	V_{PP} = 160V, V_{NN} = -40V
			-	16	25		I_{SIG} = 200mA	
2	Small Signal Switch (ON) Resistance Matching	ΔR_{ONS}	-	5	20	%	I_{SW} = 5mA, V_{PP} = 100V, V_{NN} = -100V	
3	Large Signal Switch (ON) Resistance	R_{ONL}	-	20	-	Ω	V_{PP} = 100V V_{NN} = -100V	I_{SIG} = 1A
4	Switch Off Leakage Per Switch	I_{SOL}	-	1.0	10	μA	$V_{SIG}=V_{PP}$-10V, or V_{NN}+10V	
5	DC offset Switch (OFF)	DCOFF	-	10	100	mV	R_L=100kΩ	
6	DC offset Switch (ON)	DCON	-	10	100	mV	R_L=100kΩ	
7	Positive HV Supply Current	I_{PPQ1}	-	10	50	μA	All SWs OFF	
8	Negative HV Supply Current	I_{NNQ1}	-	-10	-50	μA	All SWs OFF	
9	Positive HV Supply Current	I_{PPQ2}	-	10	50	μA	All SWs ON, ISW=5mA	
10	Negative HV Supply Current	I_{NNQ2}	-	-10	-50	μA	All SWs ON, ISW=5mA	
11	I_{PP} Supply Current	I_{PP}	-	-	7.0	mA	V_{PP} = 40V, V_{NN} = -160V	50kHz Output Switching Frequency without load
			-	-	5.0		V_{PP} = 100V, V_{NN} = -100V	
			-	-	5.0		V_{PP} = 160V, V_{NN} = -40V	
12	I_{NN} Supply Current	I_{NN}	-		7.0	mA	V_{PP} = 40V, V_{NN} = -160V	50kHz Output Switching Frequency without load
			-		5.0		V_{PP} = 100V, V_{NN} = -100V	
			-		5.0		V_{PP} = 160V, V_{NN} = -40V	
13	Logic Supply Avg. Current	IDD	-		4.0	mA	f_{CLK} = 5MHz, V_{DD} = 5.0V	
14	Logic Supply Quiescent Current	IDDQ	-		10	μA		
15	Data Out Source Current	ISOR	0.45	0.70		mA	V_{OUT} = V_{DD} -0.7V	
16	Data Out Sink Current	ISINK	0.45	0.70		mA	V_{OUT} = 0.7V	

3.2 AC Characteristics (Ta=25°C VDD=5V)

No.	Item	Symbol	Specification			Unit	Test Conditions
			Min	Typ	Max		
1	SW Turn On time	t_{ON}			5.0	μs	V_{SIG} = V_{PP}-10V, R_L = 10kΩ
2	SW Turn Off time	t_{OFF}			5.0	μs	V_{SIG} = V_{PP}-10V, R_L = 10kΩ
3	Clock Frequency	f_{CLK}	-	-	10	MHz	50% duty cycle, f_{Data}=f_{CLK}/2
4	Clock Delay Time to Data Out	t_{DO}	30	-	85	ns	D_{OUT} terminal
5	SW Off Isolation	KO	-30	-33	-	dB	f=5MHz,1kΩ//15pF load
			-54	-60	-	dB	f=5MHz, 50Ω load
6	SW Crosstalk	K_{CR}	-54	-60	-	dB	f=5MHz, 50Ω load
7	Output Voltage Spike	$+V_{SPK}$	-	-	150	mV	V_{PP} = 40V, V_{NN} = -160V, R_L = 50Ω
		$-V_{SPK}$	-	-	-200		
		$+V_{SPK}$	-	-	150	mV	V_{PP} = 100V, V_{NN} = -100V, R_L = 50Ω
		$-V_{SPK}$	-	-	-200		
		$+V_{SPK}$	-	-	150	mV	V_{PP} = 160V, V_{NN} = -40V, R_L = 50Ω
		$-V_{SPK}$	-	-	-200		

3.3 AC Characteristics (Ta=25°C VDD=5V)

Note: The Following Items are not tested when shipped.

No.	Item	Symbol	Specification			Unit	Condition
			Min	Typ	Max		
1	Off Capacitance SW to GND	$C_{SG(OFF)}$	-	9	-	pF	0V, 1MHz
2	On Capacitance SW to GND	$C_{SG(ON)}$	-	14	-	pF	0V, 1MHz

4. Test Circuits

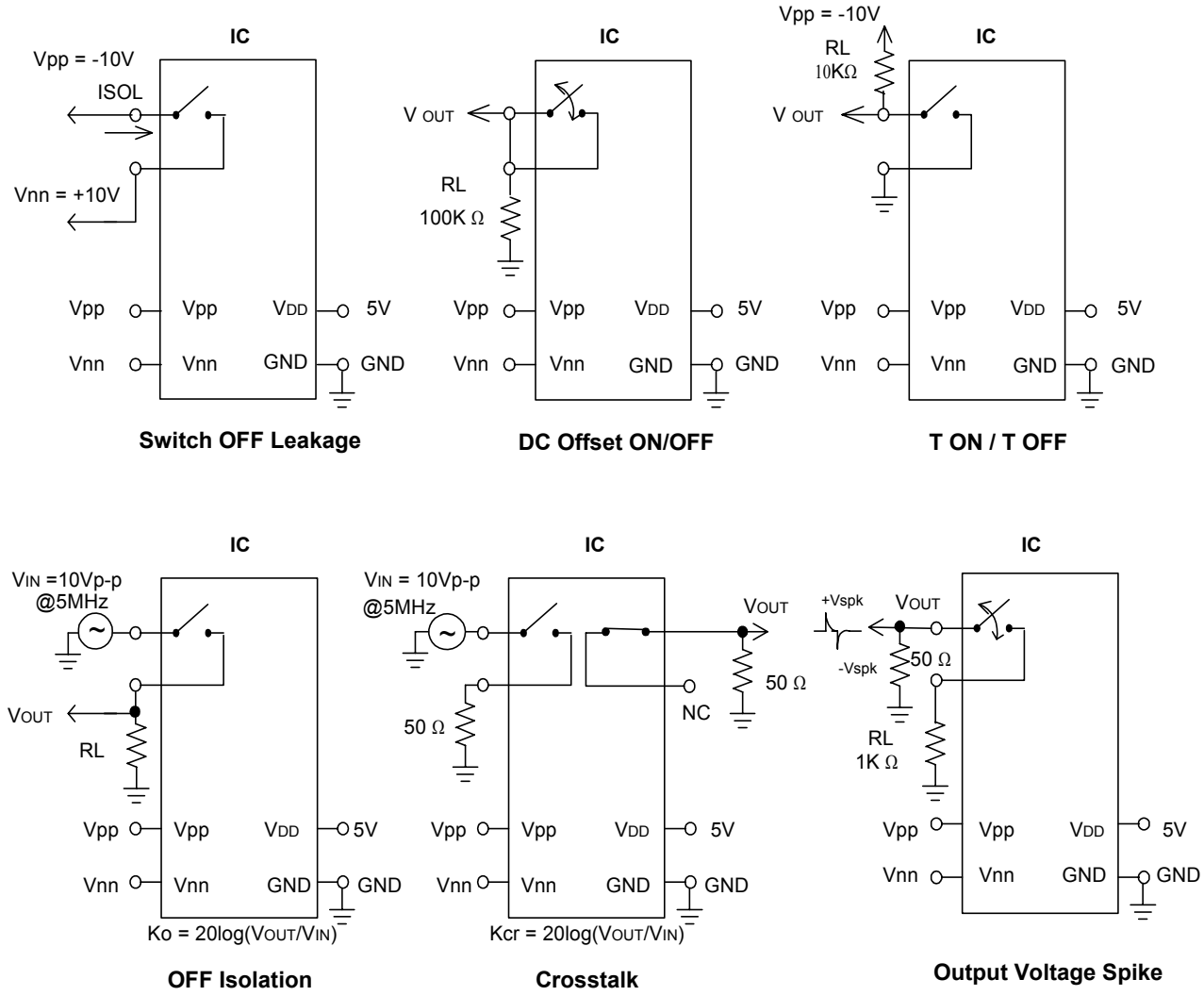


Fig. 2 Test Circuits

5. Timing Waveforms

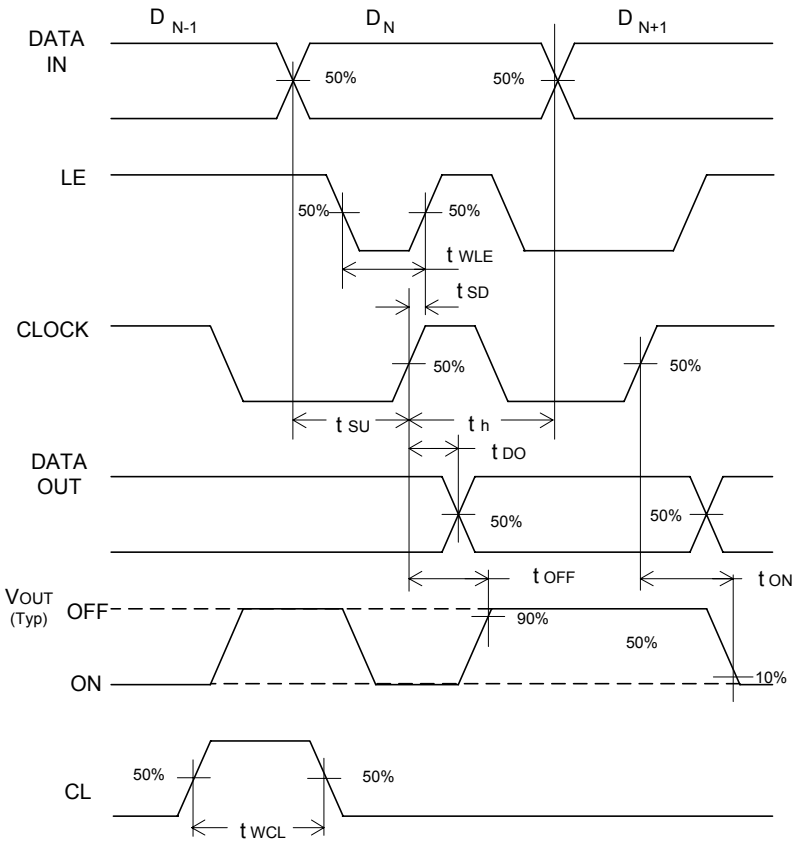


Fig. 3 Timing Waveforms

ECN3290TF/PL/FN

6. Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	LE	CL	SW 0	SW 1	SW 2	SW 3	SW 4	SW 5	SW 6	SW 7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

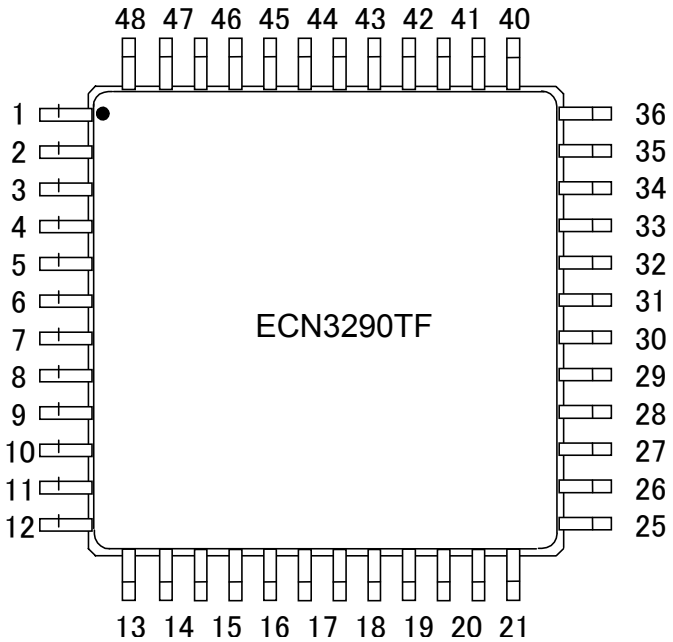
ECN3290TF/PL/FN

7. Pin Configuration

7.1) ECN3290TF TQFP48 (48Pin TQFP)

Pin Assignment

Pin#	Function	Pin#	Function	Pin#	Function
1	SW5	17	N/C	33	DIN
2	N/C	18	SW1	34	CLK
3	SW4	19	N/C	35	$\overline{\text{LE}}$
4	N/C	20	SW0	36	CL
5	SW4	21	N/C	37	DOUT
6	N/C	22	SW0	38	N/C
7	N/C	23	N/C	39	SW7
8	SW3	24	VPP	40	N/C
9	N/C	25	VNN	41	SW7
10	SW3	26	N/C	42	N/C
11	N/C	27	N/C	43	SW6
12	SW2	28	GND	44	N/C
13	N/C	29	VDD	45	SW6
14	SW2	30	N/C	46	N/C
15	N/C	31	N/C	47	SW5
16	SW1	32	N/C	48	N/C



48pin Package

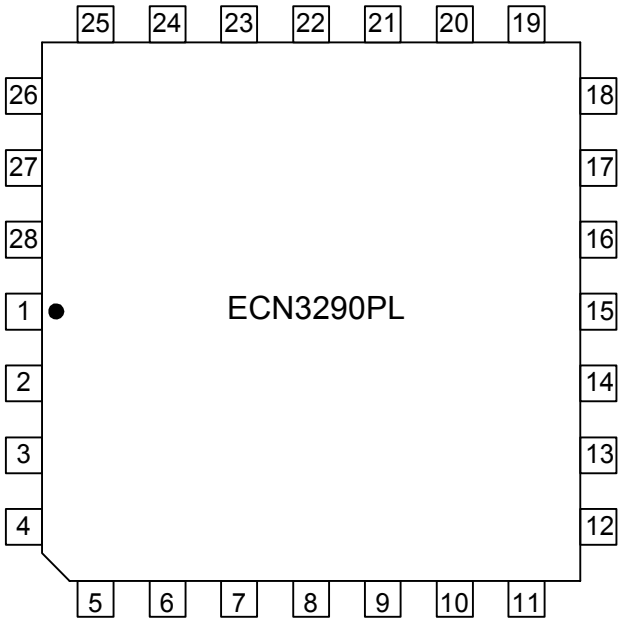
(Top View)

ECN3290TF/PL/FN

7.2) ECN3290PL QFJ28 (28Pin J-Lead)

Pin Assignment

Pin#	Function	Pin#	Function
1	SW3	15	N/C
2	SW3	16	DIN
3	SW2	17	CLK
4	SW2	18	$\overline{LE}$
5	SW1	19	CL
6	SW1	20	DOUT
7	SW0	21	SW7
8	SW0	22	SW7
9	N/C	23	SW6
10	VPP	24	SW6
11	N/C	25	SW5
12	VNN	26	SW5
13	GND	27	SW4
14	VDD	28	SW4

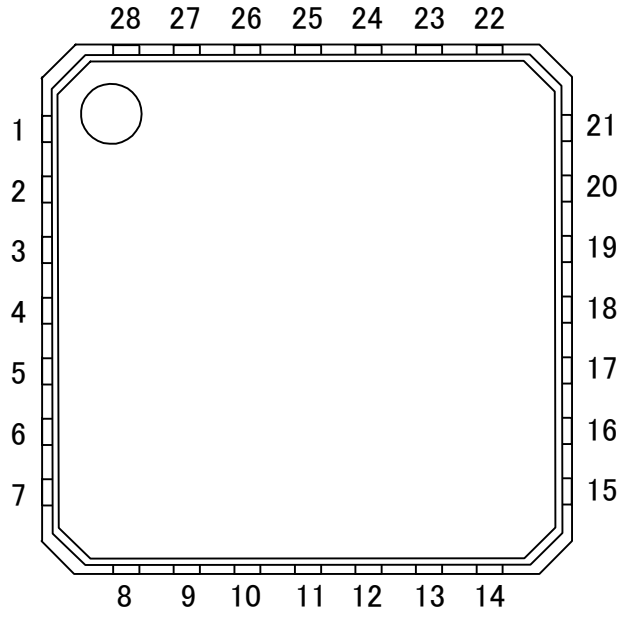


(Top View)

7.3) ECN3290FN QFN28 (28Pin Quad Flat No-lead package)

Pin Assignment

Pin#	Function	Pin#	Function
1	SW5	15	N/C
2	SW4	16	VNN
3	SW4	17	GND
4	SW3	18	VDD
5	SW3	19	DIN
6	SW2	20	CLK
7	N/C	21	$\overline{LE}$
8	SW2	22	CL
9	SW1	23	DOUT
10	SW1	24	SW7
11	SW0	25	SW7
12	SW0	26	SW6
13	N/C	27	SW6
14	VPP	28	SW5



(Top View)

8. Package Outline

8.1) ECN3290TF TQFP48 (48Pin TQFP)

Units : mm

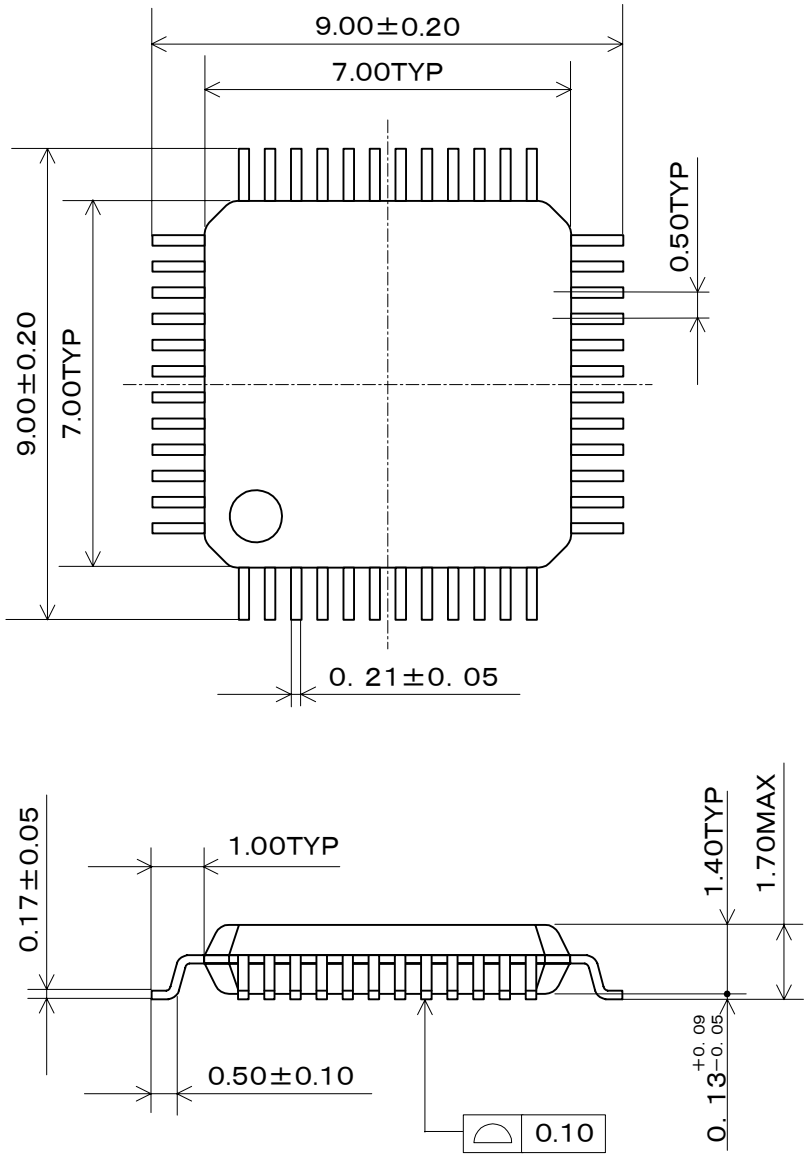
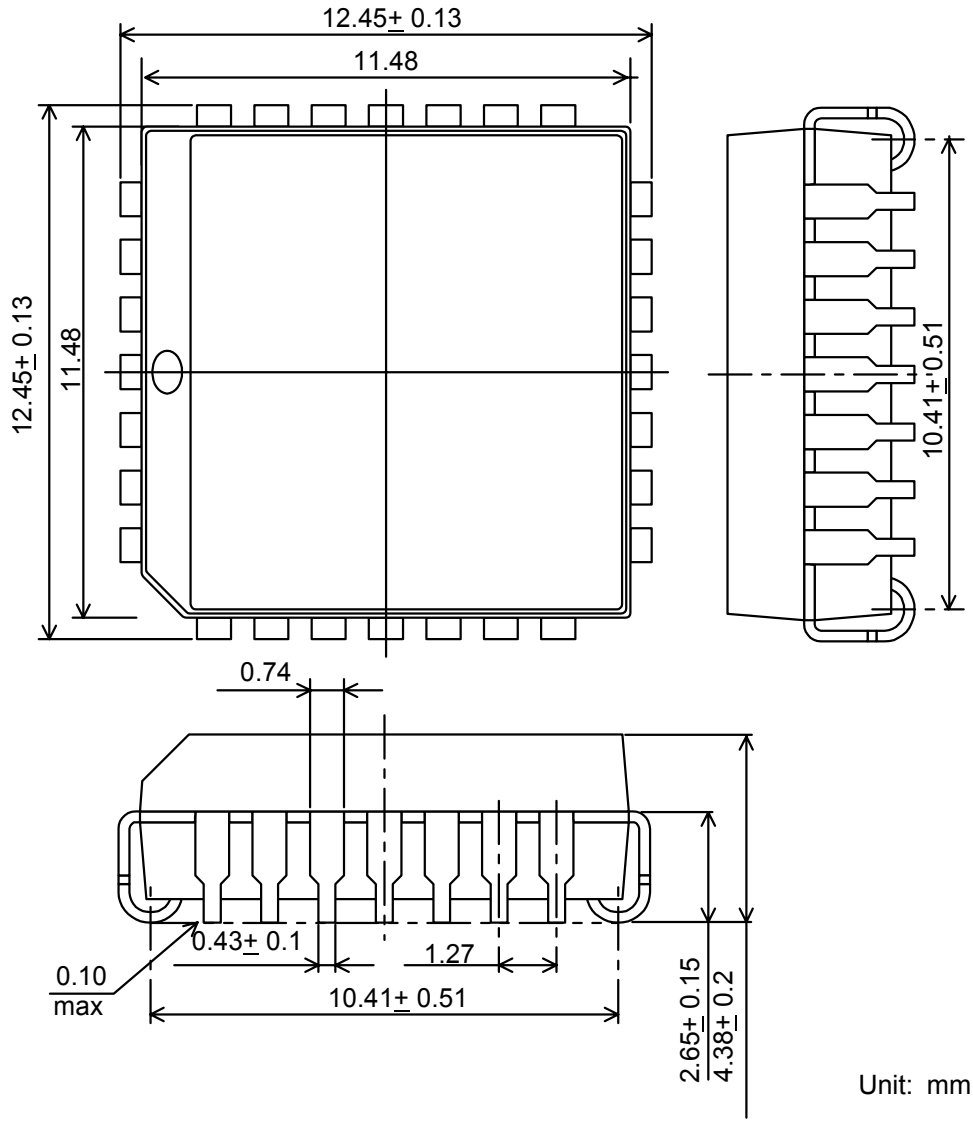


Fig.4 Package Outline (48pin TQFP Package)

8.2) ECN3290PL QFJ28 (28Pin J-Lead)

Units : mm



Unit: mm

Fig.5 Package Outline (28pin J-Lead Package)

8.3) ECN3290FN QFN28 (28Pin Quad Flat No-lead package)

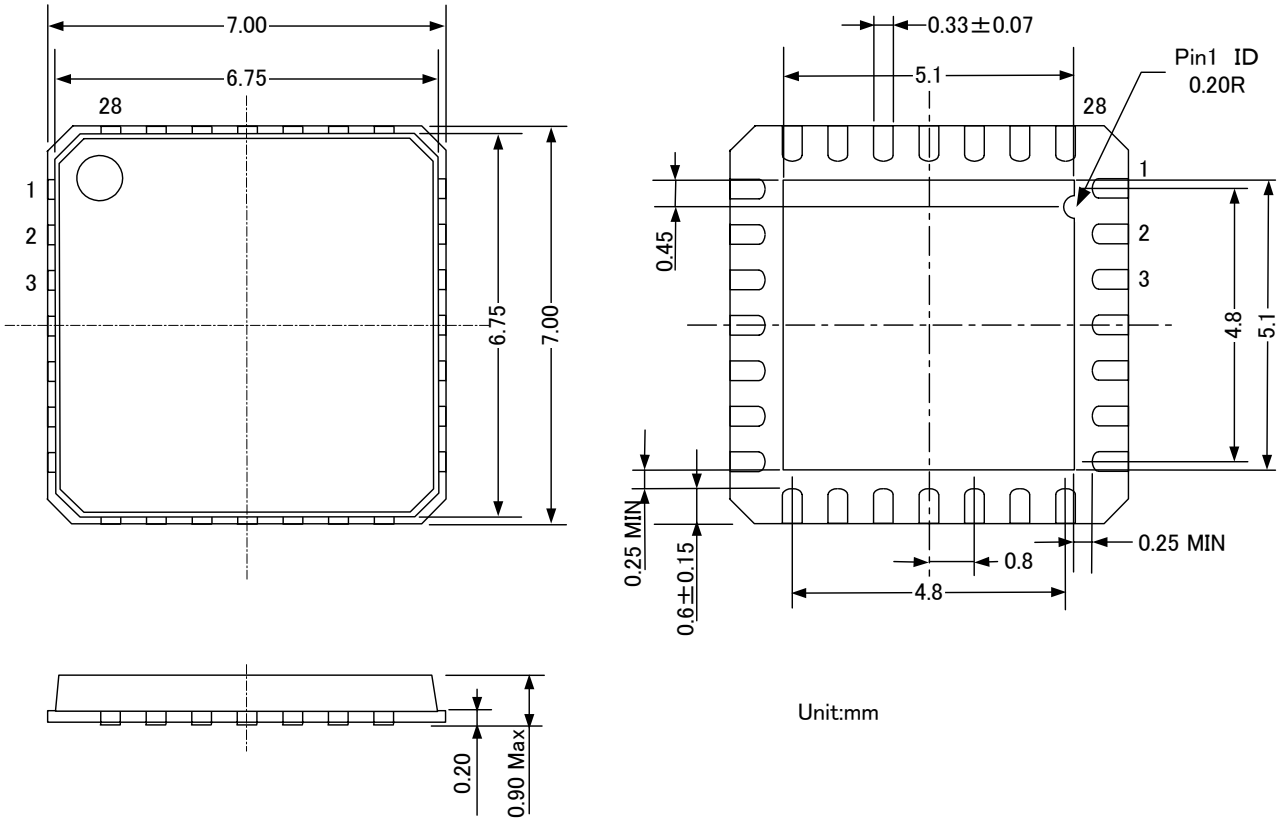


Fig.6 Package Outline (28pin QFN Package)

<Important Notice for QFN28(Quad Flat No-Lead 28 Pin) Package>

a) Connection of tab
A tab of the back of a QFN package and each terminal of IC are not connected. Please use the tab as open, or use it for GND, connecting.

Do not impress the voltage beyond 220V of a rated value between a tab and each terminal of IC.

b) Pb free
Solder plating of the terminal of a QFN package and a back tab has adopted SnBi plating.

9. Inspection

Hundred percent inspection shall be conducted on electric characteristics.

10. Important Notice

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11. Cautions

11.1 Customers are advised to follow the below cautions to protect semiconductor from electrical static discharge (ESD).

a) IC needs to be dealt with caution to protect from damage by ESD. Material of container or any device to carry semiconductor devices should be free from ESD which may be caused by vibration while transportation. To use electric-conductive container or aluminum sheet is recommended as an effective countermeasure.

b) Those what touch semiconductor devices such as work platform, machine and measuring and test equipment should be grounded.

c) Workers should be grounded connecting with high impedance around 100kΩ to 1MΩ while dealing with semiconductor to avoid damaging IC by electric static discharge.

d) Friction with other materials such as a high polymer should not be caused.

e) Attention is needed so that electric potential will be kept on the same level by short circuit terminals when PC board with mounted IC is carried and that vibration or friction might not occur.

f) Air conditioning is needed so that humidity should not drop.

11.2 Refer to “Precautions for Use of High-Voltage Monolithic ICs” (No.IC-0104E) for the other precautions and instructions on how to deal with products.

11.3 Regardless of changes in external conditions during use, “absolute maximum ratings” should never be exceeded in designing electronic circuits that employ products. In a case absolute maximum ratings are exceeded, products may be damaged or destroyed. In no event shall Hitachi be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.

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HITACHI POWER SEMICONDUCTORS

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