

ES52E9B1N-10.000M

[Click part number to visit Part Number Details page](#)

REGULATORY COMPLIANCE (Data Sheet downloaded on Dec 3, 2018)


[Click badges to download compliance docs](#)

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ITEM DESCRIPTION

Temperature Compensated Quartz Crystal Clock Oscillators TCXO (TCVCXO) Clipped Sinewave Stratum 3 3.3Vdc 10 Pad 5.0mm x 7.0mm Ceramic Surface Mount (SMD) 10.000MHz ± 0.28 ppm Maximum -10°C to +60°C

ELECTRICAL SPECIFICATIONS

Nominal Frequency	10.000MHz
Total Frequency Tolerance	± 4.6 ppm Maximum (Inclusive of Frequency Tolerance, Frequency Stability, Vdd ($\pm 1\%$), Load ($\pm 5\%$), solder reflow, and 20 year aging)
Frequency Tolerance	± 1.0 ppm Maximum (at 25°C $\pm 2^\circ\text{C}$, at Vdd=3.3Vdc (Pre-Reflow))
Frequency Stability	± 0.28 ppm Maximum (Inclusive of Operating Temperature Range, at Vdd=3.3Vdc; $(F_{\text{max}} - F_{\text{min}})/(2 \cdot F_0)$)
Frequency Stability vs. Aging	± 3.0 ppm over 20 Years Maximum (at 25°C)
Operating Temperature Range	-10°C to +60°C
Supply Voltage	3.3Vdc $\pm 5\%$
Total Holdover Stability	± 0.37 ppm Maximum (Inclusive of Frequency Stability and 24 hours aging)
Input Current	2.0mA Maximum
Output Voltage	0.8Vp-p Clipped Sinewave Minimum (External DC-Cut capacitor required, 1000pF recommended)
Load Drive Capability	10kOhms // 10pF
Output Logic Type	Clipped Sinewave
Control Voltage	None (No Connect Pad 10)
Phase Noise	All Values are Typical -80dBc/Hz at 10Hz Offset -115dBc/Hz at 100Hz Offset -135dBc/Hz at 1kHz Offset -145dBc/Hz at ≥ 10 kHz Offset
RMS Phase Jitter	1pSec Maximum ($F_j = 12$ kHz to 20MHz)
Start Up Time	10mSec Maximum
Storage Temperature Range	-40°C to +125°C

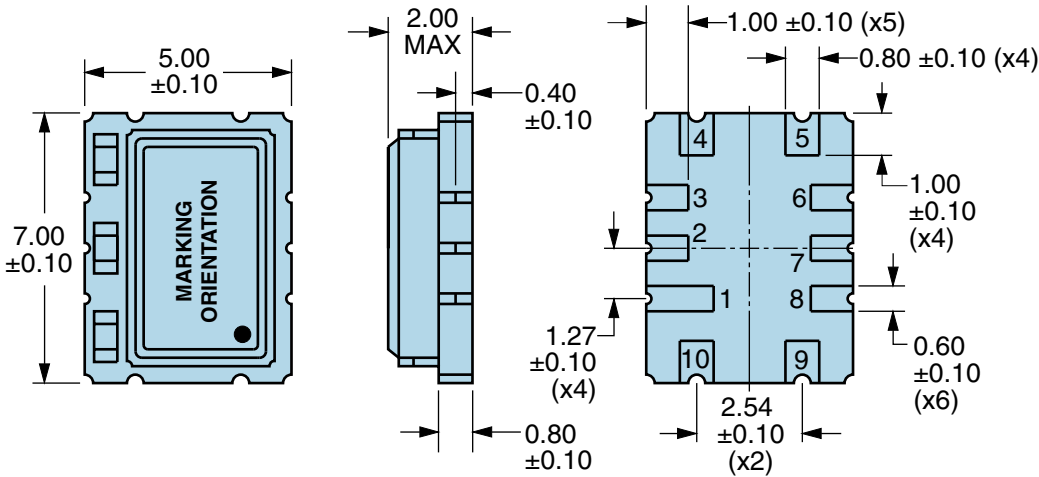
ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

Fine Leak Test	MIL-STD-883, Method 1014 Condition A
Gross Leak Test	MIL-STD-883, Method 1014 Condition C
Mechanical Shock	MIL-STD-202, Method 213 Condition C
Resistance to Soldering Heat	MIL-STD-202, Method 210
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003
Temperature Cycling	MIL-STD-883, Method 1010
Vibration	MIL-STD-883, Method 2007 Condition A

ES52E9B1N-10.000M

[Click part number to visit Part Number Details page](#)

MECHANICAL DIMENSIONS (all dimensions in millimeters)

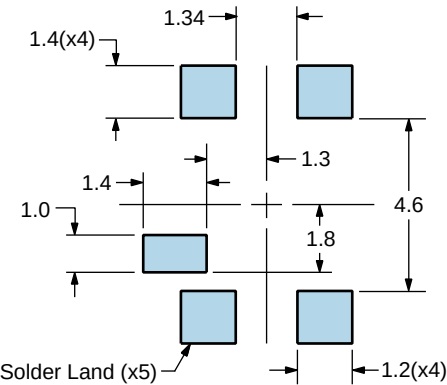


PIN	CONNECTION
1	Do Not Connect
2	Do Not Connect
3	Do Not Connect
4	Ground
5	Output
6	Do Not Connect
7	Do Not Connect
8	Do Not Connect
9	Supply Voltage
10	No Connect

LINE	MARKING
1	EXX.XXX E=Ecliptek Designator XX.XXX=Nominal Frequency in MHz
2	XXXXXX XXXXXX=Ecliptek Manufacturing Identifier

Suggested Solder Pad Layout

All Dimensions in Millimeters

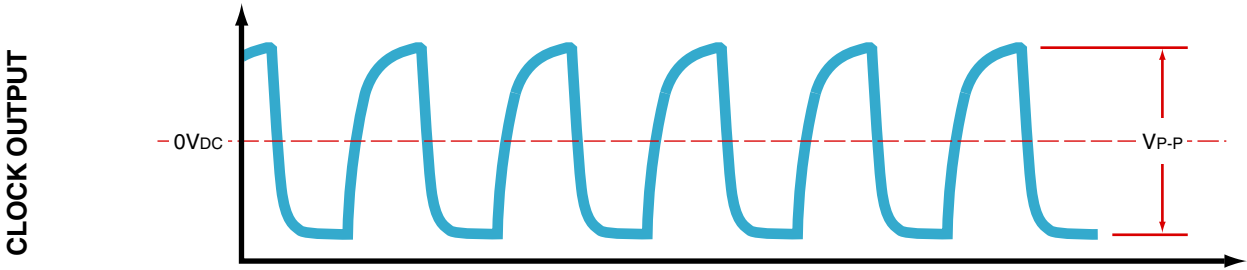


All Tolerances are ±0.1

ES52E9B1N-10.000M

[Click part number to visit
Part Number Details page](#)

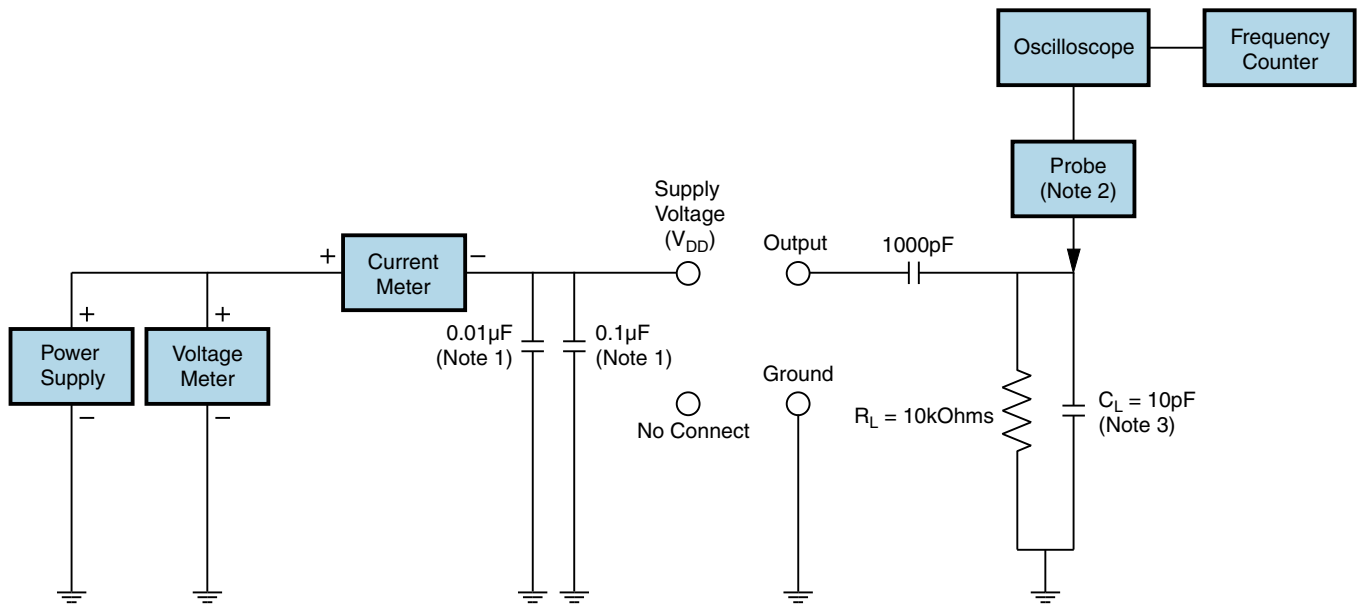
OUTPUT WAVEFORM



ES52E9B1N-10.000M

[Click part number to visit Part Number Details page](#)

Test Circuit for No Connect Option



Note 1: An external 0.01µF bypass capacitor in parallel with a 0.1µF high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.

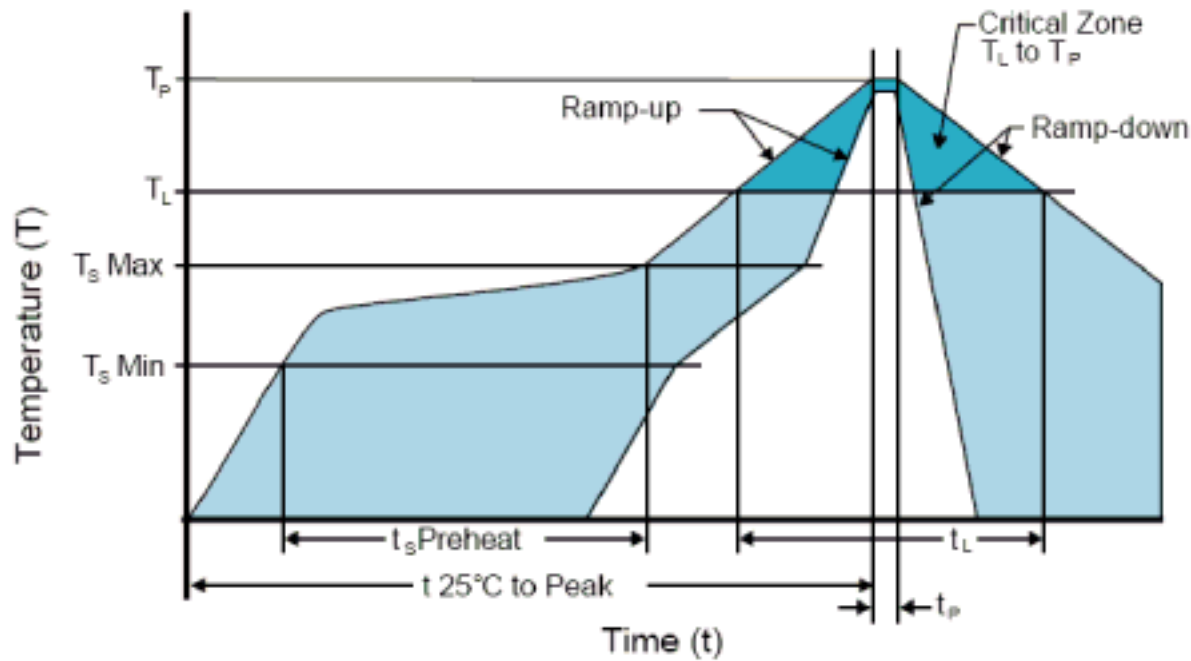
Note 2: A low input capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.

Note 3: Capacitance value C_L includes sum of all probe and fixture capacitance.

ES52E9B1N-10.000M

[Click part number to visit Part Number Details page](#)

Recommended Solder Reflow Methods



Low Temperature Infrared/Convection 230°C

Ts MAX to TL (Ramp-up Rate)	5°C/Second Maximum
Preheat	
- Temperature Minimum (Ts MIN)	N/A
- Temperature Typical (Ts TYP)	150°C
- Temperature Maximum (Ts MAX)	N/A
- Time (ts MIN)	30 - 60 Seconds
Ramp-up Rate (TL to TP)	5°C/Second Maximum
Time Maintained Above:	
- Temperature (TL)	150°C
- Time (tL)	200 Seconds Maximum
Peak Temperature (TP)	230°C Maximum
Target Peak Temperature (TP Target)	230°C Maximum 2 Times
Time within 5°C of actual peak (tP)	10 Seconds Maximum 2 Times
Ramp-down Rate	5°C/Second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1
Additional Notes	Temperatures shown are applied to body of device.

Low Temperature Manual Soldering

185°C Maximum for 10 Seconds Maximum, 2 times Maximum. (Temperatures listed are applied to body of device.)

High Temperature Manual Soldering

260°C Maximum for 5 Seconds Maximum, 2 times Maximum. (Temperatures listed are applied to body of device.)