Micro Linear

PRELIMINARY

ML2725 2.4GHz Low IF 1.5Mbps Transceiver

GENERAL DESCRIPTION

The ML2725 can be used as a single chip Direct Sequence Spread Spectrum (DSSS) telephone transceiver or general purpose Frequency Shift Keying (FSK) radio transceiver. It is designed to work in frequency ranges of 2.4GHz. The device integrates the frequency generation, receive and transmit functions for data rates up to 1.5Mbps.

The ML2725 contains a proprietary dual conversion low IF receiver with all channel selectivity. The first mixer converts the 2.4GHz RF input signal to a high IF of 800MHz. An image reject mixer brings the 800MHz IF signal down to a low IF frequency of 1.024MHz. Then all IF filtering, IF gain, and demodulation is performed at 1.024MHz. This provides all the benefits of direct conversion to baseband and minimizes the need for RF filtering. Also, the ML2725 can operate with either a low cost LC filter or a SAW filter.

A single 1.6GHz synthesizer is used for both the receiver LO and the transmitter signal generation. The VCO and PLL are completely integrated, including the VCO resonator and tuning circuits. On transmit, the ML2725 is intended to be used with an external frequency tripler. The transmit output frequency is nominally 800MHz, with a typical output power of 0 dBm. Transmit data is used to frequency modulated the VCO, with the synthesizer open loop. The transmit data filter and modulation compensation circuits are also integrated.

The ML2725 contains its own DC regulation which allows the IC to operate over a wide power supply voltage range. It also has a simple baseband interface for transmit power management, PLL control and detection, and RSSI (Receiver Signal Strength Indication).

FEATURES

- Single chip 2.4GHz radio transceiver utilizes an external frequency tripler/power amplifier
- Fully integrated filters for all IF, FM discriminator and data filtering
- Image reject mixer & proprietary Low IF architecture reduce the need for RF filtering
- Integrated 1.6GHz frequency synthesizer with internal VCO resonator
- TX/RX calibration for max power transmission
- Transmit modulation compensation for improved sensitivity
- Auxiliary control outputs correctly sequence and control PA
- PLL Programmed via 3-wire interface
- Analog Received Signal Strength Indication (RSSI) output to baseband IC

APPLICATIONS

- 2.4GHz radio transceivers with ranges from 10 feet to 1000 feet and data rates to 1.5Mbps
- Handheld devices, gadgets and gizmos
- FCC Part 15 compliant radio links
- Game controllers
- Portable computer/PDA, remote sensing
- TDD and TDMA radios
- Robust DSSS for hostile interference environments
- 2.4GHz DSSS cordless phones

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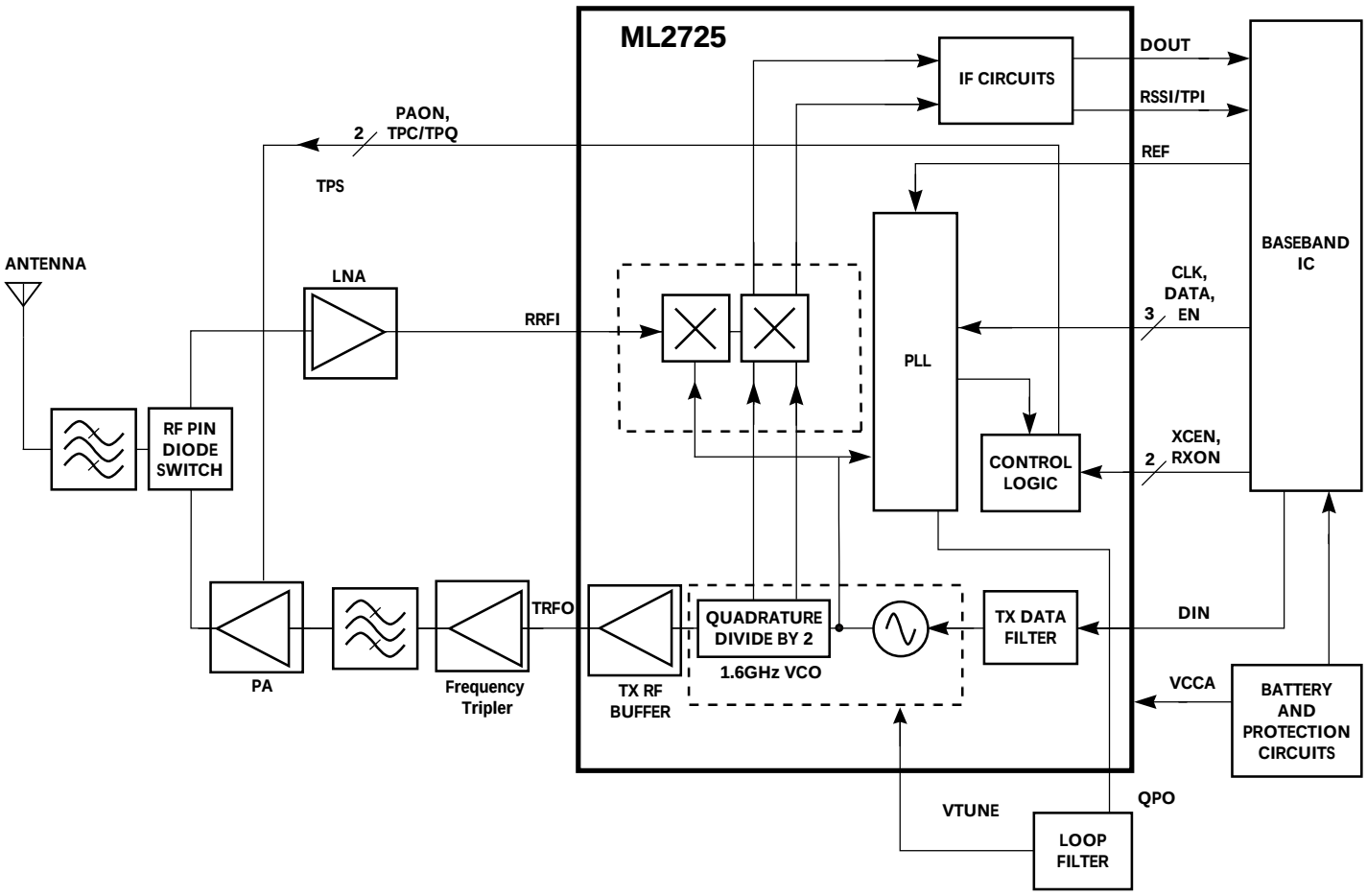
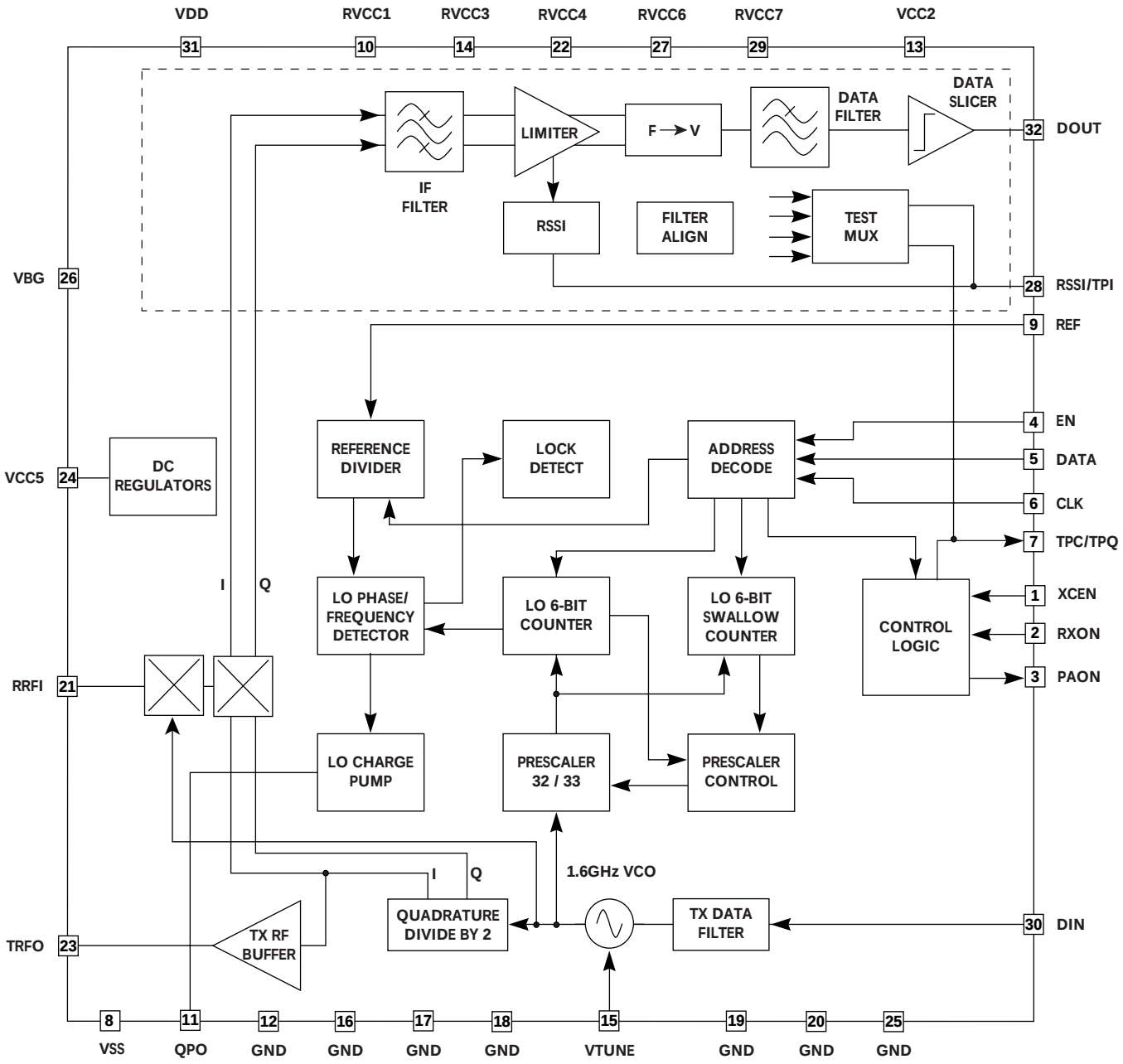
SIMPLIFIED APPLICATIONS DIAGRAM



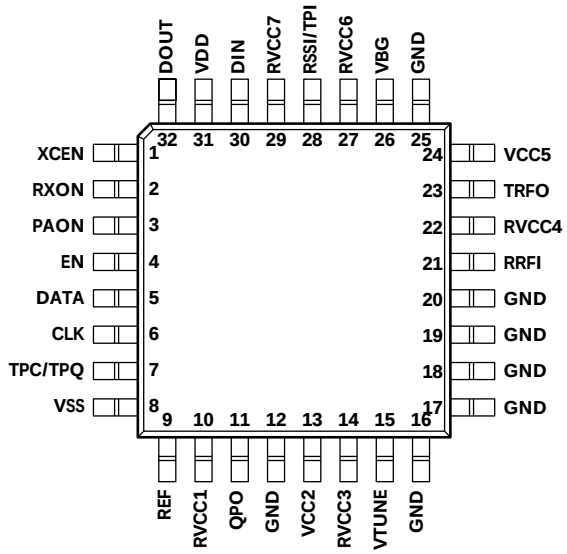
2.4GHz DSSS Application

BLOCK DIAGRAM



PIN CONFIGURATION

ML2725
32-Pin TQFP (H32-7)



TOP VIEW

PIN DESCRIPTIONS

Pin #	Signal Name	I/O	Description
Power & Ground			
13	VCC2	I (analog)	DC Power Supply Input to the VCO voltage regulator. Must be connected to RVCC6 (pin 27) or RVCC7 (pin 29) via decoupling network
24	VCC5	I (analog)	DC power supply Input to Voltage Regulators and unregulated loads: 3.0 to 5.0V. VCC5 is the main (or master) analog VCC pin. There must be a capacitor to ground from this pin to decouple (bypass) noise and to stabilize the regulator
16	GND	I (analog)	DC ground for VCO and LO circuits
10	RVCC1	O (analog)	DC power supply decoupling point for the PLL dividers, phase detector, and charge pump. This pin is connected to the output of the regulator and to the PLL supplies. There must be a capacitor to ground from this pin to decouple (bypass) noise and to stabilize the regulator
14	RVCC3	O (analog)	DC power supply decoupling point for the VCO. Connected to the output of the VCO regulator. There must be a capacitor to ground from this pin to decouple (bypass) noise and to stabilize the regulator
22	RVCC4	O (analog)	DC power supply decoupling point for the LO Chain. Connected to the output of a regulator. There must be a capacitor to ground from this pin to decouple (bypass) noise and to stabilize the regulator
27	RVCC6	O (analog)	DC power supply decoupling point for Quadrature Mixer and IF filter circuits. There must be a capacitor to ground from this pin to decouple (bypass) noise and to stabilize the regulator

PIN DESCRIPTIONS (continued)

Pin #	Signal Name	I/O	Description
Power & Ground (Continued)			
29	RVCC7	O (analog)	DC power supply decoupling point for IF, Demodulator, and Data Slicer circuits. There must be a capacitor to ground from this pin to decouple (bypass) noise and to stabilize the regulator
25	GND	I (analog)	DC Ground to IF, Demodulator, and Data Slicer circuits
12	GND	I (analog)	Ground for the PLL dividers, phase detector, and charge pump
17	GND	I (analog)	Signal ground for RF small signal circuits. Pins 17, 18, and 19 should have short, direct connections to each other and additional connections to ground
18	GND	I (analog)	Ground return for the Receive RF input
19	GND	I (analog)	Signal ground for the Receive mixers
20	GND	I (analog)	DC and Signal ground for the Transmit RF Output buffer
31	VDD	I (analog)	DC power supply input to the interface logic and control registers. This supply is not internally connected to any other supply pin, but its voltage must be less than or equal to the VCC5 supply, and greater than 3.0V. There must be a capacitor to ground from this pin to decouple (bypass) noise and to stabilize the regulator
8	VSS	I (digital)	Ground for digital I/O circuits and control logic
Transmit/Receive			
21	RRFI	I (analog)	Receive RF Input. Nominal impedance at 2.445GHz is 6-j15Ω with a simple matching network required for optimum noise figure. This input is to the base of an NPN transistor and should be AC coupled (Diagram 1)
23	TRFO	O (analog)	Transmit RF Output. A broadband 50Ω output which sources 0dBm over the 800 to 833MHz range. This output is an emitter follower and should be AC coupled (See Diagram 2)
Data			
30	DIN	I (CMOS)	Transmit Data input. Drives the transmit pulse shaping circuits. Serial digital data on this pin becomes FSK modulation on the Transmit RF output. Data timing is controlled by the logic timing on this pin. The modulation deviation is determined by internal circuits. This is a standard CMOS input referenced to VDD &VSS (Diagram 3)
32	DOUT	O (CMOS)	Serial digital output after demodulation, chip rate filtering and center data slicing. A CMOS level output (VSS to VDD) with controlled slew rates. A low drive output designed to drive a PCB trace and a CMOS logic input while generating minimal RFI. In digital test modes this pin becomes a test access port controlled by the serial control bus (Diagram 4)
Mode Control and Interface Lines			
1	XCEN	I (CMOS)	Enables the bandgap reference and voltage regulators when high. Consumes only leakage current in standby mode when low. This is a CMOS input, and the thresholds are referenced to VDD and VSS (Diagram 3)
2	RXON	I (CMOS)	Switches the transceiver between Transmit and Receive modes. Circuits are powered up and signal paths reconfigured according to the operating mode. This is a CMOS input, and the thresholds are referenced to VDD and VSS (Diagram 3)

PIN DESCRIPTIONS (continued)

Pin #	Signal Name	I/O	Description
Mode Control and Interface Lines (Continued)			
3	PAON	O (CMOS)	Enables the off chip PA at the correct times in a Transmit slot. Goes high when transmit RF is present at TRFO, goes low 5µs before transmit RF is removed from TRFO. Has interlock logic to shut down PA if the PLL does not lock (Diagram 5)
7	TPC/TPQ	O (Open Drain)	Transmit power control output. This open drain output is pulled low when the TPC bit is serial register #1 is set. Transitions on TPC are synchronized to the falling edge of RXON. In analog test modes this pin and the RSSI output become test access points controlled by the serial control bus (Diagram 6) (This pin in undefined)
9	REF	I	Input for the 12.288MHz reference frequency. This is used as the reference frequency for the PLL, and as a calibration frequency for the on chip filters. This is a self-biased CMOS input that is designed to be driven either by a an AC coupled sine wave source (recommended coupling capacitor is 470pF) or by a standard CMOS output (Diagram 7)
11	QPO	O	Charge Pump Output of the phase detector. This is connected to the external PLL loop filter (Diagram 8)
15	VTUNE	I	VCO Tuning Voltage input from the PLL loop filter. This pin is very sensitive to noise coupling and leakage currents (Diagram 9)
26	VBG	O	Internal bandgap reference voltage. Decoupled to ground with a 220nF capacitor
28	RSSI/TPI	O	Buffered Analog RSSI output with a nominal sensitivity of 35mV/dB. An RF input signal range of –95 to –20dBm gives an RSSI voltage output of zero to 2.7V (Diagram 10)
Serial Bus Signals			
4	EN	I (CMOS)	Enable pin for the three wire serial control bus which sets the operating frequency and programmable options. The control registers are loaded on a low to high transition of the signal. Serial control bus data is ignored when it is high. This is a CMOS input, and the thresholds are referenced to VDD &VSS (Diagram 11)
5	DATA	I (CMOS)	Serial control bus data. 16 bit words which include programming data and the two bit address of a control register. This is a CMOS input, and the thresholds are referenced to VDD &VSS (Diagram 11)
6	CLK	I (CMOS)	Serial control bus data is clocked in on the rising edge when EN is low. This is a CMOS input, the thresholds are referenced to VDD &VSS (Diagram 11)

PIN DIAGRAMS

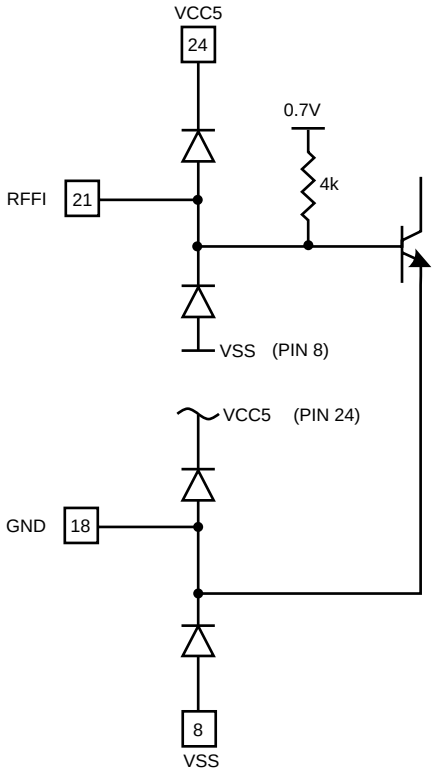


Diagram 1.

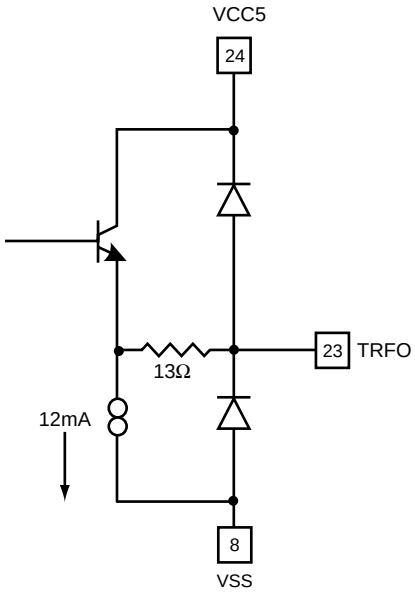


Diagram 2.

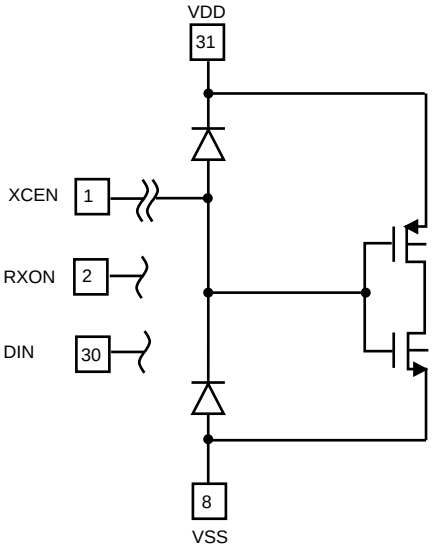


Diagram 3.

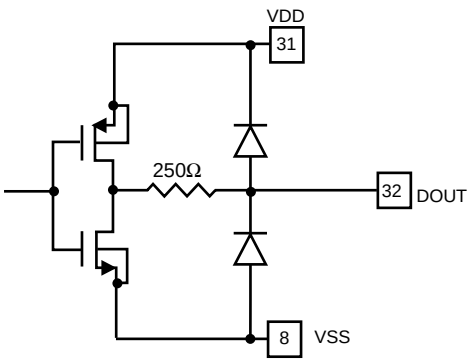


Diagram 4.

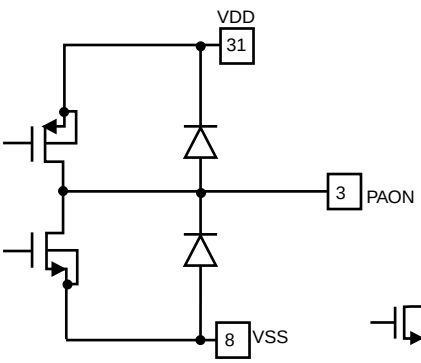


Diagram 5.

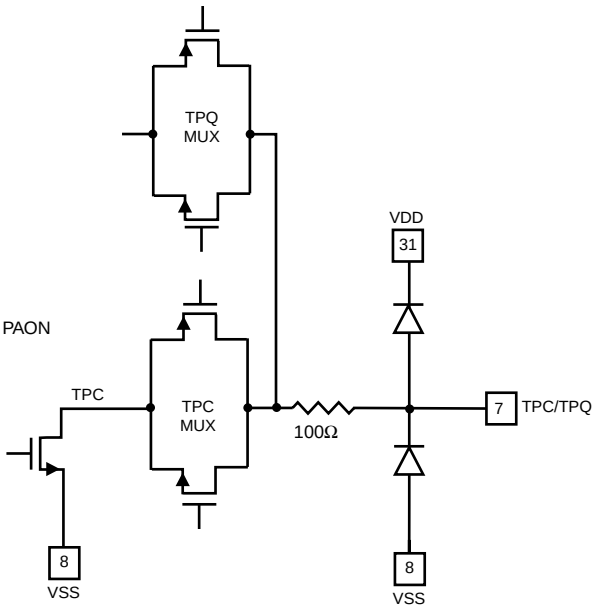


Diagram 6.

PIN DIAGRAMS (continued)

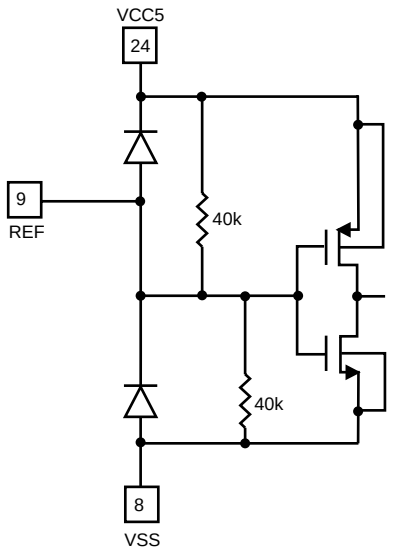
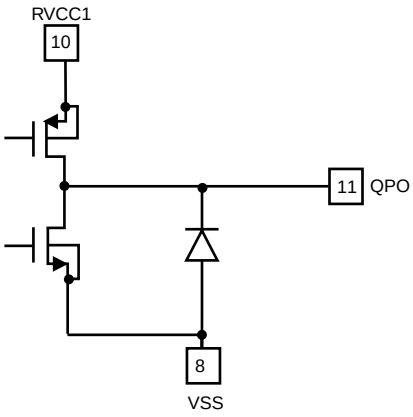


Diagram 7.



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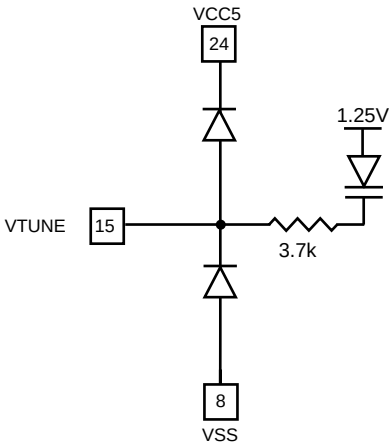


Diagram 9.

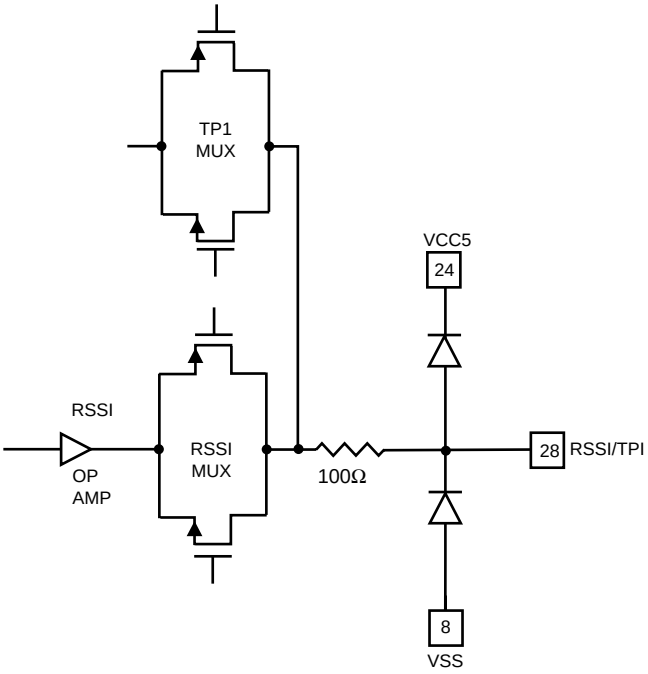


Diagram 10.

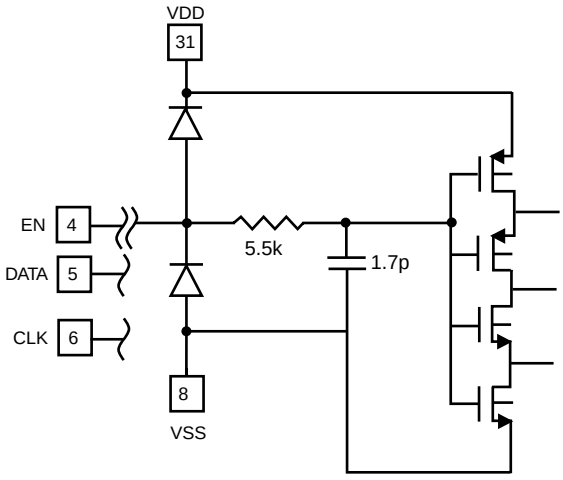


Diagram 11.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The ML2725 enables the design and manufacture of low cost, high performance, general purpose 2.4GHz transceiver. It can also be used as a digital DSSS cordless telephone transceiver. Integral to the ML2725 is a dual conversion low IF receiver whose LO ports are driven from an internal synthesizer. Included are image rejection IF filters, limiters, discriminator, data slicers, and baseband lowpass data filters. It also contains internal voltage regulators to protect critical circuits from power supply noise and transmit modulation circuits.

The ML2725 has an internal control interface that programs the synthesizer, the mode of operation, the external LNA and PA, and provides a convenient and flexible interface to various baseband processors. For power level monitoring an RSSI block is included.

The ML2725 is designed to transmit and receive 1.536M chips per second signals in 2.048MHz spaced channels in the 2.4GHz ISM band. The 1.536M chips per second rate with a 15 bit spreading code gives a 102.4kb/s data rate and provides a 11.6dB processing gain.

In the Receive mode the ML2725 is a dual conversion low IF receiver. The 1IF frequency of 800MHz gives an image response at 800MHz, simplifying the image filter. The 2IF frequency of 1.024MHz results in a second image response in an adjacent channel. An image reject mixer gives sufficient rejection in this channel. All IF filtering and demodulation is performed using active filtering, centered at 1.024MHz. The demodulator is followed by a matched bit rate filter and a data slicer. The sliced data is provided to a baseband chip for de-spreading.

In the Transmit mode the ML2725 uses the Receive mode VCO and frequency division, to drive an external frequency tripler. The third harmonic at 2.4GHz is generated by an off chip frequency tripler. The PLL frequency synthesizer loop is opened during the transmit slot, and the VCO is directly modulated by low-pass filtered circuits from the internal modulation filter.

The frequency generation circuits are an internal VCO at 1.6GHz, dividers, a phase comparator and a charge pump for a PLL frequency synthesizer. The VCO output is divided by two to produce accurate quadrature outputs at 800MHz. No external components are need for the VCO.

CIRCUIT BLOCK DESCRIPTIONS

PHASE LOCKED LOOP (PLL) AND VOLTAGE CONTROLLED OSCILLATOR (VCO)

The PLL synthesizes channel frequencies to a 1.024MHz resolution. Non-overlapping channels are spaced by 2.048MHz where the IF filter and image reject mixer give a typical adjacent channel rejection of 25dB. There are forty non-overlapping channels in the 2.4GHz ISM band.

The LO PLL is programmed via a 3-wire serial control bus. Program words are clocked in on the DATA line (pin 5) by the CLK (pin 6), and loaded into the dividers or control circuits when EN (pin 4) is asserted. There is no check for error in the program words. Once loaded, register contents are preserved regardless of power conditions. The register status and operation is independent of the mode of operation of the PLL.

The reference signal from an external crystal oscillator at 12.288MHz is fed to a programmable reference divider. The 682.67kHz reference divider output is fed to the LO phase frequency detector. The PLL prescaler input comes from the VCO at 1.6GHz, so the 682.67kHz comparison frequency gives 1.024MHz frequency resolution at 2.4GHz.

The output of the LO divider is fed to the LO phase/ frequency detector and subsequently to the charge pump.

LO VCO AND TRANSMIT DRIVER

The internal LO VCO operates at 1.67GHz, which is two-thirds the channel frequency of 2.4GHz. The VCO output is divided by 2 to give accurately matched quadrature signals at 800MHz.

In transmit mode the LO is frequency modulated by the transmitted data, using the modulation port of the VCO. The VCO output is divided by 2 and buffered. The 0dBm buffered fundamental output is used to drive an external tripler.

CIRCUIT BLOCK DESCRIPTIONS

TRANSMIT DATA FILTER AND MODULATION DRIVER

Logic level NRZ signals at DIN are scaled and filtered by a 5th-order lowpass filter. The lowpass filter is tuned to give a 1.35MHz 3dB point to pass the 1.536M chips per second transmit data. The filter data is then fed to the internal modulation port of the LO tank circuit.

In the transmit closed loop mode the modulation port is held at its midpoint so that the synthesizer locks to the center channel frequency. In the transmit open loop mode the VCO is modulated by Gaussian filtered data via the VCO modulation port. The modulation driver contains scaling circuitry to control the FM deviation over the entire VCO tuning range. This circuit is inactive in the receive mode.

RECEIVE MIXERS AND IF CHAIN

The Receive first mixer down-converts the signal to the 800 to 833MHz 1IF. The input of the mixer is single-ended and matched to 50Ω by a printed matching network on the PCB. his gives a good terminating impedance for the preceding RF filter. The Receive second mixer down-converts the 800-833MHz 1IF to the 1.024MHz receive 2IF. T The quadrature outputs of the down converter feed the IF filter. The quadrature mixer and IF filter together achieve a typical image rejection of 35dB.

A quadrature combiner for the image reject mixer and a 12th order Gaussian bandpass filter make up the active IF filters. The active filters provide an accurate Gaussian characteristic with a 1.408MHz, 3dB bandwidth which improves both sensitivity and adjacent channel rejection.

The IF amplifiers provide the bulk of the receiver's gain. An RSSI signal is generated by using the outputs of the IF amplifiers. The RSSI signal is conditioned and sent to the baseband controller. A frequency-to-voltage converter provides highly linear FM demodulation with good data recovery from the low IF.

DATA FILTER AND DATA SLICER

The FM demodulator is followed by a Gaussian lowpass filter whose 768kHz cutoff frequency is matched to the transmitted 1.536M chips per second waveform. This Gaussian filter is implemented with similar circuits to the IF filter, and is shared with the Transmit modulation path. The filter output can be AC coupled to the slicer because the spreading code is almost DC balanced. The data slicer signal is output to the baseband processor for timing recovery and decoding.

POWER SUPPLY

The ML2725 uses multiple voltage regulators to protect sensitive internal circuits from power supply noise. Separate regulators supply the PLL dividers, RF circuits and IF circuits. Each of these regulators takes its power from VCC5, and supplies power internally to its respective RVCCn pin. External capacitors are required at each RVCCn pin to decouple the outputs of the internal regulators. The VCO regulator takes its power from the VCC2 (pin 13) which is normally connected to the RVCC6 (pin 27) or RVCC7 (pin 29). An external decoupling capacitor is also used on the internal bandgap voltage reference to improve the noise performance of the regulators.

MODES OF OPERATION

OVERVIEW

- STANDBY: All circuits powered down, except the control interface (Static CMOS)
- RECEIVE: Receiver circuits active
- TRANSMIT: PLL open loop, modulated RF output available from IC

The two operational modes are RECEIVE and TRANSMIT. They are set by the RXON (pin 2) control pin. XCEN (pin 1) is the chip enable/disable pin and can be set for standby operation. The relationship between the parallel control lines and the mode of operation of the IC is given in Table 1.

XCEN	RXON	Mode	Function
0	X	STANDBY	Control interfaces active, all other circuits powered down
1	1	RECEIVE	Receiver time slot
1	0	TRANSMIT	Transmit time slot

Table 1. Mode Selection

PARALLEL MODE CONTROL

The ML2725 is intended for use in TDD and TDMA radios in battery powered equipment. To minimize power consumption it is designed to switch rapidly from a low power mode (STANDBY) to receive or transmit. The ML2725 can also make a quick transition from receive to transmit for TDD operation. Prior to transmitting or receiving time should be allowed for the PLL to lock up, and in the case of receive, for the IF filters to be aligned. The ML2725 operates as a TDD radio on one RF frequency (transmit or receive). The VCO frequency changes between receive and transmit functions because of the IF frequency. This VCO frequency step is automatically performed.

RECEIVE

In RECEIVE mode, the received signal at 2.4GHz is down converted, bandpass filtered (IF filter), fed to the frequency-to-voltage converter and low-pass filtered. The output of the low-pass filter is fed to the data slicer which outputs NRZ digital data. An RSSI voltage output indicates the signal level at the output of the IF filter.

For the first 62.5µs from RXON going high, the ML2725 performs a self calibration (RXCAL). This is to allow the IF filters to be aligned and for the PLL to switch frequency and settle to the required frequency for receiving. Filter alignment, using the Reference Frequency input signal REF, in the RXCAL mode sets:

- Discriminator center frequency
- IF filter center frequency and bandwidth
- Receiver data low pass filter bandwidth
- Transmit data low pass filter bandwidth

In receive mode the programmed center frequency sets the RF channel that will be received. This means the PLL center frequency is the programmed RF center frequency plus the IF frequency. The frequency offset required for the low frequency IF in the RXCAL mode is automatically calculated and performed.

RECEIVER CIRCUIT OPERATION

The ML2725 receive chain is a low IF receiver using advanced integrated radio techniques to eliminate external IF filters and minimize external RF filter requirements. The precise filtering and demodulation circuits give improved performance over conventional radio designs using external filters. See Figure 1.

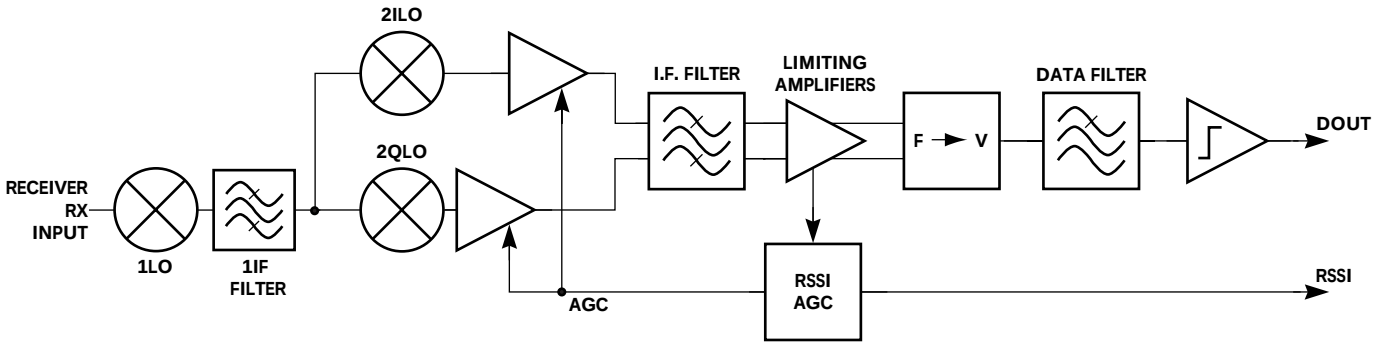


Figure 1. Receiver Block Diagram

MODES OF OPERATION (CONTINUED)

The signal flow in RECEIVE mode is from the RF input, through an image reject mixer, IF filter, hard limiter, Frequency to Voltage converter, data filter and data slicer. The ML2725 uses a double conversion super heterodyne receiver with a nominal IF of 1.024MHz. An AGC subsystem extends the dynamic range of the receiver. The IF frequency and filter bandwidths are given in Table 2.

Reference Division Ratio	18
Parameter	**RD0 = 1**
IF filter center frequency	REF/12
IF filter bandwidth	REF/8.8
Receive data filter	REF/16
F to V converter center frequency	REF/12

Table 2. Filter Parameter Settings

Major features of the receiver are:

- 6-pole bandpass IF filter, with accurate Gaussian to 12dB response. Center frequency 1.024MHz, Bandwidth 1.408 MHz (nominal)
- Limiting IF amplifiers with >80dB gain, and excellent AM rejection
- AGC to extend the dynamic range of the integrated filters & RSSI
- Logarithmic RSSI output from Limiter; AGC state is information added to give 80dB range
- FM demodulation by a linear F-to-V converter
- 5-pole low-pass data filter with an accurate Gaussian response and 3dB cutoff at 768kHz (nominal)
- 2 level data slicer with DC offset removal

The output of the receiver is quantized in amplitude (to 1 bit) but there is no internal timing recovery. Timing recovery is performed in the external baseband circuits.

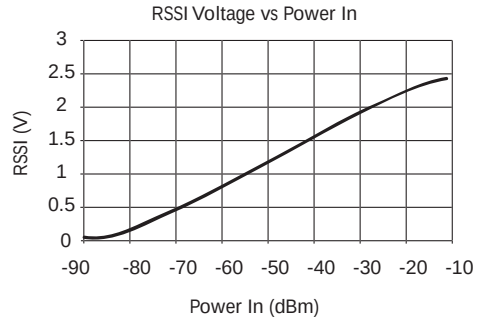


Figure 2. Typical RSSI Response

RECEIVE SIGNAL STRENGTH INDICATION (RSSI)

RSSI is an indication of field strength. It is typically used to control transmit power to conserve battery life. It may also be used to determine if a given channel is occupied. See Figure 2.

FILTER ALIGNMENT

In the first 62.5µs of RX mode the receiver is not functional. Instead, the ML2725 filter alignment function tunes all the internal filters using the reference frequency from the REF pin. See Figure 3.

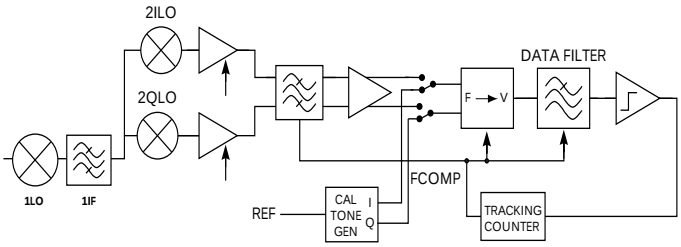


Figure 3. Filter Alignment

The IF filter, data filters, and the F-to-V converter all have their frequency responses governed by RC time constants. Capacitors that affects the frequency response includes a binary weighted capacitor array controlled by a 7 bit tuning bus. During calibration, a reference tone at the IF center frequency is routed to the F-to-V converter. A digital tracking loop then adjusts the tuning word until there is mid-rail output from the F-to-V converter. This tracking loop may take up to 256µs to tune the filter when XCEN is asserted, but the tracking loop will continue to make small adjustments whenever the ML2725 is in RXCAL mode. Because all the filters in the chip are tuned in this manner, centering the F-to-V converter sets up the correct center frequencies and bandwidths for the filters.

Data Slicer

The data slicer is a comparator that is AC coupled to the receive data filter output. The output is logic high or logic low. This circuit is designed to rapidly acquire valid data at the beginning of a received packet of data. The nominal time constant for the AC coupling is 9µs. This limits the maximum recommended run length to four ones or zeroes at 1.3Mbps.

Data Output Drive

The ML2725 DOUT pin is designed to drive a PCB trace and a single logic input with controlled slew rates. Buffer the output when driving any logic load greater than 5pF (*i.e.*, more than an ×10 oscilloscope probe or a single CMOS logic input pin).

MODES OF OPERATION (CONTINUED)

TRANSMIT MODE

TXCAL AND TRANSMIT

In TRANSMIT mode, the VCO is directly modulated with filtered FSK transmit data. The PLL is disabled or open, with the charge pump output tri-stated. This stops the PLL from contending with the applied modulation. The digital transmit data input is generated by external baseband circuits. This input signal is level shifted and filtered by the transmit modulation filter prior to modulating the VCO frequency. Due to the low leakage current of the charge pump and tank circuit the ML2725 can be in TRANSMIT mode for slot lengths of up to 10ms.

The transmit modulation filter is automatically tuned during the first part of every RX time (RXCAL) to remove the need for production alignment. When the chip is powered up (VDD first applied) the tuning information is reset to mid-range. The ML2725 should then be enabled with RXON high. The rising edge on XCEN will trigger a complete calibration of all the on chip filters, which takes 256ms. This ensures the modulation filters are aligned to prevent unwanted spurious emissions.

Prior to transmitting the PLL must tune to the intended RF center frequency of the transmission. This occurs in TXCAL mode. The Transmit modulation is disabled and any input on the DIN pin is ignored. The transmit output buffer is enabled during TXCAL mode. To prevent spurious emissions due to the PLL locking, any external TX/RX switch or PA should be disabled during TXCAL mode.

Transmitter Circuit Operation

The ML2725 transmitter is a 2-FSK transmitter using a directly modulated open loop VCO. See Figure 4. This type of transmitter is simple, low power, and well suited to a time-slotted system. The transmitter uses the stored VCO tuning voltage on the PLL loop filter to set the VCO frequency for the duration of the transmitter slot. The modulation is introduced through a second VCO tuning port. This modulation port has a much lower tuning sensitivity than the main tuning port in order to produce the ±500kHz FSK deviation at 2.4GHz. Compensation circuits stabilize the modulation deviation over the VCO tuning range, and internal logic manages the correct transition from TXCAL to TRANSMIT mode. The ML2725 design supports transmit slot lengths up to 10ms, and the time required to set up the transmit for a new slot (TXCAL mode) is typically 62.5µs.

The operating cycle of the transmitter starts with the falling edge of RXON. In the first 62.5µs after the falling edge of RXON, a calibration mode (TXCAL) is triggered. See Figure 5. The data filter input is zeroed and the PLL locks the VCO frequency to the desired RF channel center frequency. A CW signal at the selected RF channel frequency comes out of the Transmit RF output. When the PLLEN control line is de-asserted the transmitter starts its transition to TRANSMIT mode. The PLL charge pump is disabled, leaving the PLL loop filter to hold the correct tuning voltage for this channel. The data formatter injects an NRZ bipolar data waveform into the Transmit data filter. The Transmit data filter band-limits this waveform,

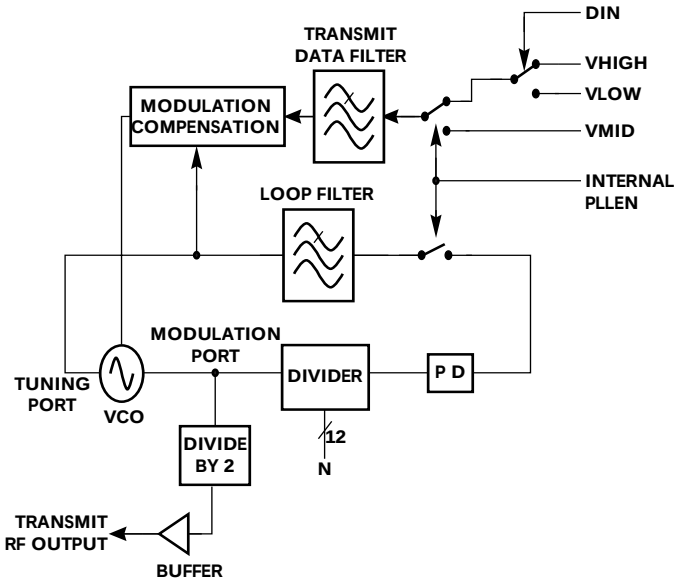


Figure 4. Transmitter Block Diagram

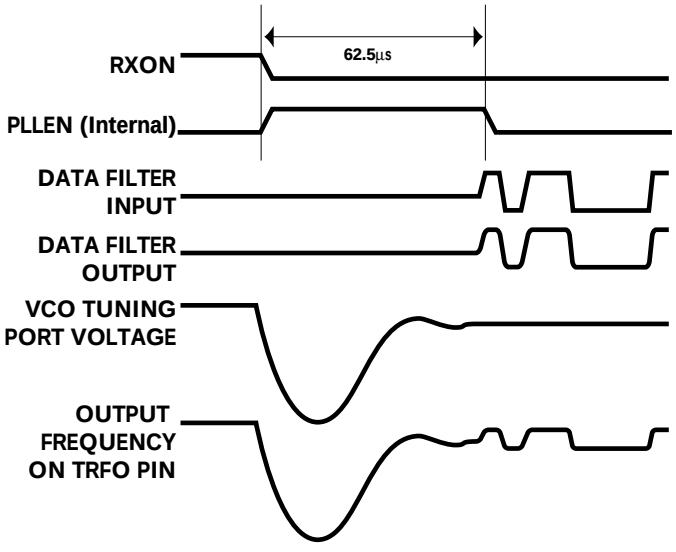
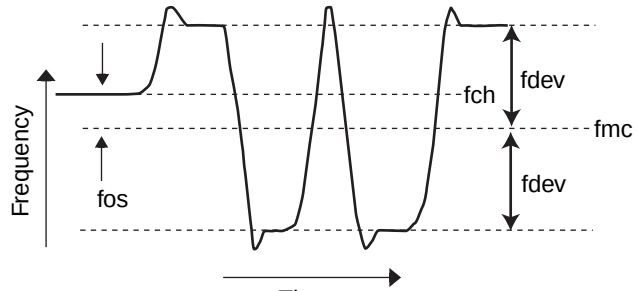


Figure 5. Transmitter Operating Cycle

MODES OF OPERATION (CONTINUED)

and feeds it to the modulation compensation circuits. These scale the modulation voltage (depending on the VCO tuning voltage) and drive the VCO tuning port with the scaled, filtered modulation. The voltage on the modulation port swings above and below its central value to produce 2-FSK modulation on the VCO (see Figure 6). The modulation filtering is sufficient to meet the FCC occupied bandwidth and out-of-band emissions requirements, and does not introduce significant ISI (Inter Symbol Interference).



fch= nominal channel center frequency
fdev= peak modulation frequency deviation, excluding overshoot
fmc= mean center frequency of modulated signal
fos= offset of fmc from nominal channel center, fch

Figure 6. Transmit Modulation

The Transmit modulation filter is a 5th order all-pole filter, designed for minimum differential group delay and good stop band attenuation at greater than 2MHz. The 3dB bandwidth of the filter is slaved to the reference frequency. See Table 3.

Parameter	Divide by 12 (RD0 = 1)
Transmit data filter nominal 3dB bandwidth	REF/8.8

Table 3. Data Filter Bandwidth Setting

Figure 7 shows an eye diagram recovered from the Transmit RF output of the transceiver with a data stream of 1.536Mb/s.

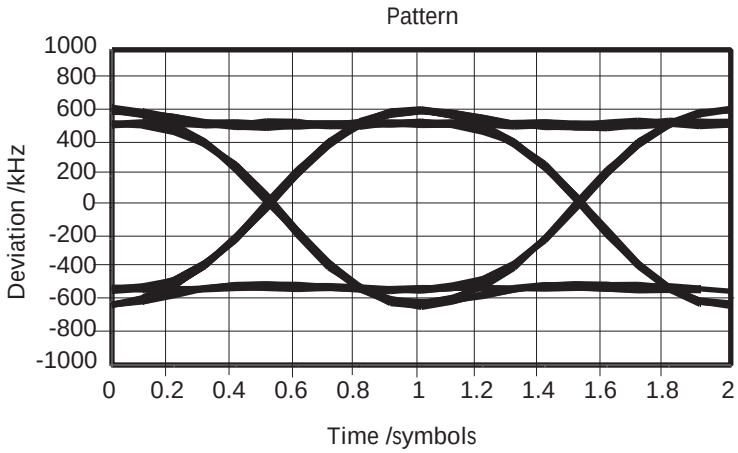


Figure 7. Transmitter Eye Diagram

For optimum performance we recommend that the second harmonic level reflected back into the output TRFO (pin 23), be less than -30dBm.

Transmitter Lockout (Low Voltage)

The ML2725 transmitter features a low voltage lockout circuit to meet spurious emissions requirements. At low supply voltage the VCO frequency may be disturbed, and the radio could transmit on an out-of-band signal. To prevent this a comparator monitors the supply voltage and trips a transmitter shutdown latch if the supply voltage drops below 2.6V. This disables the transmitter output buffer. The latch is reset by the next falling edge of RXON so that the radio cannot transmit until the next complete transmitter cycle (see Figure 8). If the ML2725 is DC powered on with RXON low, the transmitter buffer will be latched off. This helps prevent unwanted emissions.

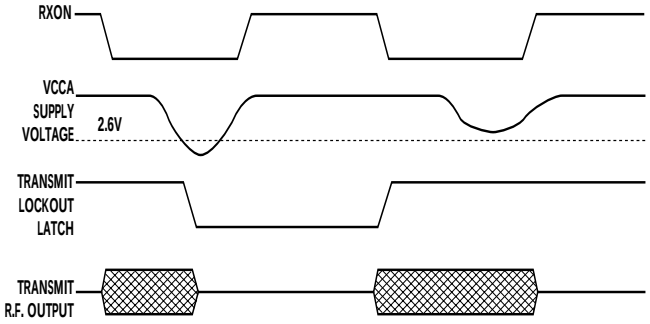


Figure 8. Transmitter Low Voltage Lockout Sequence

Programming the ML2725 integrated PLL.

For ease of use, the ML2725 PLL is programmed to the set RF center frequency of operation of the radio. See Figure 9. The RF output center frequency is half the VCO frequency during transmission. The VCO is automatically offset by two-thirds the IF, to give the correct receive LO frequency, during reception. The baseband circuits need not reprogram the PLL for every receive or transmit packet. The PLL divide register should be programmed with a binary integer which represents the desired RF channel frequency divided by 1.024MHz when using a 12.288MHz reference frequency.

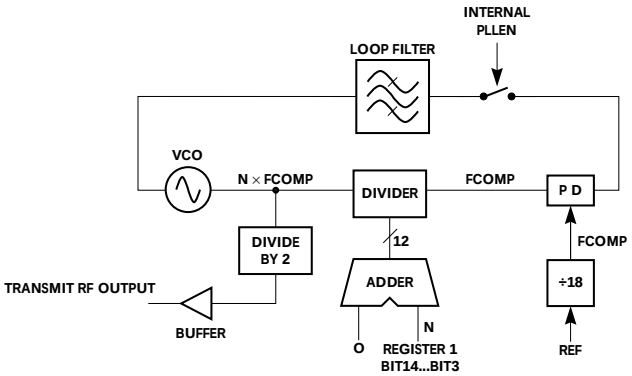


Figure 9. Phase Locked Loop in Transmit Mode

MODE OF OPERATION (CONTINUED)

When in TRANSMIT mode the PLL is disabled and the loop opened to allow modulation of the VCO. The VCO runs at two thirds the channel frequency, and the Transmit RF output is taken from one output of the quadrature divider. The PLL locks during TXCAL mode.

The frequency plan for the PLL and VCO transmit is given in Table 4.

When in RECEIVE mode the PLL frequency is set to give a LO frequency equal to two-thirds the desired RF channel frequency plus the IF frequency. The VCO signal is divided by two to provide the quadrature LO for the image reject down convert mixer. The PLL locks during RXCAL mode, and remains locked in RX mode. (See Figure 10.)

The 638kHz frequency shift is achieved by internally adding an offset of +1 counts to the PLL divider register value. The relationship between the LO frequency, the programmed RF channel frequency, and the reference frequency in RECEIVE mode is given in Table 5.

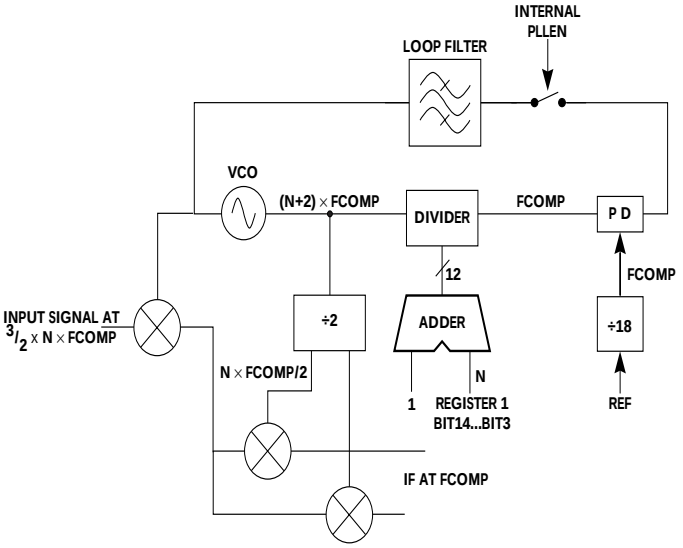


Figure 10. Phase Locked Loop in Receive Mode

Parameter	Value Formula	Definitions
RF channel frequency register	N	2048 ≤ N ≤ 4093 for the complete divider range 2344 ≤ N ≤ 2430 for the 2.4GHz ISM band
Transmit RF output frequency	N x (FCOMP/2)	Covers the range from 800 to 833MHz
PLL division ratio	N	The frequency division between the VCO and the phase comparator
VCO frequency	N x FCOMP	Range is 1.60 to 1.66GHz
PLL comparison frequency	FCOMP (683kHz)	Rate of charge pump pulses at charge pump output (QPO). REF input frequency divided by 18
Frequency resolution	FCOMP/2	At transmit RF output

Table 4. Transmit Mode Frequency Relationsships

Parameter	Value/Formula	Definitions
RF channel frequency register	N	2048 ≤ N ≤ 4093 for the complete divider range 2344 ≤ N ≤ 2430 for the 2.4GHz ISM band
Channel frequency	N x 3 x (FCOMP/2)	Covers the range from 2.4 to 2.5GHz
1LO frequency	(N + 1) x FCOMP	At the LO port of the receiver 1st mixer
2LO frequency	(N + 1) x (FCOMP/2)	At the LO port of the receiver 2nd mixer
IF frequency	1.024MHz	Difference between LO frequency and channel frequency
PLL division ratio	N + 1	The frequency division between the VCO and the phase comparator
VCO frequency	(N + 1) x FCOMP	Range is 1.60 to 1.66GHz
PLL comparison frequency	FCOMP (683kHz)	Rate of charge pump pulses at charge pump output (QPO) FREF input frequency divided by 18
Frequency resolution	3 x FCOMP/2	At Receive RF input

Table 5. Receive Mode Frequency Relationships

MODE OF OPERATION (CONTINUED)

VCO OPEN AND CLOSED LOOP OPERATION

Normally the PLL is only operational in the first 62.5µs of RX, when a closed loop PLL is formed. The PLL is a conventional single loop integer division PLL. The phase comparator has a charge pump output so that an external passive loop filter can be used. The PLL dividers support integer main divider ratios between 2048 and 4093, and reference divider ratios of 9 and 18.

In RECEIVE and TRANSMIT modes the PLL loop is opened and the stored VCO tuning voltage (on the loop filter) maintains the VCO at the desired frequency. In open loop modes the PLL charge pump is shut off and the PLL circuits are shut down to save power. Interlock logic manages the start up and shut down of the PLL to ensure that the VCO frequency is not disturbed in the transition between modes. If better frequency stability is required the RXCL bit in the PLL configuration register allows the PLL to remain in the closed loop mode during RECEIVE mode. The PLL loop must be opened in TRANSMIT mode, as the PLL would otherwise attempt to remove the FM transmit modulation.

PLL LOOP FILTER DESIGN

The PLL loop filter performs a dual function. In the closed loop modes (RXCAL and TXCAL) it acts as a second order loop filter, and in the open loop modes (TRANSMIT, RECEIVE without RXCL) it holds the VCO tuning voltage for the duration of the data slot. The correct loop filter component values are a function of the desired closed loop bandwidth, loop response damping factor charge pump current, VCO tuning sensitivity and PLL division ratio. The charge pump current, VCO tuning sensitivity, and division ratio range are fixed by the on chip circuits, so the only independent variables are the PLL's closed loop bandwidth and damping factor.

The recommended values of 10nF, 820Ω and 560pF give a 38kHz closed loop bandwidth and a nominal damping factor of 0.71 for robust closed loop operation. Ceramic capacitors can be used, but care should be taken with applications where there is significant thermal or mechanical shock.

STANDBY MODE

In STANDBY the ML2725 transceiver is powered down. The only active circuits are the control interfaces, which are static CMOS to minimize power consumption. The serial control interface (and control registers) remain powered up and will accept and retain programming data as long as the digital supply is present. The ML2725 serial control registers should be loaded with control and configuration data before any active mode is selected. The filter alignment registers are reset at power up.

TEST MODE

Special test access circuitry is needed for IC production test and radio debugging because of the RF to digital functionality of the ML2725. Two analog test outputs (TPI and TPQ) are multiplexed with the RSSI and transmit power control (TPC) output pins, and digital test outputs are multiplexed onto the received data output pin (DOUT). The test multiplexers are controlled by a test register accessed over the serial control bus.

CONTROL INTERFACES

There are two control interfaces:

Parallel mode control

Controlling the mode of operation of the ML2725. Refer to the Operational Modes section for details.

Serial Interface

Programing the PLL signal and reference dividers, internal test modes, and filter alignment.

Other signal interfaces to the IC are:

- Receiver data output
- Transmit modulation data input
- Receive RF input, the input to the receiver circuits
- Transmit RF output, the output for the modulated RF signal
- Received signal strength output: RSSI indicates the power of the received signal
- Reference frequency input for PLL dividers
- TPC: open drain transmit power control output
- PAON: control output to off-chip power amplifier

Serial Bit Allocations

Data words are entered beginning with the MSB. The word is divided into a leading 14-bit data field and a 2-bit address field. When the address field has been decoded the destination register is loaded on the rising edge of EN. Providing less than 16 bits of data will result in unpredictable behavior when EN goes high.

Parallel Interface

The chip is enabled by the XCEN (Transceiver enable) signal. The operating mode is set by the control line RXON (switches the chip between transmit and receive modes), and the 3 wire serial data bus. The logic for XCEN and RXON which is given in Table 6.

XCEN	RXON	Mode Name	Chip Mode
0	X	Standby	Programming retained, powered down
1	0	TX	Transmit synthesizer open loop and modulated
1	1	RX	Receive on

Table 6. Control Logic

CONTROL INTERFACES AND REGISTER DESCRIPTION

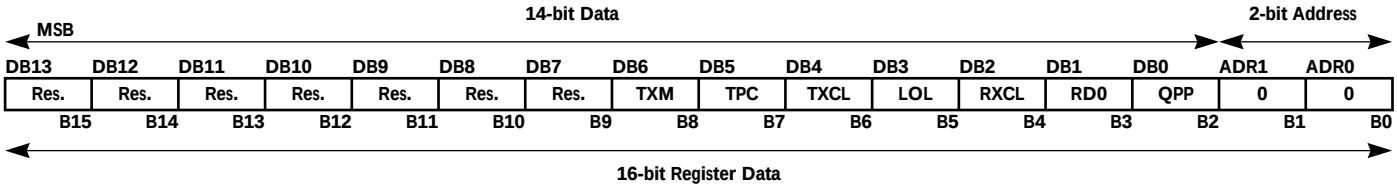
REGISTER INFORMATION

A unidirectional three wire serial bus is used to set the ML2725's transceiver parameters and to program the PLL circuits. Programming is performed by entering 16-bit words into the ML2725 serial interface. Three 16-bit registers are partitioned such that 14 bits are dedicated for data to program the operation and 2 bits are used for register addressing. The purpose of each of the registers is:

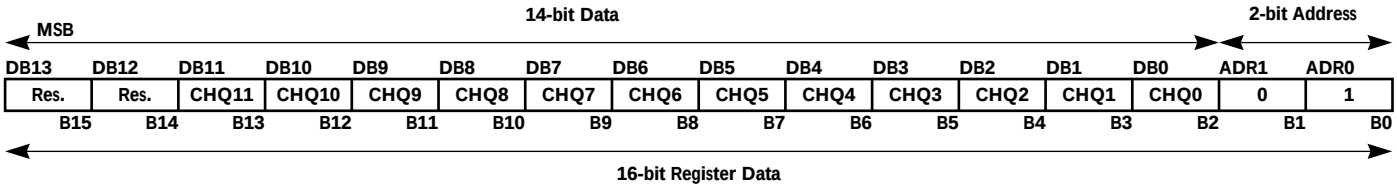
- Register 0: PLL configuration
- Register 1: PLL tuning data
- Register 2: Internal test access

Table 7 shows a register map. Tables 8A-C provide detailed diagrams of the register organization: Table 8A and 8B outline the PLL configuration and channel frequency registers and Table 8C displays the filter tuning and test mode register.

Register 0: PLL Configuration Register



Register 1: RF Channel Frequency Register



Register 2: Filter Tuning Select and Test Mode Access Register

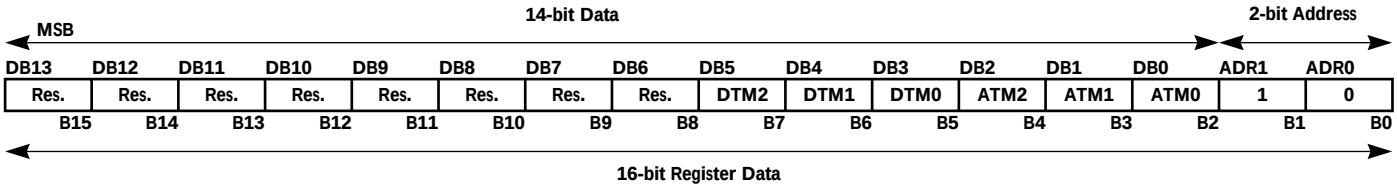


Table 7. Register Organization

CONTROL INTERFACES AND REGISTER DESCRIPTION (continued)

Data Bit	Name	Description	Use
B15 (MSB) / DB13	Reserved	Reserved	Set All Bits to 0 (zero)
B14 / DB12	Reserved	Reserved	
B13 / DB11	Reserved	Reserved	
B12 / DB10	Reserved	Reserved	
B11 / DB9	Reserved	Reserved	
B10 / DB8	Reserved	Reserved	
B9 / DB7	Reserved	Reserved	
B8 / DB6	TXM	TX RF Output Mode	0: TX RF Output active during TXCAL mode 1: TX RF Output shut off during TXCAL mode
B7 / DB5	TPC	Transmit Power Control	0: TPC pin high impedance 1: TPC pin pulled to ground
B6 / DB4	TXCL	Transmit Test Mode	0: FSK modulation in Transmit mode 1: CW (no modulation) in Transmit mode
B5 / DB3	LOL	PLL Frequency Shift	0: LO shift is 0Hz for Transmit, 1.024MHz for Receive 1: LO shift is 1.024MHz for Transmit, 0Hz for Receive
B4 / DB2	RXCL	PLL Mode in Normal Receive Operation	0: PLL open loop during Receive 1: PLL closed loop during Receive
B3 / DB1	RD0	Reference Frequency Select	0: 6.144MHz nominal reference frequency 1: 12.288MHz nominal reference frequency (preferred)
B2 / DB0	QPP	PLL Charge Pump Polarity	0: Freq. sig. < freq. ref.; Charge pump sources current 1: Freq. sig. < freq. ref.; Charge pump sinks current
B1 / ADB1	ADR1	MSB Address Bit	ADR1 = 0
B0 (LSB) / ADB0	ADR0	LSB Address Bit	ADR0 = 0

Table 8A. Register 0 — PLL Configuration Register

Data Bit	Name	Description	Use
B15 (MSB) / DB13	Reserved	Channel frequency select bits	Set all bits to 0 (zero)
B14 / DB12	Reserved		
B13 / DB11	CHQ11		Divide ratio = f_C/1.024
B12 / DB10	CHQ10		
B11 / DB9	CHQ9		
B10 / DB8	CHQ8		
B9 / DB7	CHQ7		
B8 / DB6	CHQ6		
B7 / DB5	CHQ5		
B6 / DB4	CHQ4		
B5 / DB3	CHQ3		
B4 / DB2	CHQ2		
B3 / DB1	CHQ1		
B2 / DB0	CHQ0		
B1 / ADR1	ADR1	MSB Address bit	ADR1 = 0
B0 (LSB) / ADR0	ADR0	LSB Address bit	ADR0 = 1

Table 8B. Register 1 — Channel Frequency Register

CONTROL INTERFACES AND REGISTER DESCRIPTION (continued)

Data Bit	Name	Description	Function
B15 (MSB) / DB13	Reserved	Reserved	Set All Bits to 0 (zero)
B14 / DB12	Reserved		
B13 / DB11	Reserved		
B12 / DB10	Reserved		
B11 / DB9	Reserved		
B10 / DB8	Reserved		
B9 / DB7	Reserved		
B8 / DB6	Reserved		
B7 / DB5	DTM2	Digital Test Control Bits	See Table 11
B6 / DB4	DTM1		
B5 / DB3	DTM0		
B4 / DB2	ATM2	Analog Test Control Bits	See Table 10
B3 / DB1	ATM1		
B2 / DB0	ATM0		
B1 / ADB1	ADR1	MSB Address Bit	ADR1 = 1
B0 (LSB) / ADB0	ADR0	LSB Address Bit	ADR0 = 0

Table 8C. Register 2 — Filter Tuning Select and Test Mode Register

CONTROL INTERFACES AND REGISTER DESCRIPTION (continued)

Serial Interface

Data and clock signals are ignored when EN is high. When EN is low data on the DATA pin is clocked into a shift register by rising edges on the CLK pin. The information is latched when EN goes high. This serial interface bus is similar to that commonly found on PLL devices. It can be efficiently programmed by either byte or 16-bit word oriented serial bus hardware. The data latches are implemented in static CMOS and use minimal power when the bus is inactive. Figure 11 and Table 9 provide timing and register programming illustrations.

Symbol	Parameter	Time (ns)
t_R	Clock input rise time	15
t_F	Clock input fall time	15
t_{CK}	Clock period	>50
t_W	Minimum pulse width	2000
t_D	Delay from last clock falling edge	>15
t_{SE}	Enabel setup time to ignore next rising clock	>15
t_S	Data-to-clock setup time	>15
t_H	Data-to-clock hold time	>15

Table 9. 3-Wire Bus Timing Characteristics

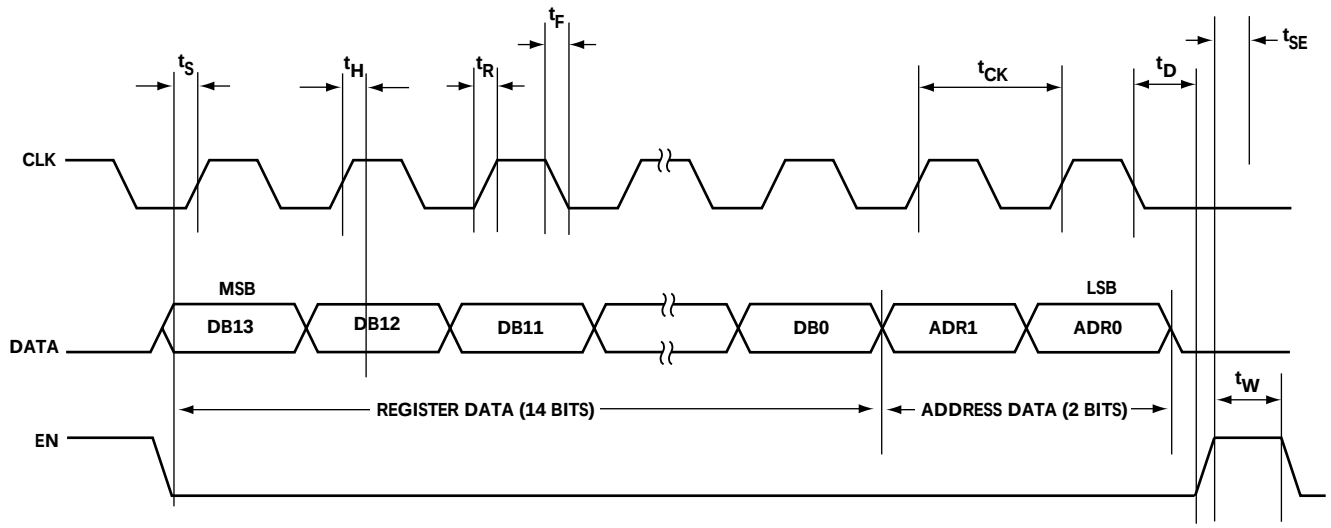


Figure 11. Serial Bus Timing for Address and Data Programming

CONTROL INTERFACES AND REGISTER DESCRIPTION (continued)

CONTROL REGISTER DESCRIPTIONS

Power On State

All register values are set to 0 (zero) on Power Up. Power up is defined as occurring when VDD (pin 31) ≥ 2.0V (typical). The register default values are valid after power up. The PLL divide ratio and PLL configuration registers must be programmed before XCEN is asserted for the first time.

Address and Data Bits (ADR)

Each of the three registers are identically configured. Each is divided into a fourteen (14) bit data field and a two (2) bit address field. The sixteen bits are input serially (see Figure 11) with the fourteen data bits, most significant bit (DB13) first followed by the two address bits, most significant bit (ADR1) first. The last sixteen bits clocked into the ML2725 will be loaded into the specified register. Lading less than sixteen bits into any register will cause unpredictable device functionality.

RES Bit Locations (Reserved)

Bits identified as reserved must always have a logic 0 (zero) value for correct device operation. Power-on reset clears all reserved bits to zero. Each reserved bit must be programmed to logic zero whenever any of the three registers are reprogrammed.

REGISTER #0 PLL CONFIGURATION

PLL Charge Pump Polarity (QPP): DB0

This bit sets the charge pump polarity to sink or source current. For a majority of applications this bit is cleared (QPP = 0). For applications where an external amplifier is in the loop filter the bit is set to 1 to change the charge pump polarity (see Table 10).

QPP	PLL Charge Pump Polarity
0	Frequency signal < frequency reference Charge pump sources current
1	Frequency signal < frequency reference Charge pump sinks current

Table 10. PLL Charge Pump Polarity

Reference Divide Bit Zero (RD0): DB1

This bit sets the reference division of the PLL to either 9 or 18 (see Table 11).

RD0	Reference Division	Nominal Reference Frequency
0	9	6.144MHz
1	18	12.288MHz (preferred)

Table 11. Reference Frequency Select

Receive Closed Loop Bit (RXCL): DB2

This bit is used in Receive mode to put the PLL into either open loop or closed loop (see Table 12).

RXCL	Receive PLL Mode
0	PLL open loop
1	PLL closed loop

Table 12. PLL Mode in Normal Receive Operation

PLL Frequency Shift Bit (LOL): DB3

LO shift for transmit and receive. For normal operations, it is recommended that LOL = 0 (see Table 13).

LOL	LO Shift for Transmit	LO Shift for Receive
0	0	+1.024MHz
1	+1.024MHz	0

Table 13. PLL Frequency Shift

Transmit Closed Loop Bit (TXCL): DB4

Used to produce a continuous CW transmitter output for product test with RXON low (see table 14).

TXCL	Transmit PLL Mode
0	PLL Open Loop, FSK Output
1	PLL Closed Loop, CW Output

Table 14. PLL Mode in Transmit Operation

Transmit Power Control Bit (TPC): DB5

Controls the state of the TPC/TPQ open drain output (pin 7). Although this bit may be set at any time, the TPC/TPQ pin only changes state at the falling edge RXON (see table 15).

TPC	TPC Pin State
0	High Impedance
1	Pulled to Ground

Table 15 TPC Pin State

Transmit RF Output Mode (TXM): DB6

Controls the TX RF buffer state during TXCAL mode. Should be set to 0 for normal operation (see table 16).

TXM	TXRF Buffer Behavior
0	RF Output Always in TX and TXCAL Mode
1	RF Output Inhibited During PLL Lock (TXCAL Mode)

Table 16. TXM Mode

CONTROL INTERFACES AND REGISTER DESCRIPTION (continued)

REGISTER #1
CHANNEL FREQUENCY REGISTER

Channel frequency selection bits (CHQ): <DB11:DB0>

These bits set the channel frequency for the transceiver (see Table 17). With the recommended 12.288MHz input to the REF (pin 9), the channel frequency value is calculated by multiplying the CHQ value by 1.024. A 1.024MHz offset is automatically added in the receiver mode to accommodate the IF frequency. The recommended operating range value of the CHQ is from 1,024 (400_{hex}) to 4,093 (FFD_{hex}). These bits should be programmed to a valid channel frequency before XCEN is asserted.

The divide ratio is calculated as $f_C/1.024$, where f_C is the channel frequency in MHz.

$$\text{Divide Ratio} = \frac{f_C}{1.024}$$

A 1.024MHz offset is automatically added in the Receive mode.

B15	B14	B13 to B2	B1	B0
0	0	PLL divide ratio	0	1

Table 17. Main Divider

REGISTER #2
FILTER TUNING SELECT TEST MODE

Analog Test Control Bits (ATM): <DB2:DB0>

The test mode selected is described in Table 18. The performance of the ML2725 is not specified in these test modes. Although primarily intended for IC test and debug, they can also help in debugging the radio system. The default (power up) state of these bits is ATM<2:0> = <0,0,0>. When a non-zero value is written to the field, RSSI/TPI (pin 28) and TPC/TPQ (pin 7) pins become analog test access ports giving access to the outputs of key signal processing stages in the transceiver. During normal operation the ATM field should be set to zero.

ATM2	ATM1	ATM0	RSSI/TPI	TPC/TPQ
0	0	0	RSSI	TPC (PA Control)
0	0	1	No Connect	
0	1	0	IF filter Output	
0	1	1	IF Buffer Output	
1	0	0	IF Buffer Output	
1	0	1	Data Slicer Input	
1	1	0	IF Limiter Outputs	
1	1	1	1.67V Ref.	VCO Mod. Voltage

Table 18. Analog Test Control Bits

Digital test control bits (DTM) <2:0>

The DTM<2:0> bits function is described in Table 19. The performance of the ML2725 is not specified in these test modes. Although primarily intended for IC test and debug, they can also help in debugging the radio system. The default (power up) state of these bits is DTM<2:0> = <0,0,0>. When a non-zero value is written to these fields the DOUT (pin 32) becomes a digital test access port for key digital signals in the transceiver. During normal operation the DTM field should be set to zero.

DTM2	DTM1	DTM0	DOUT
0	0	0	Demodulated data
0	0	1	Receiver AGC state
0	1	0	PLL main divider output
0	1	1	PLL reference divider output

Table 19. Digital Test Control Bits

CONTROL INTERFACES (continued)

TRANSMIT AND RECEIVE DATA INTERFACES

The DIN and DOUT pins are CMOS logic level for serial data that correspond to FSK modulation on the radio channel. The ML2725 is designed to operate as an FSK transceiver in the 2.4GHz ISM band. The chip rate, bit rate and spreading code are determined in the baseband processor, and the FM deviation and transmit filtering are determined in the transceiver.

DIN provides data to the Transmit data filter, which band limits the transmitted chips before they are FM modulated. There is no re-timing of the chips, so the transmitted FSK chips take their timing from the DIN pin. In the Receive chain FM demodulation, data filtering, and data slicing take place in the ML2725 receiver, with chip, bit and word rate timing recovery performed in the baseband processor.

RSSI AND REF

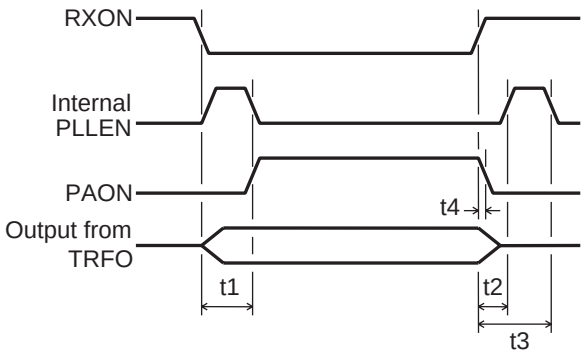
There are two other interface pins between the ML2725 transceiver and the baseband IC: the RSSI/TPI (pin 28) and REF (pin 9).

REF is the master reference frequency for the transceiver. It supplies the frequency reference for the RF channel frequency and the filter tuning. The REF pin is a CMOS input with internal biasing resistors. It can be AC coupled through a 470pF coupling capacitor to a sine wave source of at least 2.0V peak-to-peak. The REF input can also be driven by a CMOS logic output. The PLL comparison and the IF filter center frequency are both equal to the REF input frequency divided by 18. The IF filter and data filter bandwidths track the IF filter center frequency.

The Received Signal Strength Indicator (RSSI/TPI) pin supplies a voltage indicating the amplitude of the received RF signal. It is normally connected to the input of a low speed ADC on an external baseband IC, and is used during channel scanning to detect clear channels on which the radio may transmit. The RSSI voltage is proportional to the logarithm of the received power level. A voltage of 0V to 2.5V corresponds to an RF input power of -85 to -15dBm with a nominal slope of 35mV/dbB.

CONTROL OUTPUTS TO THE PA – PAON AND TPC

The ML2725 has two output pins to control and sequence the power amplifier – PAON and TPC (see Figure 12).



Symbol	Parameter	Time/µs
t1	RXON falling edge to PAON rising edge	62.5
t2	RXON rising edge to PLL recalibration	6.5
t3	RXON rising edge to receive mode	70
t4	RXON rising edge to PAON falling edge	<0.1

Figure 12. Power Amplifier Interface

The PAON (PA control) is a CMOS output to control an off chip RF PA (power amplifier). It outputs a logic high when the PA should be enabled, and a logic low at all other times. This output is inhibited if the PLL fails to lock, or the power supply to the ML2725 falls below 2.6V. The PLL lock detect or low voltage signals are latched, so that the transmitter is inhibited for the entire transmit slot. These latches are reset at the end of the transmit slot, so that the ML2725 will transmit in the next slot following a transient fault condition.

The TPC/TPQ (pin 7) is an open drain output intended for transmit power control. It is controlled by the TPC bit in serial bus register 0. This bit can be changed at any time, but the TPC pin will not change state until the beginning of the next transmit slot, triggered by a falling edge on RXON.

In analog test modes the RSSI and TPC pins become analog test access ports that allow the user to observe internal signals in the ML2725.

RF INTERFACES

The RRFI receive input (pin 21) and the TRFO transmit output (pin 23) are the only RF I/O pins. The RRFI pin requires a simple impedance matching network for best input noise figure, and the TRFO pin is matched to 50Ω by an AC coupling capacitor. The associated RF input and output ground pins must have direct connections to an RF ground plane, and the RF block supply pins must be well decoupled to the RF ground pins.

APPLICATIONS

The ML2725 operates in the 2.4 to 2.48GHz ISM band under FCC Part 15, section 247 or section 249. For Cordless telephone applications under part FCC 15 section 247 the ML2725 is used as a Direct Sequence Spread Spectrum (DSSS) transceiver with chip rates up to 1.536M chips per second. The ML2725 is used alone for short range high data rate applications under FCC Part 15 section 249.

LOW POWER STAND ALONE

The ML2725 can be used alone with a trippler as an FSK radio transceiver. Only an external PIN diode TX/RX switch and antenna filtering are required. The 0dBm (typical) output makes full use of the FCC Part 15, section 247 or section 249 transmitted field strength limits. Bit rates from 1.0M bits per second to1.5M bits per second are feasible. The data slicer achieves full performance with run lengths up to 4 consecutive 1 or 0 bits at 1.3 to 1.5M bits per second (3 consecutive bits at 1Mbps). This constraint can be met with run length limited coding, which also simplifies the clock recovery circuits.

GAMES, GADGETS AND GISMOS

Many applications require short range (<30 feet), battery operation of transceivers at modest data rates. The fast wake-up time of the ML2725 extends battery life. The ML2725 can sleep the majority of the time, wake up in less than 300µs, transmit a burst of data at up to 1.5M bits per second and go back sleep. The data throughput is the same as a low data rate radio, with considerable savings in battery power. The Receive Signal Strength Indicator (RSSI) function allows listen before talk (receive before transmit) to avoid interference on active channels and increase battery life.

A power amplifier extends the range of the ML2725 to 1000 feet or more and increases the robustness of the radio system depending on conditions. This complies with regulatory requirements at higher powers using Direct Sequence Spread Spectrum (DSSS) at 1.5M chips per second and a 100K bits per second data rate. The extra 11.6 dB of DSSS conversion gain generated by a 15 bit chipping sequence produces better performance in range or difficult interference environments. The Receive Signal Strength Indicator (RSSI) function allows listen before talk (receive before transmit) to avoid interference on active channels as well as conservation of battery and transmit power at short range.

DSSS CORDLESS TELEPHONE

The ML2725 requires a suitable digital baseband processor to operate in this mode. The baseband processor spreads the digital data (at up to 150kbytes/s) using an 11 to 15 bit chip sequence. This composite baseband signal (at up to 1.536M chips per second) is fed to the ML2725 DIN input. The ML2725 transmit circuits low pass filter the baseband signal and FM modulate the transmit RF output. The transmitted signal is a Direct Sequence-FSK signal which meets the FCC requirements for >10dB processing gain and a 6dB bandwidth >500kHz. It is a constant envelope signal which can be amplified in an efficient Class C power amplifier without suffering spectral regrowth. The ML2725 receive circuits downconvert, filter, and demodulate the FM signal to recover the original spread spectrum baseband signal. The baseband processor de-spreads this signal and recovers the lower data rate signal with a correlator. To extend the range in this DS-FSK mode a transmit power amplifier and receive low noise amplifier are used.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

VDD, VCC2, VCC5 ..... 6.0V
VSS, GND ..... 0 ±0.3V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10s) ..... 260°C

OPERATING CONDITIONS

Normal Temperature Range ..... -10°C to 60°C
VDD, VCC2, VCC5 Range ..... 3.0V to 5.5V
(VDD ≤ VCC2, VCC5)
Thermal Resistance (θ_{JA}) (Note 2) ..... 100°C/W

ELECTRICAL TABLES

Unless otherwise specified, VCC5 & VDD = 3.0V to 3.8V, TA = Operating Temperature Range. (Note 1)
12.288MHz reference frequency input

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER CONSUMPTION						
	All Circuits, Standby Mode			10	100	µA
	Receive Cal	at 25°C	37.50	57	71	mA
	Receive	at 25°C	30.75	48	59	mA
	Transmit Cal	at 25°C	36	48	61.5	mA
	Transmit	at 25°C	30	47	59	mA
	All Circuits, Standby Mode	VCC5=3.0 to 5.5V, VDD=3.0V to 4.5V		10	200	µA
	Receive Cal	at 25°C, VCC5=3.0V to 5.5V, VDD=3.0V to 4.5V	37.50	57	76	mA
	Receive	at 25°C, VCC5=3.0V to 5.5V, VDD=3.0V to 4.5V	30.75	48	64	mA
	Transmit Cal	at 25°C, VCC5=3.0V to 5.5V, VDD=3.0V to 4.5V	36	48	66.5	mA
	Transmit	at 25°C, VCC5=3.0V to 5.5V, VDD=3.0V to 4.5V	30	47	64	mA
VCO AND LO PLL						
	LO output frequency	In 341.3kHz steps	800.7		833	MHz
	Phase noise at driver output 1.2MHz 3MHz >7MHz	VCO phase locked, loop band width 50kHz. Discontinuities, other than reference spurs, not allowed.		 -95 -115 -125		dBc/Hz
	LO PLL reference frequency at phase detector	PLL main divider input is at 1.63GHz		682.67		KHz
	LO division range integer	PLL divider limits	1024		4093	count
	LO charge pump sink/source current			5.5		mA
	LO lock up time for Transmit/Receive frequency change	From RXON asserted		50		µs
	LO lock up time for channel switch	From EN asserted, any channel change in band		100		µs
	LO lock up time from sleep	From XCEN, PLL dividers programmed		240		µs
	Reference signal input level	12.288MHz sine wave, capacitively coupled	2.0		3.0	Vp-p

ELECTRICAL TABLES (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
RECEIVE CHAIN						
	Receive RF input noise figure			19	25 (Note 2)	dB
	Receive RF input level	For better than 12.5% CER	-84 (Note 2)	(-92)	+5	dBm
	Receive RF input IP3	Test tones 2 and 4 channels away		-15		dBm
	Receive conducted in-band from RF input			–80	–50	dBm
	Receive RF input impedance	2445MHz		6-j15		Ω
	Receive RF mixer image rejection	Measured at 3.5MHz offset		35		dB
	Receive adjacent channels rejection @ 2.048MHz channel spacing	–80dBm wanted signal level less than 12.5% CER (A single interferer with 2GFSK modulation to give a -20dBc bandwidth of 1.5MHz.) 1 channel 2 channels 3 or more channels		 15 40 45		 dB
IF FILTERS						
	IF filter center frequency	After 300µs of realignment		1.024		MHz
	IF filter attenuation at 320kHz	Within 10ms of alignment, referenced to 1024kHz	1.0	3	4.2	dB
	IF filter attenuation at 1725kHz	Within 10ms of alignment referenced to 1024kHz	1.0	3	4.2	dB
LIMITER, AGC AND FM DEMODULATOR						
	Recovery from overload	From 0dBm at input		5	12	µs
	Eb/No	For 12.5% CER		3	4.5 (Note 2)	dB
	Co-channel rejection, 12.5% CER	–80dBm, modulated with 1.536 Mb/s GFSK, BT = 0.5, PRBS data		4		dB
	AM tolerance for 12.5% or better CER	–80dBm wanted signal, AM modulation depth at 100kHz rate		90		%
RSSI PERFORMANCE						
	RSSI rise time: <–100dBm to –15dBm into the IF mixer	20pf load, 20% to 80%	1	5.3	10	µs
	RSSI fall time: <–15dBm to –100dBm into the IF mixer	20pf load, 20% to 80%	1	4.4	10	µs
	RSSI maximum voltage	–15dBm in	2.0	2.5		V
	RSSI minimum voltage	No signal		0.05		V
	RSSI sensitivity, mid range		28	35	42	mV/dB
	RSSI maximum signal	Sensitivity >50% mid range		–15		dBm
	RSSI minimum signal	Sensitivity >50% mid range		–85		dBm
	RSSI accuracy	Measured at -40dBm input power	1.3	1.6	1.9	V
RECEIVER SETTLING TIME						
	From RXON high to valid data	(transmit to receive time)			120	µs

ELECTRICAL TABLES (continued)

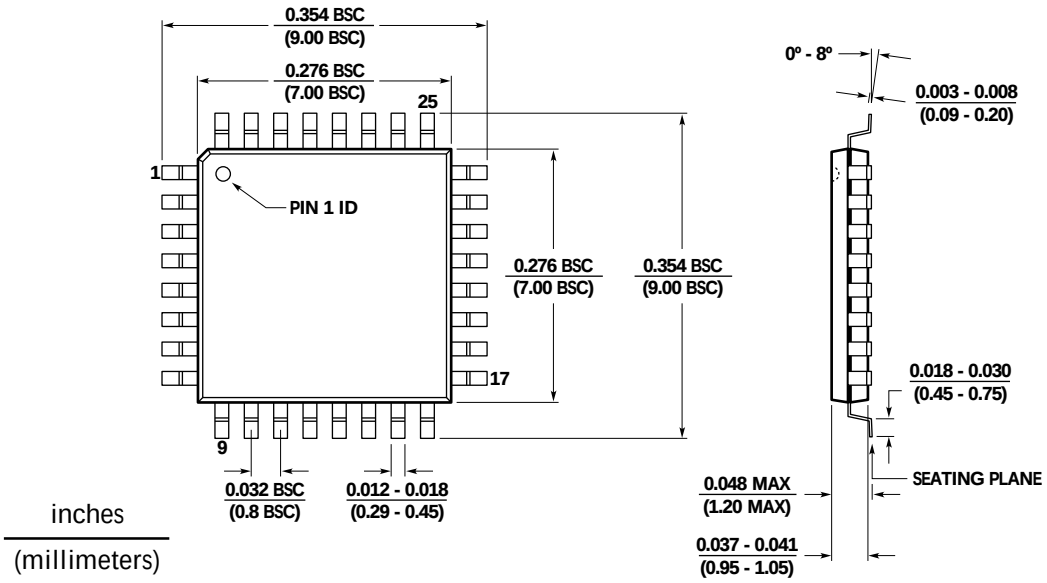
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
RECEIVE DATA FILTER						
	Bandwidth	3dB nominal		770		kHz
TRANSMIT RF DRIVER						
	Driver amplifier output power	Into 50Ω	-4.5	0	+3.2	dBm
	Driver amplifier output return loss	815MHz		14		dB
TRANSMIT MODULATION						
fdev	Modulation deviation, internal VCO/2	5 consecutive 1 or 0 bits	133	167	207	kHz
fos	Modulation center frequency offset	Between 50µs and 20ms after RXON low	-50		+50	kHz
TRANSMIT DATA FILTER						
	Bandwidth	3dB nominal		1.4		MHz
INTERFACE LOGIC LEVELS						
	Input high voltage	(never exceed VDD)	0.75 x VDD		VDD	V
	Input low voltage				0.25 x VDD	V
	Input bias current		-5	0	+5	µA
	Input capacitance	(measured at 1MHz)		4	6	pF
	DOUT high voltage	Sourcing 0.1mA	VDD - 0.6	3.08		V
	DOUT low voltage	Sinking 0.1mA		0.18	0.6	V
	DOUT sink/source current			0.4		mA
INTERFACE TIMING						
	RX to TX switching time	Time from RXON low to PAON high		62.5	70	µs
	TX to RX switching time	Time from RXON high to receiver enabled		72	80	µs
	Channel switching time	Time from write to PLL tuning register (EN high) to receiver enabled		320	342	µs
	Chip enable time	From XCEN high to receiver enabled		320	342	µs

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

Note 2: Guaranteed by design.

PHYSICAL DIMENSIONS *(inches/millimeters)*

Package: H32-7
32-Pin (7 x 7 x 1mm) TQFP



inches
(millimeters)

Leads cannot exceed $\frac{0.004}{(0.102)}$ maximum coplanarity

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PUBLICATION	DATE
ML2725DH	–10°C TO 60°C	32 PIN TQFP 7MM BODY	DS2725-01	FEBRUARY 16, 2001

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