60 dB Range (100 nA to 100 µA) Low Cost Logarithmic Converter

ADL5306

FEATURES

Optimized for fiber optic photodiode interfacing
Measures current over 3 decades
Law conformance 0.1 dB from 100 nA to 100 µA
Single- or dual-supply operation (3 V to ±5.5 V total)
Full log-ratio capabilities
Temperature stable
Nominal slope of 10 mV/dB (200 mV/decade)
Nominal intercept of 1 nA (set by external resistor)
Optional adjustment of slope and intercept
Rapid response time for a given current level
Miniature 16-lead chip scale package (LFCSP 3 mm × 3 mm)
Low power: ~5 mA quiescent current

APPLICATIONS

Low cost optical power measurement
Wide range baseband logarithmic compression
Measurement of current and voltage ratios
Optical absorbance measurement

GENERAL DESCRIPTION

The ADL5306* is a low cost microminiature logarithmic converter optimized for determining optical power in fiber optic systems. The ADL5306 is derived from the AD8304 and AD8305 translinear logarithmic converters. This family of devices provides wide measurement dynamic range in a versatile and easy-to-use form. A single-supply voltage between 3 V and 5.5 V is adequate; dual supplies may optionally be used. Low quiescent current (5 mA typical) permits use in battery-operated applications.

I_{PD}, the 100 nA to 100 µA input current applied to the INPT pin, is the collector current of an optimally scaled NPN transistor that converts this current to a voltage (V_{BE}) with a precise logarithmic relationship. A second converter is used to handle the reference current, I_{REF}, applied to IREF. These input nodes are biased slightly above ground (0.5 V). This is generally acceptable for photodiode applications where the anode does not need to be grounded. Similarly, this bias voltage is easily accounted for in generating I_{REF}. The logarithmic front end's output is available at VLOG.

The basic logarithmic slope at this output is 200 mV/decade (10 mV/dB) nominal; a 60 dB range corresponds to a 600 mV output change. When this voltage (or the buffer output) is applied to an ADC that permits an external reference voltage to be employed, the ADL5306's 2.5 V voltage reference output at VREF can be used to improve scaling accuracy.

FUNCTIONAL BLOCK DIAGRAM

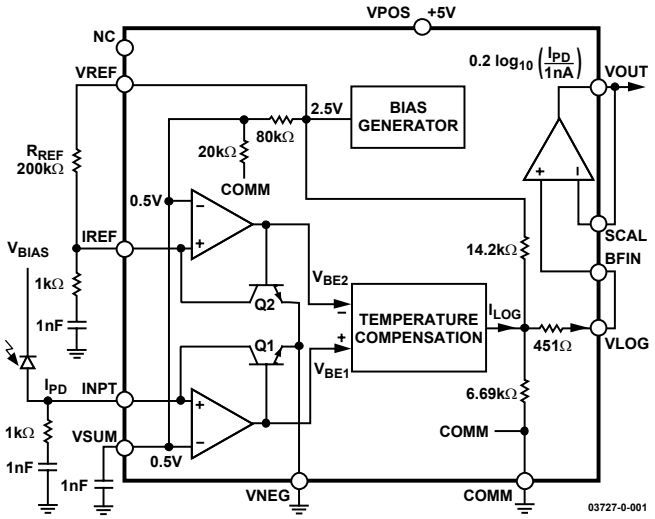

Figure 1. Functional Block Diagram

The logarithmic intercept (reference current) is nominally positioned at 1 nA by using the externally generated, 100 µA I_{REF} current provided by a 200 kΩ resistor connected between VREF, at 2.5 V, and IREF, at 0.5 V. The intercept can be adjusted over a narrow range by varying this resistor. The part can also operate in a log-ratio mode, with limited accuracy, where the numerator and denominator currents are applied to INPT and IREF, respectively.

A buffer amplifier is provided to drive substantial loads, raise the basic 10 mV/dB slope, serve as a precision comparator (threshold detector), or implement low-pass filters. Its rail-to-rail output stage can swing to within 100 mV of the positive and negative supply rails, and its peak current-sourcing capacity is 25 mA.

A fundamental aspect of translinear logarithmic converters is that small-signal bandwidth falls as current level diminishes, and low frequency noise-spectral density increases. At the 100 nA level, the ADL5306's bandwidth is about 100 kHz; it increases in proportion to I_{PD} up to a maximum of about 10 MHz. The increase in noise level at low currents can be addressed by using a buffer amplifier to realize low-pass filters of up to three poles.

The ADL5306 is available in a 16-lead LFCSP package and is specified for operation from–40°C to +85°C.

*Protected by US Patent 5,519,308.

Rev. 0

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Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADL5306 Evaluation Board

DOCUMENTATION

Application Notes

- AN-643: Closed-Loop Control Circuit Implementation of the ADuC832 MicroConverter®IC and the AD8305 Logarithmic Converter in a Digital Variable Optical Attenuator

Data Sheet

- ADL5306: 60dB-range (100nA to 100µA) Low-Cost Logarithmic Converter Data Sheet

REFERENCE DESIGNS

- CN0056
- CN0057

REFERENCE MATERIALS

Informational

- Optical and High Speed Networking ICs

Technical Articles

- Design a Logamp RF Pulse Detector
- Log Amps and Directional Couplers Enable VSWR Detection
- Logarithmic Processing Applied to Network Power Monitoring

DESIGN RESOURCES

- ADL5306 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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REVISION HISTORY

Rev. 0: Initial Version

SPECIFICATIONS

Table 1. V_P = 5 V, V_N = 0, T_A = 25°C, R_{REF} = 200 kΩ, unless otherwise noted

Parameter	Conditions	Min[1]	Typ	Max[1]	Unit
INPUT INTERFACE	INPT (Pin 4), IREF (Pin 3)				
Specified Current Range, I_{PD}	Flows toward INPT pin	100n		100µ	A
Input Current Min/Max Limits	Flows toward INPT pin			1	mA
Reference Current, I_{REF}, Range	Flows toward IREF pin	100n		100µ	A
Summing Node Voltage	Internally preset; may be altered by user	0.46	0.5	0.54	V
Temperature Drift	−40°C < T_A < +85°C		0.015		mV/°C
Input Offset Voltage	$V_{IN} - V_{SUM}$, $V_{IREF} - V_{SUM}$	−20		+20	mV
LOGARITHMIC OUTPUT	VLOG (Pin 9)				
Logarithmic Slope		190	200	210	mV/dec
	−40°C < T_A < +85°C	185		215	mV/dec
Logarithmic Intercept[2]		0.3	1	1.7	nA
	−40°C < T_A < +85°C	0.1		2.5	nA
Law Conformance Error	100 nA < I_{PD} < 100 µA		0.1	0.4	dB
Wideband Noise[3]	I_{PD} > 1 µA		0.7		µV/√Hz
Small-Signal Bandwidth[3]	I_{PD} > 1 µA		0.7		MHz
Maximum Output Voltage			1.7		V
Minimum Output Voltage	Limited by V_N = 0 V		0.01		V
Output Resistance		4.375	5	5.625	kΩ
REFERENCE OUTPUT	VREF (Pin 2)				
Voltage wrt Ground		2.435	2.5	2.565	V
	−40°C < T_A < +85°C	2.4		2.6	V
Maximum Output Current	Sourcing (grounded load)		20		mA
Incremental Output Resistance	Load current < 10 mA		2		Ω
OUTPUT BUFFER	BFIN (Pin 10); SCAL (Pin 11); VOUT (Pin 12)				
Input Offset Voltage		−20		+20	mV
Input Bias Current	Flowing out of Pin 10 or Pin 11		0.4		µA
Incremental Input Resistance			35		MΩ
Output Range	R_L = 1 kΩ to ground		V_P − 0.1		V
Incremental Output Resistance	Load current < 10 mA		0.5		Ω
Peak Source/Sink Current			50		mA
Small-Signal Bandwidth	GAIN = 1		15		MHz
Slew Rate	0.2 V to 4.8 V output swing		15		V/µs
POWER SUPPLY	VPOS (Pin 8); VNEG (Pin 6)				
Positive Supply Voltage	($V_P - V_N$) ≤ 11 V	3	5	5.5	V
Quiescent Current			5.4	6.6	mA
Negative Supply Voltage (Optional)	($V_P - V_N$) ≤ 11 V	−5.5	0		V

[1] Minimum and maximum specified limits on parameters that are guaranteed but not tested are six sigma values.
[2] Other values of logarithmic intercept can be achieved by adjusting R_{REF}.
[3] Output noise and incremental bandwidth are functions of input current measured using the output buffer connected for GAIN = 1.

ABSOLUTE MAXIMUM RATINGS

Table 2. ADL5306 Absolute Maximum Ratings

Parameter	Rating
Supply Voltage $V_P - V_N$	12 V
Input Current	20 mA
Internal Power Dissipation	500 mW
θ_{JA}	135°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION AND PIN FUNCTION DESCRIPTIONS

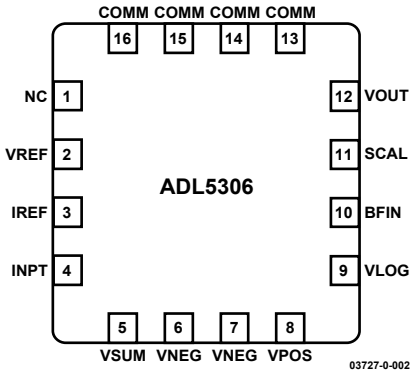

Figure 2. 16-Lead Leadframe Chip Scale Package (LFCSP)

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	NC	N/A
2	VREF	Reference Output Voltage of 2.5 V.
3	IREF	Accepts (Sinks) Reference Current I_{REF}.
4	INPT	Accepts (Sinks) Photodiode Current I_{PD}. Usually connected to photodiode anode such that photocurrent flows into INPT.
5	VSUM	Guard Pin. Used to shield the INPT current line and for optional adjustment of the INPT and IREF node potential.
6, 7	VNEG	Optional Negative Supply, V_N. This pin is usually grounded; for details of usage, see the Applications section.
8	VPOS	Positive Supply, ($V_P - V_N$) ≤ 11 V.
9	VLOG	Output of the Logarithmic Front End.
10	BFIN	Buffer Amplifier Noninverting Input.
11	SCAL	Buffer Amplifier Inverting Input.
12	VOUT	Buffer Output.
13–16	COMM	Analog Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

(V_P = 5 V, V_N = 0 V, R_{REF} = 200 kΩ, T_A = 25°C, unless otherwise noted.)

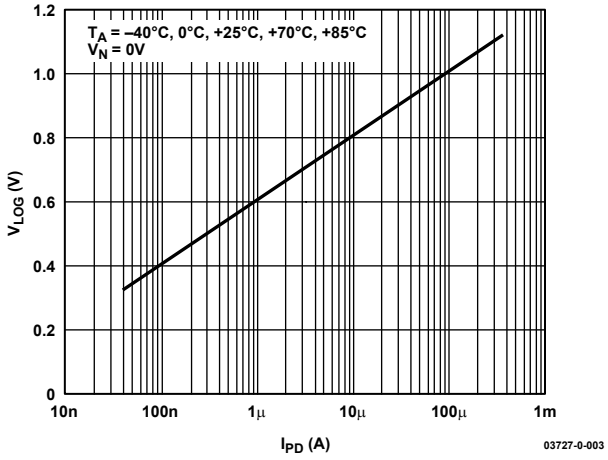

Figure 3. V_{LOG} vs. I_{PD} for Multiple Temperatures

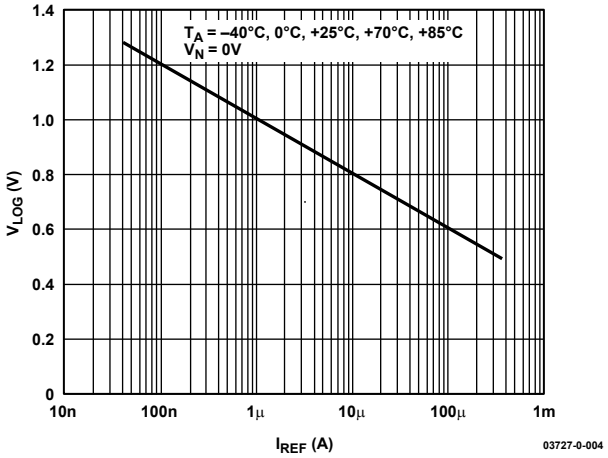

Figure 4. V_{LOG} vs. I_{REF} for Multiple Temperatures

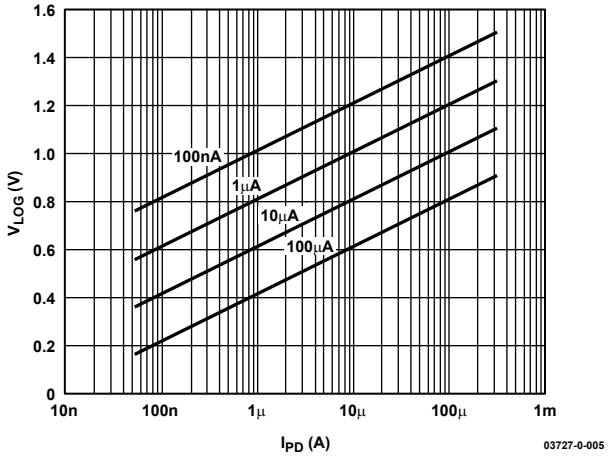

Figure 5. V_{LOG} vs. I_{PD} for Multiple Values of I_{REF} (Decade Steps from 10 nA to 1 mA)

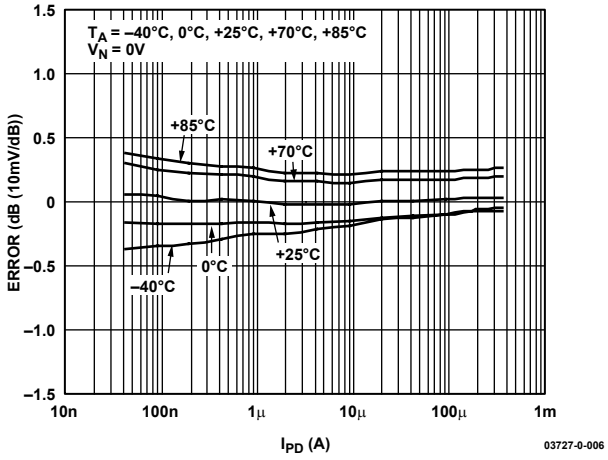

Figure 6. Law Conformance Error vs. I_{PD} (I_{REF} = 10 µA) for Multiple Temperatures, Normalized to 25°C

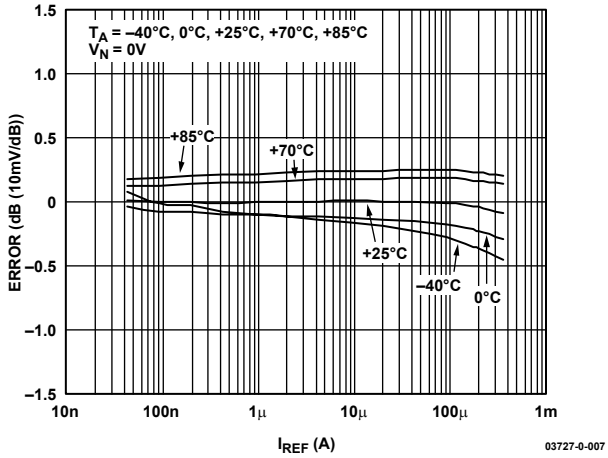

Figure 7. Law Conformance Error vs. I_{REF} (I_{PD} = 10 µA) for Multiple Temperatures, Normalized to 25°C

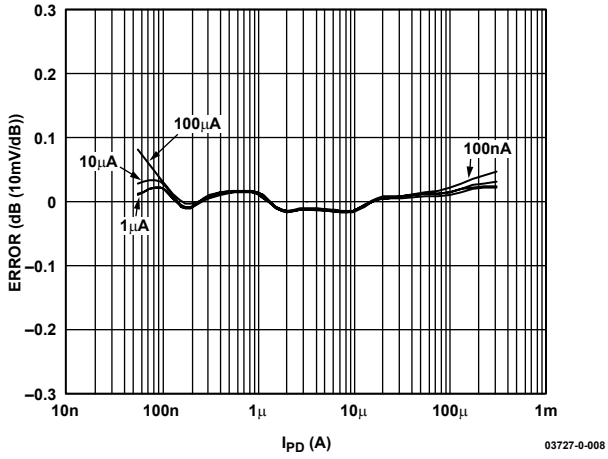

Figure 8. Law Conformance Error vs. I_{PD} for Multiple Values of I_{REF} (Decade Steps from 10 nA to 1 mA)

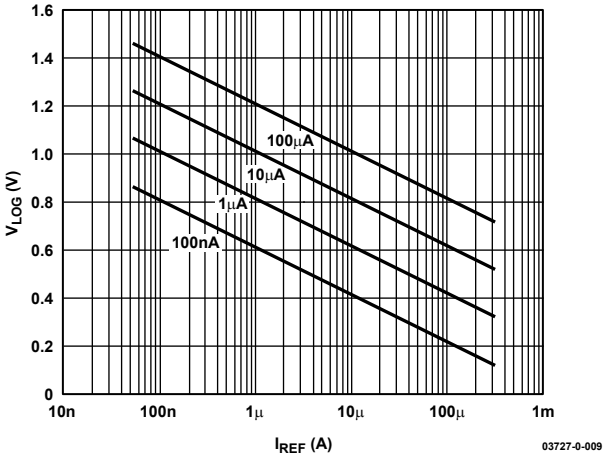

Figure 9. V_{LOG} vs. I_{REF} for Multiple Values of I_{PD} (Decade Steps from 10 nA to 1 mA)

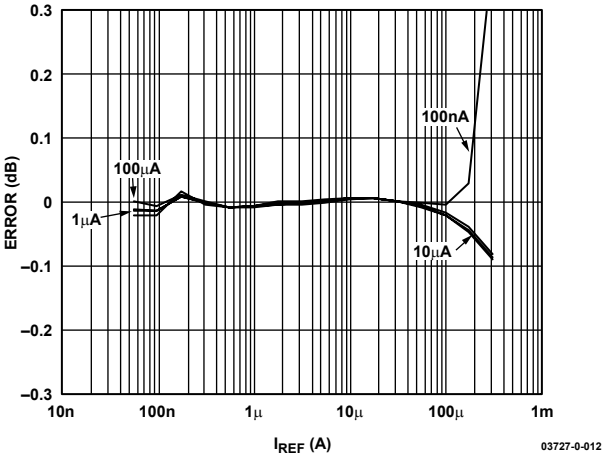

Figure 12. Law Conformance Error vs. I_{REF} for Multiple Values of I_{PD} (Decade Steps from 10 nA to 1 mA)

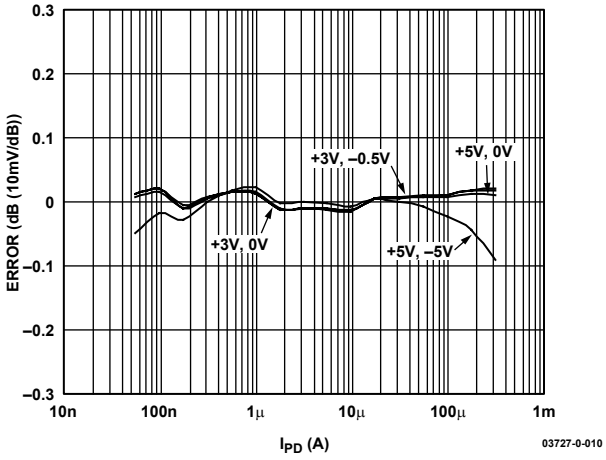

Figure 10. Law Conformance Error vs. I_{PD} for Various Supply Conditions

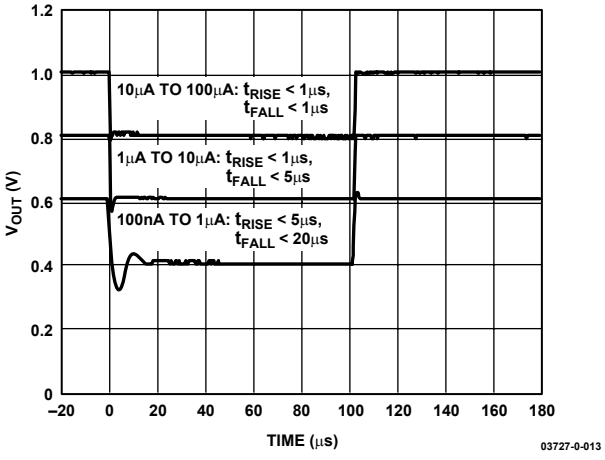

Figure 13. Pulse Response: I_{PD} to V_{OUT} (G = 1)

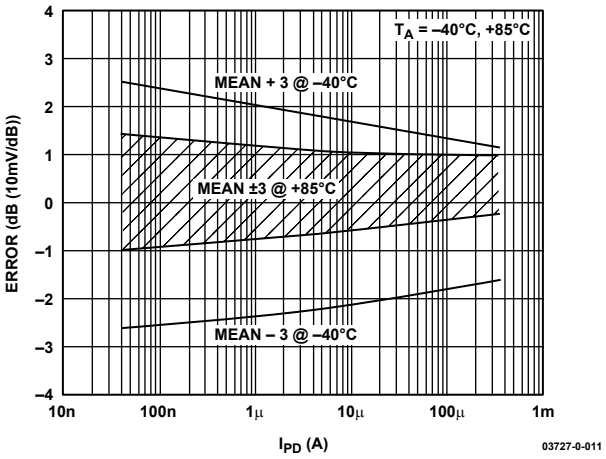

Figure 11. $V_{INPT} – V_{SUM}$ vs. I_{PD}

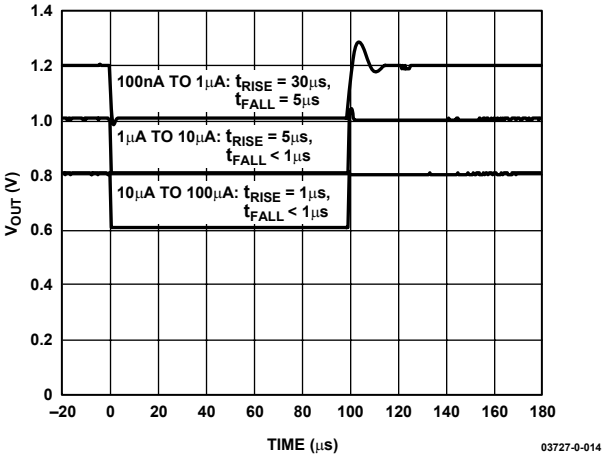

Figure 14. Pulse Response: I_{REF} to V_{OUT} (G = 1)

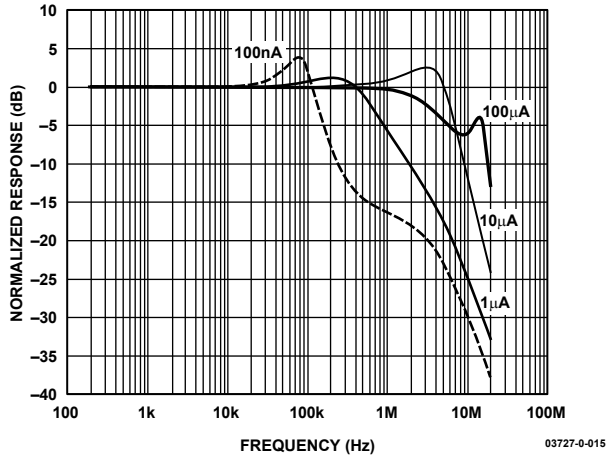

Figure 15. Small-Signal AC Response (5% Sine Modulation), from I_{PD} to V_{OUT} (G = 1) for I_{PD} in Decade Steps from 10 nA to 1 mA

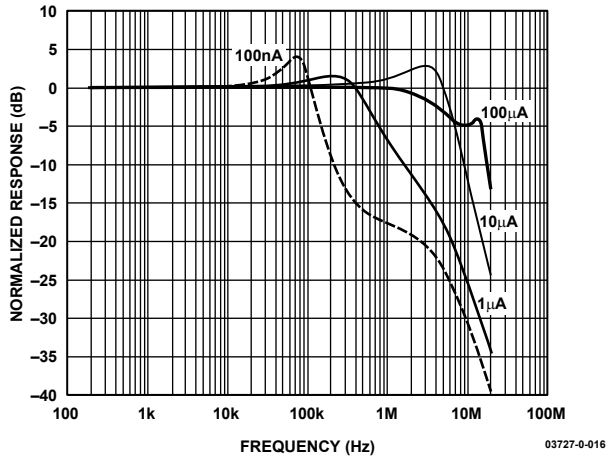

Figure 16. Small-Signal AC Response (5% Sine Modulation), from I_{REF} to V_{OUT} (G = 1) for I_{REF} in Decade Steps from 10 nA to 1 mA

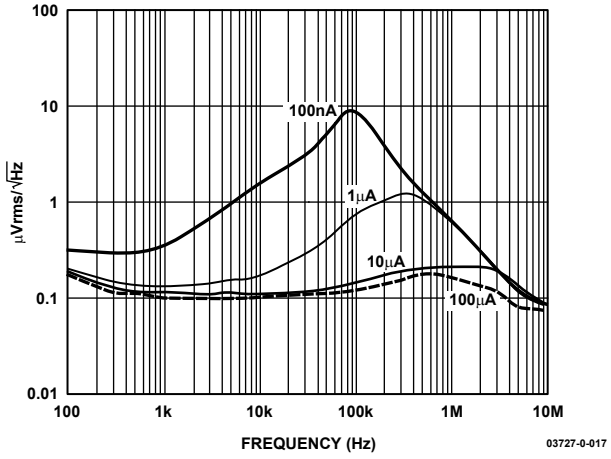

Figure 17. Spot Noise Spectral Density at V_{OUT} (G = 1) vs. Frequency for I_{PD} in Decade Steps from 10 nA to 1 mA

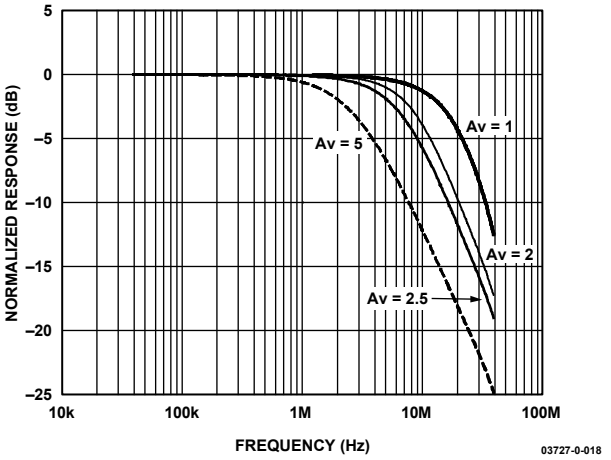

Figure 18. Small-Signal AC Response of the Buffer for Various Closed-Loop Gains (R_L = 1 kΩ, C_L < 2 pF)

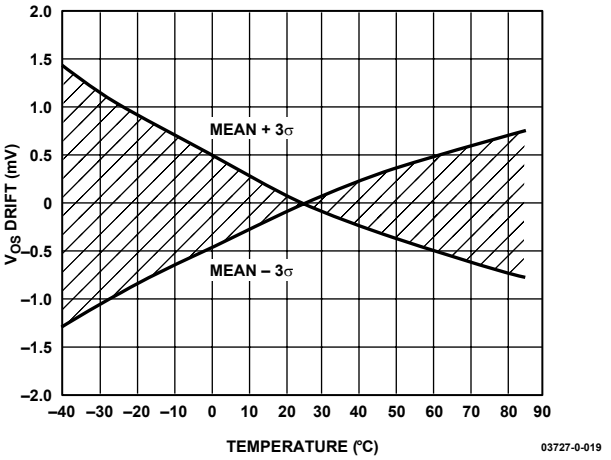

Figure 19. Buffer Input Offset Drift vs. Temperature (3σ to Either Side of Mean)

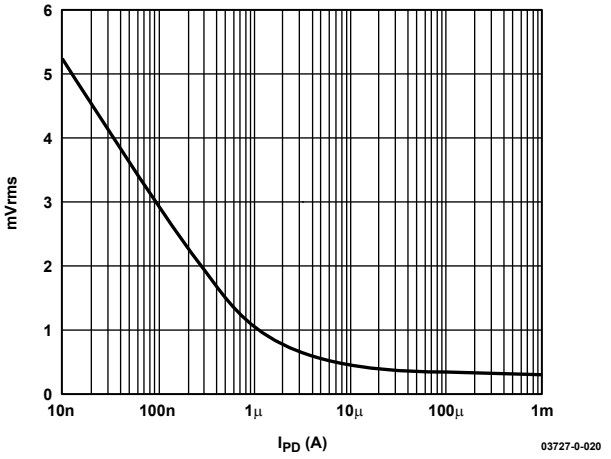

Figure 20. Total Wideband Noise Voltage at V_{OUT} vs. I_{PD} (G = 1)

GENERAL STRUCTURE

The ADL5306 addresses a wide variety of interfacing conditions to meet the needs of fiber optic supervisory systems, and is useful in many nonoptical applications. This section explains the structure of this unique style of translinear log amp. The simplified schematic in Figure 21 shows the key elements.

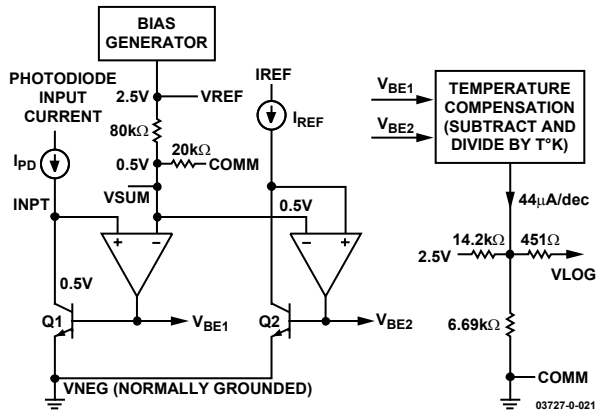

Figure 21. Simplified Schematic

The photodiode current I_{PD} is received at Pin INPT. The voltage at this node is essentially equal to the voltage on the two adjacent guard pins, VSUM and IREF, due to the low offset voltage of the JFET op amp. Transistor Q1 converts I_{PD} to a corresponding logarithmic voltage, as shown in Equation 1. A finite positive value of V_{SUM} is needed to bias the collector of Q1 for the usual case of a single-supply voltage. This is internally set to 0.5 V, one fifth of the 2.5 V reference voltage appearing on Pin VREF. The resistance at the VSUM pin is nominally 16 kΩ; this voltage is not intended as a general bias source.

The ADL5306 also supports the use of an optional negative supply voltage, V_N, at Pin VNEG. When V_N is –0.5 V or more negative, VSUM may be connected to ground; thus, INPT and IREF assume this potential. This allows operation as a voltage-input logarithmic converter by the inclusion of a series resistor at either or both inputs. Note that the resistor setting, I_{REF}, will need to be adjusted to maintain the intercept value. It should also be noted that the collector-emitter voltages of Q1 and Q2 are now the full V_N, and effects due to self-heating will cause errors at large input currents.

The input-dependent V_{BE1} of Q1 is compared with the reference V_{BE2} of a second transistor, Q2, operating at I_{REF}. This is generated externally to a recommended value of 10 µA. However, other values over a several-decade range can be used with a slight degradation in law conformance (see Figure 8).

THEORY

The base-emitter voltage of a BJT (bipolar junction transistor) can be expressed by the following equation, which immediately shows its basic logarithmic nature:

$$V_{BE} = kT/q \ln(I_C / I_S) \quad (1)$$

where:
I_C is the collector current
I_S is a scaling current, typically only 10^{-17} A
kT/q is the thermal voltage, proportional to absolute temperature (PTAT), and is 25.85 mV at 300 K.

I_S is never precisely defined and exhibits an even stronger temperature dependence, varying by a factor of roughly a billion between –35°C and +85°C. Thus, to make use of the BJT as an accurate logarithmic element, both of these temperature-dependencies must be eliminated.

The difference between the base-emitter voltages of a matched pair of BJTs, one operating at the photodiode current I_{PD} and the other operating at a reference current I_{REF}, can be written as

$$\begin{aligned} V_{BE1} - V_{BE2} &= kT/q \ln(I_{PD} / I_S) - kT/q \ln(I_{REF} / I_S) \\ &= \ln(10)\, kT/q \log_{10}(I_{PD} / I_{REF}) \\ &= 59.5\ mV \log_{10}(I_{PD} / I_{REF})\ (T = 300\ K) \end{aligned} \quad (2)$$

The uncertain, temperature-dependent saturation current, I_S, that appears in Equation 1 has therefore been eliminated. To eliminate the temperature variation of kT/q, this difference voltage is processed by what is essentially an analog divider. Effectively, it puts a variable under Equation 2. The output of this process, which also involves a conversion from voltage mode to current mode, is an intermediate, temperature-corrected current:

$$I_{LOG} = I_Y \log_{10}(I_{PD} / I_{REF}) \quad (3)$$

where I_Y is an accurate, temperature-stable scaling current that determines the slope of the function (change in current per decade). For the ADL5306, I_Y is 44 µA, resulting in a temperature-independent slope of 44 µA/decade for all values of I_{PD} and I_{REF}. This current is subsequently converted back to a voltage-mode output, V_{LOG}, scaled 200 mV/decade.

It is apparent that this output should be zero for $I_{PD} = I_{REF}$, and would need to swing negative for smaller values of input current. To avoid this, I_{REF} would need to be as small as the smallest value of I_{PD}. In the ADL5306, an internal offset voltage is added to V_{LOG} to shift it upward by 0.8 V. This moves the intercept to the left by four decades, from 10 μA to 1 nA:

$$I_{LOG} = I_Y \log_{10}(I_{PD} / I_{INTC}) \quad (4)$$

where I_{INTC} is the operational / value of the intercept current. Since values of $I_{PD} < I_{INTC}$ result in a negative V_{LOG}, a negative supply of sufficient value is required to accommodate this situation (discussed later).

The voltage V_{LOG} is generated by applying I_{LOG} to an internal resistance of 4.55 kΩ, formed by the parallel combination of a 6.69 kΩ resistor to ground and the 14.2 kΩ resistor to the internal 2.5 V reference. At the VLOG pin, the output current I_{LOG} generates a voltage of

$$\begin{aligned} V_{LOG} &= I_{LOG} \times 4.55\ \text{k}\Omega \\ &= 44\ \mu\text{A} \times 4.55\ \text{k}\Omega \times \log_{10}(I_{PD} / I_{REF}) \\ &= V_Y \log_{10}(I_{PD} / I_{REF}) \end{aligned} \quad (5)$$

where V_Y = 200 mV/decade or 10 mV/dB. Note that any resistive loading on VLOG will lower this slope and will result in an overall scaling uncertainty due to the variability of the on-chip resistors. Consequently, this practice is not recommended.

V_{LOG} may also swing below ground when dual supplies (V_P and V_N) are used. When V_N = −0.5 V or more negative, the input pins INPT and IREF may be positioned at ground level simply by grounding VSUM.

MANAGING INTERCEPT AND SLOPE

As previously noted, the internally generated 2.5 V bias combines with the on-chip resistors to introduce an accurate offset voltage of 0.8 V at the VLOG pin, equivalent to four decades. This results in a logarithmic transfer function that can be written as

$$V_{LOG} = V_Y \log_{10}(10^4 \times I_{PD} / I_{REF}) = V_Y \log_{10}(I_{PD} / I_{INTC}) \quad (6)$$

where $I_{INTC} = I_{REF} / 10^4$

Thus, the effective intercept current, I_{INTC}, is only one ten-thousandth of I_{REF}, corresponding to 10 nA when using the recommended value of I_{REF} = 100 μA.

The slope can be reduced by attaching a resistor to the VLOG pin. This is strongly discouraged because the on-chip resistors will not ratio correctly to the added resistance. Also, it is rare that one would wish to lower the basic slope of 10 mV/dB; if this is necessary, it should be done at the low impedance output of the buffer, which is provided to avoid such miscalibration and allow higher slopes to be used.

The ADL5306 buffer is essentially an uncommitted op amp with rail-to-rail output swing, good load driving capabilities, and a unity-gain bandwidth of >20 MHz. In addition to allowing the introduction of gain using standard feedback networks, thereby increasing the slope voltage, V_Y, the buffer can be used to implement multipole low-pass filters, threshold detectors, and a variety of other functions. For more details, see the AD8304 Data Sheet.

RESPONSE TIME AND NOISE CONSIDERATIONS

The response time and output noise of the ADL5306 are fundamentally a function of the signal current I_{PD}. For small currents, the bandwidth is proportional to I_{PD}. The output's low frequency voltage-noise spectral density is a function of I_{PD}, and increases for small values of I_{REF}. For details of noise and bandwidth performance of translinear log amps, see the AD8304 Data Sheet.

APPLICATIONS

The ADL5306 is easy to use in optical supervisory systems and in similar situations where a wide-ranging current is to be converted to its logarithmic equivalent (i.e., represented in decibel terms). Basic connections for measuring a single current input are shown in Figure 22, which includes various nonessential components, as will be explained.

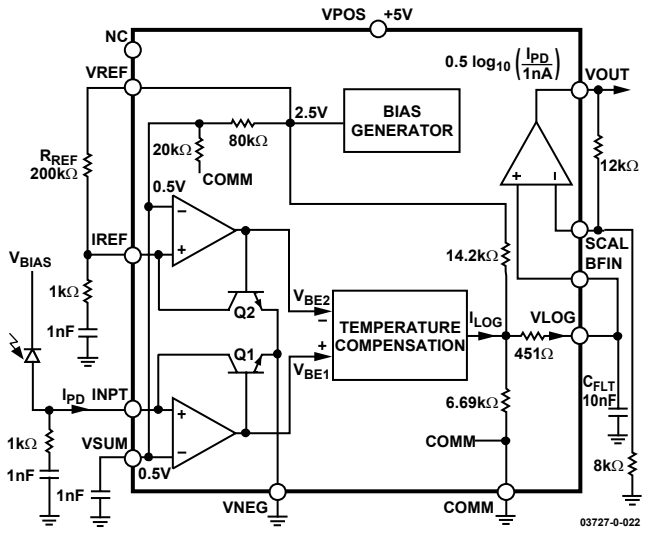

Figure 22. Basic Connections for Fixed Intercept Use

The 2 V difference in voltage between VREF and INPT, in conjunction with the external 200 kΩ resistor R_{REF}, provides a reference current I_{REF} of 100 μA into Pin IREF. The internal reference raises the voltage at VLOG by 0.8 V, effectively lowering the intercept current I_{INTC} by a factor of 10^4 to position it at 1 nA. Any temperature variation in R_{REF} must be taken into account when estimating the stability of the intercept. Also, the overall noise will increase when using very low values of I_{REF}. In fixed-intercept applications, there is little benefit in using a large reference current, since this only compresses the low current end of the dynamic range when operated from a single supply, shown here as 5 V. The capacitor between VSUM and ground is recommended to minimize the noise on this node and to help provide a clean reference current.

Since the basic scaling at VLOG is 0.2 V/dec and a swing of 4 V at the buffer output would therefore correspond to 20 decades, it will often be useful to raise the slope to make better use of the rail-to-rail voltage range. For illustrative purposes, the circuit in Figure 22 provides an overall slope of 0.5 V/dec (25 mV/dB). Thus, using I_{REF} = 100 μA, V_{LOG} runs from 0.2 V at I_{PD} = 100 nA to 0.8 V at I_{PD} = 100 μA. The buffer output runs from 0.5 V to 2.0 V, corresponding to a dynamic range of 60 dB electrical (30 dB optical) power.

The optional capacitor from VLOG to ground forms a single-pole low-pass filter in combination with the 4.55 kΩ resistance at this pin. For example, using a C_{FLT} of 10 nF, the –3 dB corner frequency is 3.2 kHz. Such filtering is useful in minimizing the output noise, particularly when I_{PD} is small. Multipole filters are more effective in reducing the total noise. For examples, see the AD8304 Data Sheet.

The dynamic response of this overall input system is influenced by the external RC networks connected from the two inputs (INPT, IREF) to ground. These are required to stabilize the input systems over the full current range. The bandwidth changes with the input current due to the widely varying pole frequency. The RC network adds a zero to the input system to ensure stability over the full range of input current levels. The network values shown in Figure 22 will usually suffice, but some experimentation may be necessary when the photodiode's capacitance is high.

Although the two current inputs are similar, some care is needed to operate the reference input at extremes of current (<100 nA) and temperature (<0°C). Modifying the RC network to 4.7 nF and 2 kΩ will allow operation to –40°C at 10 nA. By inspecting the transient response to perturbations in I_{REF} at representative current levels, the capacitor value can be adjusted to provide fast rise and fall times with acceptable settling. To fine-tune the network zero, the resistor value should be adjusted.

USING A NEGATIVE SUPPLY

Most applications of the ADL5306 require only a single supply of 3.0 V to 5.5 V. However, to provide further versatility, dual supplies may be employed, as illustrated in Figure 23.

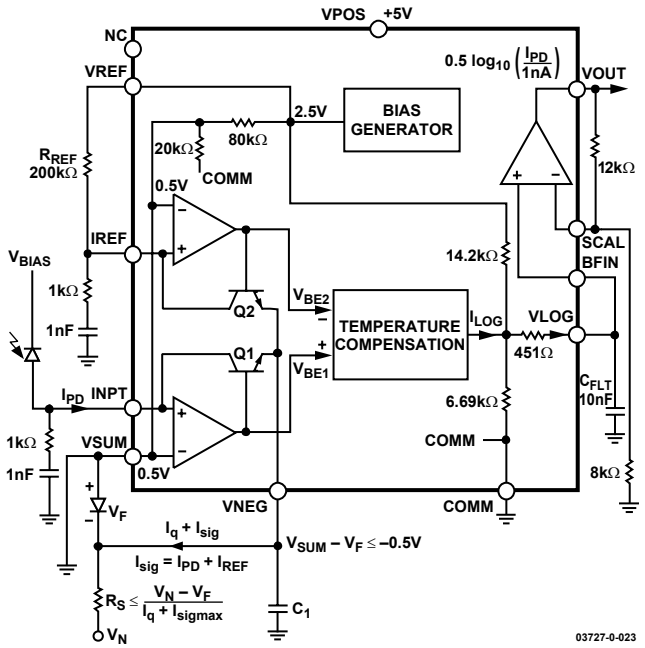

Figure 23. Negative Supply Application

The use of a negative supply, V_N, allows the summing node to be placed at ground level whenever the input transistor (Q1 in Figure 1) has a sufficiently negative bias on its emitter. When V_N = –0.5 V, the V_{CE} of Q1 and Q2 will be the same value as in the default case when VSUM is grounded. This bias need not be accurate, and a poorly defined source can be used. However, the source must be able to support the quiescent current as well as the INPT and IREF signal current. For example, it may be convenient to utilize a forward-biased junction voltage of about 0.7 V or a Schottky barrier voltage of a little over 0.5 V. With the summing node at ground, the ADL5306 may now be used as a voltage-input log amp, at either the numerator input INPT or the denominator input IREF by inserting a suitably scaled resistor from the voltage source to the relevant pin. The overall accuracy for small input voltages is limited by the voltage offset at the inputs of the JFET op amps.

The use of a negative supply also allows the output to swing below ground, thereby allowing the intercept to correspond to a midrange value of I_{PD}. However, the voltage V_{LOG} remains referenced to the ACOM pin, and while V_{LOG} does not swing negative for default operating conditions, it is free to do so. Thus, adding a resistor from VLOG to the negative supply lowers all values of V_{LOG}, which raises the intercept. The disadvantage of this method is that the slope is reduced by the shunting of the external resistor, and the poorly defined ratio of on-chip and off-chip resistance causes errors in both the slope and intercept. A more accurate method for repositioning the intercept follows.

CHARACTERIZATION METHODS

During the characterization of the ADL5306, the device was treated as a precision current-input logarithmic converter, because it is impractical to generate accurate photocurrents by illuminating a photodiode. The test currents were generated by using either a well-calibrated current source, such as the Keithley 236, or a high value resistor from a voltage source to the input pin. Great care is needed when using very small input currents. For example, the triax output connection from the current generator was used with the guard tied to VSUM. The input trace on the PC board was guarded by connecting adjacent traces to VSUM.

These measures are needed to minimize the risk of leakage current paths. With 0.5 V as the nominal bias on the INPT pin, a leakage-path resistance of 1 GΩ to ground would subtract 0.5 nA from the input, which amounts to a –0.44 dB error for a 10 nA source current. Additionally, the very high output resistance at the input pins and the long cables commonly needed during characterization allow 60 Hz and RF emissions to introduce substantial measurement errors. Careful guarding techniques are essential to reducing the pickup of these spurious signals.

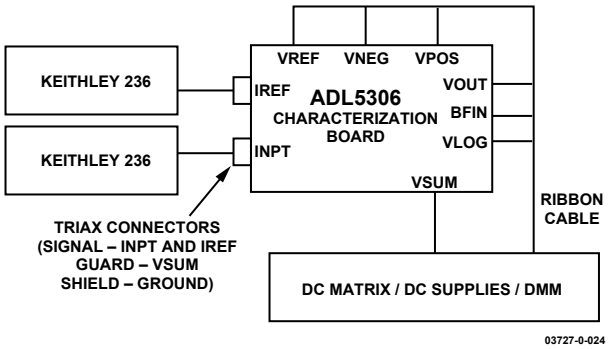

Figure 24. Primary Characterization Setup

The primary characterization setup shown in Figure 24 is used to measure V_{REF}, the static (dc) performance, logarithmic conformance, slope and intercept, the voltages appearing at Pins VSUM, INPT, and IREF, and the buffer offset and V_{REF} drift with temperature. In some cases, a fixed resistor between Pins VREF and IREF was used in place of a precision current source. For the dynamic tests, including noise and bandwidth measurements, more specialized setups are required. This includes close attention to the input stabilizing networks; for example, to ensure stable operation over the full current range of I_{REF} and temperature extremes, filter components C1 = 4.7 nF and R13 = 2 kΩ are used at Pin IREF to ground.

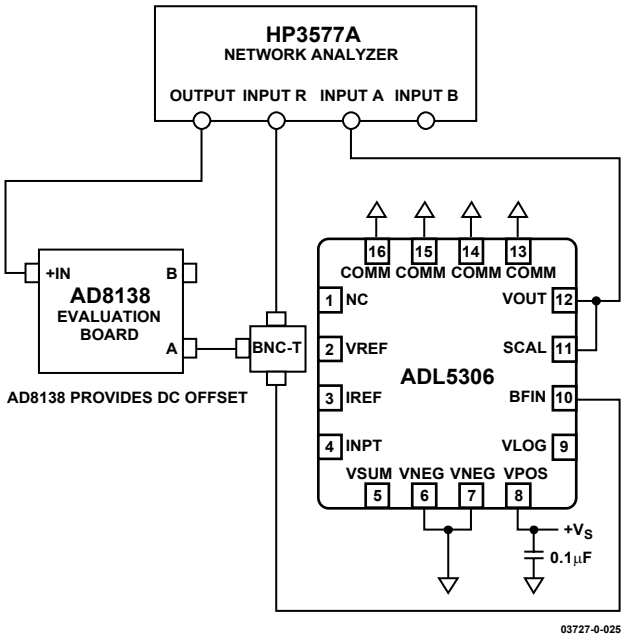

Figure 25. Configuration for Buffer Amplifier Bandwidth Measurement

Figure 25 shows the configuration used to measure the buffer amplifier bandwidth. The AD8138 evaluation board includes provisions to offset V_{LOG} at the buffer input, allowing measurements over the full range of I_{PD} using a single supply. The network analyzer input impedances are set to 1 MΩ.

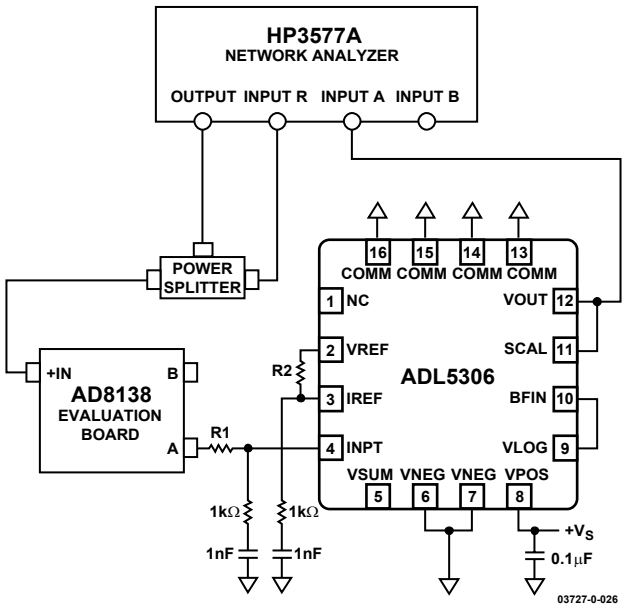

Figure 26. Configuration for Logarithmic Amplifier Bandwidth Measurement

Figure 26 shows the configuration used for frequency response measurements of the logarithmic amplifier section. The AD8138 output is offset to 1.5 V dc and modulated to a depth of 5% at frequency. R1 is chosen (over a wide range of values up to 1.0 GΩ) to provide I_{PD}. The buffer is used to deload VLOG.

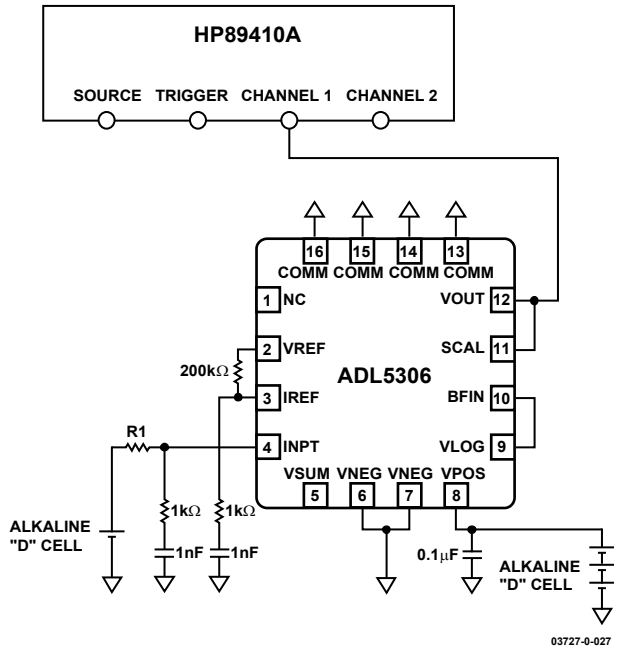

Figure 27. Configuration for Noise Spectral Density Measurement

The configuration of Figure 27 is used to measure the noise performance. Batteries provide both the supply voltage and the input current in order to minimize the introduction of spurious noise and ground loop effects. The entire evaluation system, including the current setting resistors, is mounted in a closed aluminum enclosure to provide additional shielding to external noise sources.

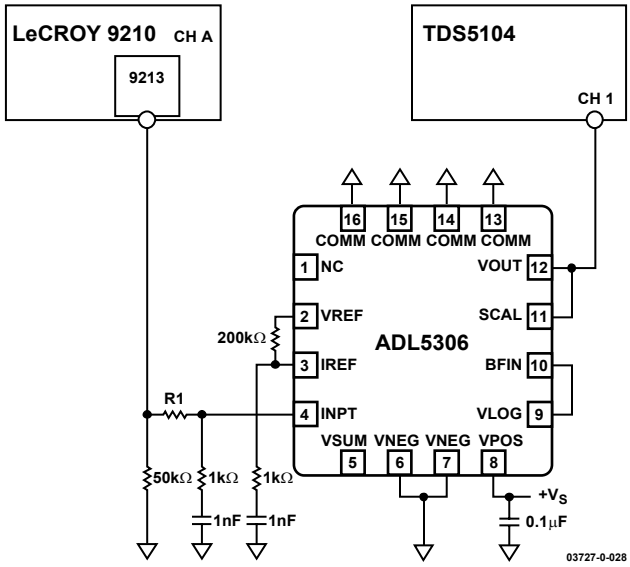

Figure 28. Configuration for Logarithmic Amplifier Pulse Response Measurement

Figure 28 shows the setup used to make the pulse response measurements. As with the bandwidth measurement, VLOG is connected directly to BFIN and the buffer amplifier is configured for a gain of 1. The buffer's output is connected through a short cable to the TDS5104 scope, with the input impedance set to 1 MΩ. The LeCroy's output is offset to create the initial pedestal current for a given R1 value. The pulse then creates a 1-decade current step.

EVALUATION BOARD

An evaluation board is available for the ADL5306, the schematic of which is shown in 29. It can be configured for a wide variety of experiments. The buffer gain is factory-set to unity, providing a slope of 200 mV/dec, and the intercept is set to 1 nA. Table 4 describes the various configuration options.

Table 4. Evaluation Board Configuration Options

Component	Function	Default Conditions
P1	**Supply Interface**. Provides access to supply pins VNEG, COMM, and VPOS.	P1 = Installed
P2, R8, R9, R10, R18	**Monitor Interface**. By adding 0 Ω resistors to R8, R9, R10, and R18, the VREF, VSUM, VOUT, and VLOG pin voltages can be monitored using a high impedance probe.	P2 = Not Installed R8 = R9 = R10 = Open (Size 0603) R18 = Open (Size 0603)
R2, R3, R4, R6, R11, R14, C2, C7, C9, C10	**Buffer Amplifier/Output Interface**. The logarithmic slope of the ADL5306 can be altered using the buffer's gain-setting resistors, R2 and R3. R4, R6, R11, R14, C2, C7, C9, and C10 are provided for a variety of filtering applications.	R2 = R6 = 0 Ω (Size 0603) R3 = R4 = Open (Size 0603) R11 = R14 = 0 Ω (Size 0603) C2 = C7 = Open (Size 0603) C9 = C10 = Open (Size 0603) VLOG = VOUT = Installed
R1, R19	**Intercept Adjustment**. The voltage dropped across resistor R1 determines the intercept reference current, nominally set to 10 μA using a 200 kΩ 1% resistor.	R1 = 200 kΩ (Size 0603) R19 = 0 Ω (Size 0603)
R12, R15, C3, C4, C5, C6	**Supply Decoupling**	C3 = C4 = 0.01 μF (Size 0603) C5 = C6 = 0.1 μF (Size 0603) R12 = R15 = 0 Ω (Size 0603)
C11	**Filtering VSUM**	C11 = 1 nF (Size 0603)
R13, R16, C1, C8	**Input Compensation**. Provides essential HF compensation at the input pins, INPT and IREF.	R13 = R16 = 1 kΩ (Size 0603) C1 = C8 = 1 nF (Size 0603)
IREF, INPT, PD, LK1, R5	**Input Interface**. The test board is configured to accept a current through the SMA connector labeled INPT. An SC style packaged photodiode can be used in place of the INPT SMA for optical interfacing. By removing R1 and adding a 0 Ω short for R5, a second current can be applied to the IREF input (also SMA) for evaluating the ADL5306 in log-ratio applications.	IREF = INPT = Installed PD = Not Installed LK1 = Installed R5 = Open (Size 0603)
J1	**SC Style Photodiode**	J1 = Open

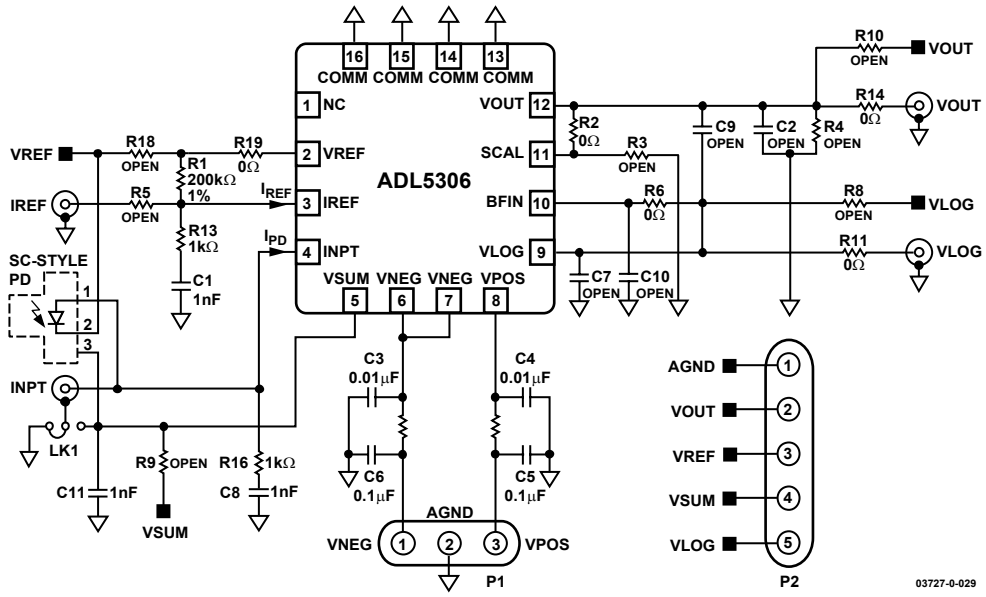

Figure 29. Evaluation Board Schematic

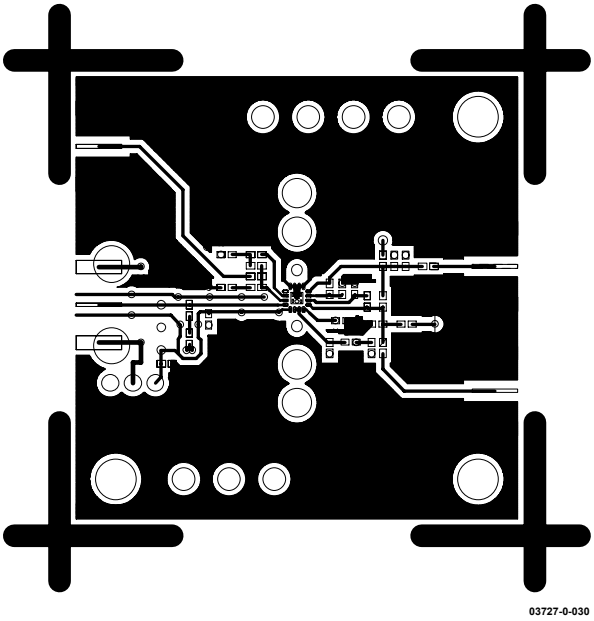

Figure 30. Component Side Layout

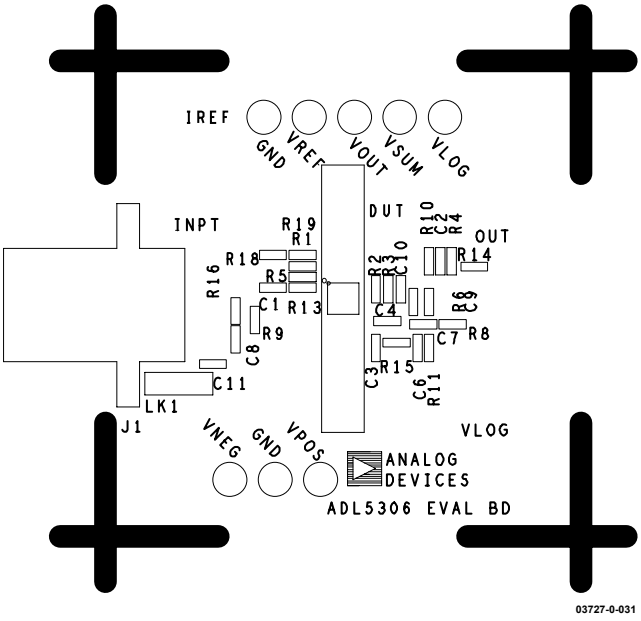

Figure 31. Component Side Silkscreen

OUTLINE DIMENSIONS

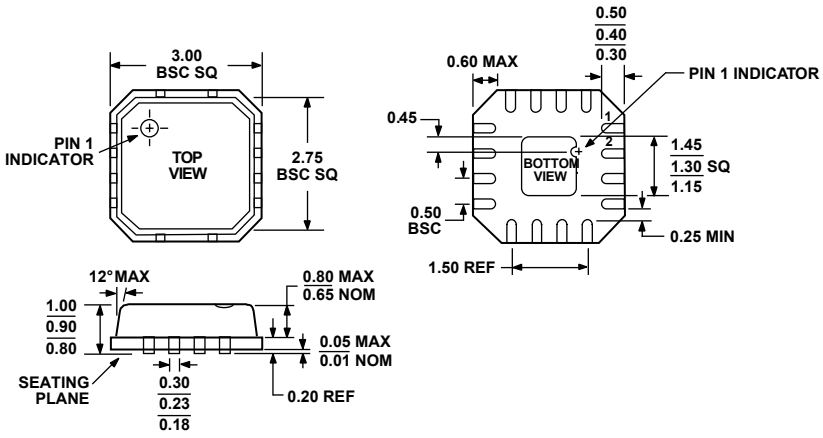

Figure 32. 16-Lead Leadframe Chip Scale Package [LFCSP]
(CP-16)
Dimensions shown in millimeters

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

ADL5306 Products	Temperature Package	Package Description	Package Outline	Branding[1]
ADL5306ACP[2]	–40°C to +85°C	16-Lead LFCSP	CP-16	JSA
ADL5306ACP-R2	–40°C to +85°C	Tape and Reel	CP-16	JSA
ADL5306ACP-REEL7	–40°C to +85°C	7″ Tape and Reel	CP-16	JSA
ADL5306-EVAL		Evaluation Board		

[1] Branding is as follows:
Line 1—Logo
Line 2—JSA
Line 3—K (Date Code). Date code is in YWW format.
[2] Contact factory for availability.

C03727–0–7/03(0)

ANALOG DEVICES

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