



IGBT

TRENCHSTOP™ IGBT4 Low Power Chip  
**IGC36T120T8L**

Data Sheet

Industrial Power Control

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**TRENCHSTOP™ IGBT4 Low Power Chip**
**Features:**

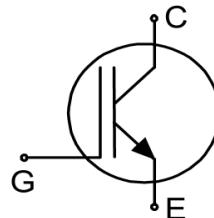
- 1200V trench & field stop technology
- Low switching losses
- Positive temperature coefficient
- Easy paralleling

**Recommended for:**

- Low / medium power modules

**Applications:**

- Low / medium power drives



Chip Type	$V_{CE}$	$I_{Cn}$ <sup>1</sup>	Die Size	Package
IGC36T120T8L	1200V	35A	6.36mm x 5.67mm	Sawn on foil

**Mechanical Parameters**

Die size	6.36 x 5.67		mm <sup>2</sup>	
Emitter pad size	See chip drawing			
Gate pad size	0.826 x 1.31			
Area total	36.06			
Thickness	115		μm	
Wafer size	200		mm	
Maximum possible chips per wafer	743			
Passivation frontside	Photoimide			
Pad metal	3200nm AlSiCu			
Backside metal	Ni Ag – system To achieve a reliable solder connection it is strongly recommended not to consume the Ni layer completely during production process			
Die bond	Electrically conductive epoxy glue and soft solder			
Wire bond	Al, ≤500μm			
Reject ink dot size	Ø 0.65mm; max. 1.2mm			
Storage environment	for original and sealed MBB bags	Ambient atmosphere air, temperature 17°C – 25°C, <6 months		
	for open MBB bags	Acc. to IEC62258-3: atmosphere >99% Nitrogen or inert gas, humidity <25%RH, temperature 17°C – 25°C, <6 months		

<sup>1</sup> Nominal collector current at  $T_C=100^\circ\text{C}$  for chip packaged in power modules, see application example cited on page 5.

**Maximum Ratings**

Parameter	Symbol	Value	Unit
Collector-emitter voltage, $T_{vj}=25^{\circ}\text{C}$	$V_{CE}$	1200	V
DC collector current, limited by $T_{vj \text{ max}}^2$	$I_C$	-	A
Pulsed collector current, $t_p$ limited by $T_{vj \text{ max}}^3$	$I_{C,\text{puls}}$	105	A
Gate-emitter voltage	$V_{GE}$	$\pm 20$	V
Operating junction temperature	$T_{vj}$	-40 ... +175	$^{\circ}\text{C}$
Short circuit data <sup>3/4</sup> $V_{GE}=15\text{V}$ , $V_{CC}=800\text{V}$ , $T_{vj}=150^{\circ}\text{C}$	$t_{sc}$	10	$\mu\text{s}$

**Static Characteristics** (tested on wafer),  $T_{vj}=25^{\circ}\text{C}$ 

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-emitter breakdown voltage	$V_{(BR)CES}$	$V_{GE}=0\text{V}$ , $I_C=1.2\text{mA}$	1200	-	-	V
Collector-emitter saturation voltage	$V_{CESat}$	$V_{GE}=15\text{V}$ , $I_C=35\text{A}$	1.58	1.85	2.07	
Gate-emitter threshold voltage	$V_{GE(\text{th})}$	$I_C=1.2\text{mA}$ , $V_{GE}=V_{CE}$	5.3	5.8	6.3	
Zero gate voltage collector current	$I_{CES}$	$V_{CE}=1200\text{V}$ , $V_{GE}=0\text{V}$	-	-	5	
Gate-emitter leakage current	$I_{GES}$	$V_{CE}=0\text{V}$ , $V_{GE}=20\text{V}$	-	-	120	nA
Integrated gate resistor	$r_G$		none			$\Omega$

**Electrical Characteristics** <sup>3</sup>

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-emitter saturation voltage	$V_{CESat}$	$V_{GE}=15\text{V}$ , $I_C=35\text{A}$ , $T_{vj}=150^{\circ}\text{C}$	-	2.25	-	V
Input capacitance	$C_{ies}$	$V_{CE}=25\text{V}$ , $V_{GE}=0\text{V}$ , $f=1\text{MHz}$ $T_{vj}=25^{\circ}\text{C}$	-	2000	-	pF
Reverse transfer capacitance	$C_{res}$		-	70	-	

<sup>2</sup> Depending on thermal properties of assembly.

<sup>3</sup> Not subject to production test - verified by design/characterization.

<sup>4</sup> Allowed number of short circuits: <1000; time between short circuits: >1s.



# IGC36T120T8L

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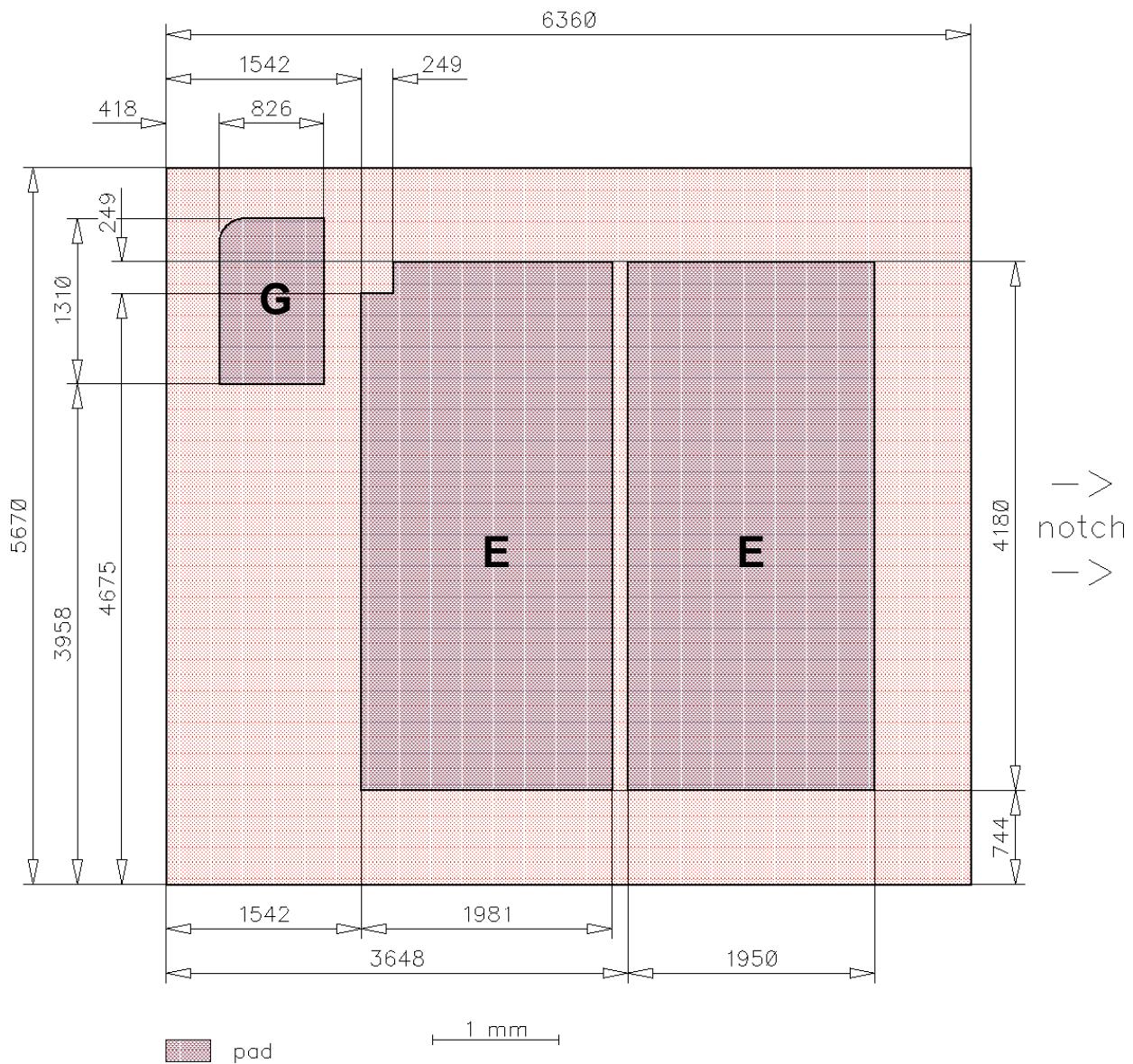
## Further Electrical Characteristics

Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.

Application example	FP35R12W2T4_B11	Rev. 2.0
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# Chip Drawing

Die-Size 6360 um x 5670 um



**E = Emitter**

**G** = Gate



# IGC36T120T8L

## Bare Die Product Specifics

Test coverage at wafer level cannot cover all application conditions. Therefore it is recommended to test all characteristics which are relevant for the application at package level, including RBSOA and SCSOA.

## Description

AQL 0.65 for visual inspection according to failure catalogue

Electrostatic Discharge Sensitive Device according to MIL-STD 883

## Revision History

Revision	Subjects (major changes since last revision)	Date
2.0	Final data sheet	18.02.2015
2.1	Update disclaimer	20.08.2015

## Relevant Application Notes

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