

## TC74VHC74F, TC74VHC74FN, TC74VHC74FT, TC74VHC74FK

### Dual D-Type Flip-Flop with Preset and Clear

The TC74VHC74 is an advanced high speed CMOS D-FLIP FLOP fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.

$\overline{\text{CLR}}$  and  $\overline{\text{PR}}$  are independent of the CK and are accomplished by setting the appropriate input low.

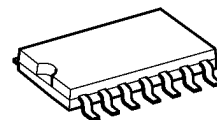
An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

### Features

- High speed:  $f_{\text{max}} = 170 \text{ MHz}$  (typ.) at  $V_{\text{CC}} = 5 \text{ V}$
- Low power dissipation:  $I_{\text{CC}} = 2 \mu\text{A}$  (max) at  $T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}$  (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays:  $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Wide operating voltage range:  $V_{\text{CC (opr)}} = 2 \text{ V}$  to  $5.5 \text{ V}$
- Pin and function compatible with 74ALS74

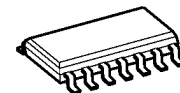
Note: The JEDEC SOP (FN) is not available in Japan.

TC74VHC74F



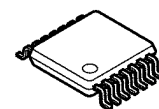
SOP14-P-300-1.27A

TC74VHC74FN



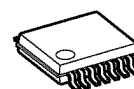
SOL14-P-150-1.27

TC74VHC74FT



TSSOP14-P-0044-0.65A

TC74VHC74FK

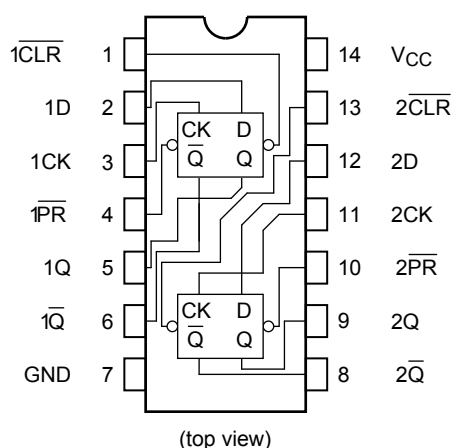


VSSOP14-P-0030-0.50

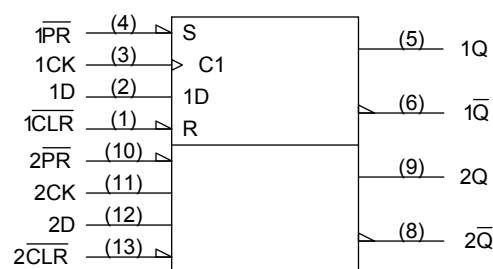
### Weight

SOP14-P-300-1.27A	: 0.18 g (typ.)
SOL14-P-150-1.27	: 0.12 g (typ.)
TSSOP14-P-0044-0.65A	: 0.06 g (typ.)
VSSOP14-P-0030-0.50	: 0.02 g (typ.)

## Pin Assignment



## IEC Logic Symbol



## Truth Table

Inputs				Outputs		Function
CLR	PR	D	CK	Q	Q̄	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Q <sub>n</sub>	Q̄ <sub>n</sub>	No Change

X: Don't care

## Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V <sub>CC</sub>	-0.5 to 7.0	V
DC input voltage	V <sub>IN</sub>	-0.5 to 7.0	V
DC output voltage	V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> + 0.5	V
Input diode current	I <sub>IK</sub>	-20	mA
Output diode current	I <sub>OK</sub>	±20	mA
DC output current	I <sub>OUT</sub>	±25	mA
DC V <sub>CC</sub> /ground current	I <sub>CC</sub>	±50	mA
Power dissipation	P <sub>D</sub>	180	mW
Storage temperature	T <sub>stg</sub>	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2.0 to 5.5	V
Input voltage	$V_{IN}$	0 to 5.5	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 ( $V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ( $V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either VCC or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
				$V_{CC}$ (V)	Min	Typ.	Max	Min	Max
High-level input voltage	$V_{IH}$	—		2.0 3.0 to 5.5	1.50 $V_{CC} \times 0.7$	— —	— —	1.50 $V_{CC} \times 0.7$	— —
Low-level input voltage	$V_{IL}$	—		2.0 3.0 to 5.5	— —	— —	0.50 $V_{CC} \times 0.3$	0.50 $V_{CC} \times 0.3$	V
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —
			$I_{OH} = -4$ mA	3.0 4.5	2.58 3.94	— —	— —	2.48 3.80	— —
			$I_{OH} = -8$ mA	4.5	3.94	—	—	3.80	—
									V
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu A$	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1
			$I_{OL} = 4$ mA	3.0 4.5	— —	— —	0.36 0.36	— —	0.44 0.44
			$I_{OL} = 8$ mA	4.5	—	—	0.36	—	0.44
									V
Input leakage current	$I_{IN}$	$V_{IN} = 5.5$ V or GND		0 to 5.5	—	—	$\pm 0.1$	—	$\pm 1.0$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND		5.5	—	—	2.0	—	20.0

**Timing Requirements (input:  $t_r = t_f = 3 \text{ ns}$ )**

Characteristics	Symbol	Test Condition	$V_{CC} \text{ (V)}$	$T_a = 25^\circ\text{C}$ Limit	$T_a = -40 \text{ to } 85^\circ\text{C}$ Limit	Unit
Minimum pulse width (CK)	$t_w \text{ (L)}$	—	$3.3 \pm 0.3$	6.0	7.0	ns
	$t_w \text{ (H)}$		$5.0 \pm 0.5$	5.0	5.0	
Minimum pulse width ( $\overline{\text{CLR}}$ , $\overline{\text{PR}}$ )	$t_w \text{ (L)}$	—	$3.3 \pm 0.3$	6.0	7.0	ns
			$5.0 \pm 0.5$	5.0	5.0	
Minimum set-up time	$t_s$	—	$3.3 \pm 0.3$	6.0	7.0	ns
			$5.0 \pm 0.5$	5.0	5.0	
Minimum hold time	$t_h$	—	$3.3 \pm 0.3$	0.5	0.5	ns
			$5.0 \pm 0.5$	0.5	0.5	
Minimum removal time ( $\overline{\text{CLR}}$ , $\overline{\text{PR}}$ )	$t_{\text{rem}}$	—	$3.3 \pm 0.3$	5.0	5.0	ns
			$5.0 \pm 0.5$	3.0	3.0	

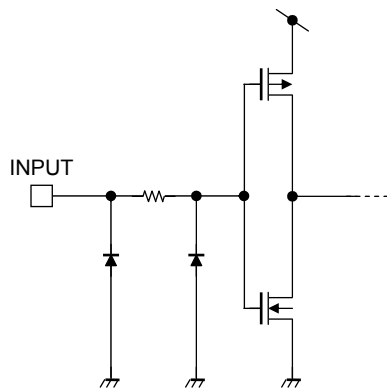
**AC Characteristics (input:  $t_r = t_f = 3 \text{ ns}$ )**

Characteristics	Symbol	Test Condition	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit
			$V_{CC} \text{ (V)}$	$C_L \text{ (pF)}$	Min	Typ.	Max	
Propagation delay time (CK-Q, $\overline{Q}$ )	$t_{\text{pLH}}$ $t_{\text{pHL}}$	—	$3.3 \pm 0.3$	15	—	6.7	11.9	ns
				50	—	9.2	15.4	
			$5.0 \pm 0.5$	15	—	4.6	7.3	
				50	—	6.1	9.3	
Propagation delay time ( $\overline{\text{CLR}}$ , $\overline{\text{PR}}$ -Q, $\overline{Q}$ )	$t_{\text{pLH}}$ $t_{\text{pHL}}$	—	$3.3 \pm 0.3$	15	—	7.6	12.3	ns
				50	—	10.1	15.8	
			$5.0 \pm 0.5$	15	—	4.8	7.7	
				50	—	6.3	9.7	
Maximum clock frequency	$f_{\text{max}}$	—	$3.3 \pm 0.3$	15	80	125	—	MHz
				50	50	75	—	
			$5.0 \pm 0.5$	15	130	170	—	
				50	90	115	—	
Input capacitance	$C_{\text{IN}}$	—	—	—	—	4	10	pF
Power dissipation capacitance	$C_{\text{PD}}$	(Note)	—	—	—	25	—	pF

Note:  $C_{\text{PD}}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

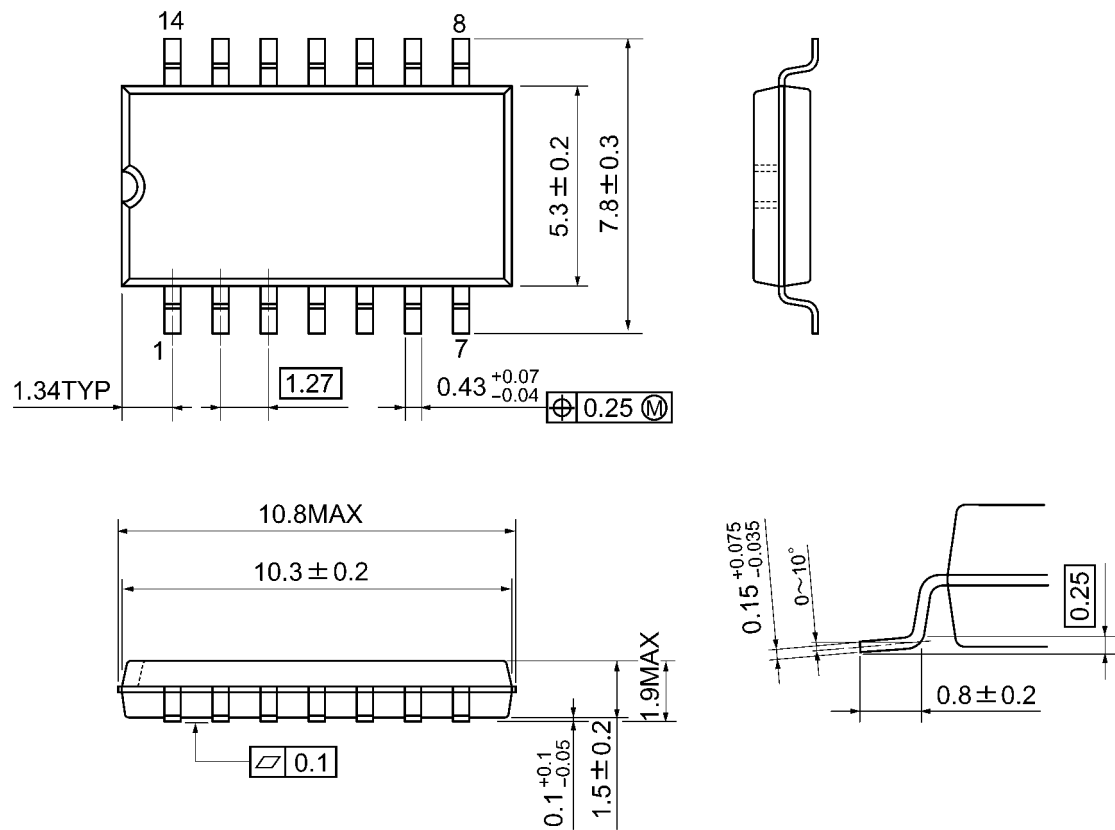
$$I_{\text{CC (opr)}} = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}/2 \text{ (per F/F)}$$

**Input Equivalent Circuit**

## Package Dimensions

SOP14-P-300-1.27A

Unit: mm

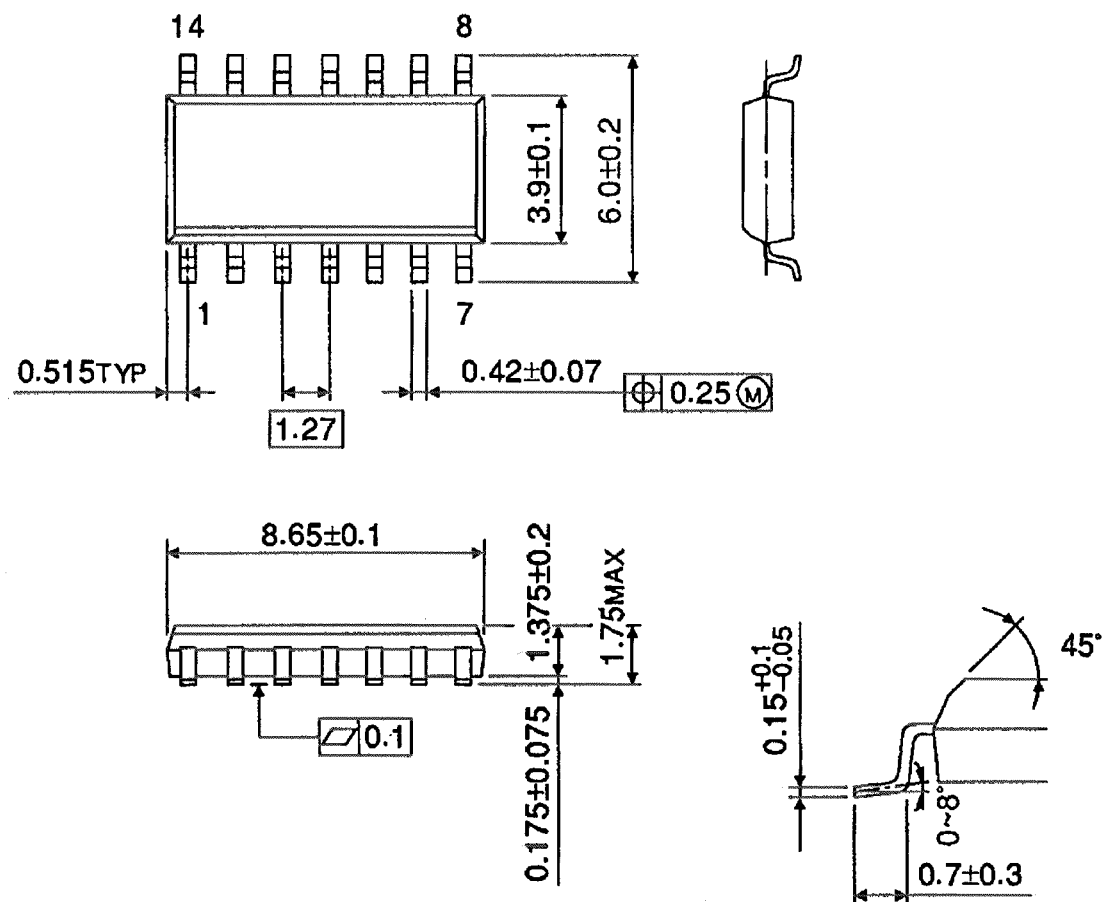


Weight: 0.18 g (typ.)

## Package Dimensions (Note)

SOL14-P-150-1.27

Unit : mm



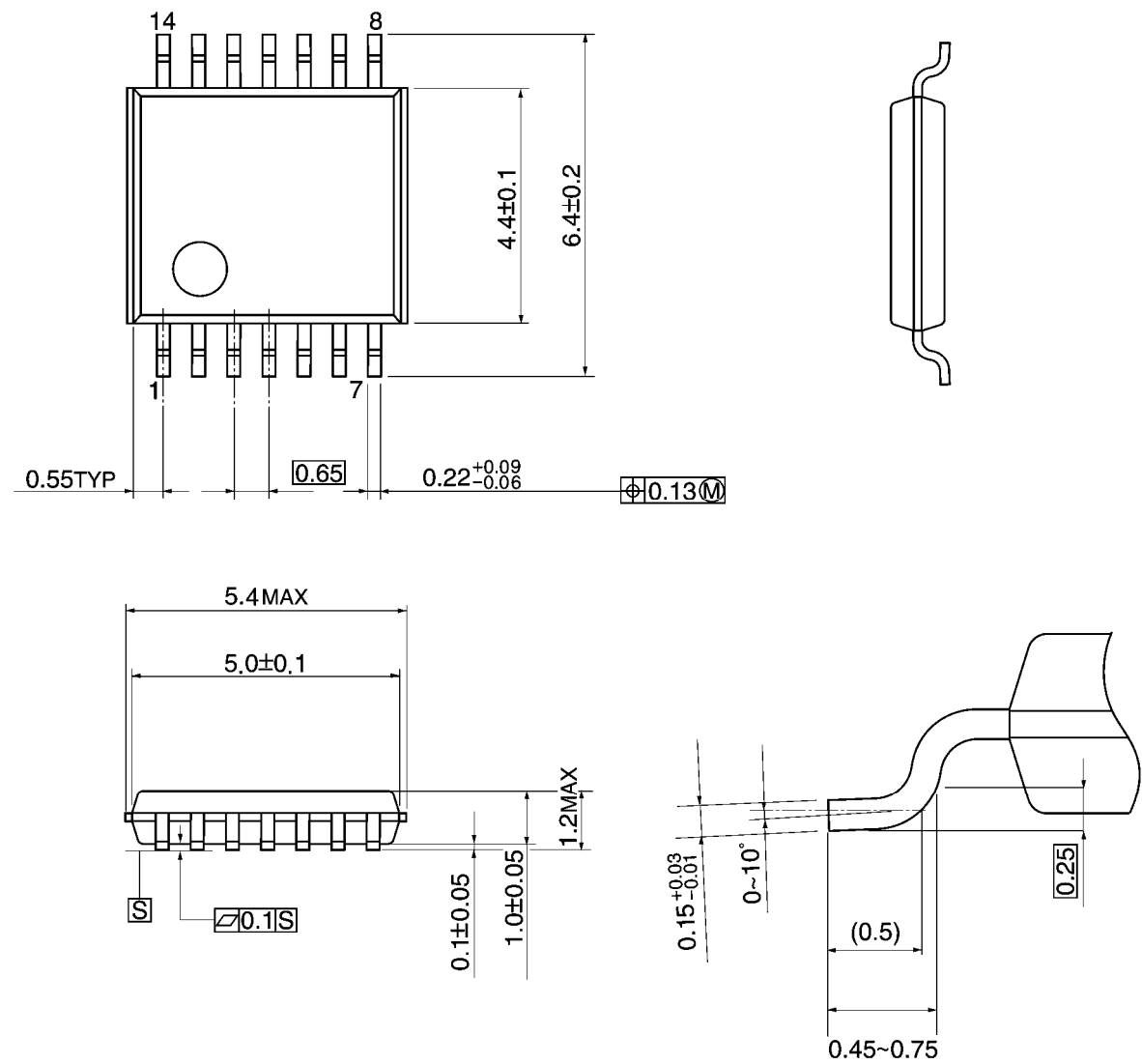
Note: This package is not available in Japan.

Weight: 0.12 g (typ.)

Package Dimensions

TSSOP14-P-0044-0.65A

Unit: mm



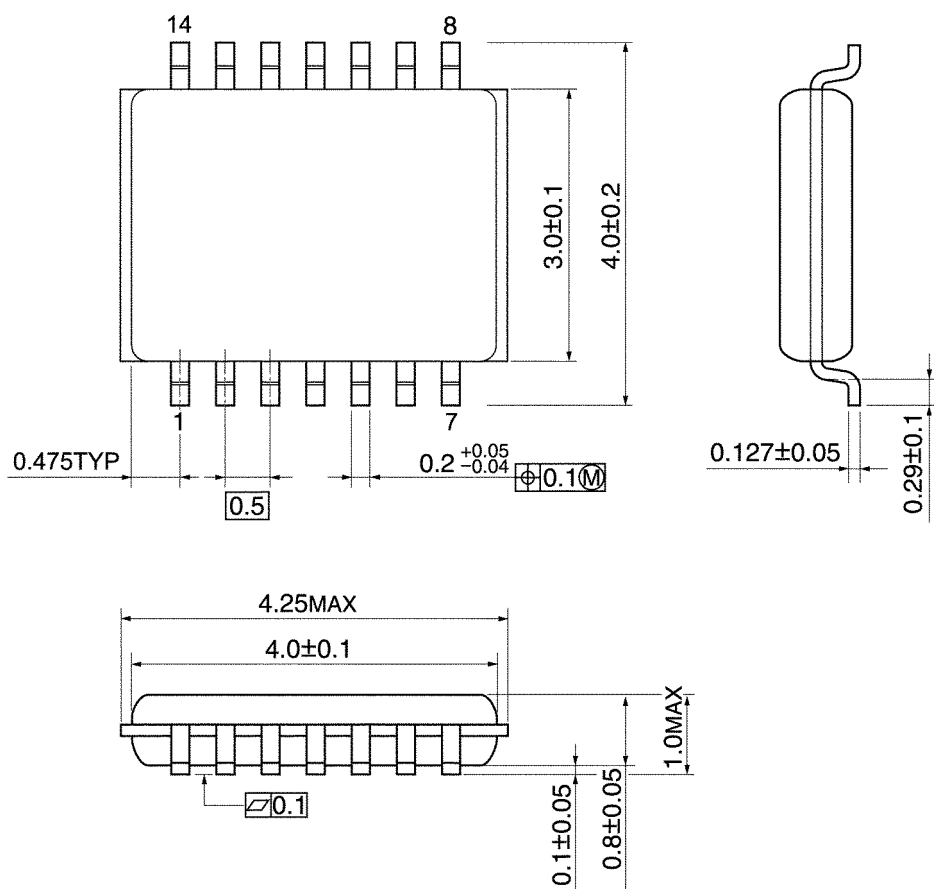
Weight: 0.06 g (typ.)



## Package Dimensions

VSSOP14-P-0030-0.50

Unit: mm



Weight: 0.02 g (typ.)

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