

- State-of-the-Art BiCMOS Design
Significantly Reduces I_{CCZ}
- ESD Protection Exceeds 2000 V Per
MIL-STD-883C, Method 3015; Exceeds
200 V Using Machine Model ($C = 200 \text{ pF}$,
 $R = 0$)
- 3-State Buffer-Type Outputs Drive Bus
Lines Directly
- Package Options Include Plastic
Small-Outline (DW) Packages and Standard
Plastic 300-mil DIPs (NT)

description

This 10-bit bus-interface flip-flop features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

DW OR NT PACKAGE
(TOP VIEW)

\overline{OE}	1	24	V_{CC}
1D	2	23	1Q
2D	3	22	2Q
3D	4	21	3Q
4D	5	20	4Q
5D	6	19	5Q
6D	7	18	6Q
7D	8	17	7Q
8D	9	16	8Q
9D	10	15	9Q
10D	11	14	10Q
GND	12	13	CLK

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be true to the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output enable (\overline{OE}) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74BCT29821 is characterized for operation from 0°C to 70°C.

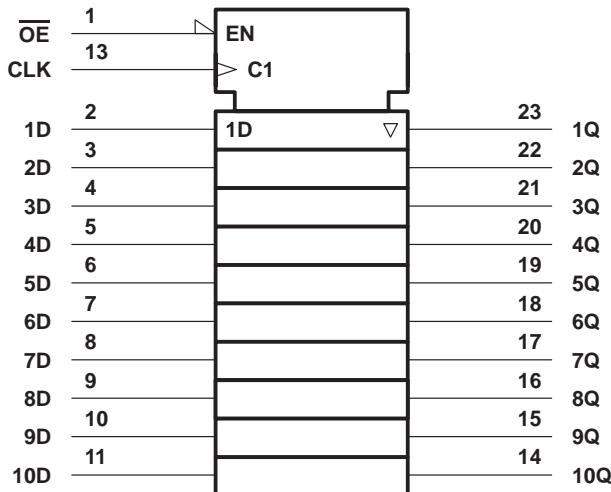
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

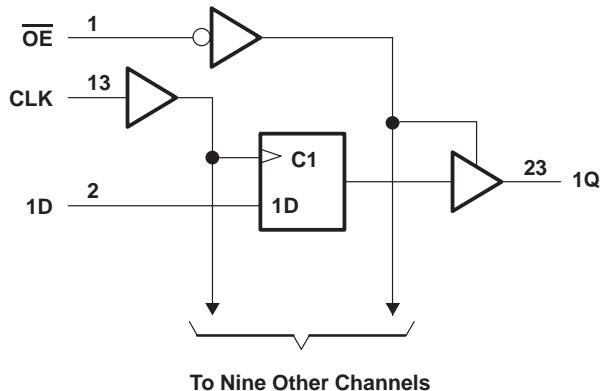
SN74BCT29821
10-BIT BUS-INTERFACE FLIP-FLOP
WITH 3-STATE OUTPUTS

SCBS021D – FEBRUARY 1989 – REVISED NOVEMBER 1993

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984
 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O	-0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O	-0.5 V to V_{CC}
Input clamp current, I_{IK} ($V_I < 0$)	-30 mA
Current into any output in the low state, I_O	96 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

SN74BCT29821
10-BIT BUS-INTERFACE FLIP-FLOP
WITH 3-STATE OUTPUTS
SCBS021D – FEBRUARY 1989 – REVISED NOVEMBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$				-1.2	V
V_{OH}	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -15 \text{ mA}$	2.4	3.3		V
		$I_{OH} = -24 \text{ mA}$	2			
V_{OL}	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 48 \text{ mA}$		0.42	0.55		V
I_I	$V_{CC} = 5.5 \text{ V}$,	$V_I = 7 \text{ V}$		0.1		mA
I_{IH}	$V_{CC} = 5.5 \text{ V}$,	$V_I = 2.7 \text{ V}$	-10		-75	μA
I_{IL}	$V_{CC} = 5.5 \text{ V}$,	$V_I = 0.5 \text{ V}$			-0.2	mA
I_{OS}^\ddagger	$V_{CC} = 5.5 \text{ V}$,	$V_O = 0$	-75		-250	mA
I_{OZH}	$V_{CC} = 5.5 \text{ V}$,	$V_O = 2.7 \text{ V}$		20		μA
I_{OZL}	$V_{CC} = 5.5 \text{ V}$,	$V_O = 0.5 \text{ V}$			-20	μA
I_{CCL}	$V_{CC} = 5.5 \text{ V}$,	Outputs open	25	35		mA
I_{CCH}	$V_{CC} = 5.5 \text{ V}$,	Outputs open	6	10		mA
I_{CCZ}	$V_{CC} = 5.5 \text{ V}$,	Outputs open	2	6		mA
C_i	$V_{CC} = 5 \text{ V}$,	$V_I = 2.5 \text{ V or } 0.5 \text{ V}$		5.5		pF
C_o	$V_{CC} = 5 \text{ V}$,	$V_O = 2.5 \text{ V or } 0.5 \text{ V}$	7			pF

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	125	0	125	MHz
t_w	Pulse duration, CLK high or low		7		7		ns
t_{su}	Setup time, data before CLK^\uparrow	High or low	7		7		ns
t_h	Hold time, data after CLK^\uparrow	High or low	1		1		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			125			125		MHz
t_{PLH}	CLK	Q	1.5	7.5	10	1.5	12	ns
			1.5	6.5	9	1.5	10	
t_{PHL}	\overline{OE}	Q	2	7.5	10	2	12	ns
			2	9	12	2	13	
t_{PZH}	\overline{OE}	Q	2	5	7	2	8	ns
			2	5	7	2	8	
t_{PLZ}	\overline{OE}	Q						

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.