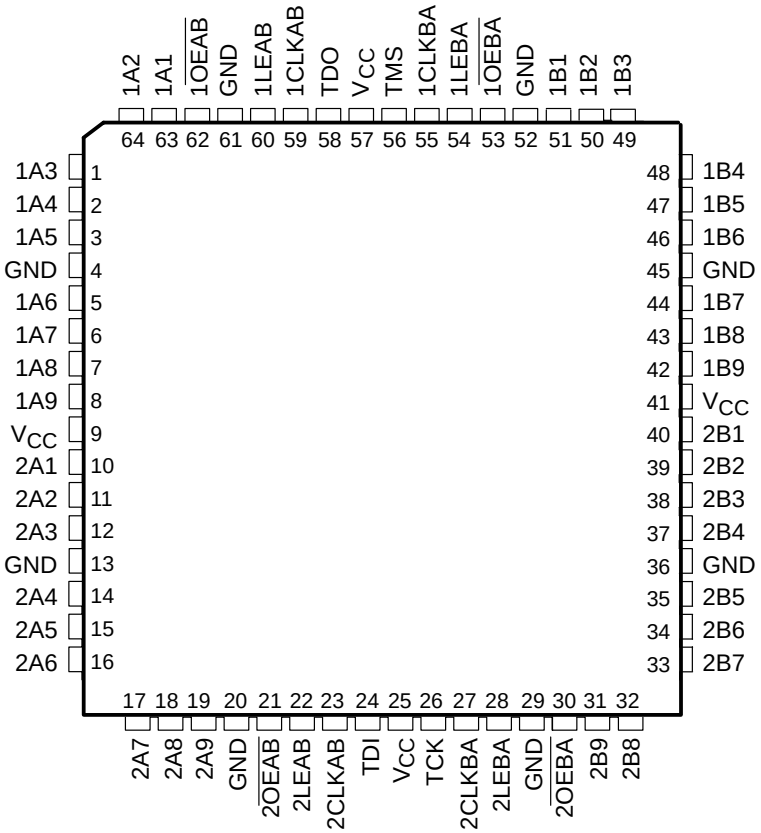
- **Member of the Texas Instruments Widebus™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **Compatible With IEEE Std 1149.1-1990 (JTAG) Test Access Port (TAP) and Boundary-Scan Architecture**
- **Includes D-Type Flip-Flops and Control Circuitry to Provide Multiplexed Transmission of Stored and Real-Time Data**
- **Two Boundary-Scan Cells (BSCs) Per I/O for Greater Flexibility**
- **SCOPE™ Instruction Set**
  - **IEEE Std 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ**
  - **Parallel Signature Analysis (PSA) at Inputs With Masking Option**
  - **Pseudorandom Pattern Generation (PRPG) From Outputs**
  - **Sample Inputs/Toggle Outputs (TOPSIP)**
  - **Binary Count From Outputs**
  - **Device Identification**
  - **Even-Parity Opcodes**

PM PACKAGE
(TOP VIEW)



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description

The SN74ABT18502 scan test device with an 18-bit universal bus transceiver is a member of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Std 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the four-wire test access port (TAP) interface.

In the normal mode, this device is an 18-bit universal bus transceiver that combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. The device can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE universal bus transceivers.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low, A-bus data is stored on a low-to-high transition of CLKAB. When $\overline{OEAB}$ is low, the B outputs are active. When $\overline{OEAB}$ is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the $\overline{OEBA}$, LEBA, and CLKBA inputs.

In the test mode, the normal operation of the SCOPE universal bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary scan test operations according to the protocol described in IEEE Std 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis (PSA) on data inputs and pseudorandom pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

Additional flexibility is provided in the test mode through the use of two boundary-scan cells (BSCs) for each I/O pin. This allows independent test data to be captured and forced at either bus (A or B). A PSA/binary count up (PSA/COUNT) instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LQFP – PM	Tray	SN74ABT18502PM	ABT18502

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

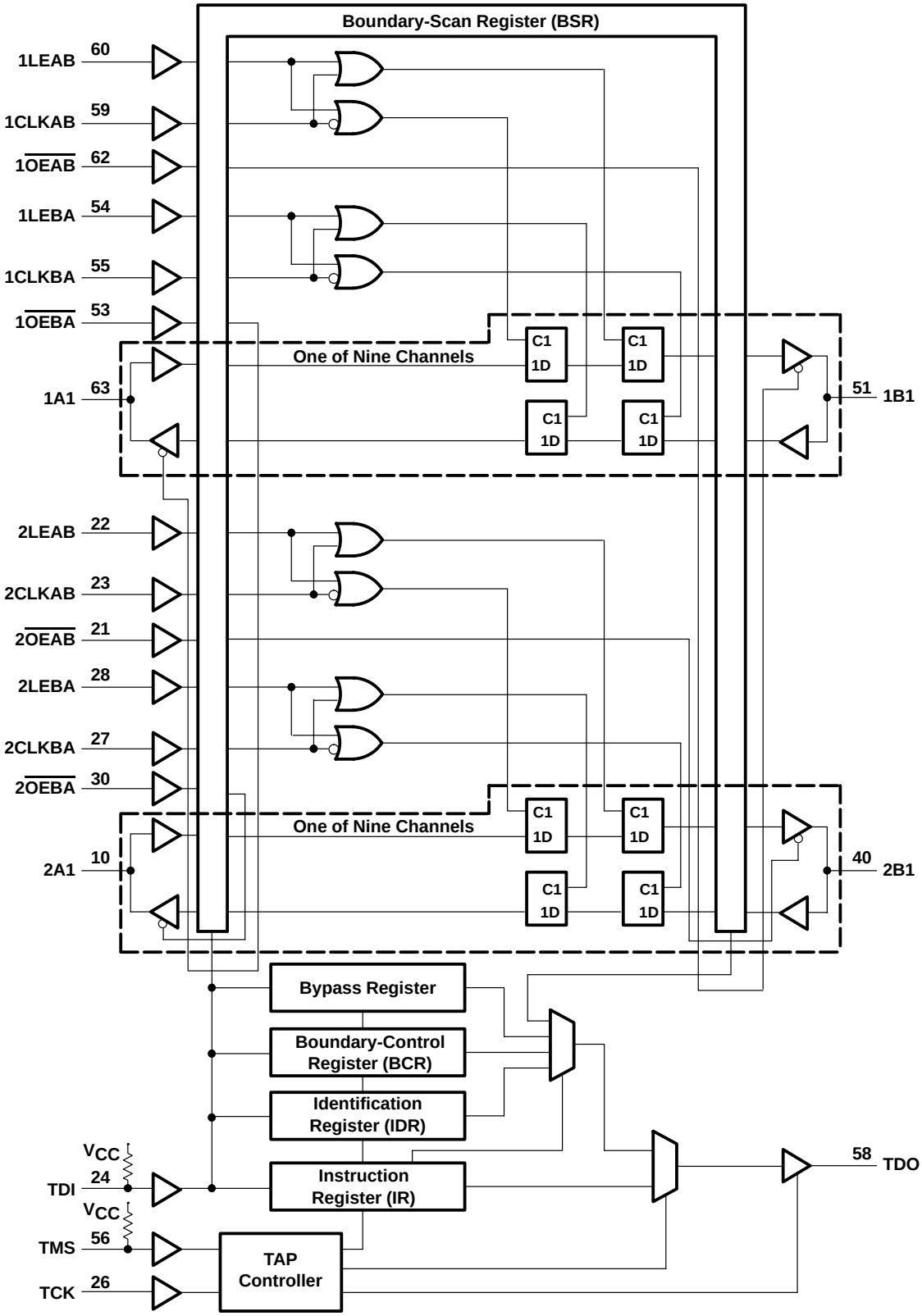
FUNCTION TABLE‡
(normal mode, each register)

INPUTS				OUTPUT
$\overline{OEAB}$	LEAB	CLKAB	A	B
L	L	L	X	B_0§
L	L	↑	L	L
L	L	↑	H	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Z

‡ A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.

§ Output level before the indicated steady-state input conditions were established

functional block diagram



Terminal Functions

PIN NAME	DESCRIPTION
GND	Ground
TCK	Test clock. One of four pins required by IEEE Std 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four pins required by IEEE Std 1149.1-1990. TDI is the serial input for shifting data through the instruction register (IR) or selected data register (DR). An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four pins required by IEEE Std 1149.1-1990. TDO is the serial output for shifting data through the IR or selected DR.
TMS	Test mode select. One of four pins required by IEEE Std 1149.1-1990. The TMS input directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage
1A1–1A9, 2A1–2A9	Normal-function A-bus I/O ports (see function table for normal-mode logic)
1B1–1B9, 2B1–2B9	Normal-function B-bus I/O ports (see function table for normal-mode logic)
1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA	Normal-function clock inputs (see function table for normal-mode logic)
1LEAB, 1LEBA, 2LEAB, 2LEBA	Normal-function latch enables (see function table for normal-mode logic)
$1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, $2\overline{OEBA}$	Normal-function output enables (see function table for normal-mode logic)

test architecture

Serial test information is conveyed by means of a four-wire test bus or TAP that conforms to IEEE Std 1149.1-1990. Test instructions, test data, and test control signals are all passed along this serial test bus. The TAP controller monitors two signals from the test bus, namely TCK and TMS. The function of the TAP controller is to extract the synchronization (TCK) and state control (TMS) signals from the test bus and generate the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Std 1149.1-1990 four-wire test bus and boundary-scan architecture and the relationship between the test bus, the TAP controller, and the test registers. As illustrated, the device contains an 8-bit instruction register (IR) and four test data registers (DRs): an 84-bit boundary-scan register (BSR), a 21-bit boundary-control register (BCR), a 1-bit bypass register, and a 32-bit device identification register (IDR).

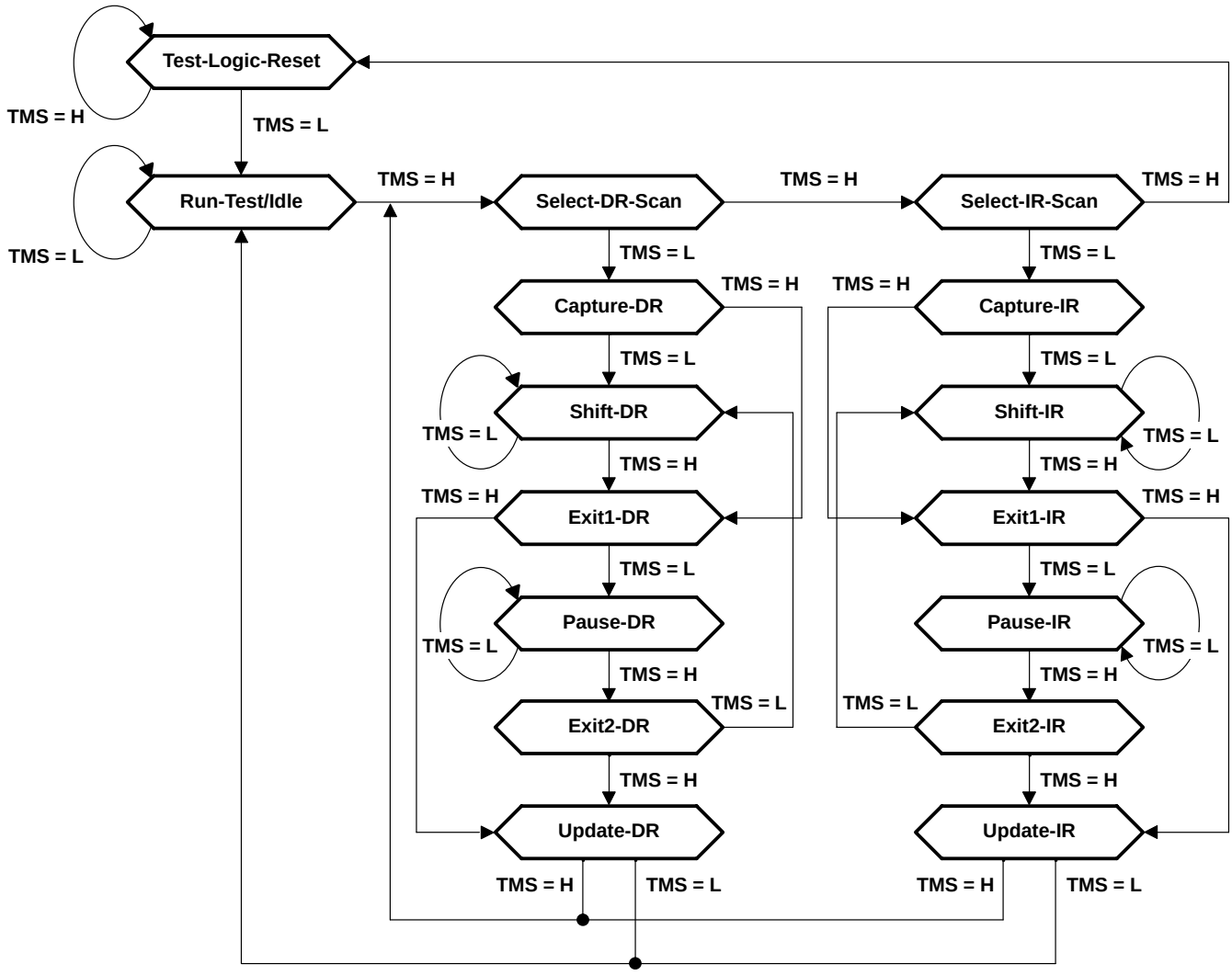


Figure 1. TAP Controller State Diagram

state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram is shown in Figure 1 and is in accordance with IEEE Std 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As illustrated, the TAP controller consists of sixteen states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is defined as a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths though the state diagram: one to access and control the selected DR and one to access and control the IR. Only one register can be accessed at a time.

Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The IR is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain DRs may also be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. TMS has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the SN74ABT18502, the IR is reset to the binary value 10000001, which selects the IDCODE instruction. Each bit in the BSR is reset to logic 0 except bits 83–80, which are reset to logic 1. The BCR is reset to the binary value 00000000000000000010, which selects the PSA test operation with no input masking.

Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state can also be entered following DR or IR scans. Run-Test/Idle is provided as a stable state in which the test logic may be actively running a test or can be idle.

The test operations selected by the BCR are performed while the TAP controller is in the Run-Test/Idle state.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states are provided to allow the selection of either DR scan or IR scan.

Capture-DR

When a DR scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected DR can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK upon which the TAP controller exits the Capture-DR state.

Shift-DR

Upon entry to the Shift-DR state, the DR is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit (LSB) of the selected DR.

While in the stable Shift-DR state, data is serially shifted through the selected DR on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-DR state.

Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states used to end a DR scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the DR.

On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state provides the capability of suspending and resuming DR scan operations without loss of data.

Update-DR

If the current instruction calls for the selected DR to be updated with current data, such update occurs on the falling edge of TCK following entry to the Update-DR state.

Capture-IR

When an IR scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the IR captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state.

For the SN74ABT18502, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

Shift-IR

Upon entry to the Shift-IR state, the IR is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the LSB of the IR.

While in the stable Shift-IR state, instruction data is serially shifted through the IR on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-IR state.

Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states used to end an IR scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the IR.

On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state provides the capability of suspending and resuming IR scan operations without loss of data.

Update-IR

The current instruction is updated and takes effect on the falling edge of TCK following entry to the Update-IR state.

register overview

With the exception of the bypass register and device IDR, any test register can be thought of as a serial shift register with a shadow latch on each bit. The bypass register and device IDR differ in that they contain only a shift register. During the appropriate capture state (Capture-IR for the IR, Capture-DR for DRs), the shift register may be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

instruction register (IR)

The IR is eight bits long and is used to tell the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four DRs is to be selected for inclusion in the scan path during DR scans, and the source of data to be captured into the selected DR during Capture-DR.

Table 4 lists the instructions supported by the SN74ABT18502. The even-parity feature specified for SCOPE devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction. The IR order of scan is shown in Figure 2.

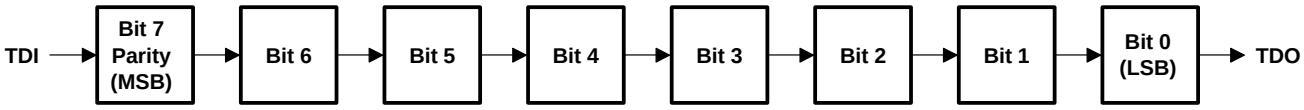


Figure 2. IR Order of Scan

data register (DR)

boundary-scan register (BSR)

The BSR is 84 bits long. It contains one BSC for each normal-function input pin and two BSCs for each normal-function I/O pin (one for input data and one for output data). The BSR is used 1) to store test data that is to be applied internally to the inputs of the normal on-chip logic and/or externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, the value of each BSC is reset to logic 0 except BSCs 83–80, which are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs are set to benign values (i.e., if test mode were invoked, the outputs would be at high impedance state). Rest values of other BSCs should be considered indeterminate.

The BSR order of scan is from TDI through bits 83–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

Table 1. BSR Configuration

BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL
83	2$\overline{\text{OEAB}}$	71	2A9-I	53	2A9-O	35	2B9-I	17	2B9-O
82	1$\overline{\text{OEAB}}$	70	2A8-I	52	2A8-O	34	2B8-I	16	2B8-O
81	2$\overline{\text{OEBA}}$	69	2A7-I	51	2A7-O	33	2B7-I	15	2B7-O
80	1$\overline{\text{OEBA}}$	68	2A6-I	50	2A6-O	32	2B6-I	14	2B6-O
79	2CLKAB	67	2A5-I	49	2A5-O	31	2B5-I	13	2B5-O
78	1CLKAB	66	2A4-I	48	2A4-O	30	2B4-I	12	2B4-O
77	2CLKBA	65	2A3-I	47	2A3-O	29	2B3-I	11	2B3-O
76	1CLKBA	64	2A2-I	46	2A2-O	28	2B2-I	10	2B2-O
75	2LEAB	63	2A1-I	45	2A1-O	27	2B1-I	9	2B1-O
74	1LEAB	62	1A9-I	44	1A9-O	26	1B9-I	8	1B9-O
73	2LEBA	61	1A8-I	43	1A8-O	25	1B8-I	7	1B8-O
72	1LEBA	60	1A7-I	42	1A7-O	24	1B7-I	6	1B7-O
—	—	59	1A6-I	41	1A6-O	23	1B6-I	5	1B6-O
—	—	58	1A5-I	40	1A5-O	22	1B5-I	4	1B5-O
—	—	57	1A4-I	39	1A4-O	21	1B4-I	3	1B4-O
—	—	56	1A3-I	38	1A3-O	20	1B3-I	2	1B3-O
—	—	55	1A2-I	37	1A2-O	19	1B2-I	1	1B2-O
—	—	54	1A1-I	36	1A1-O	18	1B1-I	0	1B1-O

boundary-control register (BCR)

The BCR is 21 bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE instruction set. Such operations include PRPG, PSA with input masking, and binary count up (COUNT). Table 5 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 000000000000000000010, which selects the PSA test operation with no input masking.

The BCR order of scan is from TDI through bits 20–0 to TDO. Table 2 shows the BCR bits and their associated test control signals.

Table 2. BCR Configuration

BCR BIT NUMBER	TEST CONTROL SIGNAL	BCR BIT NUMBER	TEST CONTROL SIGNAL	BCR BIT NUMBER	TEST CONTROL SIGNAL
20	MASK2.9	11	MASK1.9	2	OPCODE2
19	MASK2.8	10	MASK1.8	1	OPCODE1
18	MASK2.7	9	MASK1.7	0	OPCODE0
17	MASK2.6	8	MASK1.6	—	—
16	MASK2.5	7	MASK1.5	—	—
15	MASK2.4	6	MASK1.4	—	—
14	MASK2.3	5	MASK1.3	—	—
13	MASK2.2	4	MASK1.2	—	—
12	MASK2.1	3	MASK1.1	—	—

bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation. During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 3.

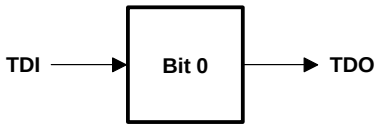


Figure 3. Bypass Register Order of Scan

device identification register (IDR)

The device IDR is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device.

During Capture-DR, the binary value 00000000000000000110000000101111 (0000602F, hex) is captured in the device IDR to identify this device as the TI SN74ABT18502, version 0. The device IDR order of scan is from TDO through bits 31–0 to TDO. Table 3 shows the device IDR bits and their significance.

Table 3. Device IDR Configuration

IDR BIT NUMBER	IDENTIFICATION SIGNIFICANCE	IDR BIT NUMBER	IDENTIFICATION SIGNIFICANCE	IDR BIT NUMBER	IDENTIFICATION SIGNIFICANCE
31	VERSION3	27	PARTNUMBER15	11	MANUFACTURER10†
30	VERSION2	26	PARTNUMBER14	10	MANUFACTURER09†
29	VERSION1	25	PARTNUMBER13	9	MANUFACTURER08†
28	VERSION0	24	PARTNUMBER12	8	MANUFACTURER07†
—	—	23	PARTNUMBER11	7	MANUFACTURER06†
—	—	22	PARTNUMBER10	6	MANUFACTURER05†
—	—	21	PARTNUMBER09	5	MANUFACTURER04†
—	—	20	PARTNUMBER08	4	MANUFACTURER03†
—	—	19	PARTNUMBER07	3	MANUFACTURER02†
—	—	18	PARTNUMBER06	2	MANUFACTURER01†
—	—	17	PARTNUMBER05	1	MANUFACTURER00†
—	—	16	PARTNUMBER04	0	LOGIC1†
—	—	15	PARTNUMBER03	—	—
—	—	14	PARTNUMBER02	—	—
—	—	13	PARTNUMBER01	—	—
—	—	12	PARTNUMBER00	—	—

† Note that for TI products, bits 11–0 of the device IDR always contains the binary value 000000101111 (02F, hex).

instruction-register (IR) opcode

The IR opcodes are shown in Table 4. The following descriptions detail the operation of each instruction.

Table 4. IR Opcodes

BINARY CODE‡ BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DR	MODE
00000000	EXTEST	Boundary scan	Boundary scan	Test
10000001	IDCODE	Identification read	Device identification	Normal
10000010	SAMPLE/PRELOAD	Sample boundary	Boundary scan	Normal
00000011	INTEST	Boundary scan	Boundary scan	Test
10000100	BYPASS§	Bypass scan	Bypass	Normal
00000101	BYPASS§	Bypass scan	Bypass	Normal
00000110	HIGHZ	Control boundary to high impedance	Bypass	Modified test
10000111	CLAMP	Control boundary to 1/0	Bypass	Test
10001000	BYPASS§	Bypass scan	Bypass	Normal
00001001	RUNT	Boundary run test	Bypass	Test
00001010	READBN	Boundary read	Boundary scan	Normal
10001011	READBT	Boundary read	Boundary scan	Test
00001100	CELLTST	Boundary self test	Boundary scan	Normal
10001101	TOPHIP	Boundary toggle outputs	Bypass	Test
10001110	SCANCN	BCR scan	Boundary control	Normal
00001111	SCANCT	BCR scan	Boundary control	Test
All others	BYPASS	Bypass scan	Bypass	Normal

‡ Bit 7 is used to maintain even parity in the 8-bit instruction.
§ The BYPASS instruction is executed in lieu of a SCOPE instruction that is not supported in the SN74ABT18502.

boundary scan

This instruction conforms to the IEEE Std 1149.1-1990 EXTEST and INTEST instructions. The BSR is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. Data scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data scanned into the output BSCs is applied to the device output pins. The device operates in the test mode.

bypass scan

This instruction conforms to the IEEE Std 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic-0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

sample boundary

This instruction conforms to the IEEE Std 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. The device operates in the normal mode.

control boundary to high impedance

This instruction conforms to the IEEE Std P1149.1A HIGHZ instruction. The bypass register is selected in the scan path. A logic-0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

control boundary to 1/0

This instruction conforms to the IEEE Std P1149.1A CLAMP instruction. The bypass register is selected in the scan path. A logic-0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the output BSCs is applied to the device output pins. The device operates in the test mode.

boundary run test

The bypass register is selected in the scan path. A logic-0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA/COUNT.

boundary read

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

boundary self test

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

boundary toggle outputs

The bypass register is selected in the scan path. A logic-0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK in Run-Test/Idle, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK in Run-Test/Idle. Data in the selected input BSCs remains constant and is applied to the inputs of the normal on-chip logic. Data appearing at the device input pins is not captured in the input BSCs. The device operates in the test mode.

BCR scan

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

BCR opcodes

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 5. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

Table 5. BCR Opcodes

BINARY CODE BIT 2 → BIT 0 MSB → LSB	DESCRIPTION
X00	Sample inputs/toggle outputs (TOPSIP)
X01	Pseudorandom pattern generation/36-bit mode (PRPG)
X10	Parallel signature analysis/36-bit mode (PSA)
011	Simultaneous PSA and PRPG/18-bit mode (PSA/PRPG)
111	Simultaneous PSA and binary count up/18-bit mode (PSA/COUNT)

In general, while the control-input BSCs (bits 83–72) are not included in the toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 83–80 of the BSR) control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are only valid when both bytes of the device are operating in one direction of data flow (that is $1\overline{OEAB} \neq 1\overline{OEBA}$ and $2\overline{OEAB} \neq 2\overline{OEBA}$) and in the same direction of data flow (that is $1\overline{OEAB} = 2\overline{OEAB}$ and $1\overline{OEBA} = 2\overline{OEBA}$). Otherwise, the bypass instruction is operated.

PSA input masking

Bits 20–3 of the BCR are used to specify device input pins to be masked from PSA operations. Bit 20 selects masking for device input pin 2A9 during A-to-B data flow or for device input pin 2B9 during B-to-A data flow. Bit 3 selects masking for device input pins 1A1 or 1B1 during A-to-B or B-to-A data flow, respectively. Bits intermediate to 20 and 3 mask corresponding device input pins in order from most significant to least significant, as indicated in Table 2. When the mask bit that corresponds to a particular device input has a logic-1 value, the device input pin is masked from any PSA operation, meaning that the state of the device input pin is ignored and has no effect on the generated signature. Otherwise, when a mask bit has a logic 0 value, the corresponding device input is not masked from the PSA operation.

sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input pins is captured in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK.

pseudorandom pattern generation (PRPG)

A pseudorandom pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK. This data also is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. Figures 4 and 5 show the 36-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

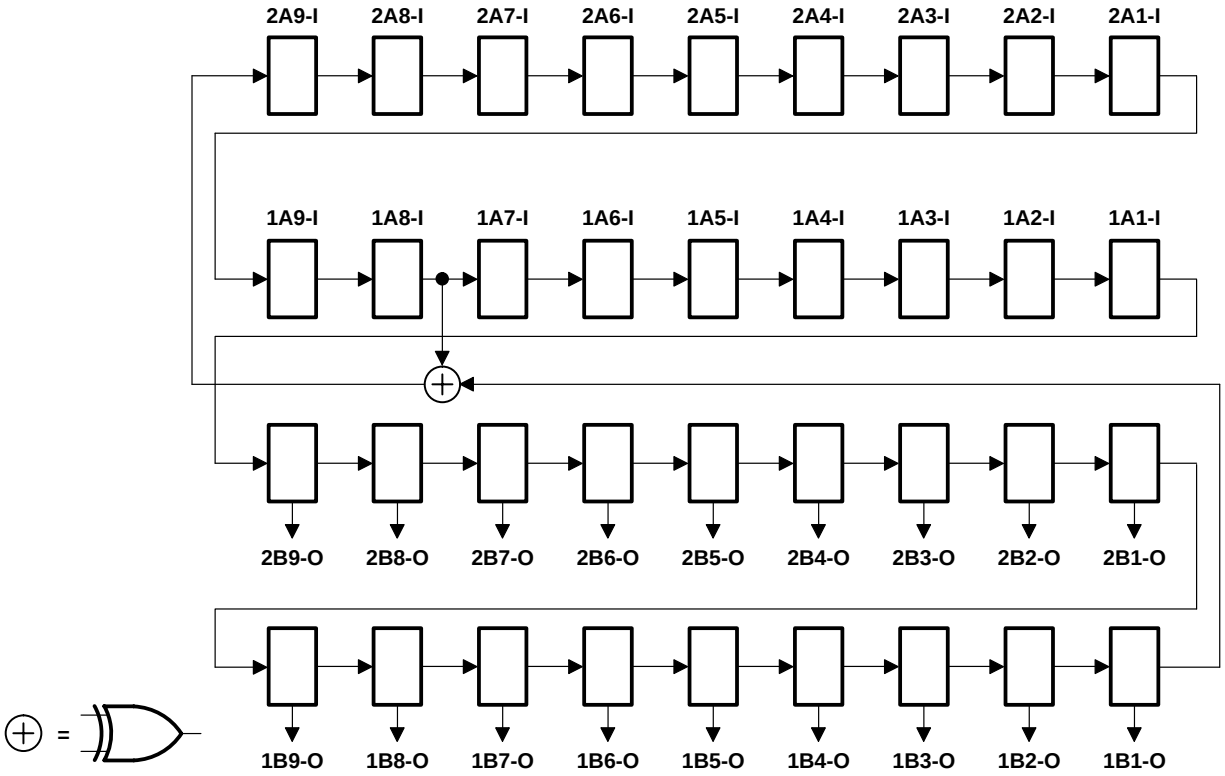


Figure 4. 36-Bit PRPG Configuration (1$\overline{\text{OEAB}}$ = 2$\overline{\text{OEAB}}$ = 0, 1$\overline{\text{OEBA}}$ = 2$\overline{\text{OEBA}}$ = 1)

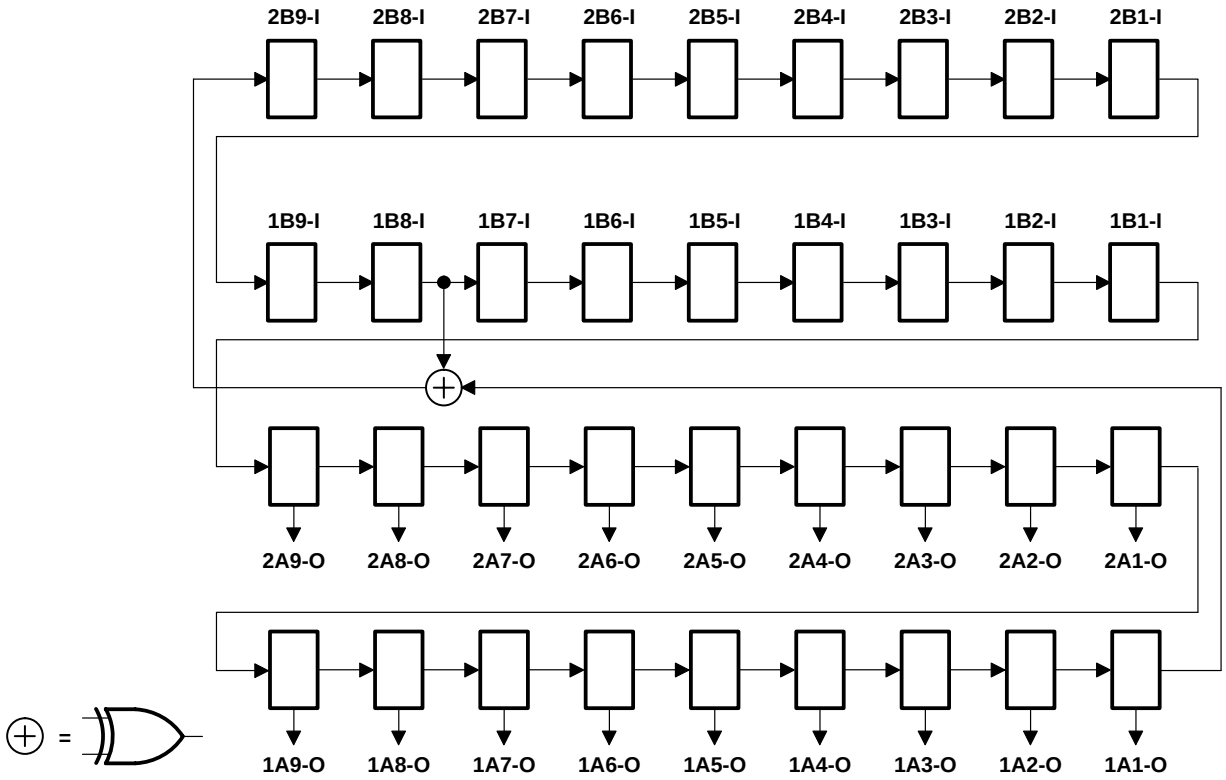


Figure 5. 36-Bit PRPG Configuration (1$\overline{OEAB}$ = 2$\overline{OEAB}$ = 1, 1$\overline{OEBA}$ = 2$\overline{OEBA}$ = 0)

parallel signature analysis (PSA)

Data appearing at the selected device input pins is compressed into a 36-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. Data in the shadow latches of the selected output BSCs remains constant and is applied to the device outputs. Figures 6 and 7 show the 36-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR prior to performing this operation.

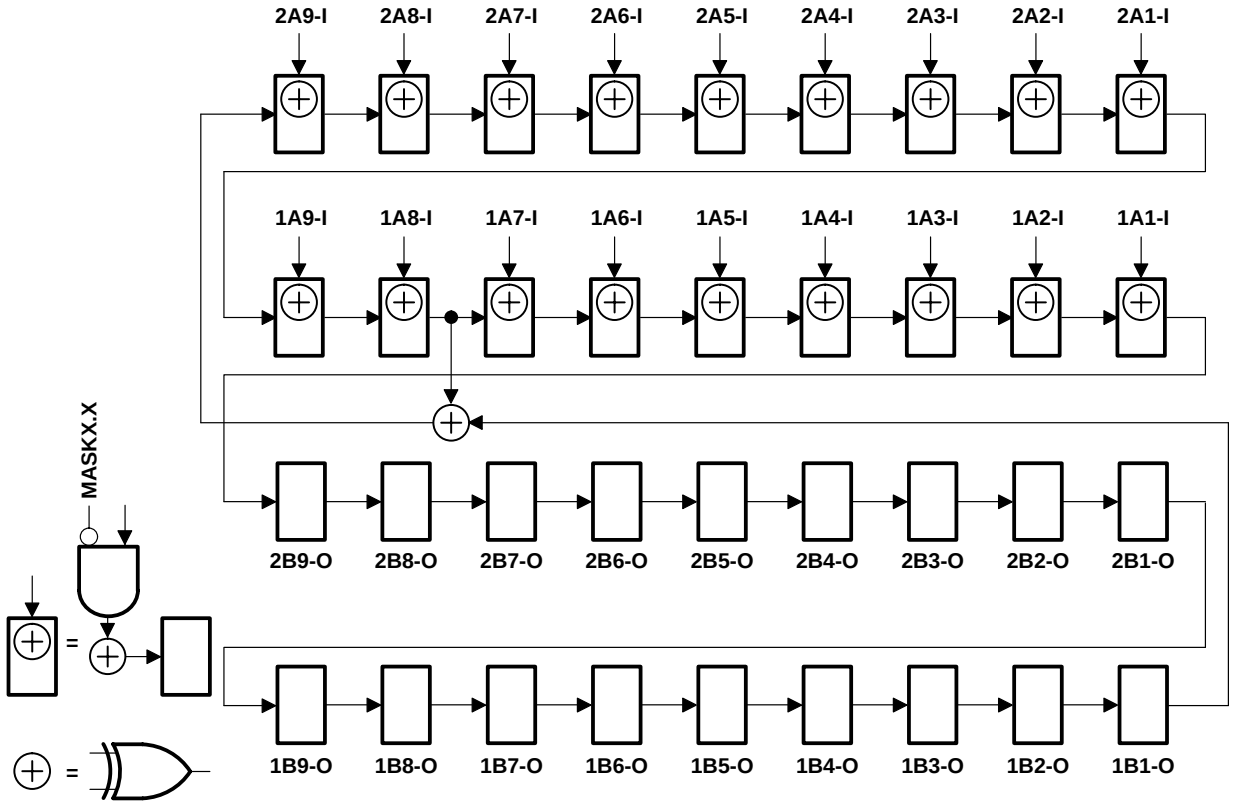


Figure 6. 36-Bit PSA Configuration (1$\overline{\text{OEAB}}$ = 2$\overline{\text{OEAB}}$ = 0, 1$\overline{\text{OEBA}}$ = 2$\overline{\text{OEBA}}$ = 1)

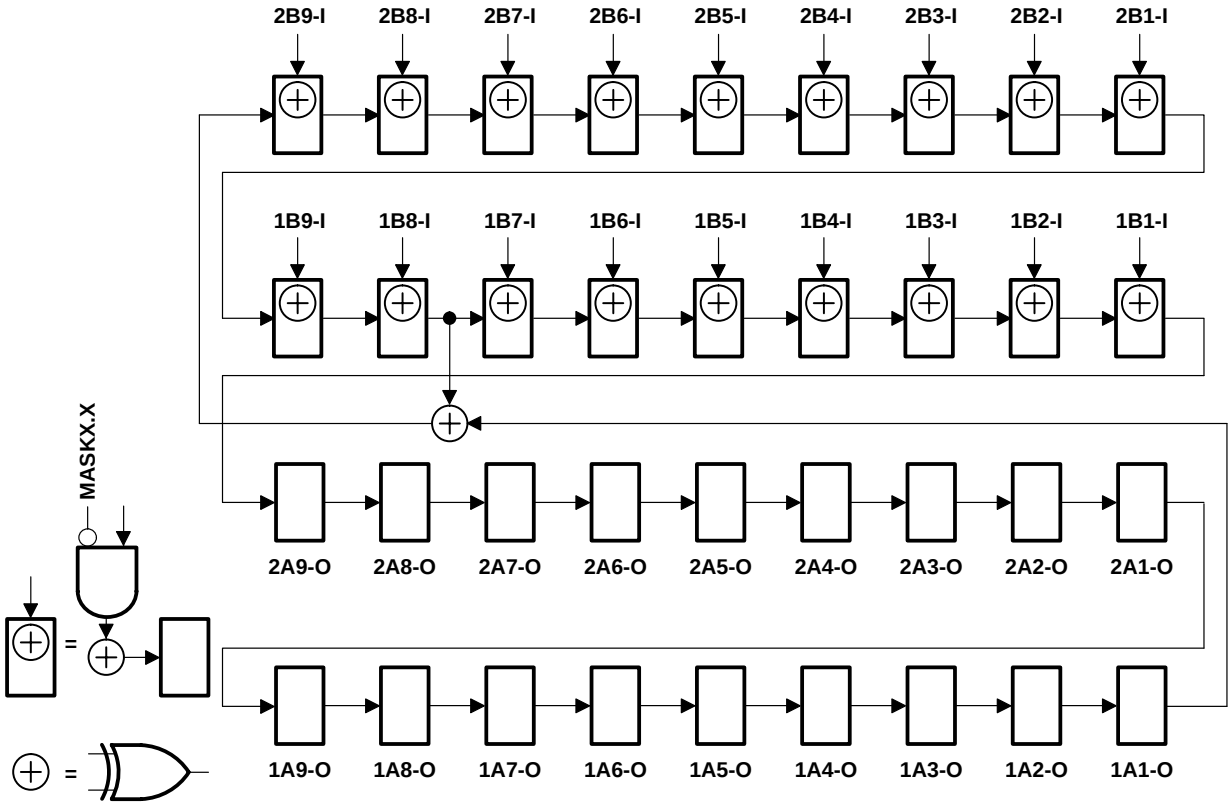


Figure 7. 36-Bit PSA Configuration (1$\overline{\text{OEAB}}$ = 2$\overline{\text{OEAB}}$ = 1, 1$\overline{\text{OEBA}}$ = 2$\overline{\text{OEBA}}$ = 0)

simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. At the same time, an 18-bit pseudorandom pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK. Figures 8 and 9 show the 18-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR prior to performing this operation. A seed value of all zeroes does not produce additional patterns.

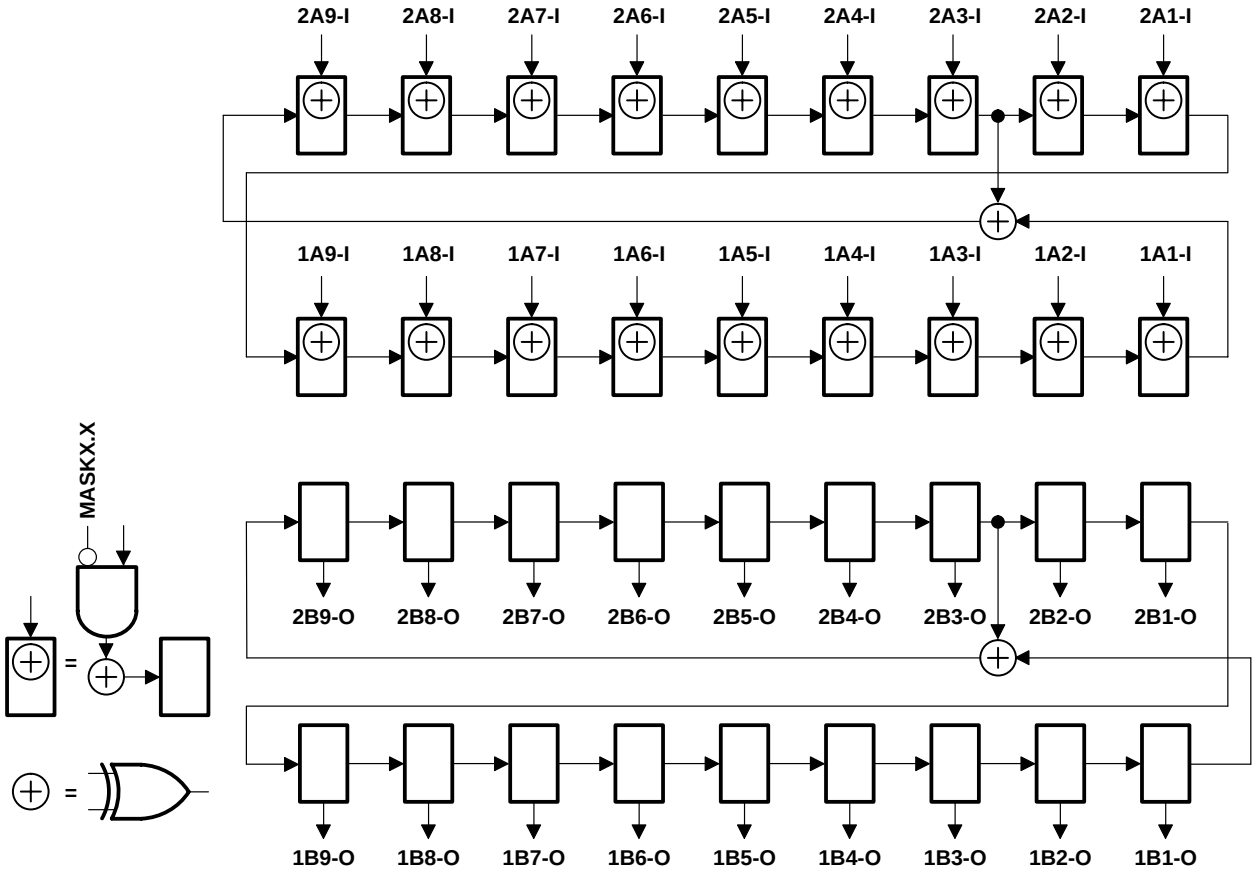


Figure 8. 18-Bit PSA/PRPG Configuration (1$\overline{\text{OEAB}}$ = 2$\overline{\text{OEAB}}$ = 0, 1$\overline{\text{OEBA}}$ = 2$\overline{\text{OEBA}}$ = 1)

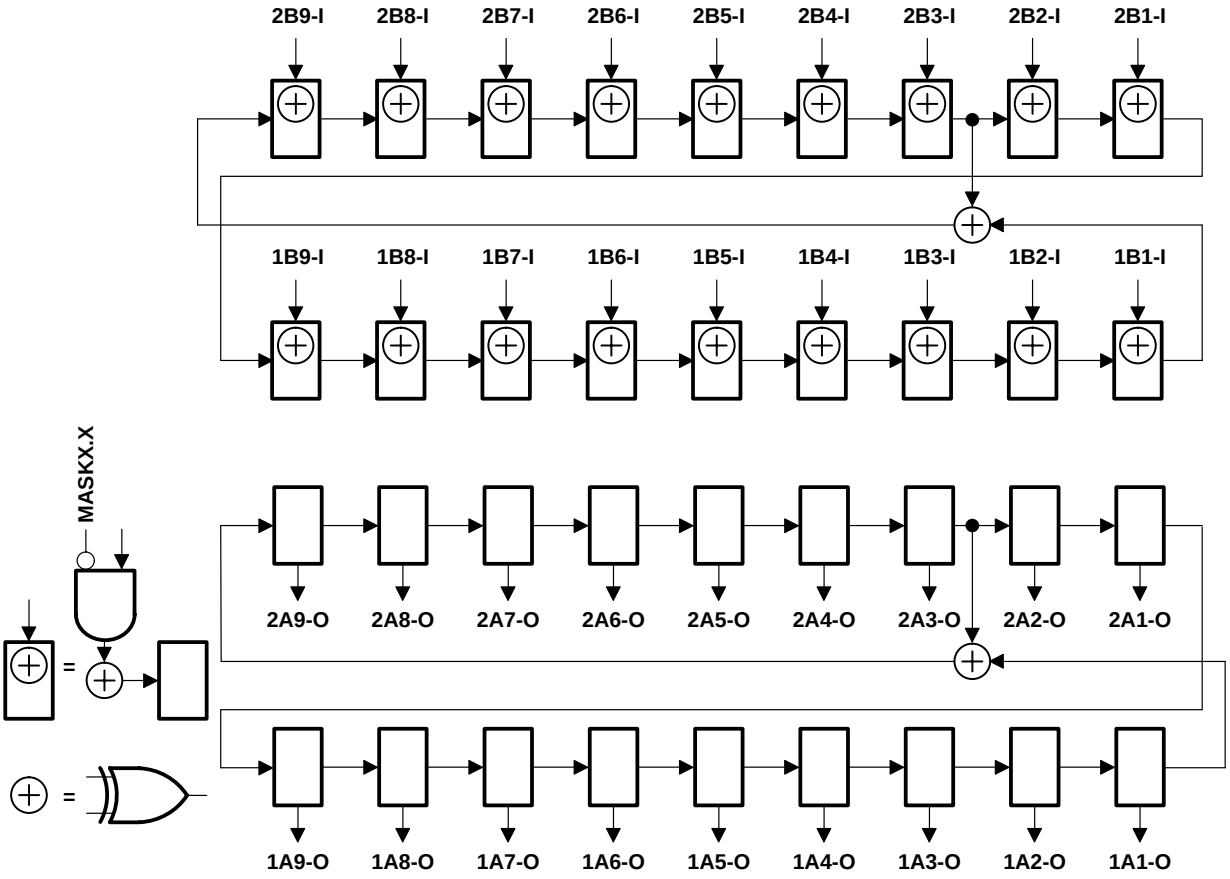


Figure 9. 18-Bit PSA/PRPG Configuration (1$\overline{OEAB}$ = 2$\overline{OEAB}$ = 1, 1$\overline{OEBA}$ = 2$\overline{OEBA}$ = 0)

simultaneous PSA and COUNT (PSA/COUNT)

Data appearing at the selected device input pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. At the same time, an 18-bit binary count-up pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK. Figures 10 and 11 show the 18-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR prior to performing this operation.

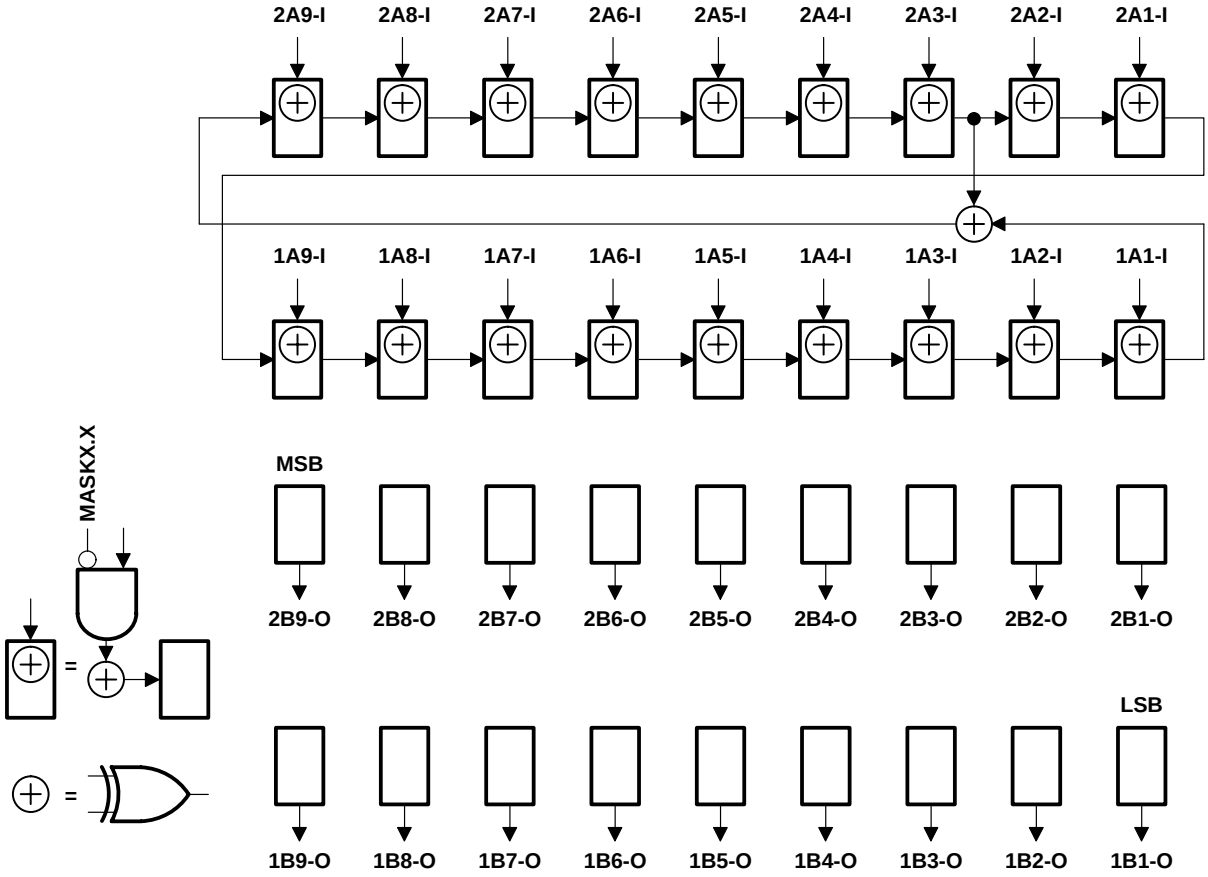


Figure 10. 18-Bit PSA/COUNT Configuration (1$\overline{OEAB}$ = 2$\overline{OEAB}$ = 0, 1$\overline{OEBA}$ = 2$\overline{OEBA}$ = 1)

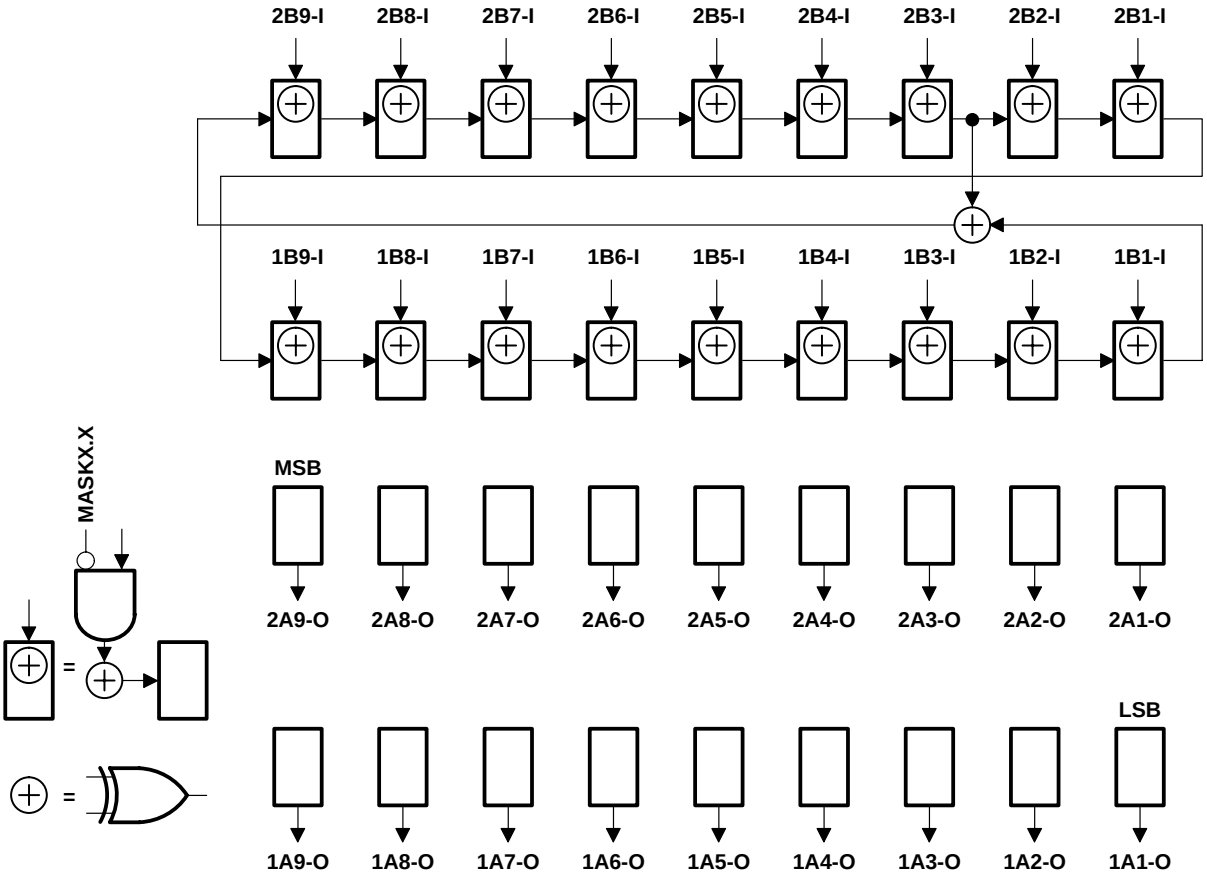


Figure 11. 18-Bit PSA/COUNT Configuration (1$\overline{OEAB}$ = 2$\overline{OEAB}$ = 1, 1$\overline{OEBA}$ = 2$\overline{OEBA}$ = 0)

timing description

All test operations of the SN74ABT18502 are synchronous to the TCK signal. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 12. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one IR scan and one DR scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data and TDO is used to output serial data. The TAP controller then is returned to the Test-Logic-Reset state. Table 6 explains the operation of the test circuitry during each TCK cycle.

Table 6. Explanation of Timing Example

TCK CYCLE(S)	TAP STATE AFTER TCK	DESCRIPTION
1	Test-Logic-Reset	TMS is changed to a logic-0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state.
2	Run-Test/Idle	
3	Select-DR-Scan	
4	Select-IR-Scan	
5	Capture-IR	The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state.
6	Shift-IR	TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
7–13	Shift-IR	One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic-1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic-1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR.
14	Exit1-IR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
15	Update-IR	The IR is updated with the new instruction (BYPASS) on the falling edge of TCK.
16	Select-DR-Scan	
17	Capture-DR	The bypass register captures a logic-0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state.
18	Shift-DR	TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
19–20	Shift-DR	The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO.
21	Exit1-DR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
22	Update-DR	In general, the selected DR is updated with the new data on the falling edge of TCK.
23	Select-DR-Scan	
24	Select-IR-Scan	
25	Test-Logic-Reset	Test operation completed

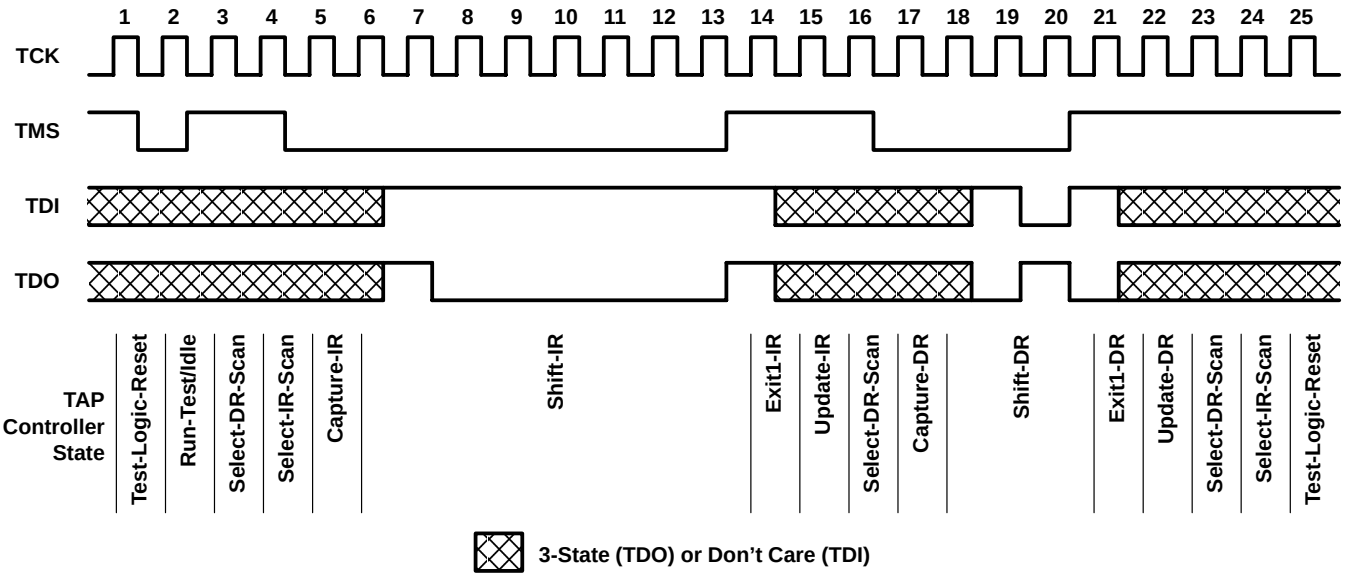


Figure 12. Timing Example

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I: Except I/O ports (see Note 1)	–0.5 V to 7 V
I/O ports (see Note 1)	–0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous current through V_{CC}	576 mA
Continuous current through GND	1152 mA
Package thermal impedance, θ_{JA} (see Note 2)	34°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP†	MAX			
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.5			2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3			3		
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA		2			2		
	V_{CC} = 4.5 V,	I_{OH} = – 32 mA		2					
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA				0.55		0.55	V
		I_{OL} = 64 mA				0.55			
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND	CLK, LE, $\overline{OE}$, TCK			±1		±1	µA
			A or B ports			±100		±100	
I_{IH}	V_{CC} = 5.5 V,	V_I = V_{CC}	TDI, TMS			10		10	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = GND	TDI, TMS			–150		–150	µA
I_{OZH}‡	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50	µA
I_{OZL}‡	V_{CC} = 5.5 V,	V_O = 0.5 V				–50		–50	µA
I_{OZPU}	V_{CC} = 0 to 2 V,	V_O = 2.7 V or 0.5 V,	$\overline{OE}$ = 0.8 V			±50		±50	µA
I_{OZPD}	V_{CC} = 2 V to 0,	V_O = 2.7 V or 0.5 V,	$\overline{OE}$ = 0.8 V			±50		±50	µA
I_{off}	V_{CC} = 0,	V_I or $V_O \le$ 4.5 V				±100		±450	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–110	–200	–50	–200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		3.5	5.5		5.5	mA
			Outputs low		33	38		38	
			Outputs disabled		2.9	5		5	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					50		50	µA
C_i	V_I = 2.5 V or 0.5 V	Control inputs			3				pF
C_{io}	V_O = 2.5 V or 0.5 V	A or B ports			10				pF
C_o	V_O = 2.5 V or 0.5 V	TDO			8				pF

† All typical values are at V_{CC} = 5 V.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 13)

				MIN	MAX	UNIT
f_{clock}	Clock frequency	CLKAB or CLKBA		0	100	MHz
t_w	Pulse duration	CLKAB or CLKBA high or low		3.5		ns
		LEAB or LEBA high		3.5		
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑		4		ns
		A before LEAB↓ or B before LEBA↓	CLK high	3.5		
			CLK low	2		
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑		0		ns
		A after LEAB↓ or B after LEBA↓		2		

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 13)

			MIN	MAX	UNIT
f_{clock}	Clock frequency	TCK	0	50	MHz
t_w	Pulse duration	TCK high or low	8		ns
t_{su}	Setup time	A, B, CLK, LE, or $\overline{OE}$ before TCK↑	4.5		ns
		TDI before TCK↑	7.5		
		TMS before TCK↑	3		
t_h	Hold time	A, B, CLK, LE, or $\overline{OE}$ after TCK↑	0.5		ns
		TDI after TCK↑	0.5		
		TMS after TCK↑	0.5		
t_d	Delay time	Power up to TCK↑	50		ns
t_r	Rise time	V_{CC} power up	1		µs

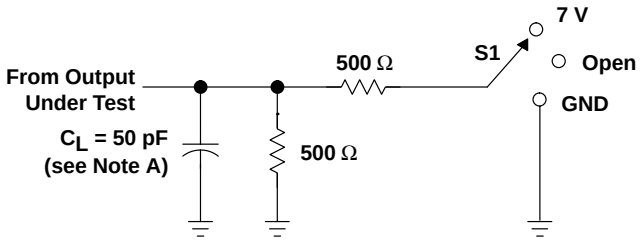
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 13)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}	CLKAB or CLKBA		100	130		100		MHz
t_{PLH}	A or B	B or A	2	3.8	5.6	2	6	ns
t_{PHL}			2	3.8	5.6	2	6	
t_{PLH}	CLKAB or CLKBA	B or A	2.5	4.7	5.7	2.5	6	ns
t_{PHL}			2.5	4.7	5.7	2.5	6	
t_{PLH}	LEAB or LEBA	B or A	2.5	4.9	6.4	2.5	7	ns
t_{PHL}			2.5	4.9	6.5	2.5	7	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2	4.9	6.3	2	7	ns
t_{PZL}			2.5	5.6	7.2	2.5	8	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	3	6.1	7.8	3	8.8	ns
t_{PLZ}			2.5	4.8	6.5	2.5	7.3	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 13)

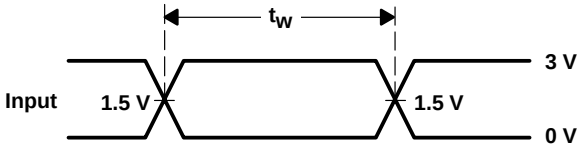
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}	TCK		50	90		50		MHz
t_{PLH}	TCK↓	A or B	2.5	9.1	11.4	2.5	13.5	ns
t_{PHL}			2.5	9.1	10.8	2.5	12.4	
t_{PLH}	TCK↓	TDO	2	3.8	5.1	2	5.6	ns
t_{PHL}			2	3.8	5.3	2	6	
t_{PZH}	TCK↓	A or B	4.5	9.5	11.5	4.5	13.4	ns
t_{PZL}			5	10.1	12.2	5	14	
t_{PZH}	TCK↓	TDO	2.5	4.6	5.9	2.5	6.8	ns
t_{PZL}			3	5.2	6.8	3	7.5	
t_{PHZ}	TCK↓	A or B	4	11.6	14.3	4	16.3	ns
t_{PLZ}			3.5	11.1	13.6	3.5	15.3	
t_{PHZ}	TCK↓	TDO	3	5.3	7.2	3	7.6	ns
t_{PLZ}			3	5.2	6.8	3	7.6	

PARAMETER MEASUREMENT INFORMATION

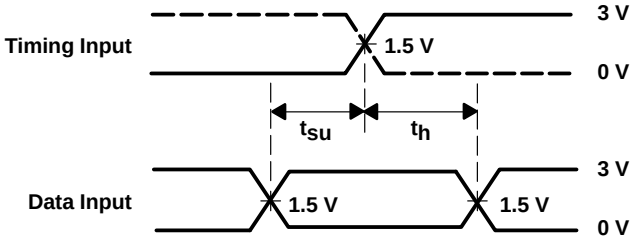


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

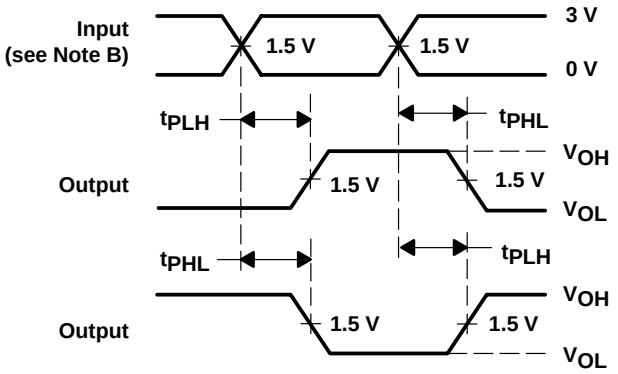
LOAD CIRCUIT FOR OUTPUTS



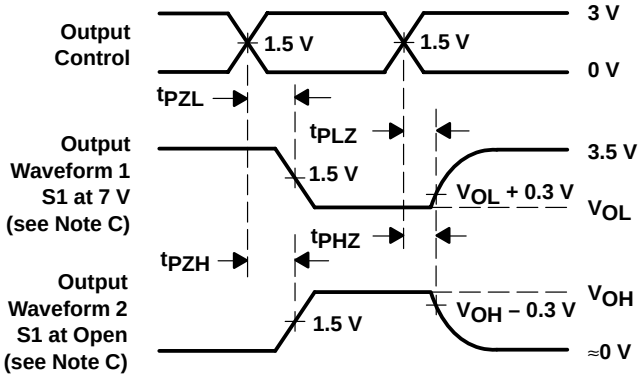
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NON-INVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 13. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ABT18502PM	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ABT18502
SN74ABT18502PM.B	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ABT18502
SN74ABT18502PMG4	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ABT18502
SN74ABT18502PMG4.B	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ABT18502
SN74ABT18502PMR	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ABT18502
SN74ABT18502PMR.B	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ABT18502

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74ABT18502 :

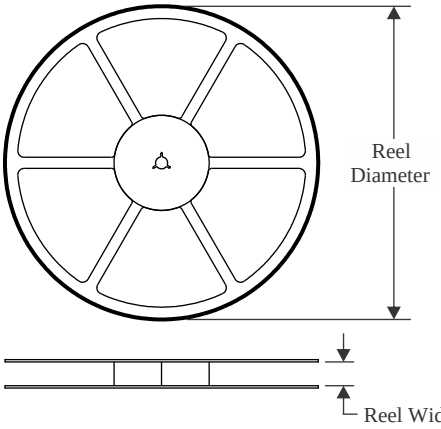
- Military : SN54ABT18502

NOTE: Qualified Version Definitions:

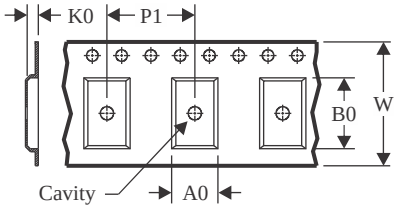
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

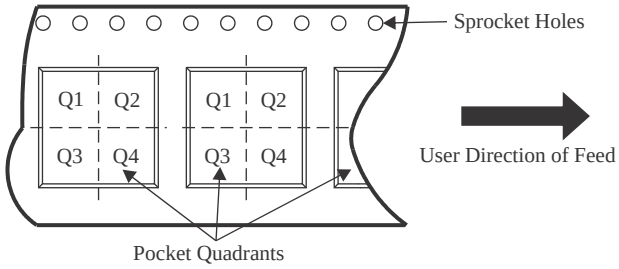


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

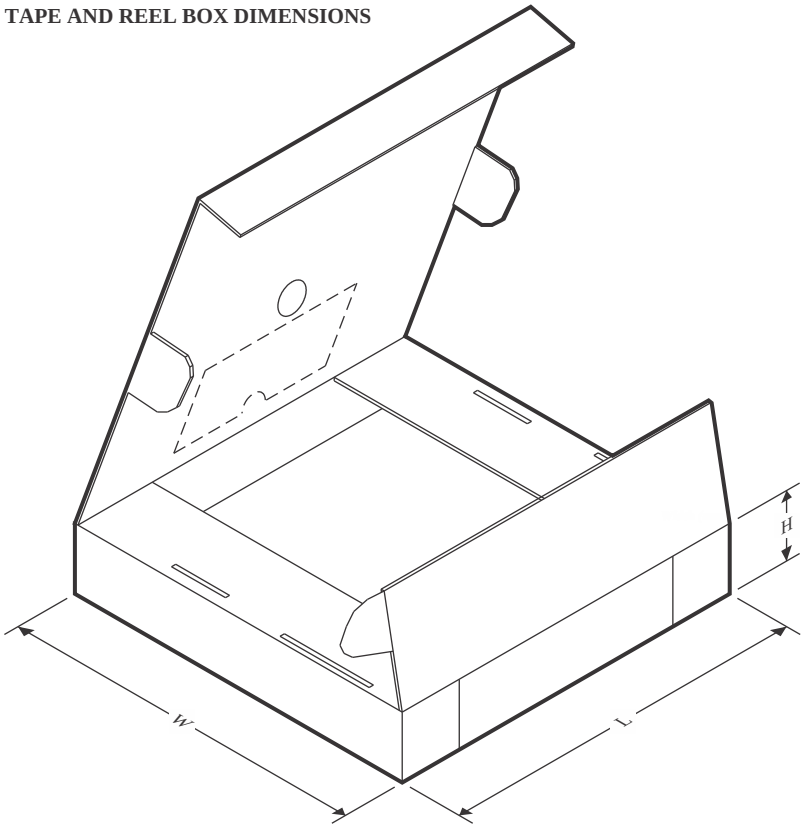
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT18502PMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2

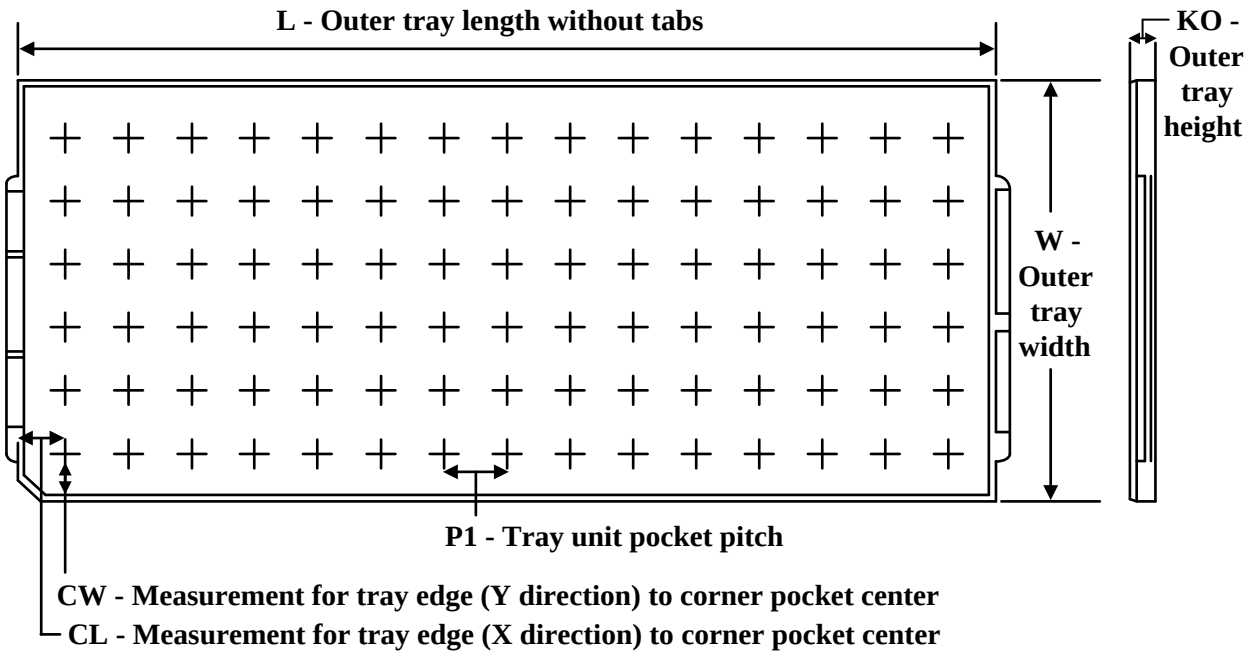
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT18502PMR	LQFP	PM	64	1000	350.0	350.0	43.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

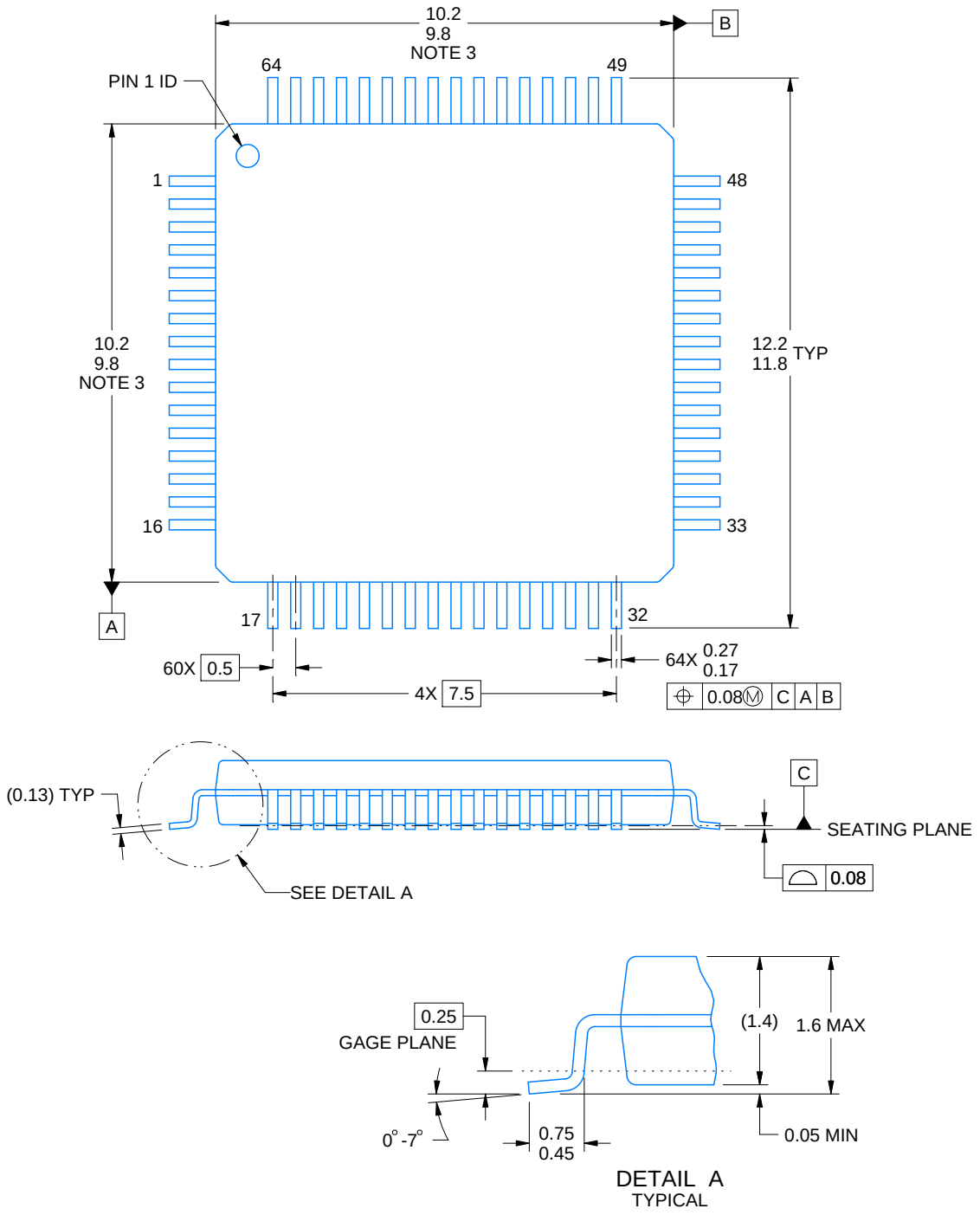
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
SN74ABT18502PM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
SN74ABT18502PM.B	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
SN74ABT18502PMG4	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
SN74ABT18502PMG4.B	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13

PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



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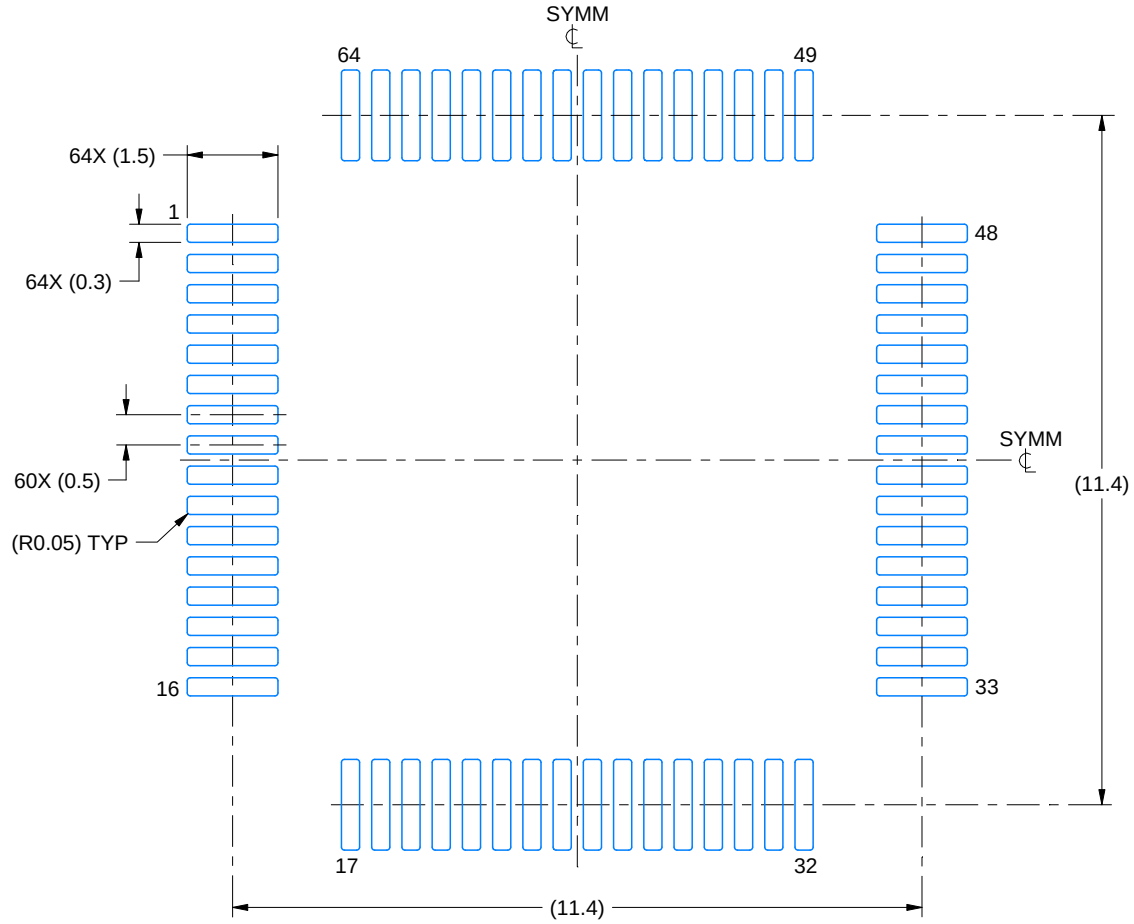
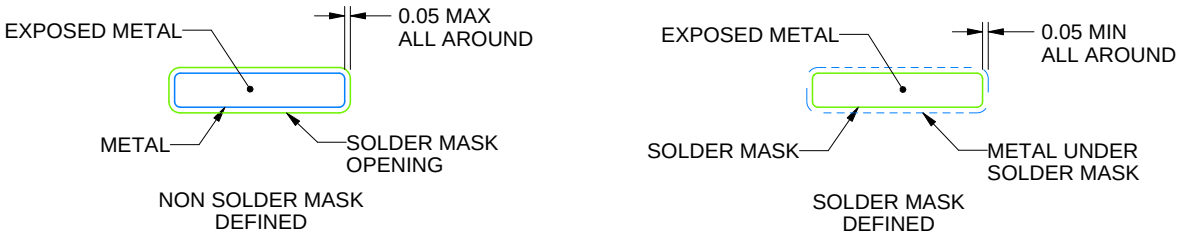
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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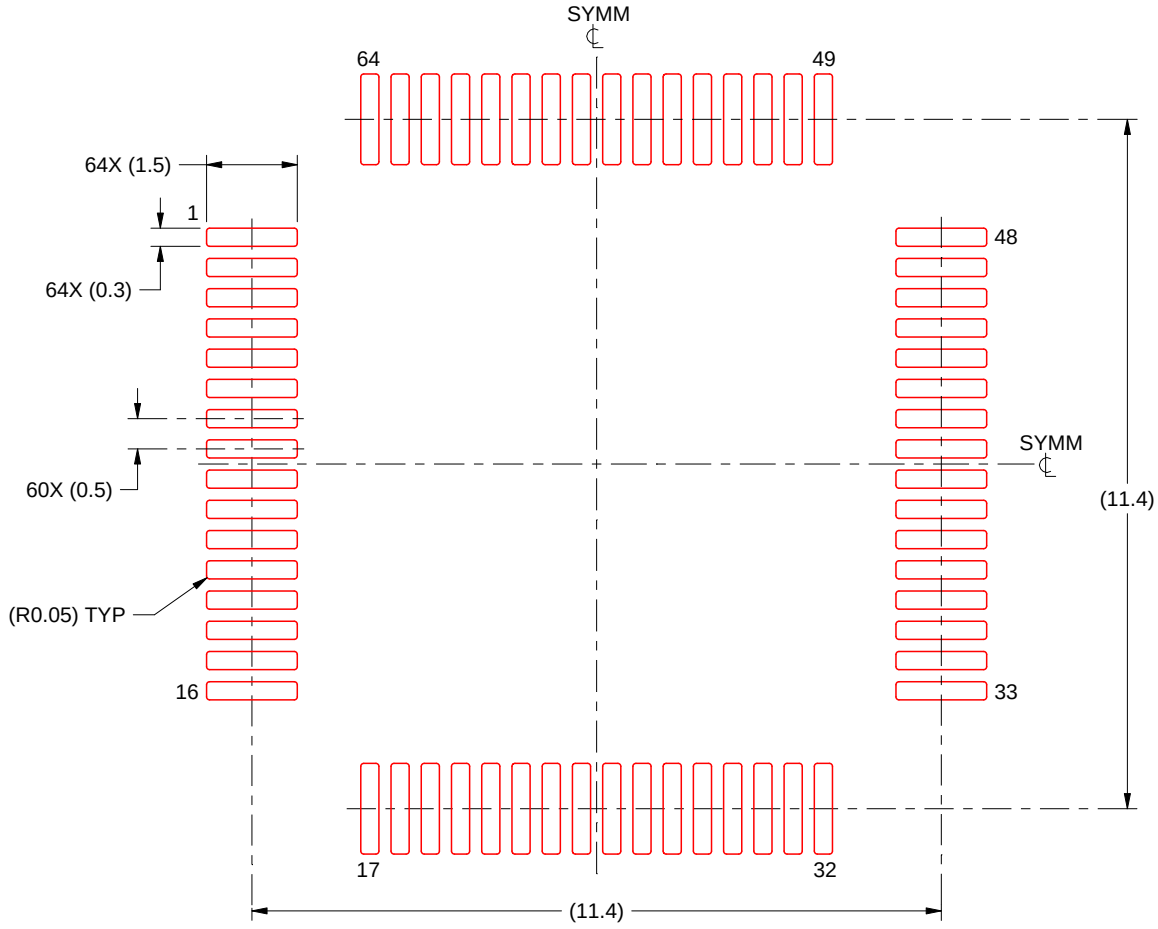
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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