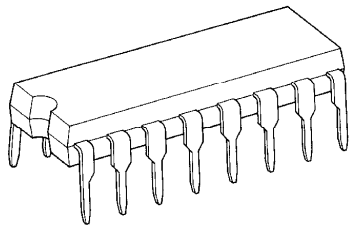
TOSHIBA DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9216P, TC9217P, TC9217F

HIGH SPEED PLL FOR DTS

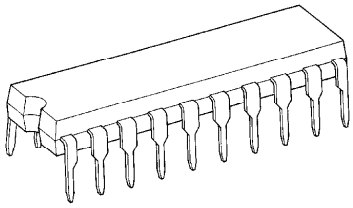
TC9216P, TC9217P, TC9217F are a high speed PLL-LSI with built-in 2 modulus prescaler. Each function is controlled through 3 serial bus lines and high performance digital tuning system can be constituted.

TC9216P



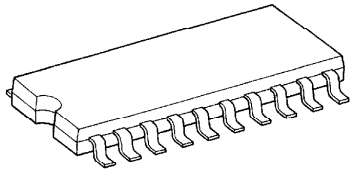
DIP16-P-300-2.54A

TC9217P



DIP20-P-300-2.54A

TC9217F



SOP20-P-300-1.27

Weight
DIP16-P-300-2.54A : 1.0g (Typ.)
DIP20-P-300-2.54A : 1.4g (Typ.)
SOP20-P-300-1.27 : 0.48g (Typ.)

FEATURES

- Suitable for DTS of Hi-Fi tuner and car stereo
- Built-in prescaler, and it can operate 30~140MHz (2 modulus type) at FM band and 0.5~40MHz (2 modulus type or direct frequency dividing type) at AM band.
- Built-in 16bit programmable counter, two parallel outputs phase comparator, crystal oscillator and reference counter.
- Crystal resonator can be used 4.5MHz or 7.2MHz.
- 15 kinds of reference frequency can be selected. (when crystal is used 4.5MHz) (Ref = 0.5k, 1k, 2.5k, 3k, 3.125k, 3.90625k, 5k, 6.25k, 7.8125k, 9k, 10k, 12.5k, 25k, 50k, 100kHz)
- Frequency measurement (HFC_{IN}, LFC_{IN}) of intermediate frequency etc. and periodic measurement (SC_{IN}) of low frequency pilot signal etc. are possible by built-in 16bit universal type frequency counter.
  (Note : TC9216P does not have periodic measurement function.)
- Built-in abundant general purpose input / output terminal and usable for control radio circuit part.
- All of function controls are performed through 3 serial bus lines.
- Operating voltage range : $V_{DD} = 5.0 \pm 0.5V$, and it is CMOS structure.
- Package is DIP-16 pin (TC9216P) and DIP-20 pin (TC9217P) and SOP-20 pin (TC9217F).

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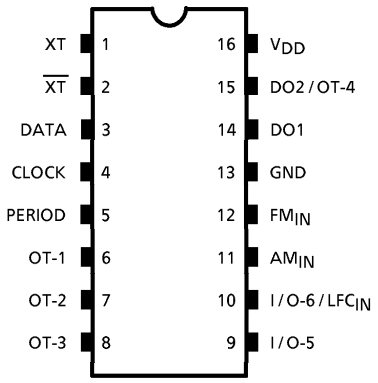
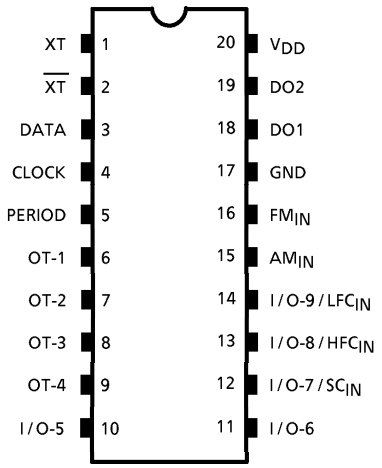
PIN CONNECTION

TC9216P



TOP VIEW
DIP-16 pin

TC9217P, TC9217F



TOP VIEW
DIP-20 pin, SOP-20 pin

980508EBA2'

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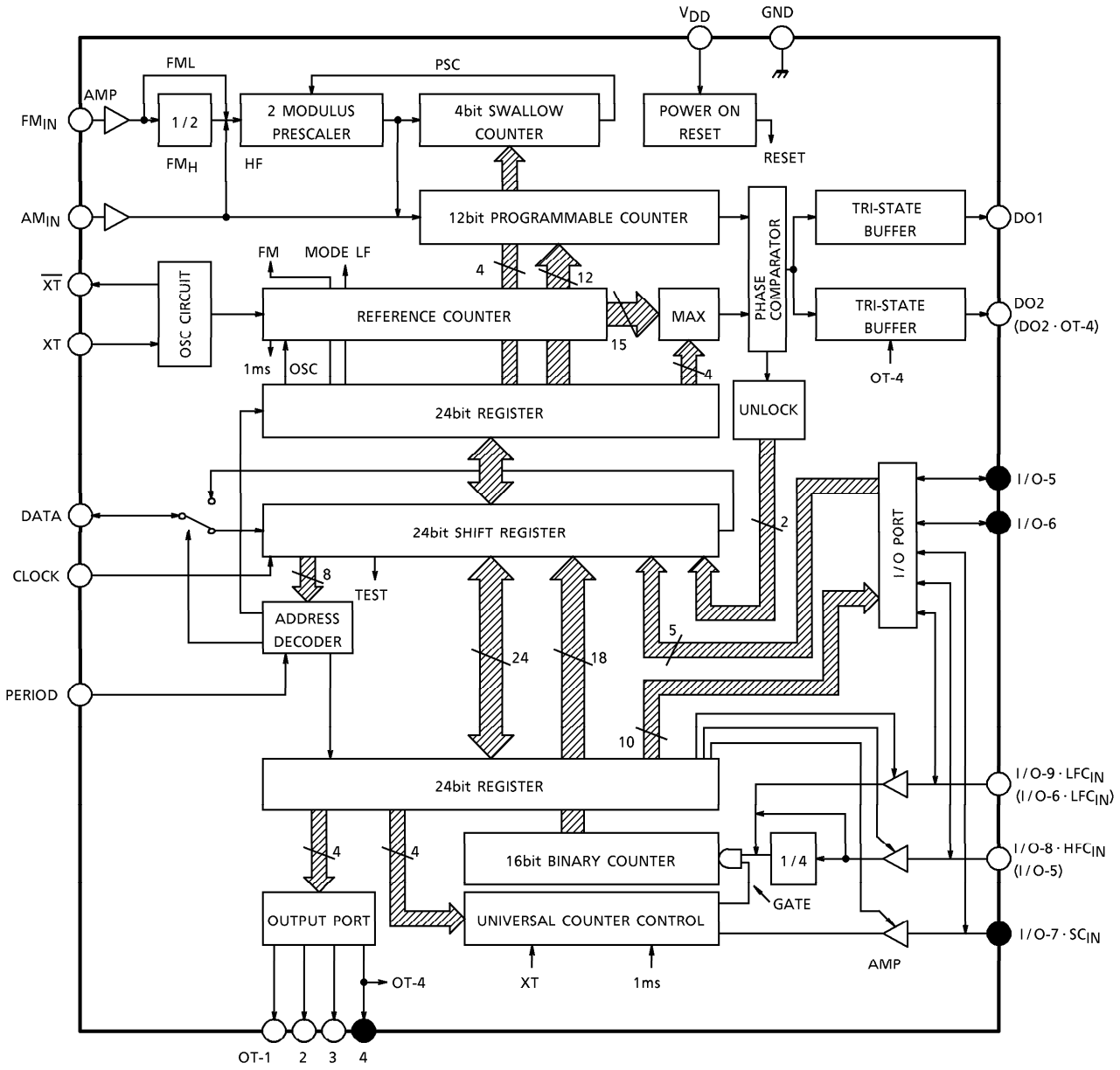
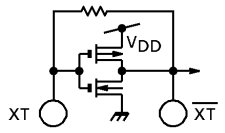
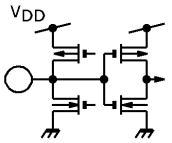
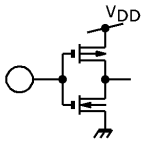
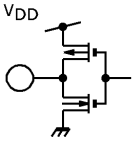
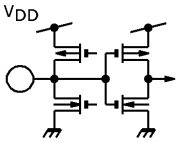
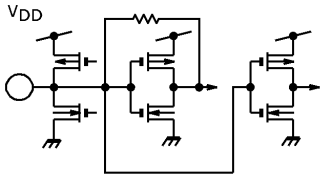
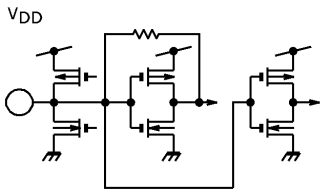
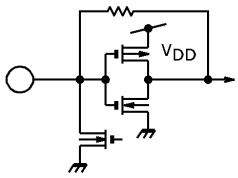
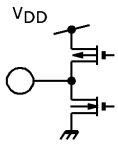
BLOCK DIAGRAM



(Note) ● Mark terminals are not existence in TC9216P.
Terminal name of TC9216P is shown in parentheses.
Others are common terminals.

PIN FUNCTION

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
1	XT	Crystal Oscillator Terminal	Crystal resonator of 7.2MHz or 4.5MHz shall be connected to this terminal to generate reference frequency and internal clock.	
2	$\overline{XT}$			
3	DATA	Serial Data Input / Output	Serial I / O port. Serial data transfer is performed between controller and these terminals to control universal counter and I / O port, and sets frequency dividing numbers and frequency dividing mode.	 DATA
4	CLOCK	Clock Signal Input		 CLOCK, PERIOD
5	PERIOD	Period Signal Input		
6	OT-1	General Purpose Output Port	These terminals are CMOS structure and used as output of control signal etc. They are set to "L" level at power "ON". (OT-4 of TC9216P can be used by switching DO2.)	
7	OT-2			
8	OT-3			
9 (–)	OT-4			
10 (9)	I / O-5	General Purpose I / O Port	These terminals are CMOS structure and can be used freely as input or output. It becomes input port at power "ON". (Exclusive terminal of I / O port is only I / O-5 in TC9216P.)	
11 (–)	I / O-6			
12 (–)	I / O-7 · SC_{IN}	General Purpose I / O Port / Universal Counter Periodic Measurement Input	This terminal is general purpose I / O port. It can be also used as signal input terminal which performs periodic measurement of low frequency signal by program control. (Note)It is set input mode of I / O port at power "ON".	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
13 (–)	I/O-8 · HFC_{IN}	General Purpose I/O port/Universal Counter Frequency Measurement Input	These terminals are general purpose I/O ports. They can be also used as input terminals for frequency measurement of universal counter by program control. Frequency measurement is available for intermediate frequency measurement etc. It is with built-in amp. and can operate small amplitude signal with capacitor coupling. (TC9216P does not have HFC_{IN} input.) (Note)It is set input mode of I/O port at power "ON".	
14 (10)	I/O-9 · LFC_{IN} (I/O-6 · LFC_{IN})			
15 (11)	AM_{IN}	Programmable Counter Input	The local oscillator signal of each FM/AM band is input to these terminals. It is with built-in amp. and can operate small amplitude signal with capacitor coupling.	
16 (12)	FM_{IN}			
18 (14)	DO1	Phase Comparator Output (General Purpose Output Port)	These terminals are tristate outputs of phase comparator. DO1 and DO2 are parallel output. (DO2 of TC9216P can be also used as general purpose output port by program control.)	
19 (15)	DO2 (DO2 · OT-4)			
17 (13)	GND	Power Supply Terminal	Power supply voltage of 5.0V ± 10% is applied to this terminal.	—
20 (16)	V_{DD}			

(*) No.1~8 pins are common terminals of TC9216P, TC9217P, TC9217F.
(*) Terminal name and number of TC9216P are shown in parentheses.

OPERATING DESCRIPTION

○ Serial I/O port

Each function is controlled by the data setting to a pair of 24bit registers, total of 48 bits. Each data of these registers is exchanged with controller side by 3 terminals of DATA, CLOCK and PERIOD through serial port.
Address 8 bits and data 24 bits, total of 32 bits, are transferred in serial at the same time.
Since all functions are controlled in the unit of register, so here explanations of address 8 bits and each register function are described chiefly. These registers are constituted in unit of 24 bits and selected by address of 8 bits. Address assignment table of each register is shown as the allocation of register in next page.

REGISTER	ADDRESS	CONSTITUTION OF 24BIT	NUMBER OF BIT
Input Register-1	D0H	Setting of PLL frequency dividing number. Selection of reference frequency. Setting of PLL input and operation mode. Selection of crystal oscillation frequency. Out-control OC.	16 4 2 1 1 (Total of 24)
Input Register-2	D2H	Control of universal counter (Control of PLL lock detection bit is included.) Test bit I/O port control Output data	9 1 5 9 (Total of 24)
Output Register	D1H (OC = 1)	Data of Register-1 (Mode B)	24 (Total of 24)
	D1H (OC = 0)	Count data of universal counter PLL lock detection data Unused (Mode A)	18 2 4 (Total of 24)
Output Register	D3H	Data of Register-2 Input data	19 5 (Total of 24)

Input data is latched to register-1 or -2 at the fall timing of PERIOD signal and each function is operated.
Each output data is latched to output register in parallel at the fall timing of the 9th of CLOCK signal and output from DATA terminal serially. Serial data of DATA, CLOCK and PERIOD is synchronized with crystal oscillation clock and taken into the internal circuit of LSI. By this reason if crystal oscillation is stopped, serial data can not be input.

(Note) When power is turned on, some internal circuits have undefined states to set internal circuit states, execute a dummy data transfer at least once before performing regular data transfer.

ALLOCATION OF REGISTER

Input Register

Address = D0H (LSB → MSB)

P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	R0	R1	R2	R3	FM	Mode	OSC	OC
Programmable Counter Data																Reference Code Data			Programmable Counter Mode			Crystal Selection	Out-Control

Address = D2H

G0	G1	CM0	CM1	CM2	SC (*1)	HFC (*1)	LFC	START RESET	TEST	C5 (*1)	C6 (*1)	C7 (*1)	C8 (C5)	C9 (C6)	O1	O2	O3	O4	O5 (*1)	O6 (*1)	O7 (*1)	O8 (O5)	O9 (O6)
Gate Time Selection		Counter Mode Selection			Counter Input Control (*3)			Start bit	Test (*5)	I/O Port Control (*3)					Output Port Data				Output Port Data (*3)				

Output Register

Address = D1H and OC = "0" (Mode A)

f0	f1	f2	f3	f4	f5	f6	f7	f8	f9	f10	f11	f12	f13	f14	f15	OVER	BUSY	ENA-BLE	UN LOCK	"0"	"0"	"0"	"0"
Universal Counter Data																Lock Detection Data				Unused			

Address = D3H

G0	G1	CM0	CM1	CM2	SC (*2)	HFC (*2)	LFC	"0"	TEST	C5 (*2)	C6 (*2)	C7 (*2)	C8 (C5)	C9 (C6)	O1	O2	O3	O4	I5 (*2)	I6 (*2)	I7 (*2)	I8 (I5)	I9 (I6)
Gate Time Selection		Counter Mode Selection			Counter Input Control (*3)			Unused	Test	I/O Port Control (*3)					Output Port Data				I/O Port Input Data (*3)				

Address = D1H and OC = "1" (Mode B)

* Usually OC = "1"

P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	R0	R1	R2	R3	FM	Mode	OSC	OC*
Programmable Counter Data																Reference Code Data			Programmable Counter Mode			Crystal Selection	Out-Control Data

At POWER ON RESET operation, each data of input register is set as shown below.

Input Register

Address = D0H (LSB → MSB)

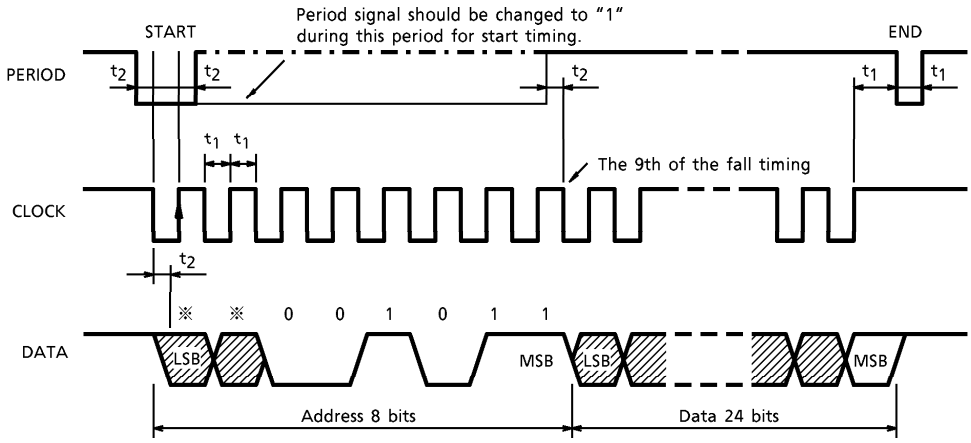
*4	*4	*4	*4	*4	*4	*4	*4	*4	*4	*4	*4	*4	*4	*4	*4	*4	*4	*4	*4	1	1	0	0

Address = D2H

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(Note) *1 : Don't care in TC9216P.
*2 : Data is set to "0" in TC9216P.
*3 : Bit name of TC9216P is shown in parentheses.
*4 : don't care
*5 : TEST bit is set to "0".

○ Serial transmission format



Min.
$t_1 \geqq 1.0\mu s$
$t_2 \geqq 0.3\mu s$

- Serial transmission format consists of address 8 bits and data 24 bits as mentioned above. Address of D0H~D3H is used in this LSI.

○ Crystal resonator connecting terminal (XT, $\overline{XT}$)

It can generate the clock signal necessary for inside operation of LSI by connecting crystal resonator and capacitors as shown in Fig.1.
Crystal resonator can be selected either 4.5MHz or 7.2MHz.
Serial Data "OSC" bit should be set to "0" at 4.5MHz selection.
Serial Data "OSC" bit should be set to "1" at 7.2MHz selection.

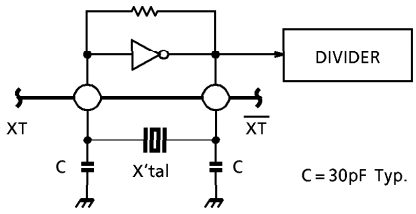


Fig.1

○ Programmable counter

Programmable counter part consists of 1/2 prescaler, 2 modulus prescaler and 4 bits + 12 bits programmable binary counter.

1. Setting of programmable counter

16 bits data of frequency dividing number and 2 bits of frequency dividing mode is set to programmable counter.

(1) Setting of frequency dividing mode

Input terminal and frequency dividing mode (pulse swallow mode or direct frequency dividing mode) shall be selected by FM and MODE bit.

Since 4 kinds of modes are prepared as shown below, so it shall be selected according to the frequency band used.

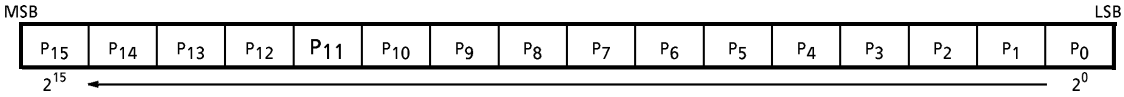
MODE	MODE	FM	FREQUENCY DIVIDING MODE	EXAMPLE OF RECEIVING BAND	INPUT FREQUENCY RANGE	INPUT TERMINAL	FREQUENCY DIVIDING NUMBER
LF	0	0	Direct frequency dividing mode	LW, MW, SW_L	0.5~ 10MHz	AM_{IN}	n
HF	1	0	Pulse swallow mode	SW_H	2~ 40MHz	AM_{IN}	n
FM_L	0	1		FM	30~ 140MHz	FM_{IN}	n
FM_H	1	1	1/2 + pulse swallow mode	FM	50~ 140MHz	FM_{IN}	2·n

(Note) n represents programmed numeral value.

(2) Setting of frequency dividing number

Frequency dividing number of programmable counter is set to P0~P15 bits in binary.

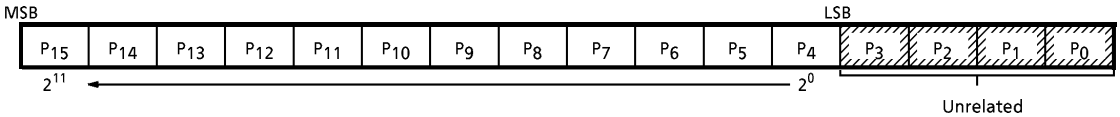
- Pulse swallow mode (16 bits)



Setting range of frequency dividing number (Pulse swallow mode) : n = 210H~FFFFH (528~65535)

(Note) Actual dividing number becomes the double of programmed numeral value in 1/2 + pulse swallow mode.

- Direct frequency dividing mode (12 bits)

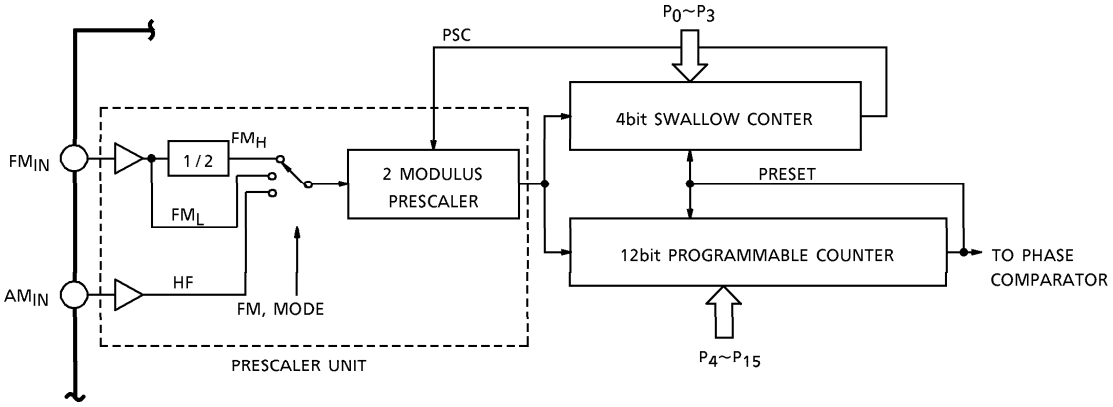


Setting range of frequency dividing number (Direct frequency dividing mode) :
n = 10H~ FFFH (16~4095)

Data of P0~P3 is unrelated and P4 bit becomes LSB at direct frequency dividing mode.

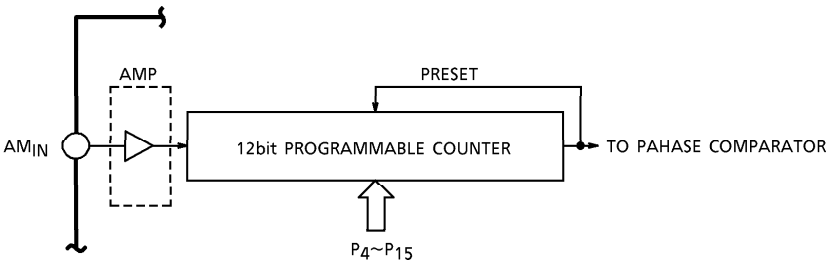
2. Circuit construction of prescaler and programmable counter

(1) Circuit construction at pulse swallow mode



It consists of 2 modulus prescaler, 4bit swallow counter and 12bit programmable counter. 1/2 prescaler is added to the front stage of 2 modulus prescaler at FM_{IN} (FM_H mode).

(2) Circuit construction at direct frequency dividing mode



Prescaler unit becomes unused at direct frequency dividing mode and 12bit programmable counter is only used.

(3) Each input of FM_{IN} / AM_{IN} has built-in amp. and can operate small amplitude signal with capacitor coupling.

○ Reference divider (Frequency divider for reference frequency)

Reference divider unit consists of crystal oscillator and counter. Crystal resonator can be selected either 4.5MHz or 7.2MHz and 15 kinds (max.) of reference frequencies are generated.

1. Setting of reference frequency

Reference frequency is setting by R0~R3 bits.

R_3	R_2	R_1	R_0	REFERENCE FREQUENCY	R_3	R_2	R_1	R_0	REFERENCE FREQUENCY
0	0	0	0	0.5kHz	1	0	0	0	※7.8125kHz
0	0	0	1	1kHz	1	0	0	1	9kHz
0	0	1	0	2.5kHz	1	0	1	0	10kHz
0	0	1	1	3kHz	1	0	1	1	12.5kHz
0	1	0	0	3.125kHz	1	1	0	0	25kHz
0	1	0	1	※3.90625kHz	1	1	0	1	50kHz
0	1	1	0	5kHz	1	1	1	0	100kHz
0	1	1	1	6.25kHz	1	1	1	1	—

※ Mark frequencies are only available at 4.5MHz crystal resonator used.

Crystal oscillation frequency is selected by crystal select bit (OSC).

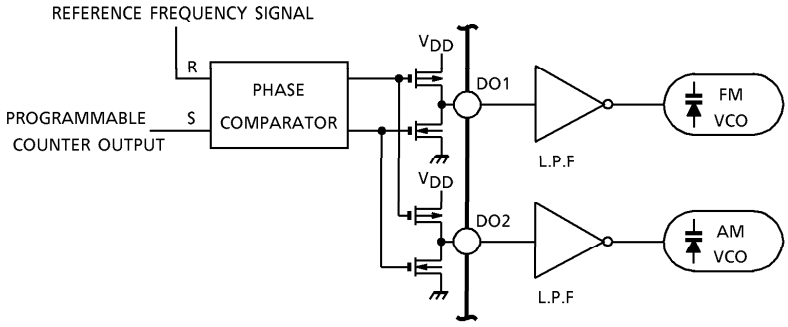
OSC = "0"……4.5MHz

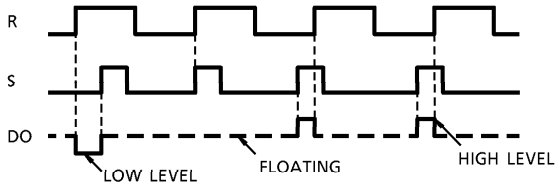
OSC = "1"……7.2MHz

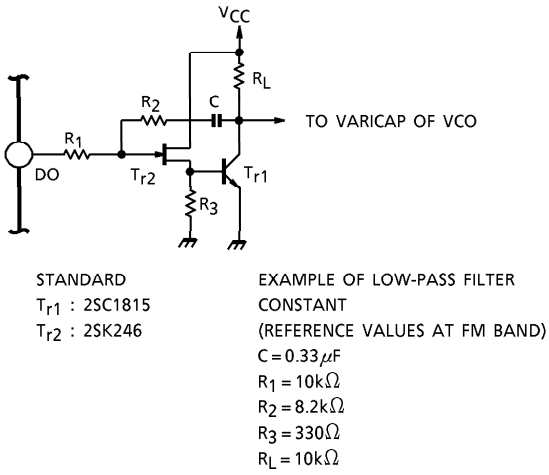
(Note) OSC bit is set "0" (4.5MHz) when power supply is "ON".

○ Phase comparator

Phase comparator compares reference frequency signal supplied from reference frequency divider and programmable counter frequency dividing output. It outputs the observational error and controls VCO through low-pass filter to make frequency and phase difference between these two signals accord.
Filter constant can be designed suitably for every band of FM / AM because Tri-state buffer DO1 and DO2 terminals are output from phase comparator in parallel.







DO Output Timing Chart

Example of Active Low-Pass Filter Circuit

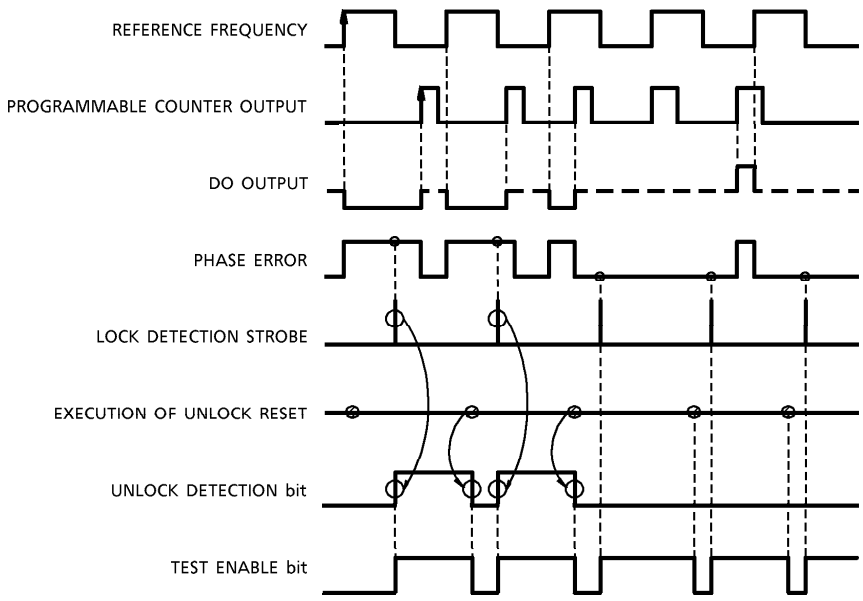
DO output timing chart and an example of active low-pass filter circuit through the darlington connection of FET and transistor are shown in the above diagram.
Besides, the filter circuit shown in the above diagram is one of example for reference and so, an actual circuit shall be examined and designed according to the receiving band constitution of the system and required characteristics.

(Note) DO2 terminal of TC9216P can be switched and used as OT-4 terminal by program control.

○ Unlock detection bit

This bit is to detect the lock condition of PLL system. Phase error pulses are output to unlock F/F from phase comparator at timing of reference frequency period in the PLL unlocked state, that is, when reference frequency does not accord with programmable counter frequency dividing output (unlock condition). The unlock F/F is set by these pulses. And whenever START/RESET bit (unlock reset bit) of register-2 is set to "1", unlock F/F is reset. Lock condition can be detected by access of unlock detection bit after resetting the unlock F/F. It is necessary to access the unlock detection bit (UNLOCK) after having a time more than reference period after resetting the unlock F/F because error pulses are input at reference period. If this time was shorter, the correct lock condition can not be detected. Therefore, the test enable F/F is provided.

This F/F is reset whenever unlock reset bit is set to "1", and it is set to "1" at the unlock detection timing. That is, the unlock condition can be detected correctly when this test enable bit (ENABLE) is set to "1".



○ Universal frequency counter

Universal frequency counter is used as frequency calculation of FM / AM band intermediate frequency (IF) for auto stop signal detection at auto search tuning, etc.
Two types of measurement mode are available by use of universal counter. One is the frequency measurement mode (HFC_{IN}, LFC_{IN} Input) that counts the input pulses enter the universal counter in a constant time (gate-time), and the other is the period measurement mode (SC_{IN} Input) that counts the reference clock pulses (period measurement pulses) enter the universal counter in a period of the input pulses. Measurement mode is selected according to the frequency measured. but in TC9216P SC_{IN}, HFC_{IN} inputs are not provided and period measurement mode is not available. Besides, each terminal can be also used as I / O port.

1. Universal counter control bit

① G_0, G_1 bit ..... Gate-time of universal counter is selected by these bits.

G_1	G_2	GATE-TIME	PERIOD MEASUREMENT PULSE
0	0	1ms	50k (20μs)
0	1	4ms	150k (6.6μs)
1	0	16ms	900k (1.1μs)
1	1	Manual *	Crystal oscillator frequency

* Gate-time can be set freely in the manual mode by using time base of controller. (The gate-time less than 2 cycles of serial transmission format can not be set because it is controlled by START bit)

② START bit ..... Measurement starts whenever START bit is set to "1".

(Note) In manual mode the count starts when START bit is set to "1" and stops when START is set to "0".

③ CM0, CM1, CM2 bit ..... Each measurement mode of universal counter and input terminal are selected by these bits. Besides, it also controls the switching of DO2 / OT-4 function in TC9216P.

CM 2	CM 1	CM 0	TC9216P			TC9217P·TC9217F	
			COUNTER INPUT TERMINAL	COUNTER MODE	DO2 · OT-4 TERMINAL	COUNTER INPUT TERMINAL	COUNTER MODE
0	0	0	LFC_{IN}	LFC Mode	DO2	LFC_{IN}	LFC Mode
0	0	1	LFC_{IN}	LFC Mode	DO2	LFC_{IN}	LFC Mode
0	1	0	*	*	*	HFC_{IN}	MFC Mode
0	1	1	*	*	*	HFC_{IN}	HFC Mode
1	0	0	LFC_{IN}	LFC Mode	OT-4	*	*
1	0	1	LFC_{IN}	LFC Mode	OT-4	*	*
1	1	0	*	*	*	*	*
1	1	1	*	*	*	SC_{IN}	SC Mode

* : Don't use

	MODE	INPUT FREQUENCY RANGE
LFC Mode	Frequency Measurement	F_{IN} = 0.3~ 15MHz
MFC Mode		F_{IN} = 5~ 20MHz
HFC Mode		F_{IN} = 5~ 60MHz
SC Mode	Period Measurement	F_{IN} = ~100kHz

(Note) 1/4-prescaler is added to the front stage of the universal counter (16 bits binary counter) in HFC mode. Therefore, signal input to HFC_{IN} is divided by 4 in the prescaler and transmitted to the universal counter.

④ LFC, HFC, SC bit ..... Input terminals of universal counter are controlled by these bits. Switching between universal counter input and I/O port are controlled by these bits.

	DATA	TC9217P·TC9217F	TC9216P
LFC	0	I/O Port (I/O-9)	I/O Port (I/O-6)
	1	Frequency Counter Input (LFC_{IN})	Frequency Counter Input (LFC_{IN})
HFC	0	I/O Port (I/O-8)	Unprepared
	1	Frequency Counter Input (HFC_{IN})	
SC	0	I/O Port (I/O-7)	
	1	Period Measurement Input (SC_{IN})	

2. Universal counter data output register

① Universal counter calculation data bits (f_0~f_{15})

The calculated result in the universal counter can be read out from output registers of f_0~f_{15} in binary. In this case, OC bit of input register-1 should be set to "0".

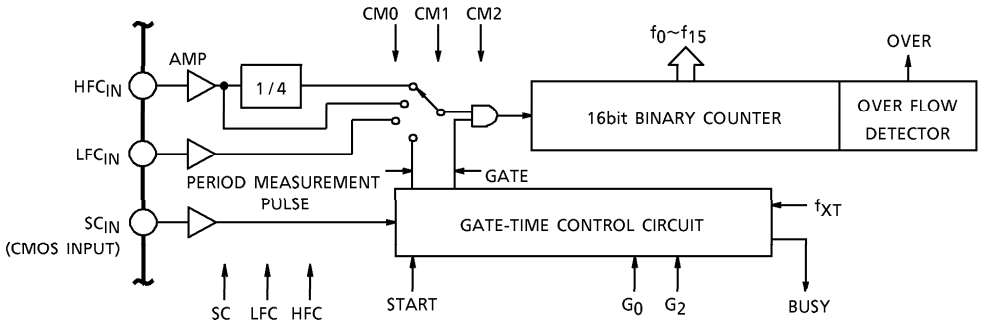
② Universal counter operational detection bit

- OVER .... Universal counter over flow bit
  - "1" ... Universal counter over flow condition
  - "0" ... Universal counter data normal condition
- BUSY ..... Universal counter operation monitor bit
  - "1" ... Under universal counter calculation
  - "0" ... Universal counter calculation end

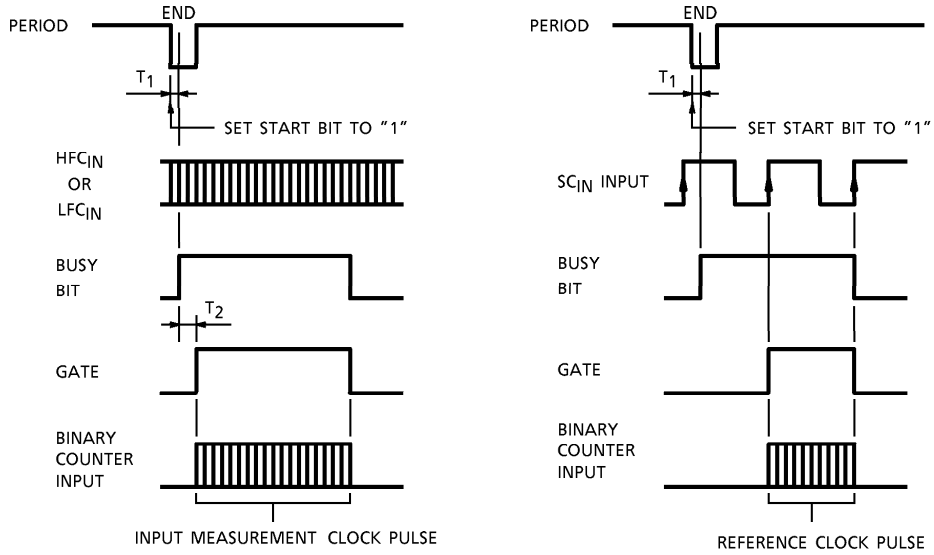
(Note) Refer to the contents of universal counter calculation data bits (f_0~f_{15}) after confirmation of BUSY bit = "0" (END of calculation) and OVER bit = "0" (Data normal condtion) at the use of universal counter.

3. Circuit construction of universal counter

Universal counter unit consists of input amp., gate-time control circuit and 16bit binary counter.



4. Measurement timing of universal counter



Frequency Measurement Timing Chart　　Period Measurement Timing Chart

$0 < T_1 \leqq 0.25$ (μs) 、 $0 < T_2 \leqq 1$ (ms)

(Note) HFC_{IN} and LFC_{IN} are with built-in amp. and can operate small amplitude signal with capacitor coupling.

(Note) SC_{IN} signal should be used with logic level because its input is CMOS structure.

(note) Calculation at manual mode is started at rise timing of PERIOD signal end (START bit is set to "1") and is also finished at the same timing (START bit is set to "0").

○ General purpose input / output port

It has general purpose I / O port controlled through serial port.

INPUT / OUTPUT	TC9217P·TC9217F	TC9216P	INPUT / OUTPUT CONSTRUCTION
Output Port	Exclusive : 4	Exclusive : 3 , (Max. : 4)	CMOS
I / O Port	Exclusive : 2 , (Max. : 5)	Exclusive : 1 , (Max. : 2)	CMOS

1. General purpose output port (OT-1~OT-4)

   The data set to 01~04 bits of input register-2 is output in parallel from each exclusive output port OT-1~OT-4 terminal. TC9216P does not have OT-4 exclusive output port but DO2 terminal can be switched and used as OT-4 output port by that CM1 bit is set to "0" and CM2 bit is set to "1" in input register-2 respectively.

2. General purpose I / O port (I / O-5~I / O-9)

   Input or output mode of I / O port is set according to the contents of C_5~C_9 bits in input register-2.
   Set each bit of C_5~C_9 to "0" at input mode setting.
   The data input from I / O-5~ I / O-9 terminals in parallel can be read out from DATA terminal as serial data of I_5~I_9.
   Input data is latched to the internal register at the fall timing of the 9th of serial clock.
   Set each bit of C_5~C_9 to "1" at output mode setting. The data set to O_5~O_9 bits of input register-2 is output from I / O port of I / O-5~I / O-9 terminal in parallel respectively.

   (Note) Since I / O-7~ I / O-9 terminal of TC9217P and I / O-6 of TC9216P are also combined with input terminal of universal counter, each bit of SC, HFC and LFC of input register-2 shall be set to "0" at the use of I / O port.

   (Note) I / O control port and output port are set to "0" at power "ON".
   (General purpose I / O port is set to input mode. General purpose I / O port terminals combined with universal counter inputs are set to input mode of I / O port and output condition of general purpose output port is set to "L" level.)

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3~6.0	V
Input Voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power Dissipation	P_D	300	mW
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−65~150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = −40~85°C, V_{DD} = 4.5~5.5V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Power Supply Voltage	V_{DD}	—	—	4.5	5.0	5.5	V
Operating Power Supply Current	I_{DD}	—	V_{DD} = 5.0V, X_T = 7.2MHz, FM_{IN} = 140MHz	—	15	25	mA

(Operating frequency range)

Crystal Oscillation Frequency	f_{XT}	—	Connect crystal resonator to XT-$\overline{XT}$ terminal	4.0	~	8.0	MHz
FM_{IN} (FM_H, FM_L)	f_{FM}	—	FM_H, FM_L mode, V_{IN} = 0.3V_{p-p}	50	~	140	MHz
FM_{IN} (FM_L)	f_{FML}	—	FM_L mode, V_{IN} = 0.4V_{p-p}	30	~	140	MHz
AM_{IN} (HF)	f_{HF}	—	HF mode V_{IN} = 0.3V_{p-p}	2	~	40	MHz
AM_{IN} (LF)	f_{LF}	—	LF mode V_{IN} = 0.3V_{p-p}	0.5	~	10	MHz
LFC_{IN} (LFC)	f_{LFC}	—	LFC mode V_{IN} = 0.3V_{p-p}	0.3	~	15	MHz
HFC_{IN} (MFC)	f_{MFC}	—	MFC mode V_{IN} = 0.3V_{p-p}	5	~	20	MHz
HFCIN (HFC)	f_{HFC}	—	HFC mode V_{IN} = 0.3V_{p-p}	5	~	60	MHz
SC_{IN}	f_{SC}	—	V_{IH} = V_{DD} × 0.7, V_{IL} = V_{DD} × 0.3, Square wave input	—	~	100	kHz

(Operating input amplitude range)

FM_{IN} (FM_H, FM_L)	V_{FM}	—	FM_H, FM_L mode f_{IN} = 50~140MHz	0.3	~	V_{DD} − 0.5	V_{p-p}
FM_{IN} (FM_L)	V_{FML}	—	FM_L mode f_{IN} = 30~140MHz	0.4	~	V_{DD} − 0.5	V_{p-p}
AM_{IN} (HF)	V_{HF}	—	HF mode f_{IN} = 2~40MHz	0.3	~	V_{DD} − 0.5	V_{p-p}
AMIN (LF)	V_{LF}	—	LF mode f_{IN} = 0.5~10MHz	0.3	~	V_{DD} − 0.5	V_{p-p}
LFC_{IN} (LFC)	V_{LFC}	—	LFC mode f_{IN} = 0.3~15MHz	0.3	~	V_{DD} − 0.5	V_{p-p}
HFC_{IN} (MFC)	V_{MFC}	—	MFC mode f_{IN} = 5~20MHz	0.3	~	V_{DD} − 0.5	V_{p-p}
HFC_{IN} (HFC)	V_{HFC}	—	HFC mode f_{IN} = 5~60MHz	0.3	~	V_{DD} − 0.5	V_{p-p}

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = −40~85°C, V_{DD} = 5V)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
(OT-1~OT-4)								
Output Current	"H" Level	$I_{OH\ 1}$	—	V_{OH} = 4.0V	−2.0	−4.0	—	mA
	"L" Level	$I_{OL\ 1}$	—	V_{OL} = 1.0V	2.0	4.0	—	
(DATA, CLOCK, PERIOD, I/O-5~I/O-9)								
Input Voltage	"H" Level	V_{IH}	—	—	V_{DD} ×0.7	~	V_{DD}	V
	"L" Level	V_{IL}	—	—	0	~	V_{DD} ×0.3	
Input Current	"H" Level	I_{IH}	—	V_{IH} = 5V	—	—	2.0	μA
	"L" Level	I_{IL}	—	V_{IL} = 0V	—	—	−2.0	
Output Current	"H" Level	$I_{OH\ 4}$	—	V_{OH} = 4.0V, Except CLOCK, PERIOD	−2.0	−4.0	—	mA
	"L" Level	$I_{OL\ 4}$	—	V_{OL} = 1.0V, Except CLOCK, PERIOD	2.0	4.0	—	
(DO1, DO2)								
Output Current	"H" Level	$I_{OH\ 3}$	—	V_{OH} = 4.0V	−2.0	−4.0	—	mA
	"L" Level	$I_{OL\ 3}$	—	V_{OL} = 1.0V	2.0	4.0	—	
DO Tri-State Leakage Current		I_{TL}	—	V_{TLH} = 5V, V_{TLL} = 0V	—	—	±1	μA
($\overline{XT}$)								
Output Current	"H" Level	$I_{OH\ 2}$	—	V_{OH} = 4.0V	−0.1	−0.3	—	mA
	"L" Level	$I_{OL\ 2}$	—	V_{OL} = 1.0V	0.1	0.3	—	

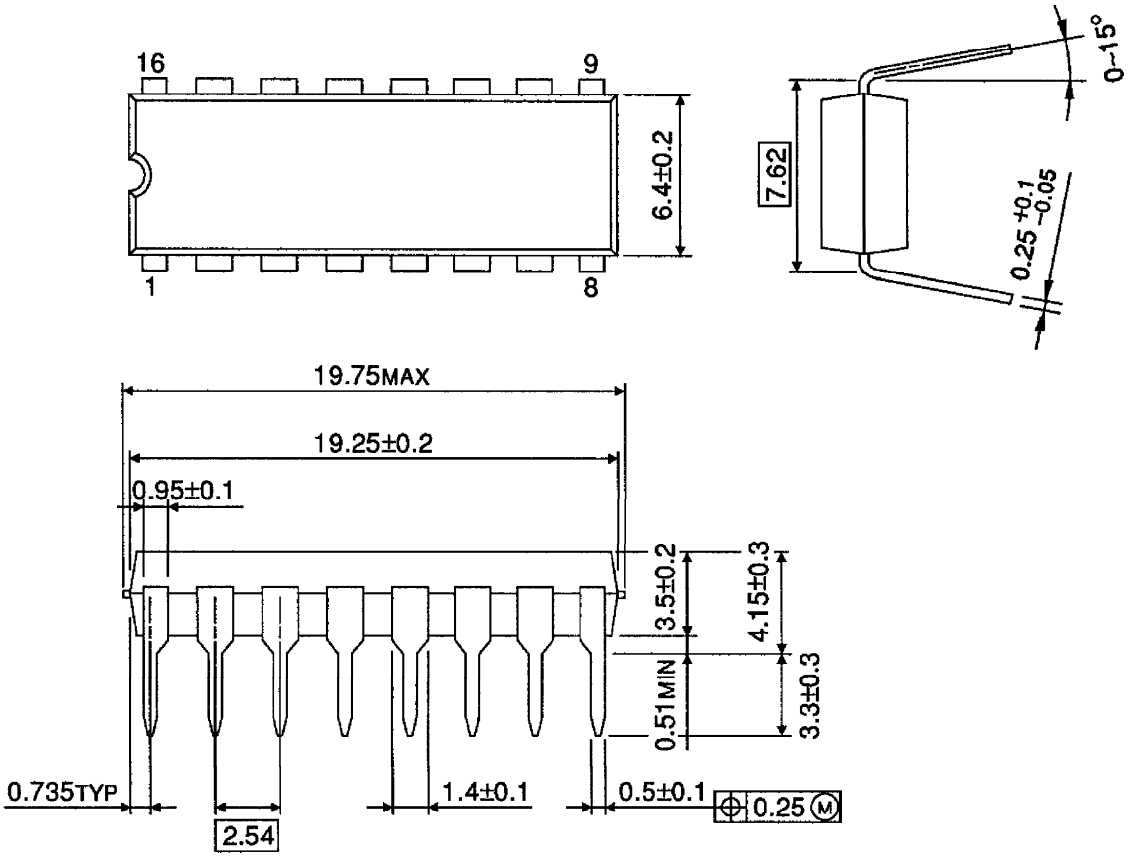
(Input feedback resistance) * Note : Ta = 25°C

Input Feedback Resistance	R_{f1}	—	FM_{IN}, AM_{IN}, LFC_{IN}, HFC_{IN}, SC_{IN}	250	500	1000	Ω
	R_{f2}	—	XT-$\overline{XT}$	250	500	1250	

OUTLINE DRAWING

DIP16-P-300-2.54A

Unit : mm

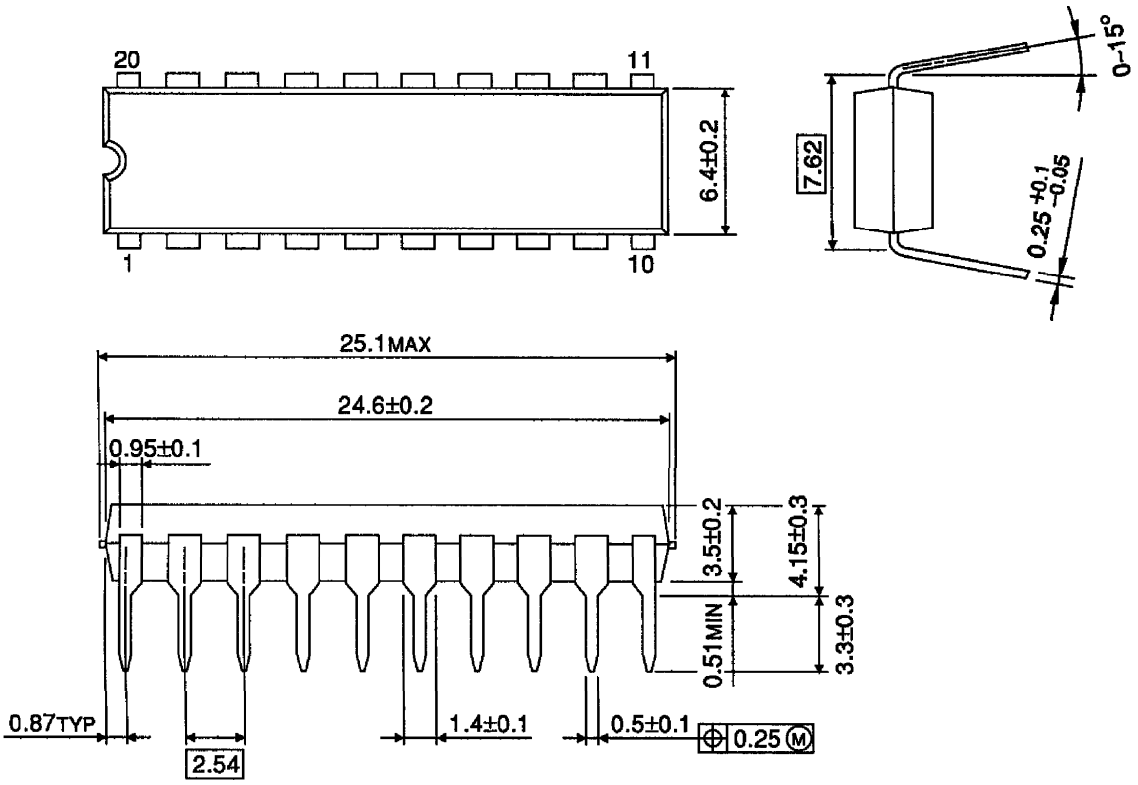


Weight : 1.0g (Typ.)

OUTLINE DRAWING

DIP20-P-300-2.54A

Unit : mm

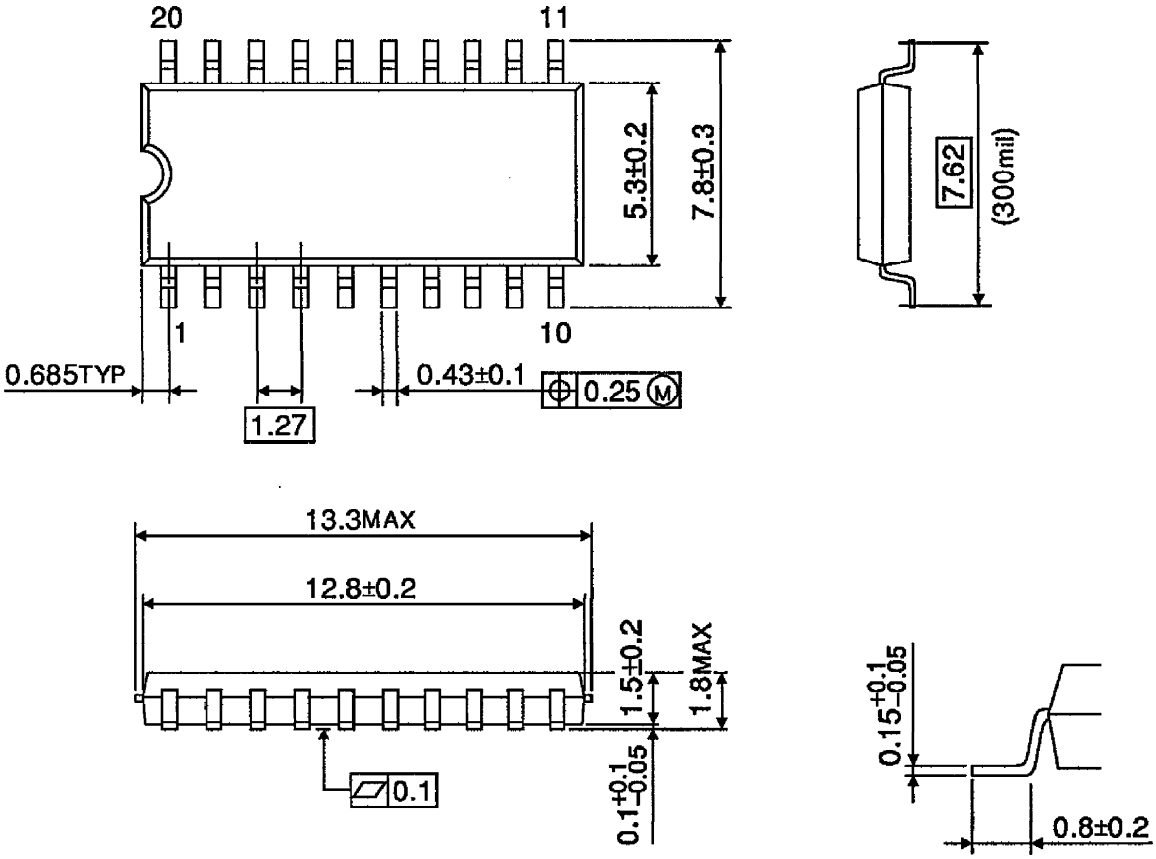


Weight : 1.4g (Typ.)

OUTLINE DRAWING

SOP20-P-300-1.27

Unit : mm



Weight : 0.48g (Typ.)