Networking Clock Generator

Features

- 3.3V ±10% Supply Voltage
- Uses 25MHz Crystal or 25MHz reference input
- One 200MHz selectable HCSL output with spread – default is spread off
- Two 25MHz LVCMOS outputs
- One 32.256MHz LVCMOS output
- Industrial temperature -40°C to 85°C
- Package: 28pin TSSOP (L)

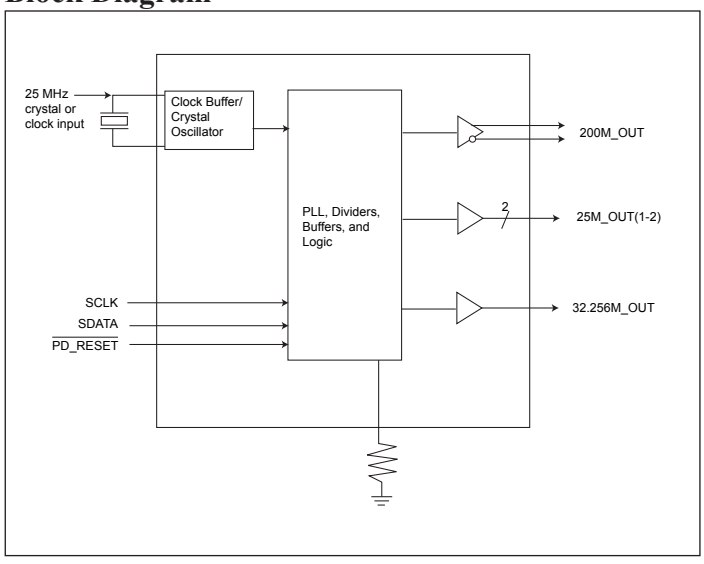
Applications

- Networking systems
- Embedded systems

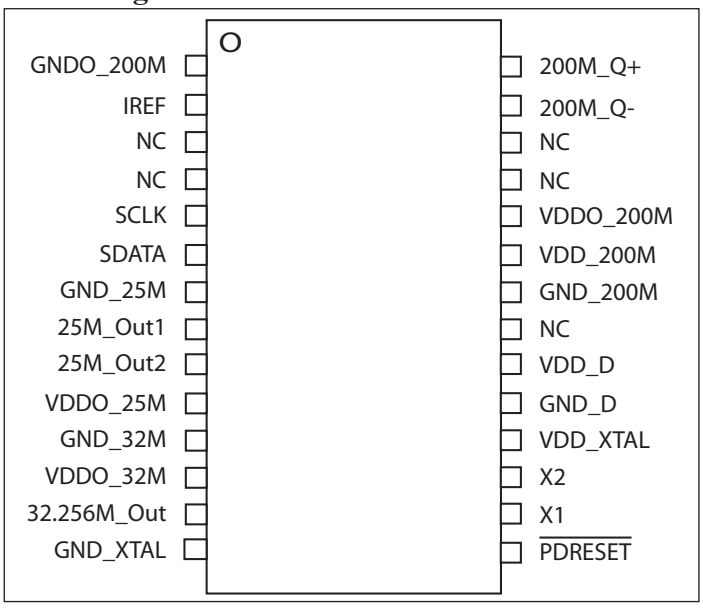
Description

The PI6C49014 is a high performance networking clock generator which generates 200MHz HCSL clock signal along with two LVCMOS 25MHz and 32.256MHz clocks from either 25MHz crystal or reference input. This integrated solution is ideal for Networking and Embedded systems that require multiple frequencies yet small foot print.

Block Diagram



Pin Configuration



Pin Description

Pin #	Pin Name	Pin Type	Pin Description
1	GNDO_200M	Power	Ground for 200MHz output
2	IREF	Output	Connect 475-Ohm resistor to set HCSL output drive current
3	NC	-	No Connect, leave open
4	NC	-	No Connect, leave open
5	SCLK	Input	SMBus compatible input clock. Supports fast mode 400 kHz input clock
6	SDATA	I/O	SMBus compatible data line
7	GND_25M	Power	Ground for 25MHz output
8	25M_Out1	Output	25MHz LVCMOS output. When disabled, output is trisated and has a normal 110kOhm pull-down
9	25M_Out2	Output	25MHz LVCMOS output. When disabled, output is trisated and has a normal 110kOhm pull-down
10	VDDO_25M	Power	3.3V supply for 25MHz output
11	GND_32M	Power	Ground for 32M output and related PLL
12	VDDO_32M	Power	3.3V supply for 32M output and related PLL
13	32.256M_Out	Output	32.256MHz LVCMOS output. When disabled, output is trisated and has a normal 110kOhm pull-down
14	GND_XTAL	Power	Ground for XTAL
15	$\overline{\text{PD\_RESET}}$	Input	Power on reset, when low all PLLs are powered down and output trisated. SMBus registers are reset to default values
16	X1	Input	Crystal input. Integrated 6pf capacitance
17	X2	Output	Crystal output. Integrated 6pf capacitance
18	VDD_XTAL	Power	3.3V supply for XTAL
19	GND_D	Power	Ground for all input and feedback divider of PLL
20	VDD_D	Power	3.3V supply for all input and feedback divider of PLL
21	NC	-	No Connect, leave open
22	GND_200M	Power	Ground for 200MHz related PLL and I2C interface
23	VDD_200M	Power	3.3V supply for 200MHz related PLL and I2C interface
24	VDDO_200M	Power	3.3V supply for 200MHz output buffer
25	NC	-	No Connect, leave open
26	NC	-	No Connect, leave open
27	200M_Q-	Output	200MHz HCSL output
28	200M_Q+	Output	200MHz HCSL output

Serial Data Interface (SMBus)

PI6C49014 is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	0/1

How to Write

1 bit	8 bits	1	8 bits	1	8 bits	1	8 bits	1		8 bits	1	1 bit
Start bit	d2H	Ack	Register offset	Ack	Byte Count = N	Ack	Data Byte 0	Ack	…	Data Byte N - 1	Ack	Stop bit

Note:

1. Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

How to Read (M: abbreviation for Master or Controller; S: abbreviation for slave/clock)

1 bit	8 bits	1 bit	8 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit	…	8 bits	1 bit	1 bit
M: Start bit	M: Send "D2h"	S: sends Ack	M: send starting data-byte location: N	S: sends Ack	M: Start bit	M: Send "D3h"	S: sends Ack	S: sends # of data bytes that will be sent: X	M: sends Ack	S: sends starting data byte N	M: sends Ack	…	S: sends data byte N+X-1	M: Not Acknowledge	M: Stop bit

Byte 0: Spread Spectrum Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Spread Spectrum Selection for 200 MHz HCSL PCI-Express clocks	RW	0	200MHz HCSL PCI Express output	0=spread off 1 = -0.5% down spread
6	Enables hardware or software control of OE bits (see Byte 0–Bit 6 and Bit 5 Functionality table)	RW	0	$\overline{\text{PD\_RESET}}$ pin, bit 5	0 = hardware cntl 1 = software ctrl
5	Software $\overline{\text{PD\_RESET}}$ bit. Enables or disables all outputs (see Byte 0–Bit 6 and Bit 5 Functionality table)	RW	1	All outputs	0 = disabled 1 = enabled
4 to 1	Reserved	RW	Undefined	Not Applicable	
0	OE for single-ended 25MHz output 25M_Out2	RW	1	Single-ended 25MHz output 25M_Out2	0 = disabled 1 = enabled

Byte 0 - Bit 6 and Bit 5 Functionality

Bit 6	Bit 5	Description
0	X	$\overline{\text{PD\_RESET}}$ HW pin/signal = enabled
1	0	Disables all outputs and tri-states the outputs, $\overline{\text{PD\_RESET}}$ HW pin/signal = DO NOT CARE
1	1	Enable all outputs, $\overline{\text{PD\_RESET}}$ HW pin/signal = DON'T CARE

Byte 1: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	OE for 32.256M_Out1	RW	1	32.256M_Out	0 = disabled 1 = enabled
6	OE for 25M_Out1	RW	1	25M_Out1	0 = disabled 1 = enabled
5 to 0	Reserved	RW	Undefined	Not Applicable	

Byte 2: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 5	Reserved	RW	Undefined	Not Applicable	
4 to 0	Reserved	R	Undefined	Not Applicable	

Byte 3: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 3	Reserved	RW	Undefined	Not Applicable	
2	OE for 200M HCSL Output	RW	1	200M	0 = disabled 1 = enabled
1 to 0	Reserved	RW	Undefined	Not Applicable	

Byte 4: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved	R	Undefined	Not Applicable	

Byte 5: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Revision ID bit 3	R	0	Not Applicable	
6	Revision ID bit 2	R	0	Not Applicable	
5	Revision ID bit 1	R	0	Not Applicable	
4	Revision ID bit 0	R	0	Not Applicable	
3	Vendor ID bit 3	R	0	Not Applicable	
2	Vendor ID bit 2	R	0	Not Applicable	
1	Vendor ID bit 1	R	1	Not Applicable	
0	Vendor ID bit 0	R	1	Not Applicable	

Byte 6: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved	R	Undefined	Not Applicable	

Maximum Ratings (Above which useful life may be impaired. For user guidelines, not tested.)

Symbol	Parameters	Test Condition	Min.	Max.	Units
V_{DD}	3.3V I/O Supply Voltage		3.0	3.6	V
I_{DD}	Total Power Supply Current	All outputs unloaded	-	64	mA
$I_{DD\_Output\ tri-stated}$	Total power supply current with Outputs are tri-stated	OE is "0", no load	-	54	mA
Idd power down	Total power supply current in power down mode	$\overline{PD\_RESET}$= "0", no load		4	mA
T_A	Operating temperature	-	-40	+85	ºC

Note:
1. Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Absolute Maximum Ratings[1] (Over operating free-air temperature range)

STORAGE TEMPERATURE……..- 65°C TO +155°C
AMBIENT TEMPERATURE WITH POWER APPLIED……-40°C TO +85°C
3.3V ANALOG SUPPLY VOLTAGE ……...- 0.5 TO +4.6V
ESD PROTECTION(HBM)…….. …… 2000V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

LVCMOS DC Electrical Characteristics

Unless otherwise specified, V_{DD}=3.3V±10%, Ambient Temperature –40°C to +85°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Supply Voltage		3.0		3.6	V
V_{IH}	Input High Voltage	-	2	-	VDD+0.3	
V_{IL}	Input Low Voltage	-	-0.3	-	0.8	
V_{IH}	Input High Voltage	SDATA, SCLK	$0.7V_{DD}$		V_{DD}	
V_{IL}	Input Low Voltage	SDATA, SCLK			$0.3V_{DD}$	
V_{OH}	Output High Voltage	I_{OH} = -8mA	V_{DD}-0.4	-	-	
V_{OL}	Output Low Voltage	I_{OL} = 8mA	-	-	0.4	
I_{IH}	Input High Current	$V_{IN} = V_{DD}$-0.1V	-	-	45	µA
I_{IL}	Input Low Current	V_{IN} = 0V	-45	-	-	
R_{PU}	Internal pull up resistance	$\overline{PD\_RESET}$	-	216	-	kOhm
R_{DN}	Internal pull down resistance	25M_Out1, 25M_Out2, 32.256M_Out	-	110	-	
C_{IN}	Input Capacitance	All input pins		6		pF

LVCMOS AC Electrical Characteristics

Unless otherwise specified, V_{DD}=3.3V±10%, Ambient Temperature –40°C to +85°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{in}	Input Frequency			25		MHz
F_{OUT}	Output Frequency	CLOAD = 15pF, 25MHz		25		MHz
$F_{OUT}E$	Output Frequency Error	Xtal Frequency = 25MHz, C_L = 18pF, +/-20ppm, output = 25MHz	-20	0	20	PPM
F_{OUT}	Output Frequency	CLOAD = 15pF, 32.256MHz		32.256		MHz
$F_{OUT}E$	Output Frequency Error	Xtal Frequency = 25MHz, C_L = 18pF, +/-20ppm, Output = 32.256MHz	-20	0	20	PPM
F_{SC}	SCLK Frequency			100	400	kHz
	Min. pulse width of $\overline{\text{PD\_RESET}}$ Input		100			ns
T_r /T_f	Output Rise/Fall time	20% of V_{DD} to 80% of V_{DD}		-	1.2	ns
T_{DC}	Output Duty Cycle	-	45	-	55	%
T_{Cj}	Cycle –to- cycle Jitter	32.256MHz	-	-	150	ps
T_{Pj}	Period Jitter	25 MHz clock output	-	-	40	
T_S	Clock Stabilization Time from Power up		3		10	ms

HCSL DC Electrical Characteristics

Unless otherwise specified, V_{DD}=3.3V±10%, Ambient Temperature –40°C to +85°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output High Voltage	-	660	-	950	mV
V_{OL}	Output Low Voltage	-	-	-	150	mV
V_{CROSS}	Absolute Crossing Point Voltages	-	250	-	550	
ΔV_{CROSS}	Total variation of VCROSS overall edges	-	-	-	140	mV
I_{OH}	Output High Current	With 475-Ohm resistor connected between IREF pin and GND	-	14	-	mA

HCSL AC Electrical Characteristics

Unless otherwise specified, V_{DD}=3.3V±10%, Ambient Temperature –40°C to +85°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{OUT}	Output Frequency	HCSL termination		200	200	MHz
$F_{OUT}E$	Output Frequency Error	Xtal Frequency = 25MHz, C_L = 18pF, +/-20ppm, output = 200 MHz, 0% Spread.	-20	0	20	PPM
T_r /T_f	Output Rise/Fall time	Between 0.175V and 0.525V *2	175	-	700	ps
ΔT_r /ΔT_f	Rise and Fall Time Variation*2	-	-	-	125	
T_{DC}	Output Duty Cycle*3	-	47	-	53	%
T_{Cj}	Cycle to cycle jitter *3	Differential waveform			70	ps
	Spread Modulation Percentage			-0.5	0	%
	Spread Modulation Frequency			32		kHz

Notes:

*1. Test configuration is Rs=33Ω, Rp=49.9Ω, and 2pF

*2. Measurement is taken from Single Ended waveform.

*3. Measurement is taken from Differential waveform.

*4. Measured from -150 mV to +150 mV on the differential waveform. The signal is monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.

HCSL output buffer characteristics

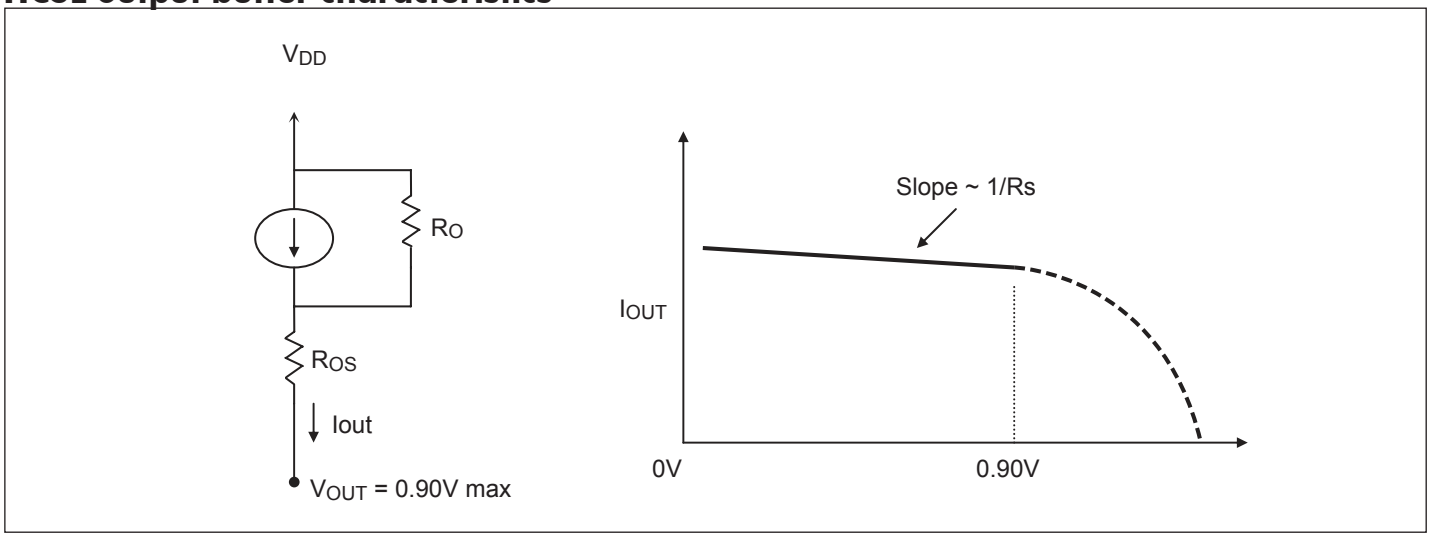


Figure 9. Simplified diagram of current-mode output buffer

HCSL Buffer characteristics

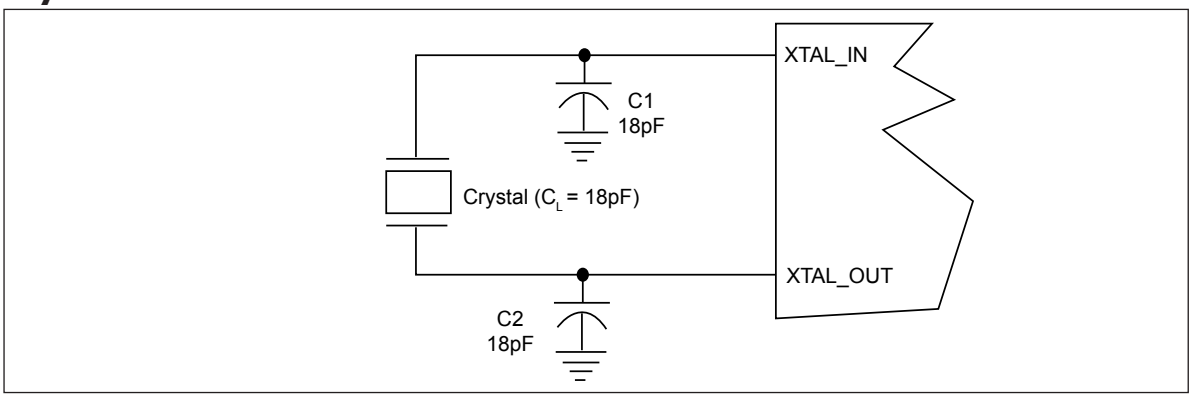
Symbol	Minimum	Maximum
R_O	3000Ω	N/A
R_{OS}	unspecified	unspecified
V_{OUT}	N/A	950mV

Application Notes

Crystal circuit connection

The following diagram shows PI6C49014 crystal circuit connection with a parallel crystal. For the CL=18pF crystal, it is suggested to use C1= 18pF, C2= 18pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.

Crystal Oscillator Circuit



Recommended Crystal Specification

Pericom recommends:

a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf

b) FY2500081, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

c) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm, http://www.pericom.com/pdf/datasheets/se/FL.pdf

Configuration test load board termination for HCSL Outputs

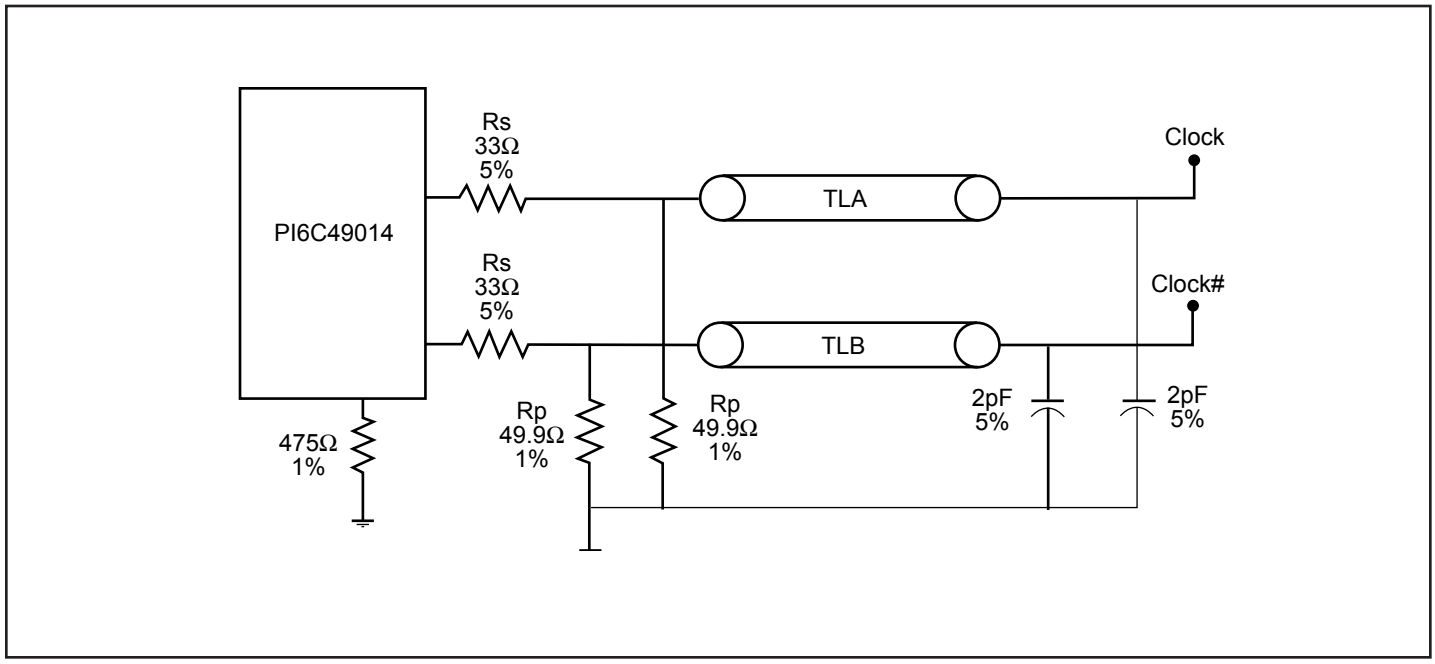


Figure 4. Configuration Test Load Board Termination

Configuration test load board termination for LVCMOS Outputs

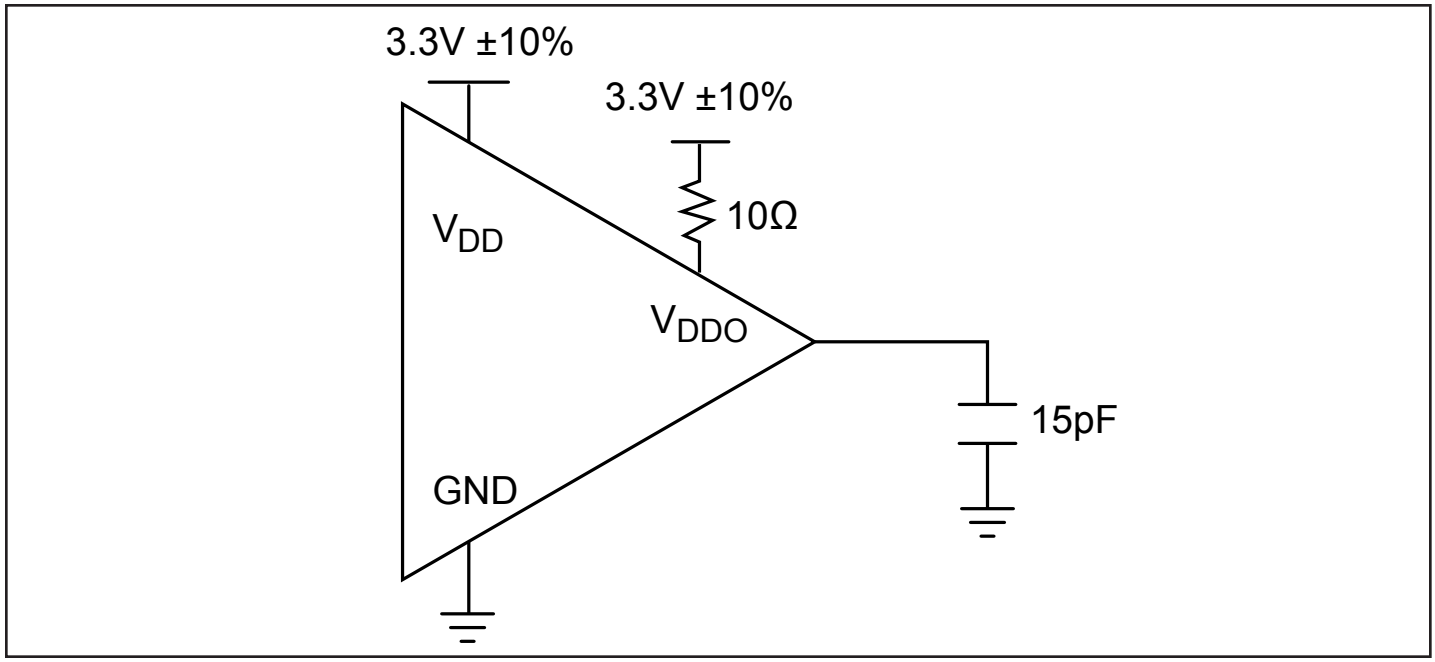
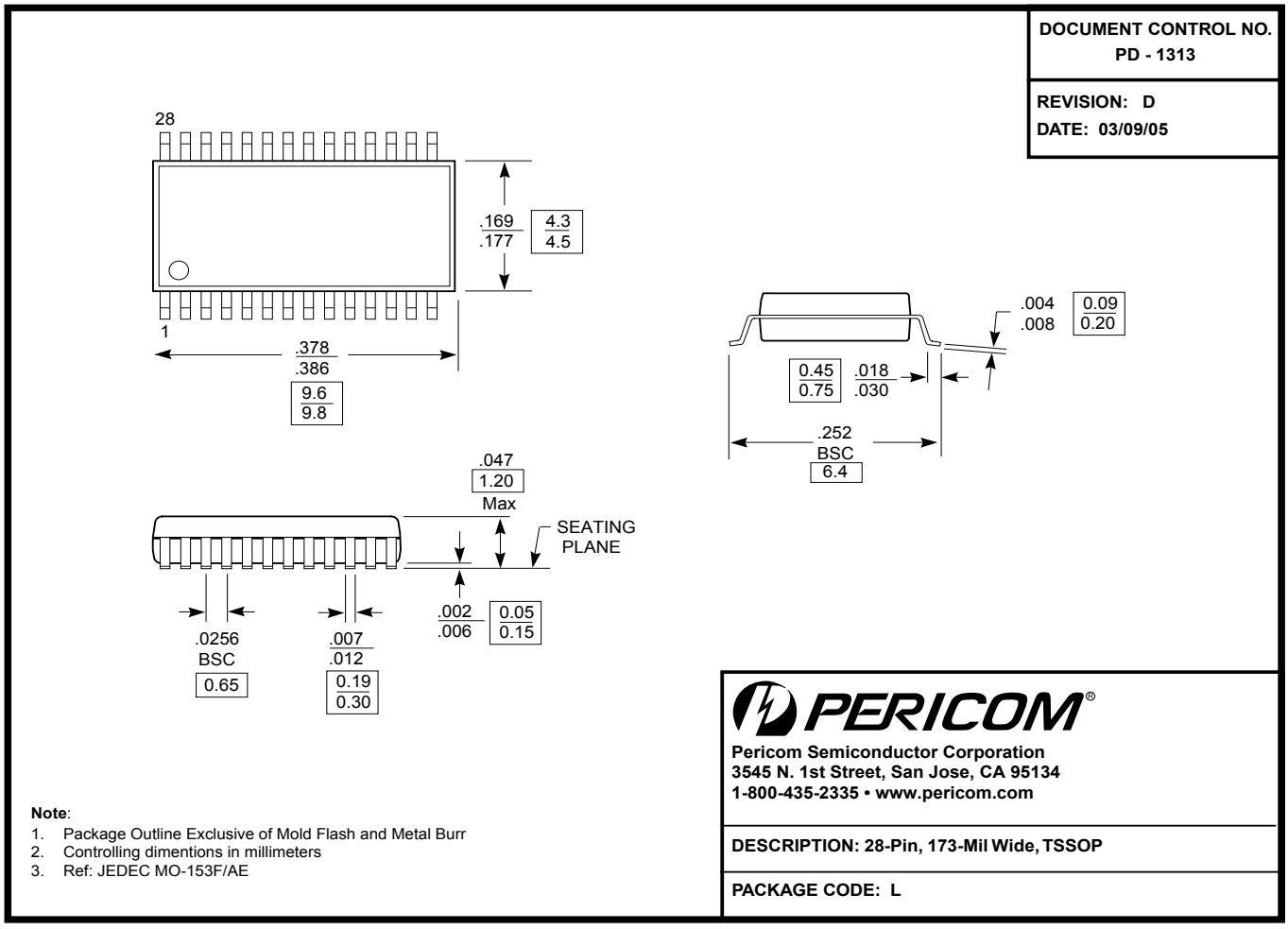


Figure 5. LVCMOS Test Load Board Termination

Packaging Mechanical: 28-Contact TSSOP (L)



Ordering Information(1-3)

Ordering Code	Package Code	Package Description
PI6C49014LIE	L	28pin TSSOP

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel