CY7C342
CY7C342B

128-Macrocell MAX® EPLD

Features

- **128 macrocells in 8 LABs**
- **8 dedicated inputs, 52 bidirectional I/O pins**
- **Programmable interconnect array**
- **0.8-micron double-metal CMOS EPROM technology (CY7C342)**
- **Advanced 0.65-micron CMOS technology to increase performance (CY7C342B)**
- **Available in 68-pin HLCC, PLCC, and PGA**

Functional Description

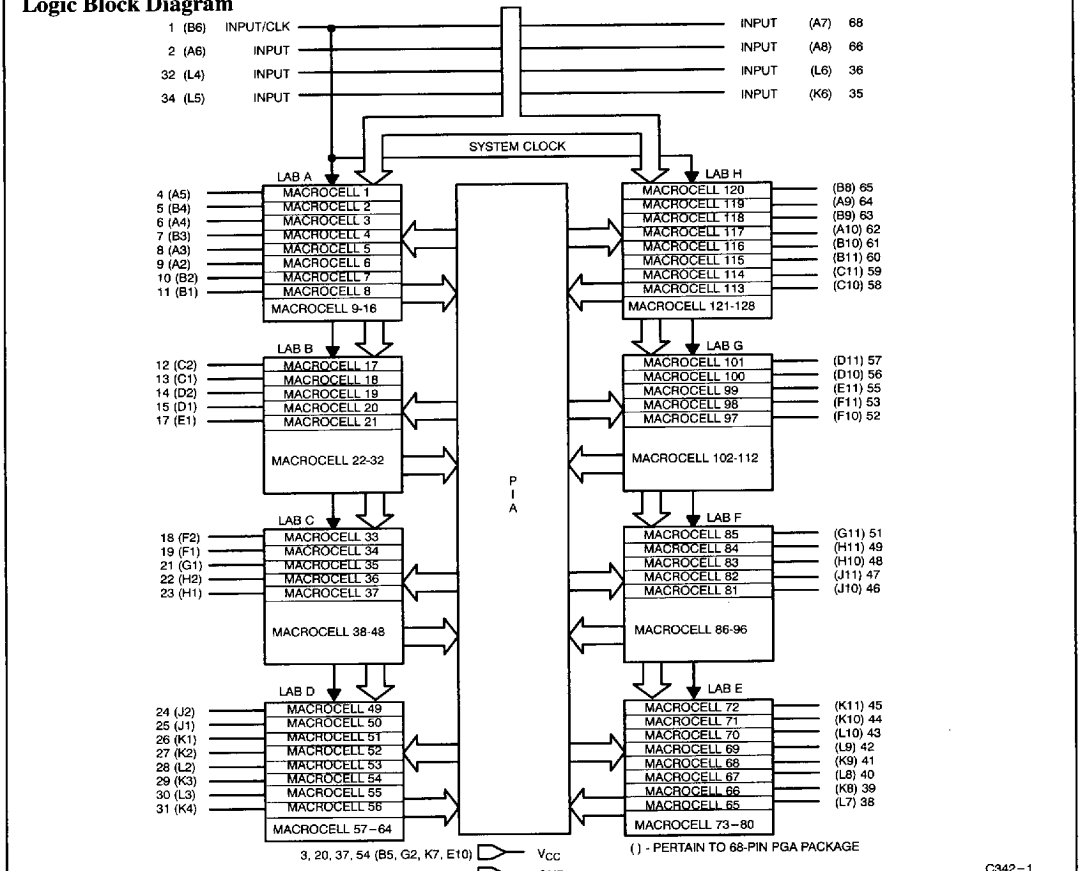
The CY7C342/CY7C342B is an Erasable Programmable Logic Device (EPLD) in which CMOS EPROM cells are used to configure logic functions within the device. The MAX architecture is 100% user configurable, allowing the devices to accommodate a variety of independent logic functions.

The 128 macrocells in the CY7C342/CY7C342B are divided into 8 Logic Array Blocks (LABs), 16 per LAB. There are 256 expander product terms, 32 per LAB, to be used and shared by the macrocells within each LAB.

Each LAB is interconnected with a programmable interconnect array, allowing all signals to be routed throughout the chip.

The speed and density of the CY7C342/CY7C342B allows it to be used in a wide range of applications, from replacement of large amounts of 7400-series TTL logic, to complex controllers and multifunction chips. With greater than 25 times the functionality of 20-pin PLDs, the CY7C342/CY7C342B allows the replacement of over 50 TTL devices. By replacing large amounts of logic, the CY7C342/CY7C342B reduces board space, part count, and increases system reliability.

Logic Block Diagram



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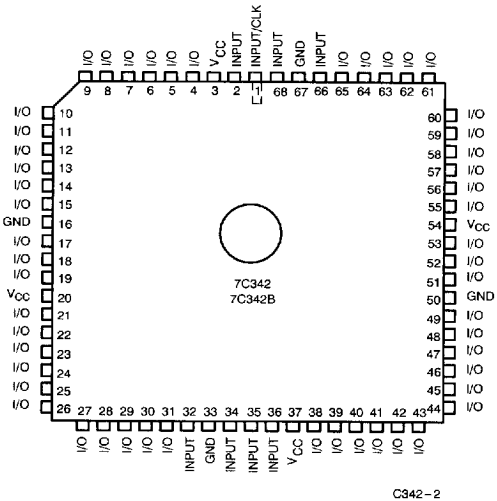
Selection Guide

		7C342B–12	7C342B–15	7C342B–20	7C342–25 7C342B–25	7C342–30 7C342B–30	7C342–35 7C342B–35
Maximum Access Time (ns)		12	15	20	25	30	35
Maximum Operating Current (mA)	Commercial	250	250	250	250	250	250
	Military		320	320	320	320	320
	Industrial		320	320	320	320	320
Maximum Static Current (mA)	Commercial	225	225	225	225	225	225
	Military		275	275	275	275	275
	Industrial		275	275	275	275	275

Shaded area contains preliminary information.

Pin Configurations

PLCC
Top View



C342–2

PGA
Bottom View

	1	2	3	4	5	6	7	8	9	10	11
L		I/O	I/O	INPUT	INPUT	INPUT	I/O	I/O	I/O	I/O	
K	I/O	I/O	I/O	I/O	GND	INPUT	VCC	I/O	I/O	I/O	I/O
J	I/O	I/O								I/O	I/O
H	I/O	I/O								I/O	I/O
G	I/O	VCC								GND	I/O
F	I/O	I/O				7C342 7C342B				I/O	I/O
E	I/O	GND								VCC	I/O
D	I/O	I/O								I/O	I/O
C	I/O	I/O								I/O	I/O
B	I/O	I/O	I/O	I/O	VCC	INPUT/ CLK	GND	I/O	I/O	I/O	I/O
A	■	I/O	I/O	I/O	I/O	INPUT	INPUT	INPUT	I/O	I/O	

C342–3

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Maximum Junction Temperature (under bias) ..... 150°C

Supply Voltage to Ground Potential ..... −3.0V to +7.0V

Maximum Power Dissipation ..... 2500 mW

DC V_{CC} or GND Current ..... 500 mA

DC Output Current per Pin ..... −25 mA to +25 mA

DC Input Voltage[1] ..... −3.0V to + 7.0V

DC Program Voltage 13.0V

Static Discharge Voltage ..... > 1100V (per MIL−STD−883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C (Case)	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} +0.3	V
V_{IL}	Input LOW Voltage			−0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	µA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or GND		−40	+40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3, 4]		−30	−90	mA
I_{CC1}	Power Supply Current (Static)	V_I = GND (No Load)	Com'l		225	mA
			Mil/Ind		275	
I_{CC2}	Power Supply Current[5]	V_I = V_{CC} or GND (No Load) f = 1.0 MHz[4]	Com'l		250	mA
			Mil/Ind		320	
t_R	Recommended Input Rise Time				100	ns
t_F	Recommended Input Fall Time				100	ns

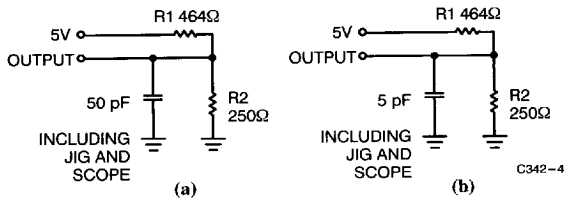
Capacitance[6]

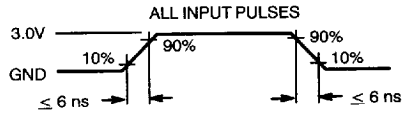
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2V, f = 1.0 MHz	10	pF

Notes:

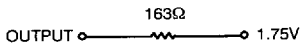
1. Minimum DC input is − 0.3V. During transitions, the inputs may undershoot to − 3.0V for periods less than 20 ns.
2. Typical values are for T_A = 25°C and V_{CC} = 5V.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Guaranteed but not 100% tested.
5. This parameter is measured with device programmed as a 16-bit counter in each LAB.
6. Part (a) in AC Test Load and Waveforms is used for all parameters except t_{ER} and t_{XZ}, which is used for part (b) in AC Test Load and Waveforms. All external timing parameters are measured referenced to external pins of the device.

AC Test Loads and Waveforms[5]





Equivalent to: THÉVENIN EQUIVALENT (commercial/military)



Logic Array Blocks

There are 8 logic array blocks in the CY7C342/CY7C342B. Each LAB consists of a macrocell array containing 16 macrocells, an expander product term array containing 32 expanders, and an I/O block. The LAB is fed by the programmable interconnect array and the dedicated input bus. All macrocell feedbacks go to the macrocell array, the expander array, and the programmable interconnect array. Expanders feed themselves and the macrocell array. All I/O feedbacks go to the programmable interconnect array so that they may be accessed by macrocells in other LABs as well as the macrocells in the LAB in which they are situated.

Externally, the CY7C342/CY7C342B provides eight dedicated inputs, one of which may be used as a system clock. There are 52 I/O pins that may be individually configured for input, output, or bidirectional data flow.

Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skews among logic signals that may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by assuring that internal signal skews or races are avoided. The result is ease of design implementation, often in a signal pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

Timing Delays

Timing delays within the CY7C342/CY7C342B may be easily determined using *Warp2™*, *Warp3™*, or MAX+PLUS® software or by the model shown in *Figure 1*. The CY7C342/CY7C342B has fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information the *Warp3* or MAX+PLUS software provides a timing simulator.

Design Recommendations

Operation of the devices described herein with conditions above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability. The CY7C342/CY7C342B contains circuitry to protect device pins from high static voltages or electric fields, but normal precautions should be taken to avoid application of any voltage higher than the maximum rated voltages.

For proper operation, input and output pins must be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 μF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled to

3

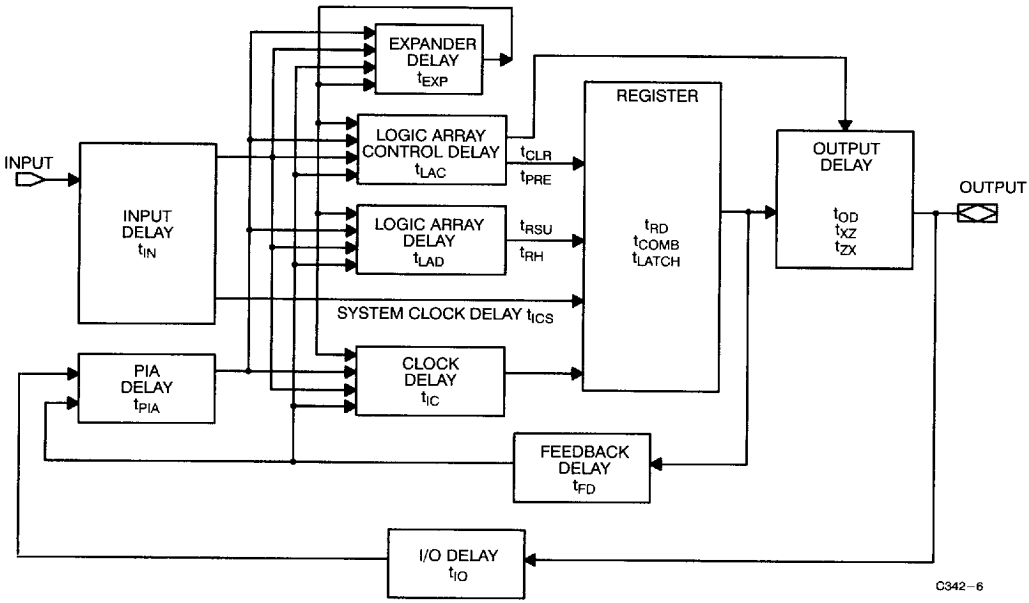


Figure 1. CY7C342/CY7C342B Internal Timing Model

GND directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types have.

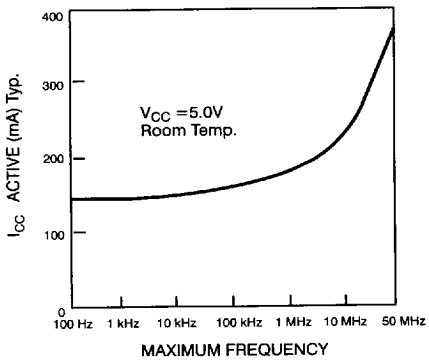
Design Security

The CY7C342/CY7C342B contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the entire device.

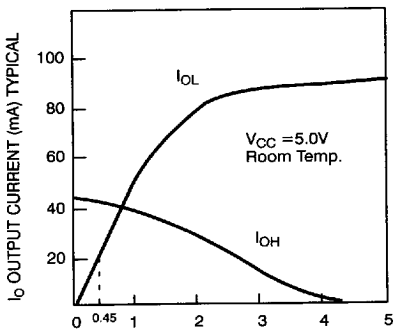
The CY7C342/CY7C342B is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

The erasable nature of these devices allows test programs to be used and erased during early stages of the production flow. The devices also contain on-board logic test circuitry to allow verification of function and AC specification once encapsulated in non-windowed packages.

Typical I_{CC} vs. f_{MAX}



Output Drive Current



Timing Considerations

Unless otherwise stated, propagation delays do not include expanders. When using expanders, add the maximum expander delay t_{EXP} to the overall delay. Similarly, there is an additional t_{PIA} delay for an input from an I/O pin when compared to a signal from straight input pin.

When calculating synchronous frequencies, use t_{S1} if all inputs are on dedicated input pins. The parameter t_{S2} should be used if data is applied at an I/O pin. If t_{S2} is greater than t_{CO1}, $1/t_{S2}$ becomes the limiting frequency in the data path mode unless $1/(t_{WH} + t_{WL})$ is less than $1/t_{S2}$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{S1}. Determine which of $1/(t_{WH} + t_{WL})$, $1/t_{CO1}$, or $1/(t_{EXP} + t_{S1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the synchronous configuration.

When calculating external asynchronous frequencies, use t_{AS1} if all inputs are on the dedicated input pins. If any data is applied to an I/O pin, t_{AS2} must be used as the required set-up time. If $(t_{AS2} + t_{AH})$ is greater than t_{ACO1}, $1/(t_{AS2} + t_{AH})$ becomes the limiting frequency in the data path mode unless $1/(t_{AWH} + t_{AWL})$ is less than $1/(t_{AS2} + t_{AH})$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{AS1}. Determine which of $1/(t_{AWH} + t_{AWL})$, $1/t_{ACO1}$, or $1/(t_{EXP} + t_{AS1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the asynchronous configuration.

The parameter t_{OH} indicates the system compatibility of this device when driving other synchronous logic with positive input hold times, which is controlled by the same synchronous clock. If t_{OH} is greater than the minimum required input hold time of the subsequent synchronous logic, then the devices are guaranteed to function properly with a common synchronous clock under worst-case environmental and supply voltage conditions.

The parameter t_{AOH} indicates the system compatibility of this device when driving subsequent registered logic with a positive hold time and using the same asynchronous clock as the CY7C342/CY7C342B.

In general, if t_{AOH} is greater than the minimum required input hold time of the subsequent logic (synchronous or asynchronous) then the devices are guaranteed to function properly under worst-case environmental and supply voltage conditions, provided the clock signal source is the same. This also applies if expander logic is used in the clock signal path of the driving device, but not for the driven device. This is due to the expander logic in the second device's clock signal path adding an additional delay (t_{EXP}) causing the output data from the preceding device to change prior to the arrival of the clock signal at the following device's register.

Commercial and Industrial External Synchronous Switching Characteristics[6] Over Operating Range

Parameter	Description	7C342B–12		7C342B–15		7C342B–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[7]		12		15		20	ns
t_{PD2}	I/O Input to Combinatorial Output Delay[8]		20		25		32	ns
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[9]		18		23		30	ns
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 10]		26		33		42	ns
t_{EA}	Input to Output Enable Delay[4, 7]		12		15		20	ns
t_{ER}	Input to Output Disable Delay[4, 7]		12		15		20	ns
t_{CO1}	Synchronous Clock Input to Output Delay		6		7		8	ns
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 11]		14		17		20	ns
t_{S1}	Dedicated Input or Feedback Set-Up Time to Synchronous Clock Input[7, 12]	8		10		13		ns
t_{S2}	I/O Input Set-Up Time to Synchronous Clock Input[7]	16		20		24		ns
t_H	Input Hold Time from Synchronous Clock Input[7]	0		0		0		ns
t_{WH}	Synchronous Clock Input HIGH Time	4.5		5		7		ns
t_{WL}	Synchronous Clock Input LOW Time	4.5		5		7		ns
t_{RW}	Asynchronous Clear Width[4, 7]	12		15		20		ns
t_{RR}	Asynchronous Clear Recovery Time[4, 7]	12		15		20		ns
t_{RO}	Asynchronous Clear to Registered Output Delay[7]		12		15		20	ns
t_{PW}	Asynchronous Preset Width[4, 7]	12		15		20		ns
t_{PR}	Asynchronous Preset Recovery Time[4, 7]	12		15		20		ns
t_{PO}	Asynchronous Preset to Registered Output Delay[7]		12		15		20	ns
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]		3		3		3	ns
t_P	External Synchronous Clock Period ($1/(f_{MAX3})$)[4]	9		12		15		ns
f_{MAX1}	External Feedback Maximum Frequency ($1/(t_{CO1} + t_{S1})$)[4, 14]	71.4		58.8		47.6		MHz
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of ($1/(t_{S1} + t_{CF})$) or ($1/t_{CO1}$)[4, 15]	90.9		76.9		62.5		MHz
f_{MAX3}	Data Path Maximum Frequency, lesser of ($1/(t_{WL} + t_{WH})$), ($1/(t_{S1} + t_H)$) or ($1/t_{CO1}$)[4, 16]	111.1		100		71.4		MHz
f_{MAX4}	Maximum Register Toggle Frequency ($1/(t_{WL}+t_{WH})$)[4, 17]	111.1		100		71.4		MHz
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	3		3		3		ns

Shaded area contains preliminary information.

Parameter	Description	7C342–25 7C342B–25		7C342–30 7C342B–30		7C342–35 7C342B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[7]		25		30		35	ns
t_{PD2}	I/O Input to Combinatorial Output Delay[8]		39		46		55	ns
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[9]		37		44		55	ns
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 10]		51		60		75	ns
t_{EA}	Input to Output Enable Delay[4, 7]		25		30		35	ns
t_{ER}	Input to Output Disable Delay[4, 7]		25		30		35	ns
t_{CO1}	Synchronous Clock Input to Output Delay		14		16		20	ns

Commercial and Industrial External Synchronous Switching Characteristics (continued)

Parameter	Description	7C342–25 7C342B–25		7C342–30 7C342B–30		7C342–35 7C342B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 11]		30		35		42	ns
t_{S1}	Dedicated Input or Feedback Set-Up Time to Synchronous Clock Input[7, 12]	15		20		25		ns
t_{S2}	I/O Input Set-Up Time to Synchronous Clock Input[7]	29		36		45		ns
t_H	Input Hold Time from Synchronous Clock Input[7]	0		0		0		ns
t_{WH}	Synchronous Clock Input HIGH Time	8		10		12.5		ns
t_{WL}	Synchronous Clock Input LOW Time	8		10		12.5		ns
t_{RW}	Asynchronous Clear Width[4, 7]	25		30		35		ns
t_{RR}	Asynchronous Clear Recovery Time[4, 7]	25		30		35		ns
t_{RO}	Asynchronous Clear to Registered Output Delay[7]		25		30		35	ns
t_{PW}	Asynchronous Preset Width[4, 7]	25		30		35		ns
t_{PR}	Asynchronous Preset Recovery Time[4, 7]	25		30		35		ns
t_{PO}	Asynchronous Preset to Registered Output Delay[7]		25		30		35	ns
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]		3		3		6	ns
t_P	External Synchronous Clock Period ($1/(f_{MAX3})$)[4]	16		20		25		ns
f_{MAX1}	External Feedback Maximum Frequency ($1/(t_{CO1} + t_{S1})$)[4, 14]	34.5		27.7		22.2		MHz
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of ($1/(t_{S1} + t_{CF})$) or ($1/t_{CO1}$)[4, 15]	55.5		43.4		32.2		MHz
f_{MAX3}	Data Path Maximum Frequency, lesser of ($1/(t_{WL} + t_{WH})$), ($1/(t_{S1} + t_H)$) or ($1/t_{CO1}$)[4, 16]	62.5		50		40		MHz
f_{MAX4}	Maximum Register Toggle Frequency ($1/(t_{WL}+t_{WH})$)[4, 17]	62.5		50		40		MHz
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	3		3		3		ns

Notes:

7. This specification is a measure of the delay from input signal applied to a dedicated input (68-pin PLCC input pin 1, 2, 32, 34, 35, 66, or 68) to combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.
   When this note is applied to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic.
   If an input signal is applied to an I/O pin an additional delay equal to t_{PIA} should be added to the comparable delay for a dedicated input. If expanders are used, add the maximum expander delay t_{EXP} to the overall delay for the comparable delay without expanders.
8. This specification is a measure of the delay from input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
9. This specification is a measure of the delay from an input signal applied to a dedicated input (68-pin PLCC input pin 1, 2, 32, 34, 35, 36, 66, or 68) to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic.
10. This specification is a measure of the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
11. This specification is a measure of the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used, register is synchronously clocked and all feedback is within the same LAB. This parameter is tested periodically by sampling production material.
12. If data is applied to an I/O input for capture by a macrocell register, the I/O pin input set-up time minimums should be observed. These parameters are t_{S2} for synchronous operation and t_{AS2} for asynchronous operation.
13. This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous clock to LAB logic array input. This delay plus the register set-up time, t_{S1}, is the minimum internal period for an internal synchronous state machine configuration. This delay is for feedback within the same LAB. This parameter is tested periodically by sampling production material.
14. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and feedback signals are applied to dedicated inputs. All feedback is assumed to be local originating within the same LAB.
15. This specification indicates the guaranteed maximum frequency at which a state machine with internal-only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{CO1}$.
16. This frequency indicates the maximum frequency at which the device may operate in data path mode (dedicated input pin to output pin). This assumes data input signals are applied to dedicated input pins and no expander logic is used. If any of the data inputs are I/O pins, t_{S2} is the appropriate t_S for calculation.
17. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycled by a clock signal applied to the dedicated clock input pin.
18. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

Commercial and Industrial External Asynchronous Switching Characteristics[6] Over Operating Range

Parameter	Description	7C342B–12		7C342B–15		7C342B–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO1}	Asynchronous Clock Input to Output Delay[7]		12		15		20	ns
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]		20		25		32	ns
t_{AS1}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input[7]	4		5		5		ns
t_{AS2}	I/O Input Set-Up Time to Asynchronous Clock Input[7]	12		14.5		17		ns
t_{AH}	Input Hold Time from Asynchronous Clock Input[7]	4		5		6		ns
t_{AWH}	Asynchronous Clock Input HIGH Time[7]	8		9		10		ns
t_{AWL}	Asynchronous Clock Input LOW Time[7, 20]	6		7		8		ns
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 21]		9		11		13	ns
t_{AP}	External Asynchronous Clock Period ($1/(f_{MAXA4})$)[4]	14		16		18		ns
f_{MAXA1}	External Feedback Maximum Frequency in Asynchronous Mode ($1/(t_{ACO1} + t_{AS1})$)[4, 22]	62.5		50		40		MHz
f_{MAXA2}	Maximum Internal Asynchronous Frequency[4, 23]	71.4		62.5		55.5		MHz
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[4, 24]	83.3		66.6		50		MHz
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[4, 25]	71.4		62.5		55.5		MHz
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 26]	12		12		12		ns

Shaded area contains preliminary information.

Notes:

19. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in the logic of combinatorial output or the asynchronous clock input. The clock signal is applied to the dedicated clock input pin and all feedback is within a single LAB. This parameter is tested periodically by sampling production material.
20. This parameter is measured with a positive-edge triggered clock at the register. For negative edge triggering, the t_{AWH} and t_{AWL} parameters must be swapped. If a given input is used to clock multiple registers with both positive and negative polarity, t_{AWH} should be used for both t_{AWH} and t_{AWL}.
21. This specification is a measure of the delay associated with the internal register feedback path for an asynchronous clock to LAB logic array input. This delay plus the asynchronous register set-up time, t_{AS1}, is the minimum internal period for an internal asynchronously clocked state machine configuration. This delay is for feedback within the same LAB, assumes no expander logic in the clock path, and assumes that the clock input signal is applied to a dedicated input pin. This parameter is tested periodically by sampling production material.
22. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs and that no expander logic is employed in the clock signal path or data path.
23. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal-only feedback can operate. This parameter is determined by the lesser of $(1/(t_{ACF} + t_{AS1}))$ or $(1/(t_{AWH} + t_{AWL}))$. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$.
    This specification assumes no expander logic is utilized, all data inputs and clock inputs are applied to dedicated inputs, and all state feedback is within a single LAB. This parameter is tested periodically by sampling production material.
24. This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the lesser of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS1} + t_{AH})$ or $1/t_{ACO1}$. It assumes data and clock input signals are applied to dedicated input pins and no expander logic is used.
25. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.
26. This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input applied to an external dedicated input pin.

Commercial and Industrial External Asynchronous Switching Characteristics[6] Over Operating Range (continued)

Parameter	Description	7C342–25 7C342B–25		7C342–30 7C342B–30		7C342–35 7C342B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO1}	Asynchronous Clock Input to Output Delay[7]		25		30		35	ns
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]		39		46		55	ns
t_{AS1}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input[7]	5		6		8		ns
t_{AS2}	I/O Input Set-Up Time to Asynchronous Clock Input[7]	19		22		28		ns
t_{AH}	Input Hold Time from Asynchronous Clock Input[7]	6		8		10		ns
t_{AWH}	Asynchronous Clock Input HIGH Time[7]	11		14		16		ns
t_{AWL}	Asynchronous Clock Input LOW Time[7, 20]	9		11		14		ns
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 21]		15		18		22	ns
t_{AP}	External Asynchronous Clock Period ($1/(f_{MAXA4})$)[4]	20		25		30		ns
f_{MAXA1}	External Feedback Maximum Frequency in Asynchronous Mode ($1/(t_{ACO1} + t_{AS1})$)[4, 22]	33.3		27.7		23.2		MHz
f_{MAXA2}	Maximum Internal Asynchronous Frequency[4, 23]	50		40		33.3		MHz
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[4, 24]	40		33.3		28.5		MHz
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[4, 25]	50		40		33.3		MHz
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 26]	15		15		15		ns

Commercial and Industrial Typical Internal Switching Characteristics Over Operating Range

Parameter	Description	7C342B–12		7C342B–15		7C342B–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay		2.5		3		4	ns
t_{IO}	I/O Input Pad and Buffer Delay		2.5		3		4	ns
t_{EXP}	Expander Array Delay		6		8		10	ns
t_{LAD}	Logic Array Data Delay		6		8		10	ns
t_{LAC}	Logic Array Control Delay		5		5		7	ns
t_{OD}	Output Buffer and Pad Delay		3		3		3	ns
t_{ZX}	Output Buffer Enable Delay[27]		5		5		5	ns
t_{XZ}	Output Buffer Disable Delay		5		5		5	ns
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	2		4		5		ns
t_{RH}	Register Hold Time Relative to Clock Signal at Register	4		4		5		ns
t_{LATCH}	Flow Through Latch Delay		1		1		2	ns
t_{RD}	Register Delay		0.5		1		1	ns
t_{COMB}	Transparent Mode Delay[28]		1		1		2	ns
t_{CH}	Clock HIGH Time	3		4		6		ns
t_{CL}	Clock LOW Time	3		4		6		ns
t_{IC}	Asynchronous Clock Logic Delay		5		6		8	ns
t_{ICS}	Synchronous Clock Delay		0.5		0.5		0.5	ns
t_{FD}	Feedback Delay		1		1		1	ns
t_{PRE}	Asynchronous Register Preset Time		3		3		3	ns
t_{CLR}	Asynchronous Register Clear Time		3		3		3	ns
t_{PCW}	Asynchronous Preset andClear Pulse Width	2		3		4		ns
t_{PCR}	Asynchronous Preset and Clear Recovery Time	2		3		4		ns
t_{PIA}	Programmable Interconnect Array Delay Time		8		10		12	ns

Shaded area contains preliminary information.

Commercial and Industrial Typical Internal Switching Characteristics Over Operating Range (continued)

Parameter	Description	7C342–25 7C342B–25		7C342–30 7C342B–30		7C342–35 7C342B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay		5		7		9	ns
t_{IO}	I/O Input Pad and Buffer Delay		6		6		9	ns
t_{EXP}	Expander Array Delay		12		14		20	ns
t_{LAD}	Logic Array Data Delay		12		14		16	ns
t_{LAC}	Logic Array Control Delay		10		12		13	ns
t_{OD}	Output Buffer and Pad Delay		5		5		6	ns
t_{ZX}	Output Buffer Enable Delay[27]		10		11		13	ns
t_{XZ}	Output Buffer Disable Delay		10		11		13	ns
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	6		8		10		ns
t_{RH}	Register Hold Time Relative to Clock Signal at Register	6		8		10		ns
t_{LATCH}	Flow Through Latch Delay		3		4		4	ns
t_{RD}	Register Delay		1		2		2	ns
t_{COMB}	Transparent Mode Delay[28]		3		4		4	ns
t_{CH}	Clock HIGH Time	8		10		12.5		ns
t_{CL}	Clock LOW Time	8		10		12.5		ns
t_{IC}	Asynchronous Clock Logic Delay		14		16		18	ns
t_{ICS}	Synchronous Clock Delay		2		2		3	ns
t_{FD}	Feedback Delay		1		1		2	ns
t_{PRE}	Asynchronous Register Preset Time		5		6		7	ns
t_{CLR}	Asynchronous Register Clear Time		5		6		7	ns
t_{PCW}	Asynchronous Preset and Clear Pulse Width	5		6		7		ns
t_{PCR}	Asynchronous Preset and Clear Recovery Time	5		6		7		ns
t_{PIA}	Programmable Interconnect Array Delay Time		14		16		20	ns

Notes:
27. Sample tested only for an output change of 500 mV.
28. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

Military External Synchronous Switching Characteristics[6] Over Operating Range

Parameter	Description	7C342B–15		7C342B–20		7C342B–25		7C342–30 7C342B–30		7C342–35 7C342B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[7]		15		20		25		30		35	ns
t_{PD2}	I/O Input to Combinatorial Output Delay[8]		25		32		39		46		55	ns
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[9]		23		30		37		44		55	ns
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 10]		33		42		51		60		75	ns
t_{EA}	Input to Output Enable Delay[4, 7]		15		20		25		30		35	ns
t_{ER}	Input to Output Disable Delay[4, 7]		15		20		25		30		35	ns
t_{CO1}	Synchronous Clock Input to Output Delay		7		8		14		16		20	ns
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 11]		17		20		30		35		42	ns
t_{S1}	Dedicated Input or Feedback Set-Up Time to Synchronous Clock Input[7, 12]	10		13		15		20		25		ns
t_{S2}	I/O Input Set-Up Time to Synchronous Clock Input[7]	20		24		29		36		45		ns
t_H	Input Hold Time from Synchronous Clock Input[7]	0		0		0		0		0		ns
t_{WH}	Synchronous Clock Input HIGH Time	5		7		8		10		12.5		ns
t_{WL}	Synchronous Clock Input LOW Time	5		7		8		10		12.5		ns
t_{RW}	Asynchronous Clear Width[4, 7]	15		20		25		30		35		ns
t_{RR}	Asynchronous Clear Recovery Time[4, 7]	15		20		25		30		35		ns
t_{RO}	Asynchronous Clear to Registered Output Delay[7]		15		20		25		30		35	ns
t_{PW}	Asynchronous Preset Width[4, 7]	15		20		25		30		35		ns
t_{PR}	Asynchronous Preset Recovery Time[4, 7]	15		20		25		30		35		ns
t_{PO}	Asynchronous Preset to Registered Output Delay[7]		15		20		25		30		35	ns
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]		3		3		3		3		6	ns
t_P	External Synchronous Clock Period ($1/(f_{MAX3})$)[4]	12		14		16		20		25		ns

Military External Synchronous Switching Characteristics[6] Over Operating Range (continued)

Parameter	Description	7C342B–15		7C342B–20		7C342B–25		7C342–30 7C342B–30		7C342–35 7C342B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX1}	External Feedback Maximum Frequency $(1/(t_{CO1} + t_{S1}))$[4, 14]	58.8		47.6		34.5		27.7		22.2		MHz
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of $(1/(t_{S1} + t_{CF}))$ or $(1/t_{CO1})$[4, 15]	76.9		62.5		55.5		43.4		32.2		MHz
f_{MAX3}	Data Path Maximum Frequency, lesser of $(1/(t_{WL} + t_{WH}))$, $(1/(t_{S1} + t_H))$ or $(1/t_{CO1})$[4, 16]	100		71.4		62.5		50		40		MHz
f_{MAX4}	Maximum Register Toggle Frequency $(1/(t_{WL} + t_{WH}))$[4, 17]	100		71.4		62.5		50		40		MHz
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	3		3		3		3		3		ns

Shaded area contains preliminary information.

Military External Asynchronous Switching Characteristics[6] Over Operating Range

Parameter	Description	7C342B–15		7C342B–20		7C342B–25		7C342–30 7C342B–30		7C342–35 7C342B–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO1}	Asynchronous Clock Input to Output Delay[7]		15		20		25		30		35	ns
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]		25		32		39		46		55	ns
t_{AS1}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input[7]	5		6		5		6		8		ns
t_{AS2}	I/O Input Set-Up Time to Asynchronous Clock Input[7]	14.5		17		19		22		28		ns
t_{AH}	Input Hold Time from Asynchronous Clock Input[7]	5		6		6		8		10		ns
t_{AWH}	Asynchronous Clock Input HIGH Time[7]	9		10		11		14		16		ns
t_{AWL}	Asynchronous Clock Input LOW Time[7, 20]	7		8		9		11		14		ns
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 21]		11		13		15		18		22	ns
t_{AP}	External Asynchronous Clock Period $(1/(f_{MAXA4}))$[4]	16		18		20		25		30		ns
f_{MAXA1}	External Feedback Maximum Frequency in Asynchronous Mode $(1/(t_{ACO1} + t_{AS1}))$[4, 22]	50.0		40		33.3		27.7		23.2		MHz
f_{MAXA2}	Maximum Internal Asynchronous Frequency[4, 23]	62.5		55.5		50		40		33.3		MHz
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[4, 24]	66.6		50		40		33.3		28.5		MHz
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[4, 25]	62.5		55.5		50		40		33.3		MHz
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 26]	12		12		15		15		15		ns

Shaded area contains preliminary information.

3

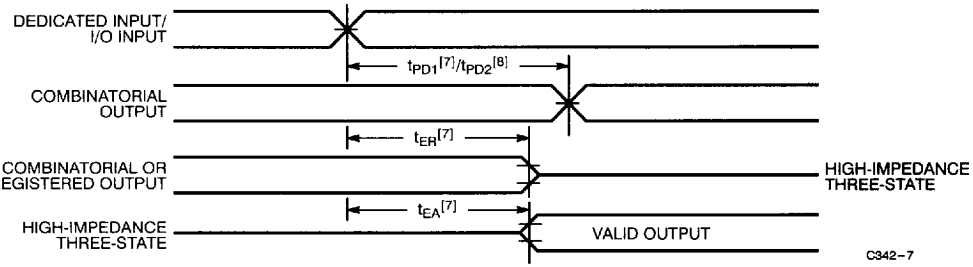
Military Typical Internal Switching Characteristics Over Operating Range

Parameter	Description	7C342B–15		7C342B–20		7C342B–25		7C342–30		7C342–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay		3		4		5		7		9	ns
t_{IO}	I/O Input Pad and Buffer Delay		3		4		6		6		9	ns
t_{EXP}	Expander Array Delay		8		10		12		14		20	ns
t_{LAD}	Logic Array Data Delay		8		10		12		14		16	ns
t_{LAC}	Logic Array Control Delay		5		7		10		12		13	ns
t_{OD}	Output Buffer and Pad Delay		3		3		5		5		6	ns
t_{ZX}	Output Buffer Enable Delay[27]		5		5		10		11		13	ns
t_{XZ}	Output Buffer Disable Delay		5		5		10		11		13	ns
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	4		5		6		8		10		ns
t_{RH}	Register Hold Time Relative to Clock Signal at Register	4		5		6		8		10		ns
t_{LATCH}	Flow Through Latch Delay		1		2		3		4		4	ns
t_{RD}	Register Delay		1		1		1		2		2	ns
t_{COMB}	Transparent Mode Delay[28]		1		2		3		4		4	ns
t_{CH}	Clock HIGH Time	4		6		8		10		12.5		ns
t_{CL}	Clock LOW Time	4		6		8		10		12.5		ns
t_{IC}	Asynchronous Clock Logic Delay		6		8		14		16		18	ns
t_{ICS}	Synchronous Clock Delay		0.5		0.5		2		2		3	ns
t_{FD}	Feedback Delay		1		1		1		1		2	ns
t_{PRE}	Asynchronous Register Preset Time		3		3		5		6		7	ns
t_{CLR}	Asynchronous Register Clear Time		3		3		5		6		7	ns
t_{PCW}	Asynchronous Preset and Clear Pulse Width	3		4		5		6		7		ns
t_{PCR}	Asynchronous Preset and Clear Recovery Time	3		4		5		6		7		ns
t_{PIA}	Programmable Interconnect Array Delay Time		10		12		14		16		20	ns

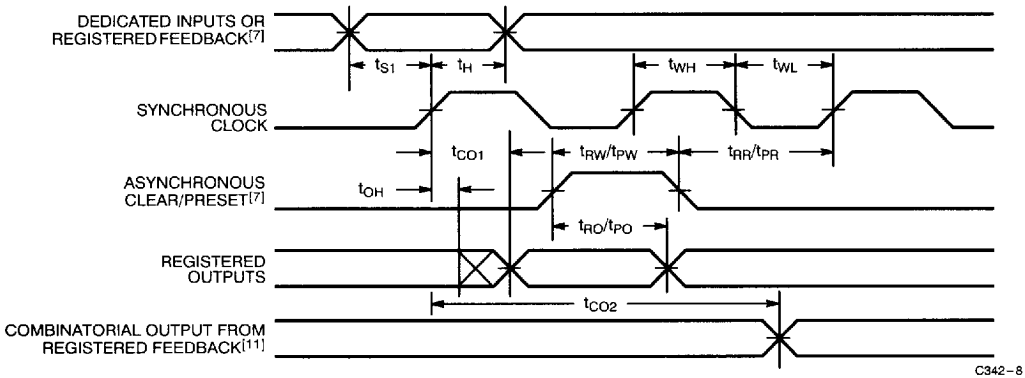
Shaded area contains preliminary information.

Switching Waveforms

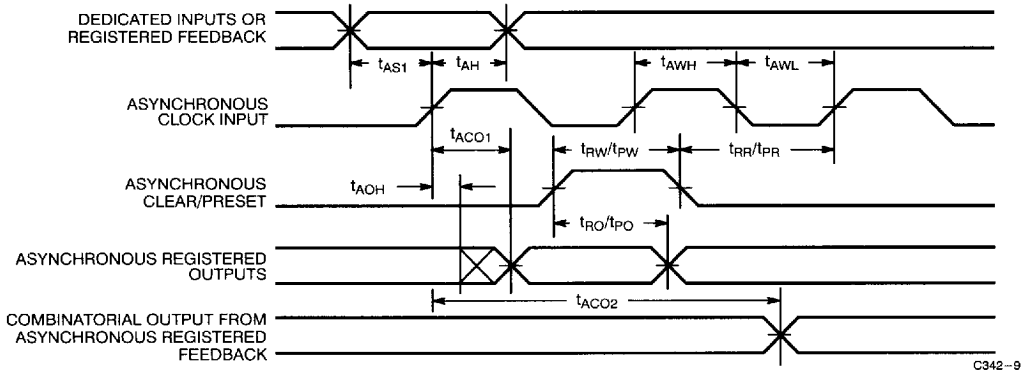
External Combinatorial



External Synchronous

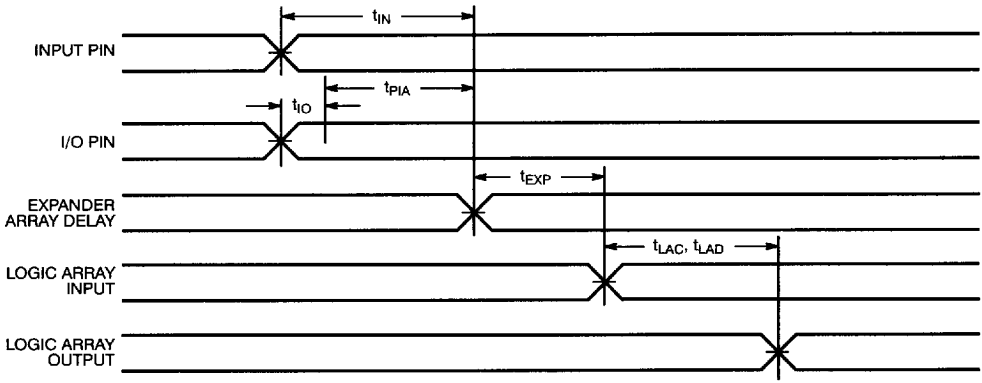


External Asynchronous



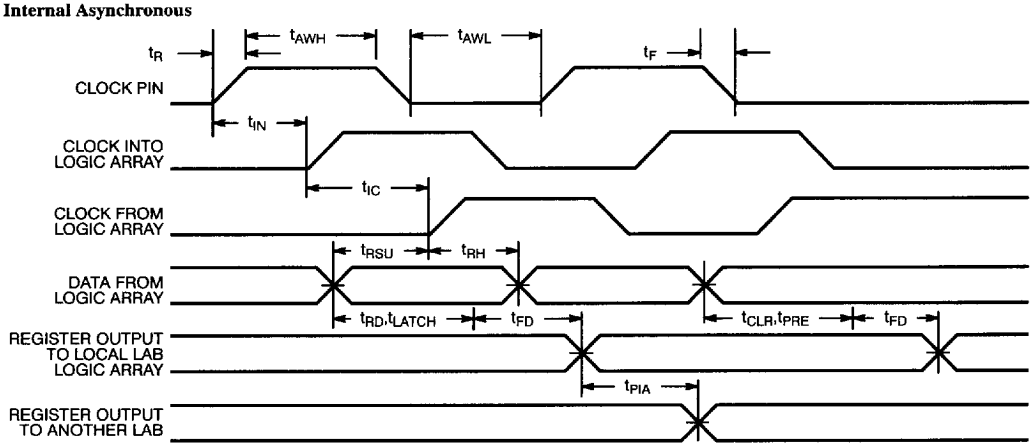
Switching Waveforms (continued)

Internal Combinatorial



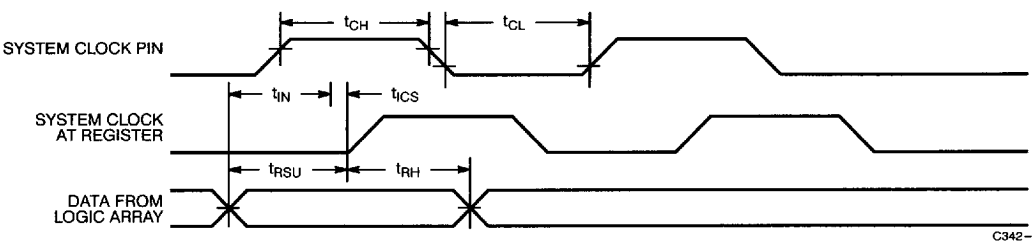
C342-10

Internal Asynchronous



C342-11

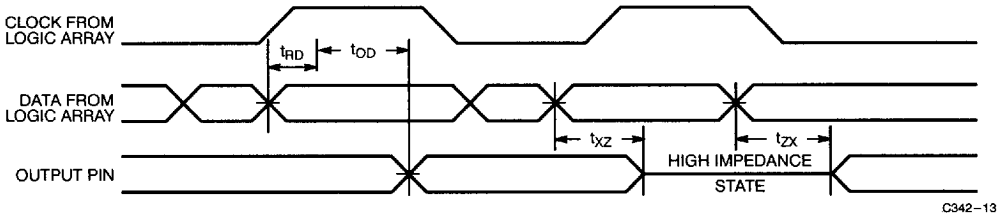
Internal Synchronous



C342-12

Switching Waveforms (continued)

Internal Synchronous



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C342B–12HC	H81	68-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C342B–12JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342B–12RC	R68	68-Pin Windowed Ceramic Pin Grid Array	
15	CY7C342B–15HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	Commercial/ Industrial
	CY7C342B–15JC/JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342B–15RC/RI	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342B–15HMB	H81	68-Pin Windowed Leaded Chip Carrier	Military
	CY7C342B–15RMB	R68	68-Pin Windowed Ceramic Pin Grid Array	
20	CY7C342B–20HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	Commercial/ Industrial
	CY7C342B–20JC/JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342B–20RC/RI	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342B–20HMB	H81	68-Pin Windowed Leaded Chip Carrier	Military
	CY7C342B–20RMB	R68	68-Pin Windowed Ceramic Pin Grid Array	
25	CY7C342–25HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	Commercial/ Industrial
	CY7C342–25JC/JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342–25RC/RI	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342B–25HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	
	CY7C342B–25JC/JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342B–25RC/RI	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342B–25HMB	H81	68-Pin Windowed Leaded Chip Carrier	Military
	CY7C342B–25RMB	R68	68-Pin Windowed Ceramic Pin Grid Array	
30	CY7C342–30HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	Commercial/ Industrial
	CY7C342–30JC/JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342–30RC/RI	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342B–30HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	
	CY7C342B–30JC/JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342B–30RC/RI	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342–30HMB	H81	68-Pin Windowed Leaded Chip Carrier	Military
	CY7C342–30RMB	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342B–30HMB	H81	68-Pin Windowed Leaded Chip Carrier	
	CY7C342B–30RMB	R68	68-Pin Windowed Ceramic Pin Grid Array	
35	CY7C342–35HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	Commercial/ Industrial
	CY7C342–35JC/JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342–35RC/RI	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342B–35HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	
	CY7C342B–35JC/JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C342B–35RC/RI	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342–35HMB	H81	68-Pin Windowed Leaded Chip Carrier	Military
	CY7C342–35RMB	R68	68-Pin Windowed Ceramic Pin Grid Array	
	CY7C342B–35HMB	H81	68-Pin Windowed Leaded Chip Carrier	
	CY7C342B–35RMB	R68	68-Pin Windowed Ceramic Pin Grid Array	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD1}	7, 8, 9, 10, 11
t_{PD2}	7, 8, 9, 10, 11
t_{PD3}	7, 8, 9, 10, 11
t_{CO1}	7, 8, 9, 10, 11
t_{S1}	7, 8, 9, 10, 11
t_{S2}	7, 8, 9, 10, 11
t_{H}	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{WL}	7, 8, 9, 10, 11
t_{RO}	7, 8, 9, 10, 11
t_{PO}	7, 8, 9, 10, 11
t_{ACO1}	7, 8, 9, 10, 11
t_{AS1}	7, 8, 9, 10, 11
t_{AH}	7, 8, 9, 10, 11
t_{AWH}	7, 8, 9, 10, 11
t_{AWL}	7, 8, 9, 10, 11

Document #: 38–00119–F