

## 74F175 Quad D-Type Flip-Flop

### General Description

The 74F175 is a high-speed quad D-type flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, LOW.

### Features

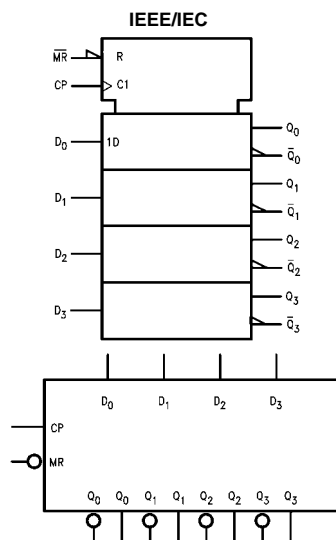
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Asynchronous common reset
- True and complement output

### Ordering Code:

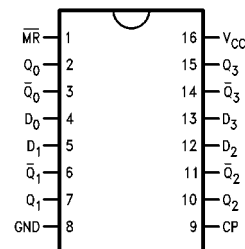
| Order Number | Package Number | Package Description   |
|--------------|----------------|---|
| 74F175SC     | M16A           | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow |
| 74F175SJ     | M16D           | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide               |
| 74F175PC     | N16E           | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide       |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



Unit Loading/Fan Out

| Pin Names                       | Description                            | U.L.     | Input $I_{IH}/I_{IL}$  |
|---------------------------------|--|----------|------------------------|
|                                 |  | HIGH/LOW | Output $I_{OH}/I_{OL}$ |
| $D_0-D_3$                       | Data Inputs                            | 1.0/1.0  | 20 $\mu$ A/-0.6 mA     |
| CP                              | Clock Pulse Input (Active Rising Edge) | 1.0/1.0  | 20 $\mu$ A/-0.6 mA     |
| $\overline{MR}$                 | Master Reset Input (Active LOW)        | 1.0/1.0  | 20 $\mu$ A/-0.6 mA     |
| $Q_0-Q_3$                       | True Outputs                           | 50/33.3  | -1 mA/20 mA            |
| $\overline{Q_0}-\overline{Q_3}$ | Complement Outputs                     | 50/33.3  | -1 mA/20 mA            |

Functional Description

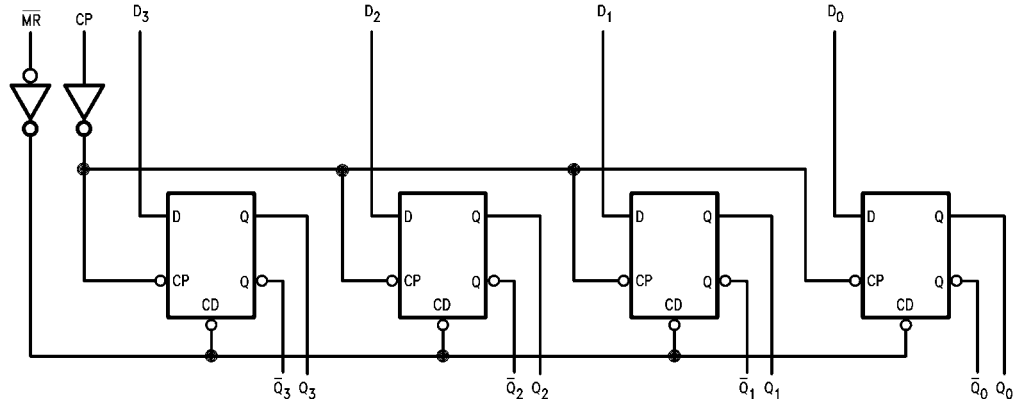
The 74F175 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and  $\overline{Q}$  outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and  $\overline{Q}$  outputs to follow. A LOW input on the Master Reset ( $\overline{MR}$ ) will force all Q outputs LOW and  $\overline{Q}$  outputs HIGH independent of Clock or Data inputs. The 74F175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

Truth Table

| Inputs          |            |       | Outputs |                  |
|-----------------|------------|-------|---------|------------------|
| $\overline{MR}$ | CP         | $D_n$ | $Q_n$   | $\overline{Q_n}$ |
| L               | X          | X     | L       | H                |
| H               | $\nearrow$ | H     | H       | L                |
| H               | $\nearrow$ | L     | L       | H                |

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
 $\nearrow$  = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

|   |                   |
|---|-------------------|
| Storage Temperature                         | -65°C to +150°C   |
| Ambient Temperature under Bias              | -55°C to +125°C   |
| Junction Temperature under Bias             | -55°C to +150°C   |
| V <sub>CC</sub> Pin Potential to Ground Pin | -0.5V to +7.0V    |
| Input Voltage (Note 2)                      | -0.5V to +7.0V    |
| Input Current (Note 2)                      | -30 mA to +5.0 mA |

Voltage Applied to Output

in HIGH State (with V<sub>CC</sub> = 0V)Standard Output -0.5V to V<sub>CC</sub>

3-STATE Output -0.5V to +5.5V

Current Applied to Output


in LOW State (Max) twice the rated I<sub>OL</sub> (mA)**Recommended Operating Conditions**

|                              |                |
|------------------------------|----------------|
| Free Air Ambient Temperature | 0°C to +70°C   |
| Supply Voltage               | +4.5V to +5.5V |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

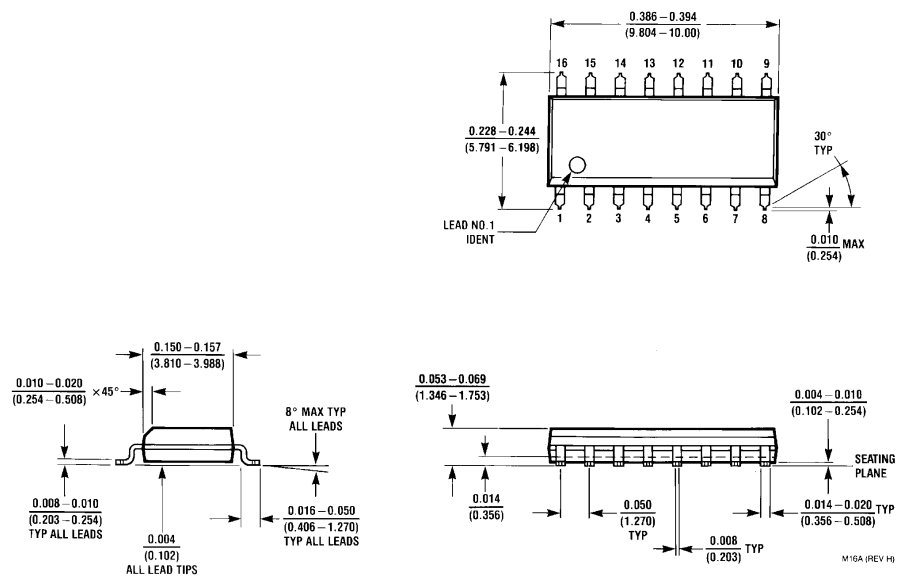
| Symbol           | Parameter                         | Min                                       | Typ        | Max  | Units | V <sub>CC</sub> | Conditions   |
|------------------|-----------------------------------|---|------------|------|-------|-----------------|--|
| V <sub>IH</sub>  | Input HIGH Voltage                | 2.0                                       |            |      | V     |                 | Recognized as a HIGH Signal  |
| V <sub>IL</sub>  | Input LOW Voltage                 |   |            | 0.8  | V     |                 | Recognized as a LOW Signal   |
| V <sub>CD</sub>  | Input Clamp Diode Voltage         |   |            | -1.2 | V     | Min             | I <sub>IN</sub> = -18 mA   |
| V <sub>OH</sub>  | Output HIGH Voltage               | 10% V <sub>CC</sub><br>5% V <sub>CC</sub> | 2.5<br>2.7 |      | V     | Min             | I <sub>OH</sub> = -1 mA<br>I <sub>OH</sub> = -1 mA   |
| V <sub>OL</sub>  | Output LOW Voltage                | 10% V <sub>CC</sub>                       |            | 0.5  | V     | Min             | I <sub>OL</sub> = 20 mA  |
| I <sub>IH</sub>  | Input HIGH Current                |   |            | 5.0  | μA    | Max             | V <sub>IN</sub> = 2.7V   |
| I <sub>BVI</sub> | Input HIGH Current Breakdown Test |   |            | 7.0  | μA    | Max             | V <sub>IN</sub> = 7.0V   |
| I <sub>CEX</sub> | Output HIGH Leakage Current       |   |            | 50   | μA    | Max             | V <sub>OUT</sub> = V <sub>CC</sub>   |
| V <sub>ID</sub>  | Input Leakage Test                | 4.75                                      |            |      | V     | 0.0             | I <sub>ID</sub> = 1.9 μA<br>All Other Pins Grounded  |
| I <sub>OD</sub>  | Output Leakage Circuit Current    |   |            | 3.75 | μA    | 0.0             | V <sub>ID</sub> = 150 mV<br>All Other Pins Grounded  |
| I <sub>IL</sub>  | Input LOW Current                 |   |            | -0.6 | mA    | Max             | V <sub>IN</sub> = 0.5V   |
| I <sub>OS</sub>  | Output Short-Circuit Current      | -60                                       |            | -150 | mA    | Max             | V <sub>OUT</sub> = 0V  |
| I <sub>CC</sub>  | Power Supply Current              |   | 22.5       | 34.0 | mA    | Max             | CP = <br>D <sub>n</sub> = MR = HIGH |

## AC Electrical Characteristics

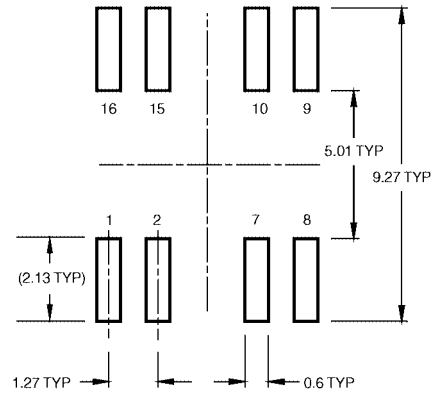
| Symbol           | Parameter   | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50 pF |     |      | T <sub>A</sub> = -55°C to +125°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50 pF |      | T <sub>A</sub> = 0°C to +70°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50 pF |      | Units |
|------------------|---|---|-----|------|---|------|--|------|-------|
|                  |   | Min   | Typ | Max  | Min   | Max  | Min  | Max  |       |
| f <sub>MAX</sub> | Maximum Clock Frequency                                       | 100   | 140 |      | 80  |      | 100  |      | MHz   |
| t <sub>PLH</sub> | Propagation Delay<br>CP to Q <sub>n</sub> or $\overline{Q}_n$ | 4.0   | 5.0 | 6.5  | 3.5   | 8.5  | 4.0  | 7.5  | ns    |
| t <sub>PHL</sub> | Propagation Delay<br>$\overline{MR}$ to Q <sub>n</sub>        | 4.0   | 6.5 | 8.5  | 4.0   | 10.5 | 4.0  | 9.5  |       |
| t <sub>PHL</sub> | Propagation Delay<br>$\overline{MR}$ to Q <sub>n</sub>        | 4.5   | 9.0 | 11.5 | 4.5   | 15.0 | 4.5  | 13.0 | ns    |
| t <sub>PLH</sub> | Propagation Delay<br>$\overline{MR}$ to $\overline{Q}_n$      | 4.0   | 6.5 | 8.0  | 4.0   | 10.0 | 4.0  | 9.0  | ns    |

## AC Operating Requirements

| Symbol             | Parameter                            | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = +5.0V |     | T <sub>A</sub> = -55°C to +125°C<br>V <sub>CC</sub> = +5.0V |     | T <sub>A</sub> = 0°C to +70°C<br>V <sub>CC</sub> = +5.0V |     | Units |
|--------------------|--------------------------------------|---|-----|---|-----|--|-----|-------|
|                    |                                      | Min   | Max | Min   | Max | Min  | Max |       |
| t <sub>S</sub> (H) | Setup Time, HIGH or LOW              | 3.0   |     | 3.0   |     | 3.0  |     | ns    |
| t <sub>S</sub> (L) | D <sub>n</sub> to CP                 | 3.0   |     | 3.0   |     | 3.0  |     |       |
| t <sub>H</sub> (H) | Hold Time, HIGH or LOW               | 1.0   |     | 1.0   |     | 1.0  |     |       |
| t <sub>H</sub> (L) | D <sub>n</sub> to CP                 | 1.0   |     | 2.0   |     | 1.0  |     |       |
| t <sub>W</sub> (H) | CP Pulse Width                       | 4.0   |     | 4.0   |     | 4.0  |     | ns    |
| t <sub>W</sub> (L) | HIGH or LOW                          | 5.0   |     | 5.0   |     | 5.0  |     |       |
| t <sub>W</sub> (L) | $\overline{MR}$ Pulse Width, LOW     | 5.0   |     | 5.0   |     | 5.0  |     | ns    |
| t <sub>REC</sub>   | Recovery Time, $\overline{MR}$ to CP | 5.0   |     | 5.0   |     | 5.0  |     | ns    |

**Physical Dimensions** inches (millimeters) unless otherwise noted


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow  
Package Number M16A**



Technical drawing of a 12-pin connector. The drawing shows two views: a side view on the left and a front view on the right. Dimensions and tolerances are specified as follows:

- Overall height: 2.1 MAX.
- Lead tip diameter: ALL LEAD TIPS,  $\varnothing 0.1$  C
- Pin pitch: 1.27 TYP
- Pin diameter:  $\varnothing 0.12$  M C A
- Pin length: 1.8  $\pm$  0.1
- Pin thickness: 0.15  $\pm$  0.05
- Pin spacing: 0.35-0.51
- Mounting hole diameter:  $\varnothing 0.12$  M C A
- Mounting hole position: 0.15  $\pm$  0.05

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

7° TYP

0°-8° TYP

GAGE PLANE

0.25

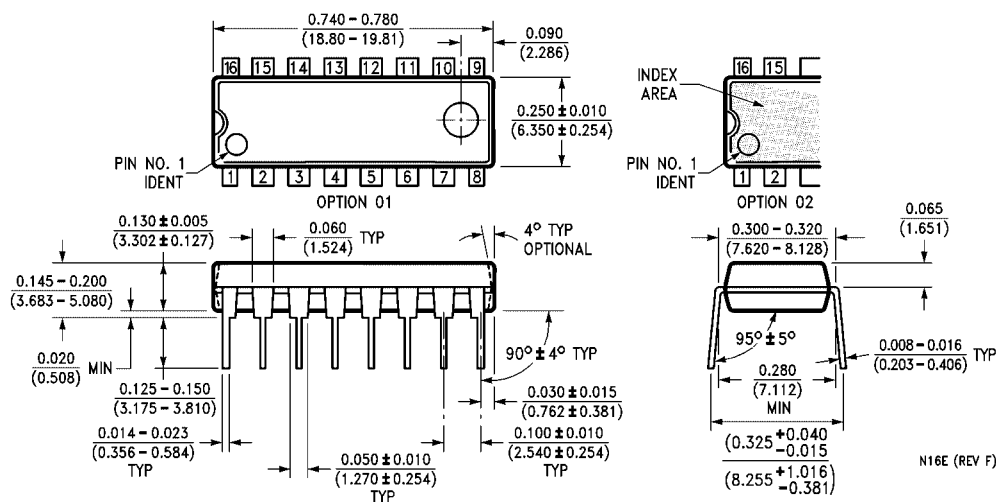
0.60±0.15

1.25

SEATING PLANE

DETAIL A

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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