

74F175

Quad D-Type Flip-Flop

General Description

The 74F175 is a high-speed quad D-type flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, LOW.

Features

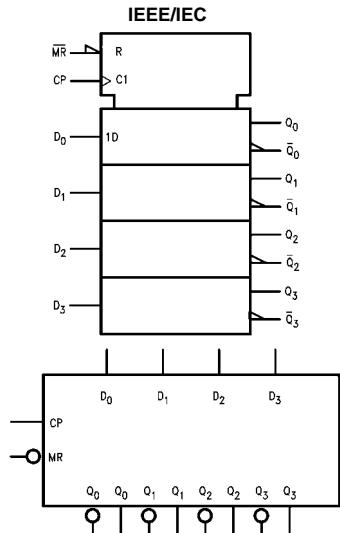
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Asynchronous common reset
- True and complement output

Ordering Code:

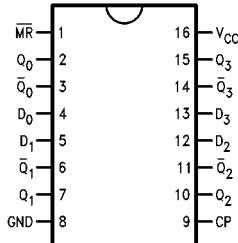
Order Number	Package Number	Package Description
74F175SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F175SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F175PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0-D_3	Data Inputs	1.0/1.0	$20 \mu A/0.6 \text{ mA}$
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	$20 \mu A/0.6 \text{ mA}$
MR	Master Reset Input (Active LOW)	1.0/1.0	$20 \mu A/0.6 \text{ mA}$
Q_0-Q_3	True Outputs	50/33.3	$-1 \text{ mA}/20 \text{ mA}$
$\bar{Q}_0-\bar{Q}_3$	Complement Outputs	50/33.3	$-1 \text{ mA}/20 \text{ mA}$

Functional Description

The 74F175 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and \bar{Q} outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and \bar{Q} outputs to follow. A LOW input on the Master Reset (MR) will force all Q outputs LOW and \bar{Q} outputs HIGH independent of Clock or Data inputs. The 74F175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

Truth Table

Inputs			Outputs	
MR	CP	D_n	Q_n	\bar{Q}_n
L	X	X	L	H
H	✓	H	H	L
H	✓	L	L	H

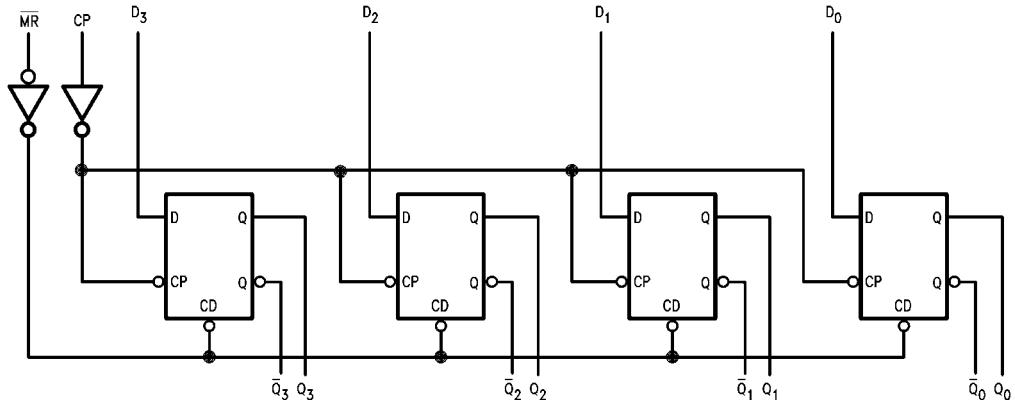
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

✓ = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V_{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with $V_{CC} = 0V$)	
Standard Output	-0.5V to V_{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

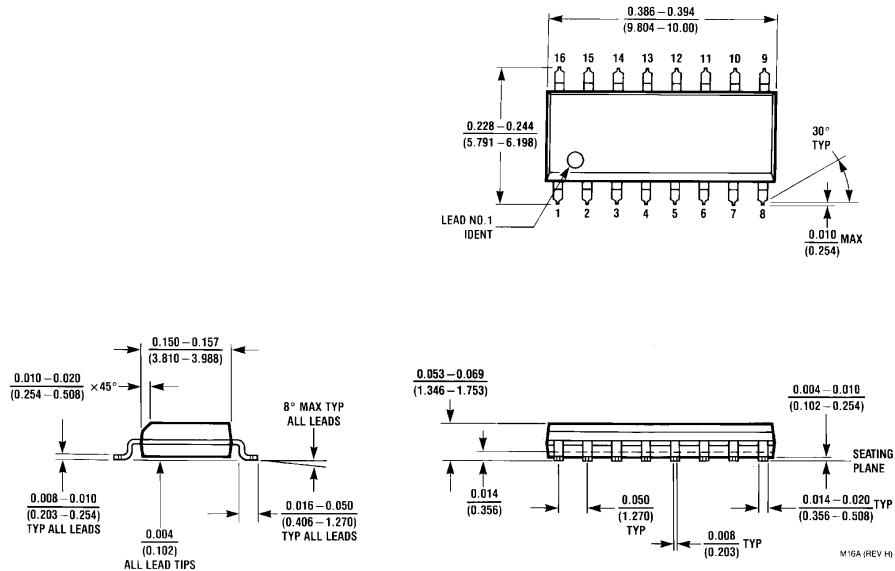
Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			-1.2	V	Min	$I_{IN} = -18$ mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5		V	Min	$I_{OH} = -1$ mA
	5% V_{CC}		2.7				$I_{OH} = -1$ mA
V_{OL}	Output LOW Voltage	10% V_{CC}		0.5	V	Min	$I_{OL} = 20$ mA
	5% V_{CC}						
I_{IH}	Input HIGH Current			5.0	μ A	Max	$V_{IN} = 2.7V$
I_{BVI}	Input HIGH Current Breakdown Test			7.0	μ A	Max	$V_{IN} = 7.0V$
I_{CEX}	Output HIGH Leakage Current			50	μ A	Max	$V_{OUT} = V_{CC}$
V_{ID}	Input Leakage Test	4.75			V	0.0	$I_{ID} = 1.9$ μ A All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current			3.75	μ A	0.0	$V_{IOD} = 150$ mV All Other Pins Grounded
I_{IL}	Input LOW Current			-0.6	mA	Max	$V_{IN} = 0.5V$
I_{OS}	Output Short-Circuit Current	-60	-150		mA	Max	$V_{OUT} = 0V$
I_{CC}	Power Supply Current		22.5	34.0	mA	Max	$CP = \text{--}$ $D_n = \overline{MR} = \text{HIGH}$

AC Electrical Characteristics

Symbol	Parameter	TA = +25°C VCC = +5.0V CL = 50 pF			TA = -55°C to +125°C VCC = +5.0V CL = 50 pF			TA = 0°C to +70°C VCC = +5.0V CL = 50 pF			Units
		Min	Typ	Max	Min	Max	Min	Max	Min	Max	
t _{MAX}	Maximum Clock Frequency	100	140		80		100				MHz
t _{PLH}	Propagation Delay CP to Q _n or \bar{Q}_n	4.0	5.0	6.5	3.5	8.5	4.0	7.5	4.0	9.5	ns
t _{PLH}	Propagation Delay MR to Q _n	4.0	6.5	8.0	4.0	10.0	4.0	13.0	4.0	9.0	ns
t _{PLH}	Propagation Delay MR to \bar{Q}_n	4.5	9.0	11.5	4.5	15.0	4.5				

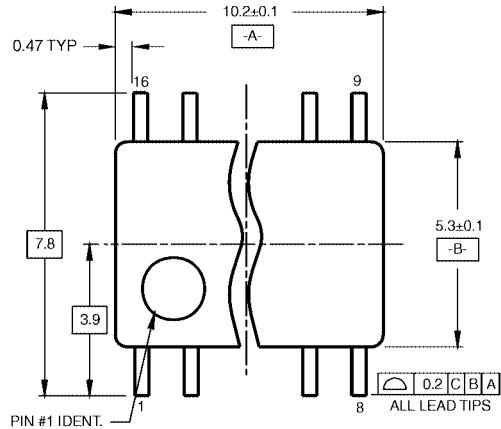
AC Operating Requirements

Symbol	Parameter	TA = +25°C VCC = +5.0V			TA = -55°C to +125°C VCC = +5.0V			TA = 0°C to +70°C VCC = +5.0V			Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	
t _{S(H)}	Setup Time, HIGH or LOW D _n to CP	3.0		3.0		3.0		3.0		3.0	
t _{S(L)}		3.0		3.0		3.0		3.0		3.0	
t _{H(H)}	Hold Time, HIGH or LOW D _n to CP	1.0		1.0		1.0		1.0		1.0	
t _{H(L)}		1.0		2.0		1.0		1.0		1.0	
t _{W(H)}	CP Pulse Width HIGH or LOW	4.0		4.0		4.0		4.0		4.0	
t _{W(L)}		5.0		5.0		5.0		5.0		5.0	
t _{W(L)}	MR Pulse Width, LOW	5.0		5.0		5.0		5.0		5.0	
t _{REC}	Recovery Time, \bar{MR} to CP	5.0		5.0		5.0		5.0		5.0	

Physical Dimensions inches (millimeters) unless otherwise noted

16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



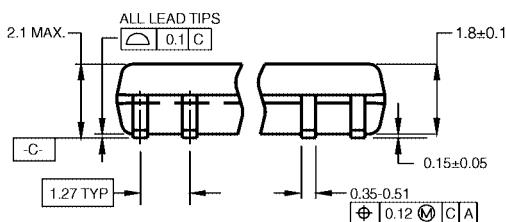
The diagram illustrates a structural frame with the following dimensions:

- Bay 16: 16 TYP (Total height)
- Bay 15: 15 TYP (Total height)
- Bay 10: 10 TYP (Total height)
- Bay 9: 9 TYP (Total height)
- Bay 1: 1 TYP (Total height)
- Bay 2: 2 TYP (Total height)
- Bay 7: 7 TYP (Total height)
- Bay 8: 8 TYP (Total height)

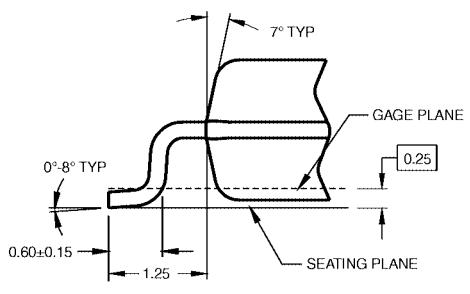
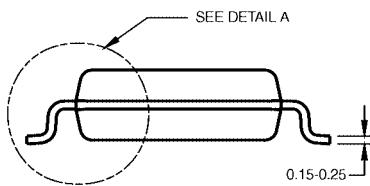
Vertical dimensions are indicated by arrows:

- From the bottom of Bay 1 to the top of Bay 16: 1.27 TYP
- From the bottom of Bay 1 to the top of Bay 10: 5.01 TYP
- From the bottom of Bay 1 to the top of Bay 9: 9.27 TYP
- From the bottom of Bay 1 to the top of Bay 7: 2.13 TYP
- From the bottom of Bay 1 to the top of Bay 8: 0.6 TYP

LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



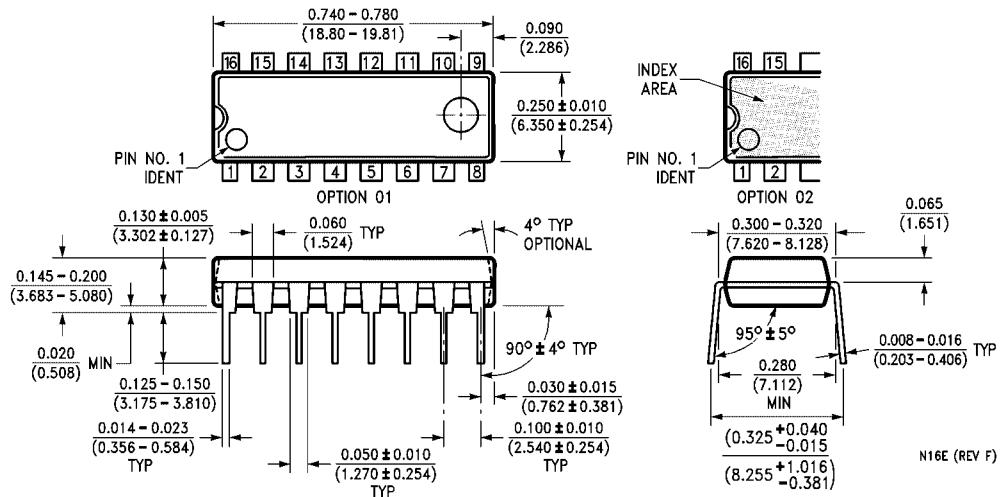
NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION,
ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

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