19-0222; Rev 0; 5/05

EVALUATION KIT AVAILABLE

Complete 450MHz Quadrature Transmitter

General Description

The MAX2370 integrated quadrature transmitter is designed for 450MHz applications. The device takes a differential I/Q baseband input and converts it up to intermediate frequency (IF) through a quadrature modulator and IF variable-gain amplifier (VGA). The signal is then routed to an external IF filter and upconverted to RF through an image-reject mixer and RF VGA. The signal is further amplified with an on-chip power amplifier (PA) driver. An IF synthesizer, an RF synthesizer, a local oscillator buffer, and an SPI™/QSPI™/MICROWIRE™-compatible, 3-wire programmable bus complete the basic functional blocks of this IC.

The MAX2370 is available in a 48-pin TQFN package with exposed paddle and is specified for the extended temperature range (-40°C to +85°C).

Features

- **450MHz Operating Frequency**
- **+8dBm Output Power**
  - **-64dBc Typical ACPR at ±885kHz Offset**
  - **-66dBc Typical ACPR at ±1.125MHz Offset**
- **100dB Power-Control Range**
- **Dual Synthesizer for RF and IF Local Oscillators**
- **SPI/QSPI/MICROWIRE-Compatible 3-Wire Interface Bus**
- **Single-Sideband Upconverter**
- **Directly Drives External Power Amplifier**

Applications

450MHz CDMA/WCDMA Phones

OFDM, cdma2000®, WCDMA, NMT

Wireless Data Links

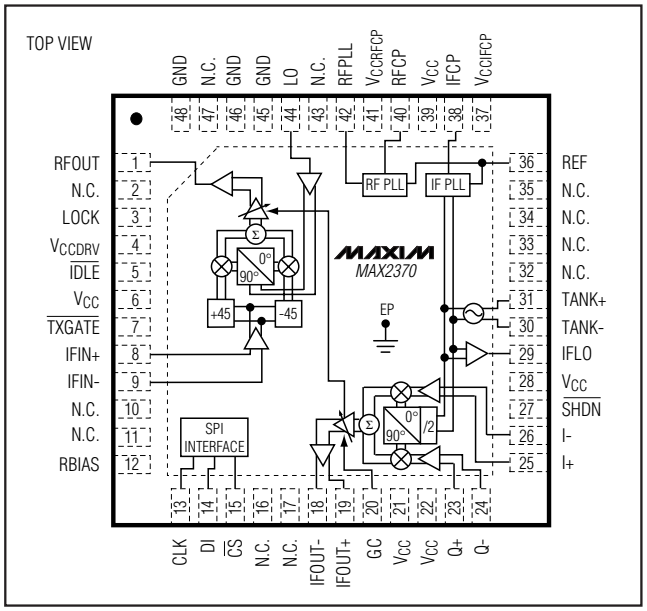
SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.
cdma2000 is a registered trademark of Telecommunications Industry Association.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX2370ETM	-40°C to +85°C	48 Thin QFN-EP* (7mm x 7mm)	T4877-3
MAX2370ETM+	-40°C to +85°C	48 Thin QFN-EP* (7mm x 7mm)	T4877+3

**EP = Exposed paddle.*
+Denotes lead-free package.

Pin Configuration/ Functional Diagram



Complete 450MHz Quadrature Transmitter

ABSOLUTE MAXIMUM RATINGS

V_{CC}, RFOUT, V_{CCIFCP}, V_{CCRFCP}, V_{CCDRV} to GND .....-0.3V to +3.6V
DI, SCLK, $\overline{CS}$, GC, $\overline{SHDN}$, $\overline{TXGATE}$, $\overline{IDLE}$, LOCK to GND .....-0.3V to (V_{CC} + 0.3V)
AC Input Pins (IFIN_, Q_, I_, TANK_, REF, RFPLL, LO) to GND .....1V Peak
Digital Input Current ($\overline{SHDN}$, $\overline{TXGATE}$, $\overline{IDLE}$, SCLK, DI, $\overline{CS}$) .....±10mA

Continuous Power Dissipation (T_A = +70°C)
48-Pin Thin QFN (derate 38.5mW/°C above +70°C).....3077mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

CAUTION! ESD SENSITIVE DEVICE

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +3.3V, $\overline{SHDN}$ = $\overline{IDLE}$ = $\overline{TXGATE}$ = high, V_{GC} = 2.5V, R_{BIAS} = 10kΩ, registers set according to Table 1, f_{REF} = 19.2MHz, no AC signals applied, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	2.7		3.3	V
Operating Supply Current	V_{GC} = 0.6V		53	79	mA
	V_{GC} = 1.95V		57	87	
	P_{RFOUT} = +5.5dBm, IFG[2:0] = 011		118		
	P_{RFOUT} = +8dBm, IFG[2:0] = 011		134		
	Addition for IFLO buffer		3.4	7.7	
	$\overline{IDLE}$ = low		6	10	
	$\overline{TXGATE}$ = low		5	7	
Sleep-Mode Supply Current	$\overline{SHDN}$ = 0V		0.5	20	µA
Logic-High Voltage		0.7 x V_{CC}			V
Logic-Low Voltage				0.3 x V_{CC}	V
Logic Input Current		-5		+5	µA
GC Input Current	V_{GC} = 0.5V to 2.5V		3.3	5	µA
GC Input Current During Shutdown	$\overline{SHDN}$ = low, V_{GC} = 2.5V		7	11	µA
Lock Indicator High Voltage (Locked)	47kΩ pullup load	V_{CC} - 0.4V			V
Lock Indicator Low Voltage (Unlocked)	47kΩ pullup load			0.5	V

AC ELECTRICAL CHARACTERISTICS

(MAX2370 EV kit, V_{CC} = +2.7V to +3.3V, $\overline{SHDN}$ = $\overline{IDLE}$ = $\overline{TXGATE}$ = high, V_{GC} = 2.5V, R_{BIAS} = 10kΩ, 50Ω system, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = $\overline{SHDN}$ = $\overline{IDLE}$ = $\overline{TXGATE}$ = $\overline{CS}$ = 3.0V, f_{REF} = 19.2MHz, LO input power = -15dBm, f_{LO} = 575MHz, f_{RFOUT} = 455MHz, f_{IF} = 120MHz, registers set according to Table 1, input voltage at I and Q = 130mV_{RMS} differential, cascade specifications assume 400Ω IF filter with 5dB insertion loss, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
MODULATOR						
IF Frequency Range	Typically meets 30dB sideband suppression over this frequency range			95 to 195		MHz
I/Q Common-Mode Input Voltage	(Notes 2, 3)		1.35		V_{CC} - 1.25	V
I/Q Input Current	V_{CM} = 1.4V				6	µA
Gain-Control Range	V_{GC} = 0.5V to 2.5V	+25°C < T_A < +85°C	70	87		dB
		T_A = -40°C		85		
Gain Variation Over Temperature	Relative to +25°C, T_A = -40°C to +85°C			-2.4, +3.4		dB
Carrier Suppression	V_{GC} = 2.5V		30	40		dB
Sideband Suppression	V_{GC} = 2.5V		30	40		dB
IF Output Noise at Rx Band	V_{GC} set to give -12dBm IF output power, noise measured at 10MHz offset (Note 4)			-138	-135	dBm/Hz
IF Adjacent Channel Power Ratio IS-95 Reverse Modulation	V_{GC} set to give -12dBm IF output power, IFG[2:0] = 011	f_{OFFSET} = ±885kHz in 30kHz BW		-66		dBc
		f_{OFFSET} = ±1.125MHz in 30kHz BW		-69		
		f_{OFFSET} = ±1.98MHz in 30kHz BW		-84		
		f_{OFFSET} = ±4MHz in 30kHz BW		-89		
UPCONVERTER AND PREDRIVER						
RFOUT Frequency Range	See the *Typical Operating Characteristics* for typical gain vs. frequency			410 to 500		MHz
LO Frequency Range	Typically meets 30dB image suppression over this range			530 to 695		MHz
LO and RFPLL Input Power			-15	-7	0	dBm
Conversion Gain				23		dB
MPL Gain Change	MPL = 0, gain relative to MPL = 1			-3.4		dB
RF Gain-Control Range	V_{GC} = 0.5V to 2.5V	+25°C < T_A < +85°C	30	44		dB
		T_A = -40°C		46		
RF Image Suppression	At maximum output power			-20		dBc
Rx Band Noise Power	P_{RFOUT} = +8dBm, noise measured at +10MHz offset (Note 4)			-130	-128.5	dBm/Hz
CASCADED MODULATOR, UPCONVERTER, AND PREDRIVER						
RFOUT Output Power	Meets ACPR specifications (Note 4)		5.5	10		dBm
Adjacent Channel Power Ratio IS-95 Reverse Modulation (Note 4)	P_{OUT} = +8dBm, IFG[2:0] = 011	f_{OFFSET} = ±885kHz in 30kHz BW		-64	-57	dBc
		f_{OFFSET} = ±1.125MHz in 30kHz BW		-66	-61	
		f_{OFFSET} = ±1.98MHz in 30kHz BW		-82	-78	
		f_{OFFSET} = ±4MHz in 30kHz BW		-86	-78	
	P_{OUT} = +5.5dBm, IFG[2:0] = 011	f_{OFFSET} = ±885kHz in 30kHz BW		-64	-58	
		f_{OFFSET} = ±1.125MHz in 30kHz BW		-67	-62	
		f_{OFFSET} = ±1.98MHz in 30kHz BW		-81	-78	
		f_{OFFSET} = ±4MHz in 30kHz BW		-86	-85	

Complete 450MHz Quadrature Transmitter

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2370 EV kit, V_{CC} = +2.7V to +3.3V, $\overline{SHDN}$ = $\overline{IDLE}$ = $\overline{TXGATE}$ = high, V_{GC} = 2.5V, R_{BIAS} = 10kΩ, 50Ω system, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = $\overline{SHDN}$ = $\overline{IDLE}$ = $\overline{TXGATE}$ = $\overline{CS}$ = 3.0V, f_{REF} = 19.2MHz, LO input power = -15dBm, f_{LO} = 575MHz, f_{RFOUT} = 455MHz, f_{IF} = 120MHz, registers set according to Table 1, input voltage at I and Q = 130mV_{RMS} differential, cascade specifications assume 400Ω IF filter with 5dB insertion loss, T_A = +25°C, unless otherwise noted.) (Note 1)

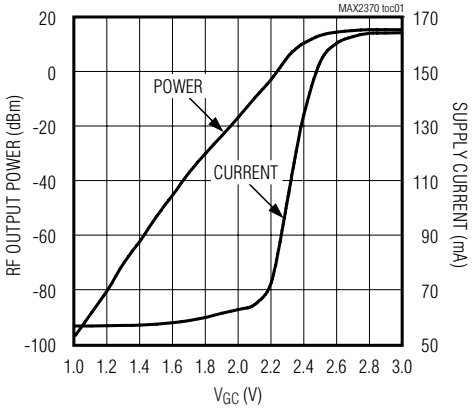
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Power Variation Over Temperature	Relative to +25°C, T_A = -40°C to +85°C		0, -2		dB
IF PLL					
Reference Frequency		5		30	MHz
Reference Frequency Signal Level		0.1		0.6	V_{P-P}
IF Main-Divide Ratio		256		16,383	
IF Reference-Divide Ratio		2		2047	
VCO Operating Range			190 to 390		MHz
Charge-Pump Source/Sink Current	ICP = 00	96	139	174	µA
	ICP = 01	135	192	240	
	ICP = 10	190	278	348	
	ICP = 11	267	390	488	
Turbolock Boost Current	ICP = 11, ICP_MAX = 1	533	774	968	µA
Charge-Pump Source/Sink Current Matching	All values of ICP, over compliance range			6	%
IF Charge-Pump Compliance		0.5		V_{CCIFCP} - 0.5V	V
RF PLL					
RF PLL Frequency Range	RF PLL operated at 2x LO frequency			1300	MHz
Reference Frequency		5		30	MHz
RF Main-Divide Ratio		4096		262,143	
RF Reference-Divide Ratio		2		8191	
Charge-Pump Source/Sink Current	RCP = 00	220	325	406	µA
	RCP = 01	441	650	813	
	RCP = 10	499	738	923	
	RCP = 11	717	1063	1329	
Turbolock Boost Current	(Note 5)	1152	1694	2118	µA
Charge-Pump Source/Sink Current Matching	All values of RCP, over compliance range			6	%
RF Charge-Pump Compliance		0.5		V_{CCRFCP} - 0.5V	V
Phase-Detector Noise Floor	RCP = 11, RCP_TURBO1 = RCP_TURBO2 = 0, 50kHz comparison frequency		-162		dBc/Hz

Note 1: Guaranteed by production test at T_A = +25°C to +85°C, design and characterization at T_A = -40°C.
Note 2: ACPR is met over the specified V_{CM} range.
Note 3: V_{CM} must be supplied by the I/Q baseband source with ±8µA current capability.
Note 4: Guaranteed by design and characterization to 6σ.
Note 5: When enabled with RCP_TURBO1 and RCP_TURBO2 (see Tables 3 and 4), the total charge-pump current is specified. For all values of RCP, the total turbolock current is 1.63 times the corresponding nonturbo current value.

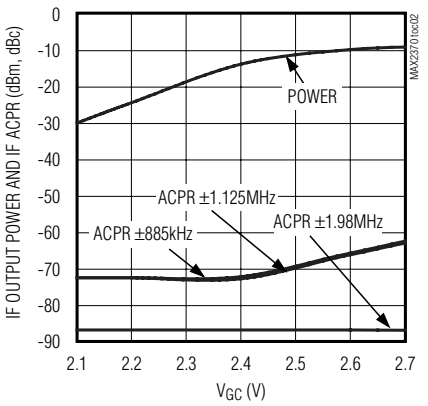
Typical Operating Characteristics

(MAX2370 EV kit, $V_{CC\_}$ = $\overline{SHDN}$ = $\overline{IDLE}$ = $\overline{TXGATE}$ = $\overline{CS}$ = 3.0V, f_{REF} = 19.2MHz, LO input power = -15dBm, f_{LO} = 575MHz, f_{RFOUT} = 455MHz, f_{IF} = 120MHz, R_{BIAS} = 10kΩ, V_{GC} = 2.5V, registers set according to Table 1, input voltage at I and Q = 130mV_{RMS} differential, T_A = +25°C, unless otherwise noted.)

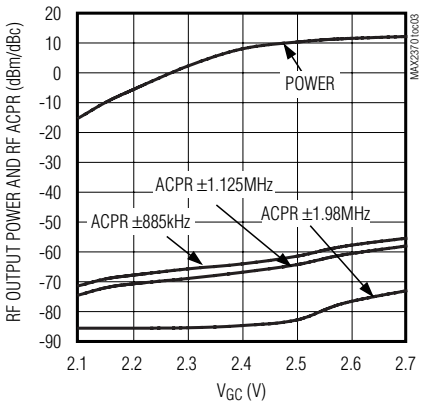
RF OUTPUT POWER AND SUPPLY CURRENT vs. GAIN-CONTROL VOLTAGE



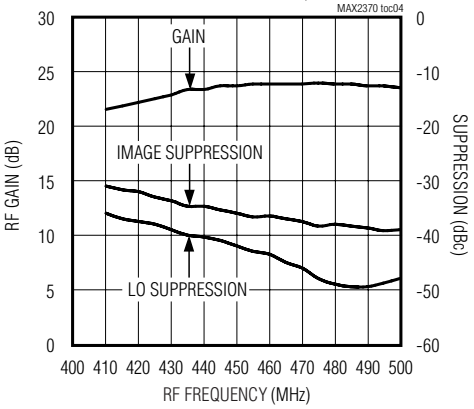
IF OUTPUT POWER AND IF ACPR vs. GAIN-CONTROL VOLTAGE



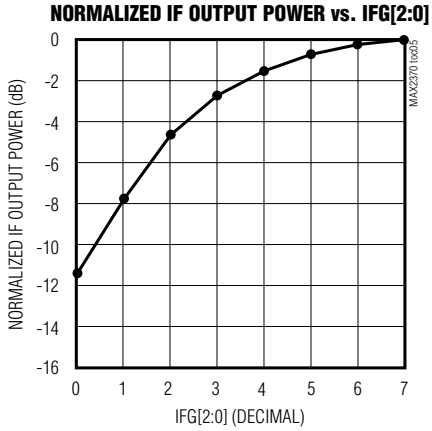
RF OUTPUT POWER AND RF ACPR vs. GAIN-CONTROL VOLTAGE



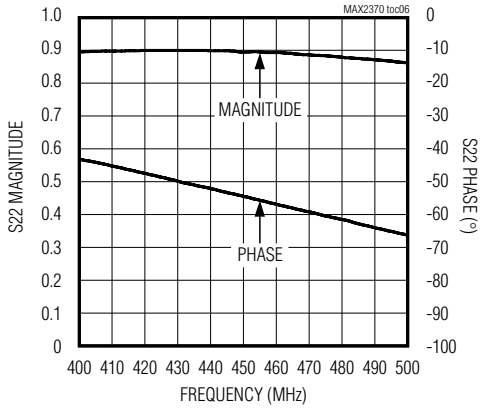
RF GAIN, IMAGE SUPPRESSION, AND LO SUPPRESSION vs. FREQUENCY



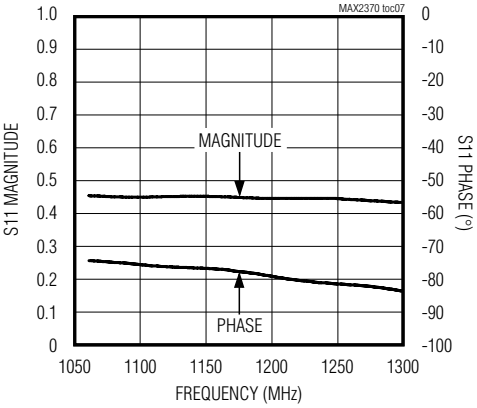
NORMALIZED IF OUTPUT POWER vs. IFG[2:0]



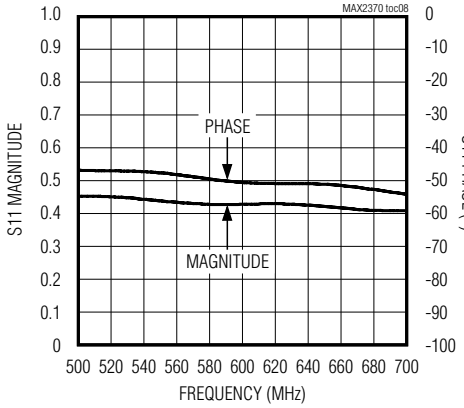
RFOUT PORT S22



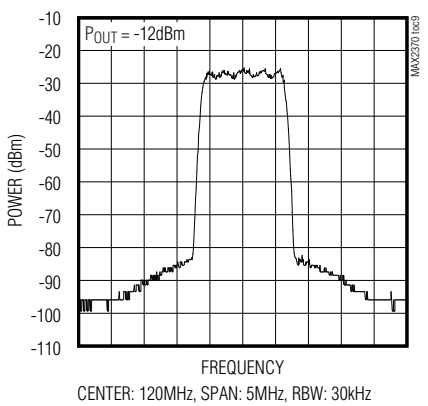
RFPLL PORT S11



LO PORT S11



IF OUTPUT SPECTRUM

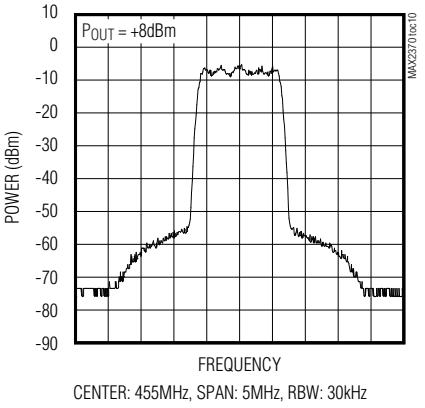


Complete 450MHz Quadrature Transmitter

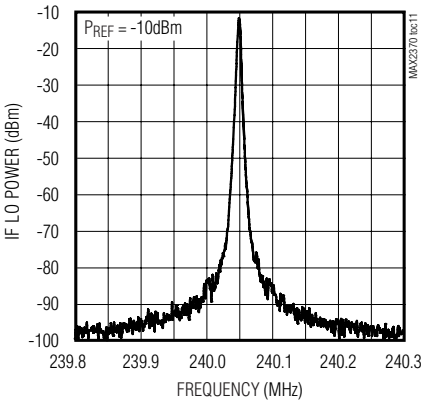
Typical Operating Characteristics (continued)

(MAX2370 EV kit, $V_{CC\_}$ = $\overline{SHDN}$ = $\overline{IDLE}$ = $\overline{TXGATE}$ = $\overline{CS}$ = 3.0V, f_{REF} = 19.2MHz, LO input power = -15dBm, f_{LO} = 575MHz, f_{RFOUT} = 455MHz, f_{IF} = 120MHz, R_{BIAS} = 10kΩ, V_{GC} = 2.5V, registers set according to Table 1, input voltage at I and Q = 130mV_{RMS} differential, T_A = +25°C, unless otherwise noted.)

RF OUTPUT SPECTRUM



IF LOCAL OSCILLATOR SPECTRUM



Pin Description

PIN	NAME	FUNCTION
1	RFOUT	Transmitter RF Output. This open-collector output requires a pullup inductor to the supply voltage, which can be part of the output matching network.
2, 10, 11, 16, 17, 32–35, 43, 47	N.C.	No Connection. Leave these pins open-circuit. Some of these pins are internally connected.
3	LOCK	Open-Drain Output Indicating LOCK Status of the IF and/or the RF PLLs. Requires an external pullup resistor. Control using configuration register bits LD_MODE[1:0].
4	V_{CCDRV}	Power Supply for the RF Driver Stage. Bypass to PC board ground with a capacitor placed as close to the pin as possible. Do not share capacitor ground vias with other ground connections.
5	$\overline{IDLE}$	Digital Input. Drive to logic-high for normal operation. Logic-low on $\overline{IDLE}$ shuts down everything except the RF PLL. A small RC lowpass filter can be used to filter digital noise.
6	V_{CC}	Power Supply for the Upconverter Stage. Bypass to PC board ground with a capacitor placed as close to the pin as possible. Do not share capacitor ground vias with other ground connections.
7	$\overline{TXGATE}$	Digital Input. Drive to logic-high for normal operation. Logic-low on $\overline{TXGATE}$ shuts down everything except the RF PLL, IF PLL, IF VCO. A small RC lowpass can be used to filter digital noise.
8, 9	IFIN+, IFIN-	Differential IF Inputs to the RF Upconverter. IFIN+ and IFIN- are internally biased to typically V_{CC} - 1.5V. The input impedance for this port is nominally 400Ω differential. AC-couple the output of the differential IF filter to this port. Keep the differential lines as short as possible to minimize the effects of stray pickup.
12	RBIAS	Bias Resistor Connection. Internally biased to typically 1.18V. An external resistor must be connected from RBIAS to ground to set the bias current for the upconverters and PA driver stages. The nominal resistor value is 10kΩ. This value can be altered to optimize the linearity of the driver stage.

Pin Description (continued)

PIN	NAME	FUNCTION
13, 14, 15	CLK, DI, $\overline{CS}$	CMOS Inputs from the 3-Wire Serial Bus (SPI/QSPI/MICROWIRE Compatible). A small RC lowpass filter on each of these pins can be used to reduce noise on these lines.
18, 19	IFOUT-, IFOUT+	Differential IF Outputs. This port is active when IF_SEL is LOW and supports both FM and CDMA modes. IFOUT+ and IFOUT- must be inductively pulled up to V_{CC} and differentially loaded with typically 560Ω. A 400Ω differential IF bandpass filter is connected between this port and IFIN+/-. The pullup inductors can be part of the filter structure. The differential output impedance of this port is nominally 400Ω, including the 560Ω external differential resistor. Keep the transmission lines from these pins as short as possible to minimize the unintentional pickup of spurious signals and noise.
20	GC	RF and IF Gain-Control Analog Input. Accepts input voltages from 0.5V (minimum gain) to 2.5V (maximum gain). When not driven, GC is internally biased to typically 1.5V. RC lowpass filter the voltage applied to this pin to remove DAC noise or PDM clock spurs.
21	V_{CC}	Power Supply for the IF VGA. Bypass to PC board ground with a 0.1µF capacitor placed as close to the pin as possible. Do not share capacitor ground vias with other ground connections.
22	V_{CC}	Power Supply for the I/Q Modulator. Bypass to PC board ground with a 0.1µF capacitor placed as close to the pin as possible. Do not share capacitor ground vias with other ground connections.
23, 24	Q+, Q-	Differential Q-Channel Baseband Inputs to the Modulator. Q+ and Q- connect directly to the bases of a differential pair and require a typical 1.35V to (V_{CC} - 1.5V) external common-mode bias voltage.
25, 26	I+, I-	Differential I-Channel Baseband Inputs to the Modulator. I+ and I- connect directly to the bases of a differential pair and require a typical 1.35V to (V_{CC} - 1.5V) external common-mode bias voltage.
27	$\overline{SHDN}$	Digital Input. Drive LOW to shut down the entire IC, drive high for normal operation. A small RC lowpass filter can be used to filter digital noise.
28	V_{CC}	Power Supply for the VCO Section. Bypass to PC board ground with a 0.1µF capacitor placed as close to the pin as possible. Do not share capacitor ground vias with other ground connections.
29	IFLO	IF LO Output. Provides access to the IF VCO output and can be used to drive an external PLL. It can be disabled by logic-low on the BUF_EN control bit. IFLO is internally biased to typically 1.5V.
30, 31	TANK-, TANK+	Differential Tank Connections for the IF VCO. TANK+ and TANK- are internally biased to approximately 1.6V and must be AC-coupled to the external tank (can be DC-coupled if tank does not sink or source current).
36	REF	Reference Frequency Input. REF is internally biased to approximately 1.0V and must be AC-coupled to the reference source. This is a high-impedance port and must be externally terminated in the desired impedance.
37	V_{CCIFCP}	Power Supply for the IF Charge Pump. This supply can be different from the system V_{CC}. Bypass to PC board ground with a minimum 0.1µF capacitor placed as close to the pin as possible. Do not share capacitor ground vias with other ground connections.
38	IFCP	High-Impedance IF Charge-Pump Output. Connect to the tune input of the IF VCO through the IF PLL loop filter. Keep the connection from IFCP to the tune input as short as possible to prevent spurious pickup.
39	V_{CC}	Power Supply for Digital Circuitry. Bypass to PC board ground with a minimum 0.1µF capacitor placed as close to the pin as possible. Do not share capacitor ground vias with other ground connections.

Complete 450MHz Quadrature Transmitter

Pin Description (continued)

PIN	NAME	FUNCTION
40	RFCP	High-Impedance RF Charge-Pump Output. Connect to the tune input of the RF VCO through the RF PLL loop filter. Keep the connection from RFCP to the tune input as short as possible to prevent spurious pickup.
41	V_{CCRFCP}	Power Supply for the RF Charge Pump. This supply can be different from the system V_{CC}. Bypass to PC board ground with a minimum 0.1µF capacitor placed as close to the pin as possible. Do not share capacitor ground vias with other ground connections.
42	RFPLL	RF PLL Input. This port drives the RF PLL. RFPLL is internally biased to typically V_{CC} - 0.8V.
44	LO	RF LO Input. LO is internally biased to typically V_{CC} - 0.8V.
45, 46, 48, EP	GND	Ground Connection. Solder the exposed paddle (EP) evenly to the board's ground plane for proper operation.

Detailed Description

The MAX2370 complete quadrature transmitter accepts differential I/Q baseband inputs with external common-mode bias. A modulator upconverts the baseband inputs to a 95MHz to 195MHz IF frequency. A gain-control voltage pin (GC) controls the gain of both the IF and RF VGAs simultaneously to achieve the best current consumption and linearity performance. The IF signal is brought off-chip for filtering, then fed to a single sideband upconverter followed by the RF VGA and PA driver. The RF upconverter requires an external VCO for operation. The IF PLL, RF PLL, and operating mode can be programmed by an SPI/QSPI/ MICROWIRE-compatible 3-wire interface.

The following sections describe each block in the *Functional Diagram*.

I/Q Modulator

Differential in-phase (I) and quadrature-phase (Q) inputs are designed to be DC-coupled and biased with the baseband output from a digital-to-analog converter (DAC). The I and Q inputs need a typical DC bias of V_{CC} / 2 and a current-drive capability of 8µA. However, common-mode voltages in the 1.35V to (V_{CC} - 1.25V) range are also acceptable. The I and Q input capacitances are typically 0.6pF to ground on each pin. The IF VCO output is fed into a divide-by-two quadrature generator block to derive quadrature LO components to drive the I/Q modulator. The output of the modulator is fed into the IF VGA.

IF VCO

The IF VCO oscillates at twice the desired IF frequency. The oscillation frequency is determined by external tank components (see the *IF Tank Design* section). Typical spurious performance for the IF VCO is shown in the *Typical Operating Characteristics*.

IFLO Output Buffer

IFLO provides a buffered LO output when BUF_EN is 1. The IFLO output frequency is equal to the IF VCO frequency, and the typical output power is -12dBm. This output is intended for applications where the receive IF is the same frequency as the transmit IF.

IF/RF PLL

The IF/RF PLL uses a charge-pump output to drive external loop filters. The loop filter is typically a passive second-order lead-lag filter. Outside the filter's bandwidth, phase noise is determined by the tank components. The two components that contribute most significantly to phase noise are the inductor and varactor. Use high-Q inductors and varactors to maximize equivalent parallel resistance. The IF_TURBO_CHARGE, RCP_TURBO1, and RCP_TURBO2 bits can be set to enable turbo mode. Turbo mode provides maximum charge-pump current during frequency acquisition. Turbo mode is disabled after frequency acquisition is achieved. When turbo mode is disabled, charge-pump current returns to the programmed levels as set by the ICP and RCP bits in the CONFIG register (Table 3).

IF VGA

The IF VGA allows the IF output level to be controlled by a voltage applied to the GC pin. The 0.5V to 2.5V voltage range on GC provides a gain-control range of > 70dB, with 2.5V providing maximum gain. The differential IF output ports are optimized for the 95MHz to 195MHz frequency range. Do not allow V_{GC} to exceed V_{CC} - 0.2V as this may cause oscillations at cold temperatures.

Single-Sideband Mixer and RF VGA

The RF transmit mixer uses a single-sideband architecture to eliminate an off-chip RF filter. The RF VGA follows the single-sideband mixer and is controlled by the same GC voltage as the IF VGA to provide optimum

current consumption and linearity performance. The power-control range of the RF VGA is typically 44dB.

PA Driver

The MAX2370 includes a PA driver that is optimized for the 410MHz to 500MHz RF frequency range. The PA driver is an open-collector output and requires a pullup inductor to V_{CC}. The pullup inductor can act as a shunt element in a shunt-series matching network.

Programmable Registers

The MAX2370 includes eight programmable registers consisting of four divide registers, a configuration register, an operational control register, a current control register, and a test register. Each register consists of 24 bits. The 4 least significant bits (LSBs) are the register's address. The 20 most significant bits (MSBs) are used for register data. All registers contain some "don't care" bits. These can be either a 0 or 1 and do not affect operation (Figure 1). Data is shifted in MSB first, followed by the 4-bit address. When $\overline{CS}$ is low, the clock is active and data is shifted with the rising edge of the clock. When $\overline{CS}$ transitions to high, the shift register is latched into the register selected by the contents of the address bits. Typical register settings for the eight registers are shown in Table 1. The dividers and control registers are programmed from the SPI/QSPI/MICROWIRE-compatible serial port.

The RFM register sets the main frequency divide ratio for the RF PLL. The RFR register sets the reference frequency divide ratio. The RF VCO frequency can be determined by the following:

$$\text{RF VCO frequency} = f_{REF} \times (RFM / RFR)$$

The IFM and IFR registers are similar:

$$\text{IF VCO frequency} = f_{REF} \times (IFM / IFR)$$

where f_{REF} is the external reference frequency.

The operational control register (OPCTRL) controls the state of the MAX2370. See Table 2 for a description of each bit's function.

The configuration register (CONFIG) sets the configuration for the RF and IF PLL and the baseband I/Q input levels. See Table 3 for a description of each bit's function.

The current-control register (I_{CC}CTRL) modifies the bias current to accommodate different operating modes. In the high-power mode, MPL = 1 sets the bias current and conversion gain to deliver an output power of at least +5.5dBm from the PA drivers. In the low-noise mode, MPL = 0 reduces output noise by 2.5dB for any given output power at the expense of 3.4dB less maximum obtainable output power.

Power Management

Bias control is distributed among several functional sections and can be controlled to accommodate many different power-down modes as shown in Table 8.

The serial interface remains active during shutdown. Setting bit SHDN_BIT = 0 or pin $\overline{SHDN}$ = GND powers down the device. In either case, PLL programming and register information is retained.

Applications Information

3-Wire Serial Interface

Figure 3 shows the 3-wire interface timing diagram. The 3-wire bus is SPI/QSPI/MICROWIRE compatible.

Electromagnetic Compliance Considerations

To produce a low-spur and EMC-compliant transmitter, minimize circular current-loop area to reduce H-field radiation. To minimize circular current-loop area, bypass all V_{CC} pins as close to the device as possible and use the distributed capacitance of a ground plane. To minimize voltage drops, make V_{CC} traces short and wide.

Program only the necessary bits in any register to minimize cycling of the serial interface's clock. RC filtering can also be used to slow the clock edges on the 3-wire interface, reducing high-frequency spectral content. RC filtering also provides transient protection by shunting high frequencies to ground, while the series resistance attenuates the transients for error-free operation. The same applies to the logic input pins ($\overline{SHDN}$, $\overline{TXGATE}$, $\overline{IDLE}$).

Place high-frequency bypass capacitors close to the pins with a dedicated via for each capacitor to ground. The 48-pin thin QFN-EP package provides minimal ground inductance by using an exposed paddle under the part. Provide at least five low-inductance vias under the exposed paddle to ground. Use a solid ground plane wherever possible. Any cutout in the ground plane may act as a slot radiator and reduce its shield effectiveness.

Keep RF LO traces as short as possible to reduce LO radiation and susceptibility to interference.

IF Tank Design

The IF tank is fully differential. The external tank components for 120MHz IF operation are shown in the *Typical Application Circuit*. See Maxim Application Note *IF Tank Design for the MAX2360* at www.maxim-ic.com for more information on designing tanks for alternate IFs.

Complete 450MHz Quadrature Transmitter

Internal to the IC, the charge pump has a leakage of less than 10nA. This is equivalent to a 300MΩ shunt resistor. The charge-pump output must see an extremely high DC resistance of greater than 300MΩ. This minimizes charge-pump spurs at the comparison frequency. Make sure there is no solder flux under the varactor or loop filter and use low-leakage capacitors.

Layout Considerations

The MAX2370 EV kit can be used as a starting point for layout. For best performance, take into consideration power-supply issues as well as RF, LO, and IF layout.

Power-Supply Layout

To minimize coupling between different sections of the IC, the ideal power-supply layout is a star configuration, which has a large decoupling capacitor at a central V_{CC} node. The V_{CC} traces branch out from this node, each going to a separate V_{CC} pin of the MAX2370. At the end of each trace is a bypass capacitor with impedance to ground less than 1Ω at the frequency of interest. This arrangement provides local decoupling at each V_{CC} pin. Use at least one via per bypass capacitor for a low-inductance ground connection. Also, connect the exposed paddle to the PC board GND with multiple vias to provide the lowest inductance ground connection possible.

Matching Network Layout

The layout of a matching network can be very sensitive to parasitic circuit elements. To minimize parasitic inductance, keep all traces short and place components as close to the IC as possible. To minimize parasitic capacitance, a cutout in the ground plane (and any other planes) below the matching network components can be used.

Keep traces short on the high-impedance ports (e.g., IF inputs and outputs) to minimize shunt capacitance.

Tank Layout

Keep the traces coming out of the tank short to reduce series inductance and shunt capacitance. Keep the inductor pads and coupling capacitor pads small to minimize stray shunt capacitance.

Chip Information

PROCESS: BiCMOS

	MSB																							LSB
	DATA 20 BITS																				ADDRESS 4 BITS			
	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	A3	A2	A1	A0
RFM-DIVIDE REGISTER			RFM-DIVIDE RATIO (18)																		ADDRESS			
	X	X	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	0	0
RFR-DIVIDE REGISTER								RFR-DIVIDE RATIO (13)													ADDRESS			
	X	X	X	X	X	X	X	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	0	1
IFM-DIVIDE REGISTER							IFM-DIVIDE RATIO (14)														ADDRESS			
	X	X	X	X	X	X	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	1	0
IFR-DIVIDE REGISTER										IFR-DIVIDE RATIO (11)											ADDRESS			
	X	X	X	X	X	X	X	X	X	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	1	1
CONTROL REGISTER					OPERATION CONTROL BITS (16)																ADDRESS			
	X	X	X	X	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	1	0	0
CONFIGURATION REGISTER					CONFIGURATION BITS (16)																ADDRESS			
	X	X	X	X	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	1	0	1
CURRENT-CONTROL REGISTER					CURRENT CONTROL BITS (16)																ADDRESS			
	X	X	X	X	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	1	1	0
TEST REGISTER												TEST BITS (9)									ADDRESS			
	X	X	X	X	X	X	X	X	X	X	X	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	1	1	1

X = DON'T CARE

Figure 1. Register Configuration

Table 1. Register Settings for Typical Operation

REGISTER NAME	TYPICAL SETTINGS	REGISTER ADDRESS	FUNCTION
RFM[17:0]	23000_{DEC}	0000_b	RF M-Divider Count
RFR[12:0]	384_{DEC}	0001_b	RF R-Divider Count
IFM[13:0]	4800_{DEC}	0010_b	IF M-Divider Count
IFR[10:0]	384_{DEC}	0011_b	IF R-Divider Count
OPCTRL[15:0]	$090F_{hex}$	0100_b	Operational Control Settings
CONFIG[15:0]	$D03F_{hex}$	0101_b	Configuration and Setup Control
I_{CC}CTRL[15:0]	$0C38_{hex}$	0110_b	Current Multiplication Factor, Throttle-Back Control, Modulator Bypass, Compensation for Gain Variation Over Temperature, Maximum Power-Level Setting
TEST[8:0]	100_{hex}	0111_b	Test Mode Control

Table 2. Operation Control Register (OPCTRL, Address: 0100_b)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTINGS	FUNCTION
RESERVED	15	0	Reserved. Set to 0 for normal operation.
RCP_TURBO1	14	0	Works with RCP_TURBO2 (in the configuration register) to set the turbo charge-pump mode (see Table 7).
ICP_MAX	13	0	0 = Normal operation. 1 = Sets IF charge-pump current to turbo level and keeps it there even after lock is established. This mode provides the highest charge-pump current, but effectively no turbo mode since current is already at maximum.
RESERVED	12, 11	01	Reserved. Set to 01 for normal operation.
RESERVED	10, 9	00	Reserved. Set to 00 for normal operation.
IFG	8, 7, 6	100	3-bit gain balancing control. Increases IF gain by approximately 2dB per LSB. Provides a means for adjusting balance between RF and IF gain for optimized linearity.
RESERVED	5	0	Reserved. Set to 0 for normal operation.
BUF_EN	4	0	LO buffer enable. 0 = LO buffer off. 1 = LO buffer on.
MOD_TYPE	3	1	Selects type of modulation. 0 = Selects direct VCO modulation (IF VCO is directly modulated and the I/Q modulator is bypassed). 1 = Selects quadrature modulation.
$\overline{\text{STBY}}$	2	1	Standby control. 0 = Shuts down everything except the registers and serial interface. 1 = Normal operation.
$\overline{\text{TXSTBY}}$	1	1	Transmitter standby control. 0 = Shuts down the modulator and upconverter leaving PLLs locked and registers active. This bit's functionality is equivalent to that of the $\overline{\text{TX\_GATE}}$ pin. 1 = Normal operation.
SHDN_BIT	0	1	Shutdown control. 0 = Shuts down everything except the serial interface. 1 = Normal operation.

Table 3. Configuration Register (CONFIG, Address: 0101_b)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTINGS	FUNCTION
IF_PLL_SHDN	15	1	IF PLL shutdown control. 0 = Shuts down IF PLL. This mode is used with an external IF PLL. 1 = Normal operation.
RF_PLL_SHDN	14	1	RF PLL shutdown control. 0 = Shuts down RF PLL. This mode is used with an external RF PLL. 1 = Normal operation.
RESERVED	13	0	Reserved. Set to 0 for normal operation.
IQ_LEVEL	12	1	Selects the nominal I/Q input levels. 0 = Selects 300mV$_{P-P}$ input mode. 1 = Selects 600mV$_{P-P}$ input mode.
RESERVED	11, 10	00	Reserved. Set to 00 for normal operation.
ICP	9, 8	00	Sets the IF charge-pump current. 00 = 139µA. 01 = 192µA. 10 = 278µA. 11 = 390µA.
RCP	7, 6	00	Sets the RF charge-pump current. 00 = 325µA. 01 = 650µA. 10 = 738µA. 11 = 1063µA.
RESERVED	5, 4	11	Reserved. Set to 11 for normal operation.
IF_TURBO_CHARGE	3	1	IF turbo-charge control. 0 = Disables extra charge-pump current during acquisition. 1 = Activates turbo-charge feature providing extra current during acquisition.
RCP_TURBO2	2	1	Works with RCP_TURBO1 (in the operation control register) to set the turbo charge-pump mode (see Table 7).
LD_MODE	1, 0	11	Determines output mode for LOCK pin as defined below: 00 = Test mode. 01 = IF PLL lock detector. 10 = RF PLL lock detector. 11 = Logical AND of IF PLL and RF PLL lock detectors.

Table 4. Current-Control Register (I_{CC}CTRL, Address: 0110_b)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTINGS	FUNCTION
RESERVED	15, 14, 13, 12	0000	Reserved. Set to 0000 for normal operation.
MPL	11	1	Sets the maximum RF output power level. 0 = Sets to low-noise mode. 1 = Sets to normal power mode.
RESERVED	10, 9, 8, 7	1000	Reserved. Set to 1000 for normal operation.
THROTTLE_BACK	6, 5, 4	011	Controls the throttleback rate (see Table 6).
I_MULT	3, 2, 1, 0	1000	Sets the current scale factor for the PA driver (see Table 5).

Table 5. Typical Current Scale Factors Set By I_MULT Bits

BIT NAME	BITS	NOMINAL CURRENT SCALE FACTOR
I_MULT	0011	0.69
	0100	0.75
	0101	0.81
	0110	0.88
	0111	0.94
	1000 (default)	1.00
	1001	1.13
	1010	1.25
	1011	1.38
	1100	1.50

Table 6. Typical Throttleback Rate Set By THROTTLE_BACK Bits

BIT NAME	BITS	NOMINAL RATE (dBmA/dB)
THROTTLE_BACK	000	1.3
	001	1.2
	010	1.1
	011	1.0
	100	0.9
	101	0.8
	110	0.7
	111	0.6

Table 7. RF Turbo Charge-Pump Current Setting

RCP_TURBO1	RCP_TURBO2	FUNCTION
0	0	No turbo current. Charge-pump current is set by RCP bits.
0	1	Turbo current turns on every time RF PLL is reprogrammed. Turbo current is automatically turned off after RF PLL is locked.
1	0	Turbo current is always on.
1	1	Turbo current is turned on every time RF PLL is out of lock.

Table 8. Power-Down Modes

POWER-DOWN MODE	COMMENTS	UPCONVERTER	MODULATOR	RF PLL	IF VCO	IF PLL
$\overline{\text{SHDN}}$ Pin	Ultra-low shutdown current	OFF	OFF	OFF	OFF	OFF
$\overline{\text{IDLE}}$ Pin	Rx only mode	OFF	OFF	—	OFF	OFF
$\overline{\text{TXGATE}}$ Pin	For punctured Tx mode	OFF	OFF	—	—	—
RF_PLL_SHDN Bit	For external RF PLL use	—	—	OFF	—	—
IF_PLL_SHDN Bit	For external IF PLL use	—	—	—	—	OFF
$\overline{\text{TXSTBY}}$ Bit	Tx is OFF, but IF and RF LOs stay locked	OFF	OFF	—	—	—

Complete 450MHz Quadrature Transmitter

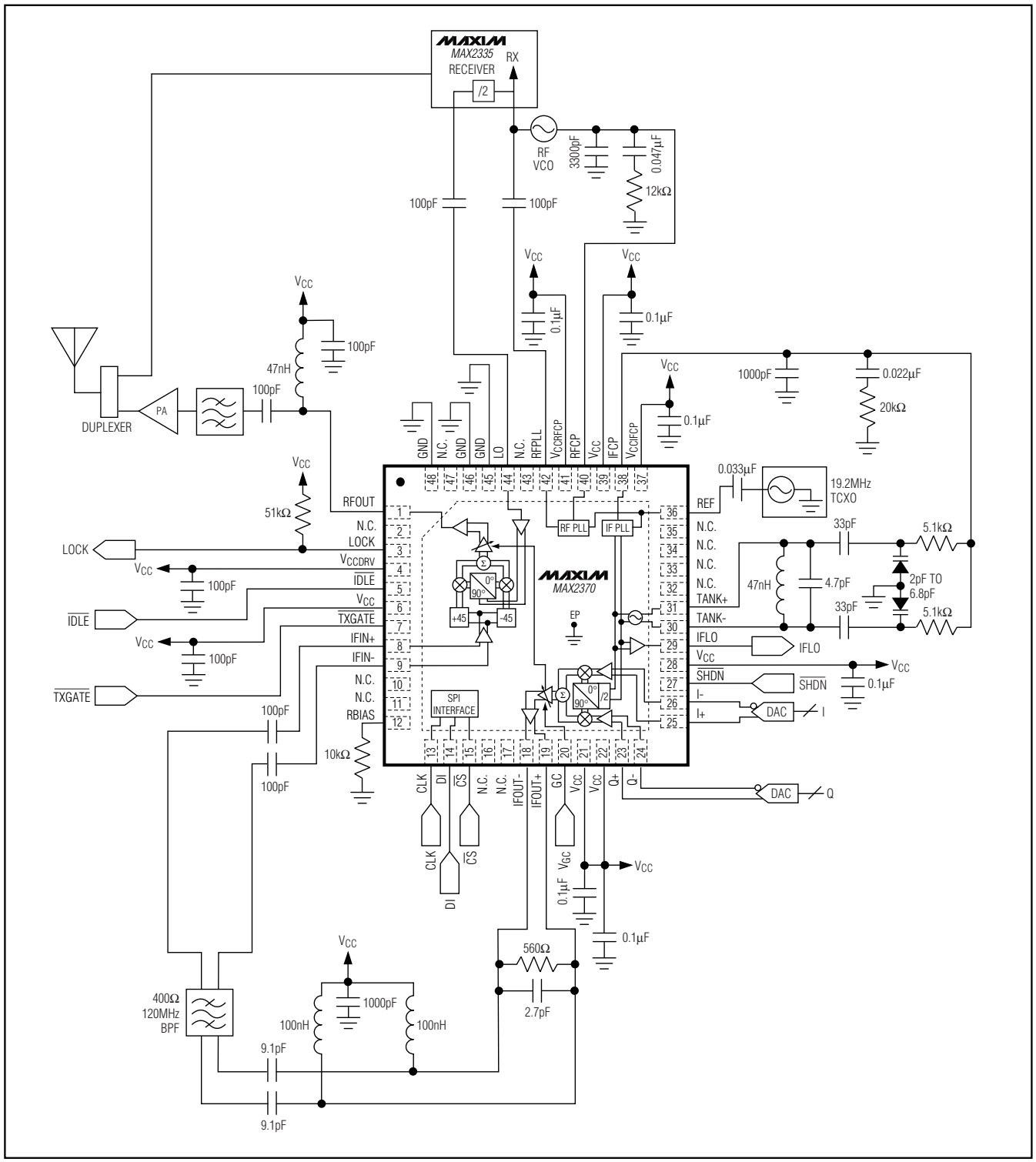


Figure 2. MAX2370 Typical Application Circuit

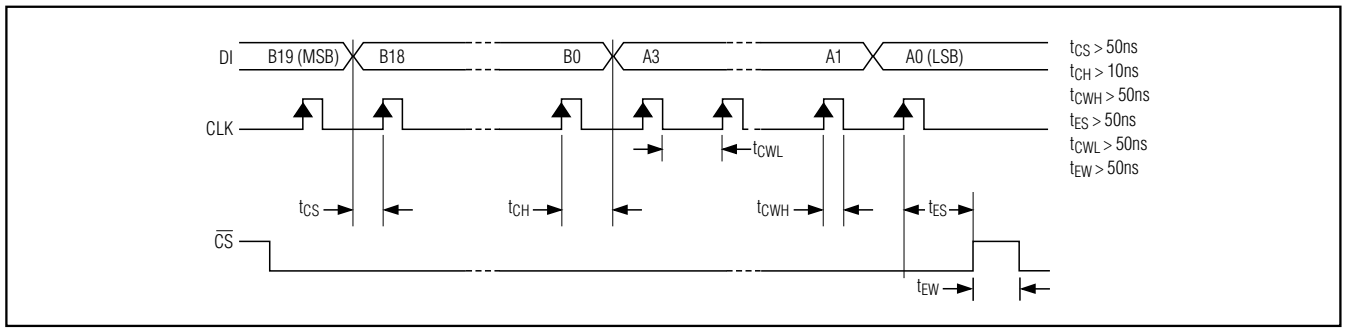


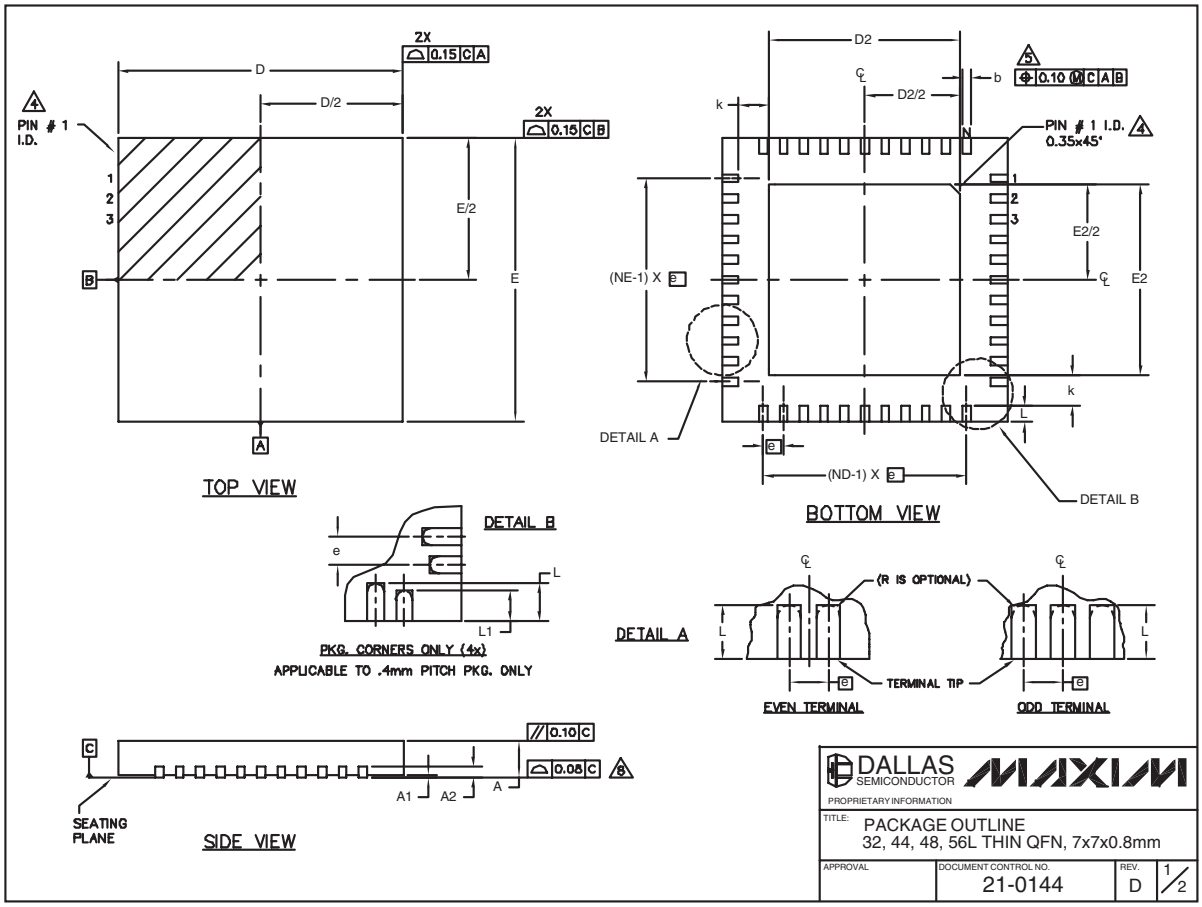
Figure 3. 3-Wire Interface Timing Diagram

Complete 450MHz Quadrature Transmitter

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

32, 44, 48L QFN.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7			56L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	0.35	0.45
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65	0.40	0.50	0.60
L1	–	–	–	–	–	–	–	–	–	–	–	–	0.30	0.40	0.50
N	32			44			48			44			56		
ND	8			11			12			10			14		
NE	8			11			12			12			14		

EXPOSED PAD VARIATIONS

PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C	DOWN BONDS ALLOWED
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T3277-1	–	4.55	4.70	4.85	4.55	4.70	4.85	–	NO
T3277-2	–	4.55	4.70	4.85	4.55	4.70	4.85	–	YES
T4477-1	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1	NO
T4477-2	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1	YES
T4477-3	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1	YES
T4877-1**	13,24,37,48	4.20	4.30	4.40	4.20	4.30	4.40	–	NO
T4877-2	–	5.45	5.60	5.63	5.45	5.60	5.63	–	NO
T4877-3	–	4.95	5.10	5.25	4.95	5.10	5.25	–	YES
T4877-4	–	5.45	5.60	5.63	5.45	5.60	5.63	–	YES
T4877-5	–	2.40	2.50	2.60	2.40	2.50	2.60	–	NO
T4877-6	–	5.45	5.60	5.63	5.45	5.60	5.63	–	NO
T5677-1	–	5.20	5.30	5.40	5.20	5.30	5.40	–	YES

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 EXCEPT THE EXPOSED PAD DIMENSIONS OF T3277-1; T4877-1/-2/-3/-4/-5/-6 & T5677-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 32, 44, 48, 56L THIN QFN, 7x7x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0144	D	2/2

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX2370ETM+ MAX2370ETM+T MAX2370ETM MAX2370ETM-T