SN54AHCT257, SN74AHCT257
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SCLS351D – MAY 1996 – REVISED JULY 1998

- **Inputs Are TTL-Voltage Compatible**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs**

description

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 4.5-V to 5.5-V V_{CC} operation.

The 'AHCT257 devices are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ($\overline{OE}$) input is at the high logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54AHCT257 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT257 is characterized for operation from –40°C to 85°C.

SN54AHCT257 . . . J OR W PACKAGE
SN74AHCT257 . . . D, DB, DGV, N, OR PW PACKAGE
(TOP VIEW)

$\overline{A}/B$	1	16 V_{CC}
1A	2	15 $\overline{OE}$
1B	3	14 4A
1Y	4	13 4B
2A	5	12 4Y
2B	6	11 3A
2Y	7	10 3B
GND	8	9 3Y
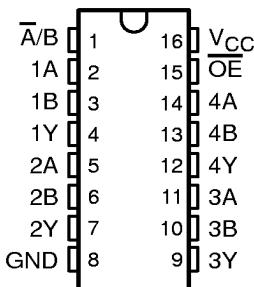
SN54AHCT257 . . . FK PACKAGE
(TOP VIEW)

Pins (top, left to right): 1A, $\overline{A}/B$, NC, V_{CC}, $\overline{OE}$ — positions 3, 2, 1, 20, 19

1B	4	18 4A
1Y	5	17 4B
NC	6	16 NC
2A	7	15 4Y
2B	8	14 3A

Bottom pins (9 10 11 12 13): 2Y, GND, NC, 3Y, 3B
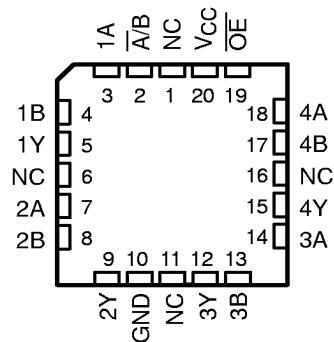
NC – No internal connection

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	$\overline{A}/B$	A	B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

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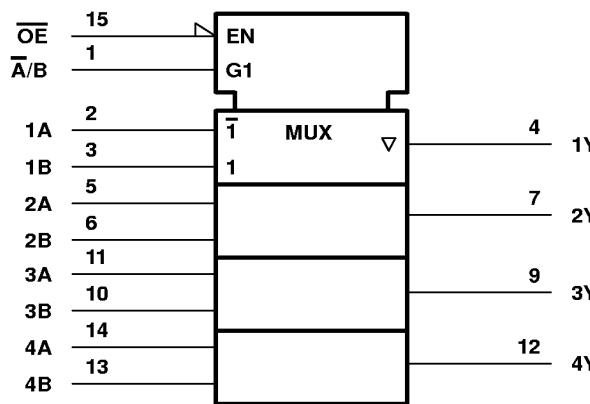
logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

logic diagram (positive logic)
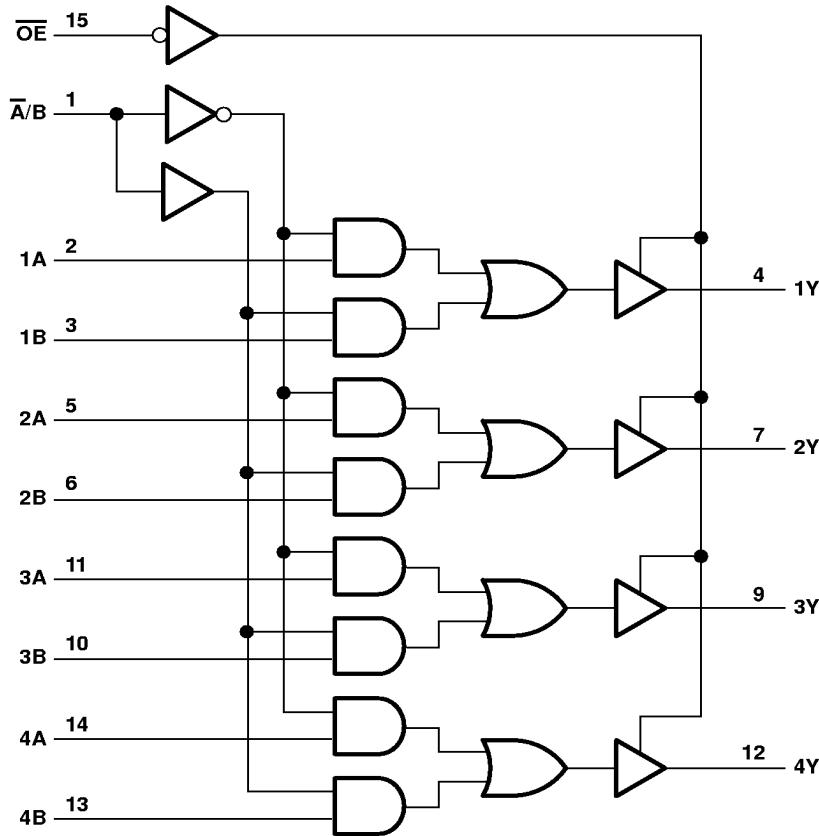
Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) .... −20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) .... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±25 mA
Continuous current through V_{CC} or GND .... ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package .... 113°C/W
                                                        DB package .... 131°C/W
                                                        DGV package .... 180°C/W
                                                        N package .... 78°C/W
                                                        PW package .... 149°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT257		SN74AHCT257		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−8		−8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall time		20		20	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V$_{CC}$	T$_A$ = 25°C MIN	TYP	MAX	SN54AHCT257 MIN	MAX	SN74AHCT257 MIN	MAX	UNIT
V$_{OH}$	I$_{OH}$ = −50 µA	4.5 V	4.4	4.5		4.4		4.4		V
	I$_{OH}$ = −8 mA		3.94			3.8		3.8		
V$_{OL}$	I$_{OL}$ = 50 µA	4.5 V			0.1		0.1		0.1	V
	I$_{OL}$ = 8 mA				0.36		0.44		0.44	
I$_I$	V$_I$ = V$_{CC}$ or GND	5.5 V		±0.1		±1		±1		µA
I$_{CC}$	V$_I$ = V$_{CC}$ or GND, I$_O$ = 0	5.5 V		4		40		40		µA
∆I$_{CC}$†	One input at 3.4 V, Other inputs at V$_{CC}$ or GND	5.5 V		1.35		1.5		1.5		mA
I$_{OZ}$	V$_O$ = V$_{CC}$ or GND	5.5 V		±0.25		±2.5		±2.5		µA
C$_i$	V$_I$ = V$_{CC}$ or GND	5 V								pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V$_{CC}$.

switching characteristics over recommended operating free-air temperature range, V$_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT257 T$_A$ = 25°C MIN	TYP	MAX	MIN	MAX	UNIT
t$_{PLH}$* t$_{PHL}$*	A or B	Y	C$_L$ = 15 pF						ns
t$_{PLH}$* t$_{PHL}$*	A̅/B	Y	C$_L$ = 15 pF						ns
t$_{PZH}$* t$_{PZL}$*	O̅E̅	Y	C$_L$ = 15 pF						ns
t$_{PHZ}$* t$_{PLZ}$*	O̅E̅	Y	C$_L$ = 15 pF						ns
t$_{PLH}$ t$_{PHL}$	A or B	Y	C$_L$ = 50 pF						ns
t$_{PLH}$ t$_{PLH}$	A̅/B	Y	C$_L$ = 50 pF						ns
t$_{PZH}$ t$_{PZL}$	O̅E̅	Y	C$_L$ = 50 pF						ns
t$_{PHZ}$ t$_{PLZ}$	O̅E̅	Y	C$_L$ = 50 pF						ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT257					UNIT
				$T_A = 25°C$			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF						ns
t_{PHL}									
t_{PLH}	$\overline{A}/B$	Y	C_L = 15 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PLZ}									
t_{PLH}	A or B	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PLH}	$\overline{A}/B$	Y	C_L = 50 pF						ns
t_{PLH}									
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PLZ}									

noise characteristics V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		SN74AHCT257		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}			V
$V_{IH(D)}$	High-level dynamic input voltage			V
$V_{IL(D)}$	Low-level dynamic input voltage			V

NOTE 4:   Characteristics are for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz		pF

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PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}
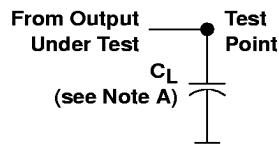
LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS
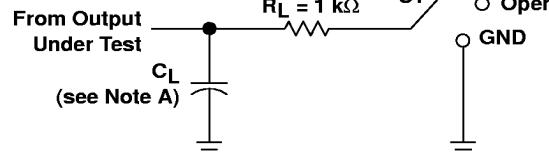
LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS
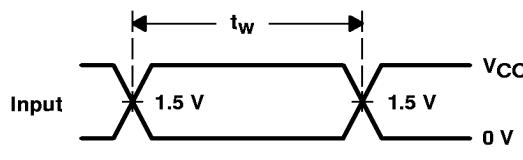
VOLTAGE WAVEFORMS
PULSE DURATION
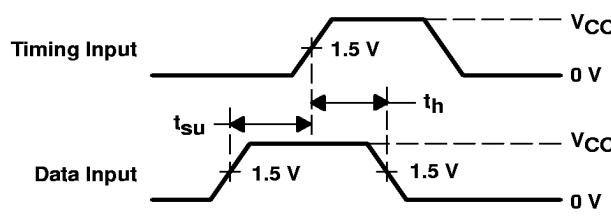
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
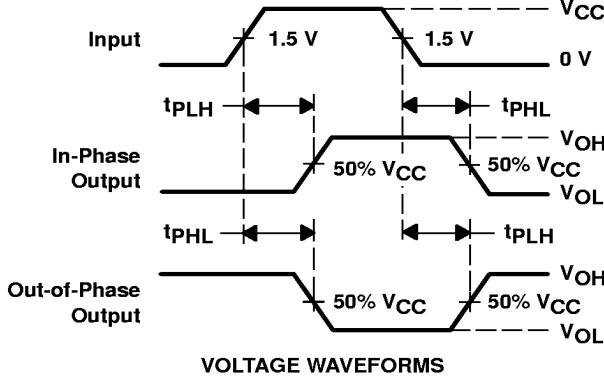
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS
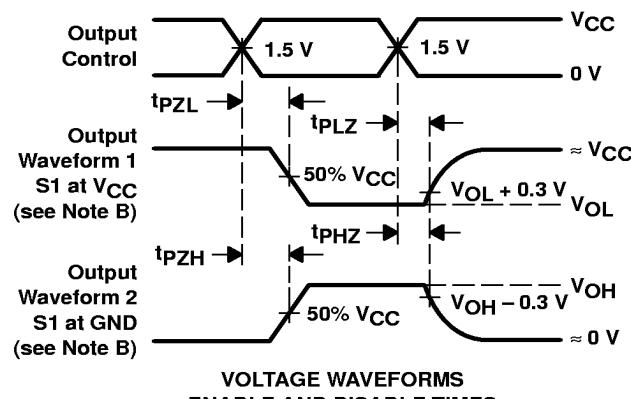
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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